*TI Designs: Verified Design*
# Reinforced Isolated M-LVDS Transceiver

**TEXAS INSTRUMENTS**

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## Circuit Description

This reference design combines TI's ISO7842 reinforced digital isolator with the SN65MLVD203 transceiver to create a reinforced, isolated, full-duplex, 100 Mbps M-LVDS transceiver node.

An isolated DC-DC converter provides a power supply across the isolation barrier utilizing the push-pull converter principle.

## Design Resources

| | |
|---|---|
| Design Archive | All Design Files |
| ISO7842 | Product Folder |
| SN65MLVD203 | Product Folder |
| SN6501 | Product Folder |
| TPS76333 | Product Folder |

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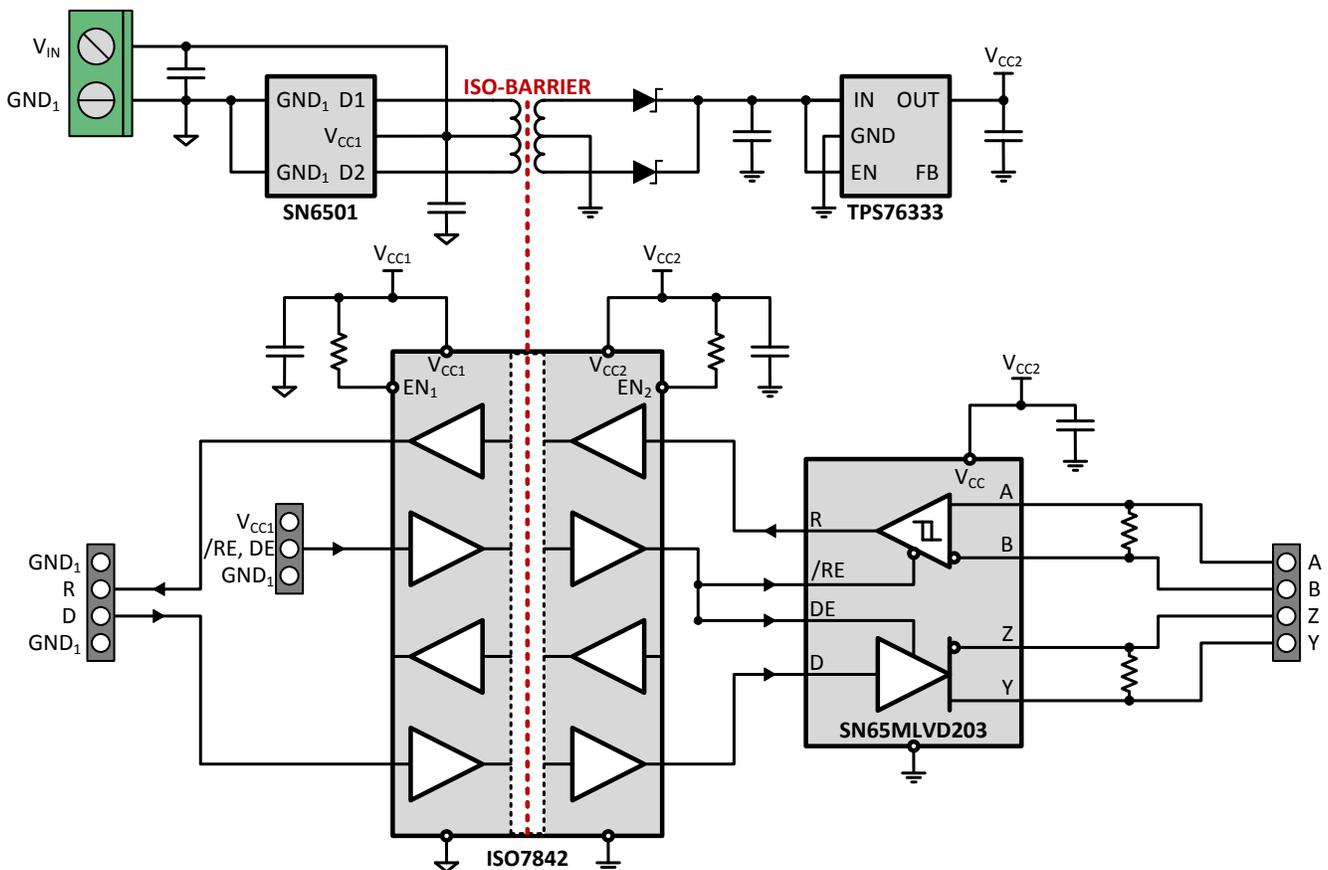


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# 1 Design Summary

## 1.1 Overview

Isolation is a means of preventing DC and unwanted AC currents between two parts of a system, while allowing signal and power transfer between the two sections. To make systems compact and lower-cost, it is desirable to have only one level of isolation, while providing the required electrical strength, reliability, and shock protection of two levels of basic isolation. This is referred to as *reinforced isolation*.

LVDS is a high speed differential signaling standard that achieves high data rates over long distances at low power. The M-LVDS standard extends LVDS to support multi-point applications.

Modern isolation system architectures are moving toward consolidating multiple low-speed channels into fewer high speed channels in order to reduce the number of isolated channels, and thus reduce cost and conserve board area. CMOS signaling at high data rates has limited reach, large power consumption, and large electromagnetic emissions. Beyond 50 Mbps, LVDS is a suitable choice, and introduces the need for isolated LVDS designs.

An isolated LVDS design combines a high-speed digital isolator for isolation, and an LVDS transceiver for high-speed communication over long distances.

This reference design demonstrates a reinforced isolated M-LVDS transceiver node consisting of TI's ISO7842 reinforced digital isolator and the SN65MLVD203 full-duplex M-LVDS transceiver. An isolated DC-DC converter provides a power supply across the isolation barrier using the SN6501 transformer driver.

## 1.2 Features

The M-LVDS transceiver node is designed to meet the following specifications:

- Reinforced isolation: $V_{ISO}$ = 5 k$V_{RMS}$

- M-LVDS common mode range: -1V to 3.4V

- Data rate up to 100 Mbps

# 2 Design Considerations

## 2.1 M-LVDS Transceiver

The SN65MLVD203 is a full-duplex MLVDS optimized for signaling rates up to 200 Mbps. The driver supports multipoint buses presenting as low as 30 Ω, and the driver transition times are controlled to allow for stubs off of the trunk of an MLVDS network.

## 2.2 Digital Isolator

The control side of the SN65MLVD203 is isolated from the node controller via a four-channel, digital isolator, ISO7841/2, providing isolation with the following specifications:

- $V_{ISO}$ = 5.7 k$V_{RMS}$

- $V_{SURGE}$ = 12.8 kV

- $V_{IOTM}$ = 8000 $V_{PK}$

- $V_{IORM}$/$V_{IOWM}$ = 1.5 k$V_{RMS}$/2121 $V_{PK}$

This isolator utilizes capacitive isolation with silicon dioxide ($SiO_2$) as dielectric. Digital capacitive isolators are industry's most reliable and most precise, low-power isolators.

The ISO7841 is ideal for half- and full-duplex transceivers which require independent control lines for the driver and receiver enable inputs. Alternatively, the driver and receiver enable pins may be controlled with a single signal, allowing the fourth channel of the ISO7841 or ISO7842 to transmit additional data. This design includes multiple 0 Ω resistors to accommodate both the ISO7841 and ISO7842.

## 2.3 Power Supply

The isolated DC-DC power supply converter utilizes the push-pull converter principle. The transformer driver SN6501 drives an isolated transformer with center-tap. The transformer output is rectified by two Schottky diodes (D1, D2) and capacitor (C3). The subsequent low dropout regulator, TPS76333, provides a regulated 3.3V output for up to 150mA output current. For best stability and lowest ripple, a low-ESR, 4.7µF ceramic capacitor (C4) buffers the regulator output.

## 3 Measurement

## 3.1 Data Transmission

For point-to-point applications, only one transceiver must be isolated to provide reinforced isolation. Using one non-isolated transceiver reduces the total jitter of the signal path.
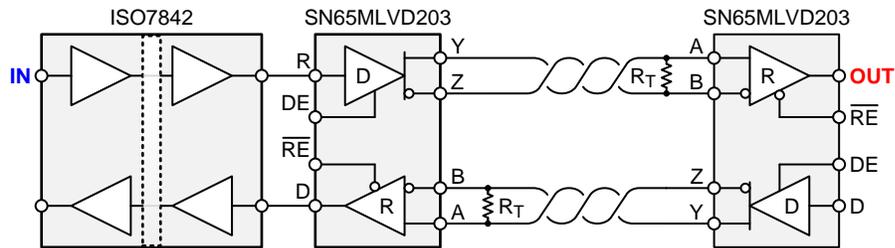


**Figure 1: Point-to-point eye diagram measurement**
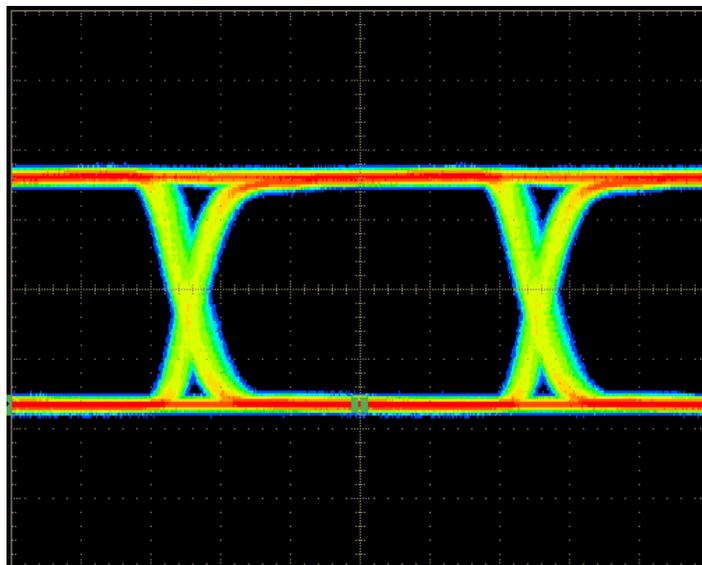


**Figure 2: Eye diagram – 100Mbps**

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For multipoint applications, each transceiver must be isolated from the bus. Total jitter, therefore, consists of a driver, a receiver, and two isolator channels.
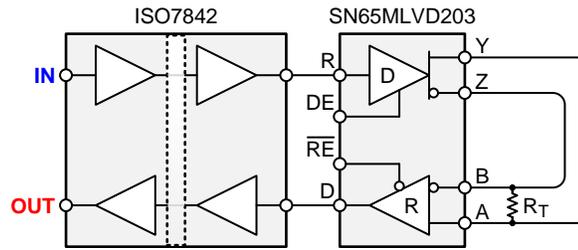


**Figure 3: Multipoint eye diagram measurement**
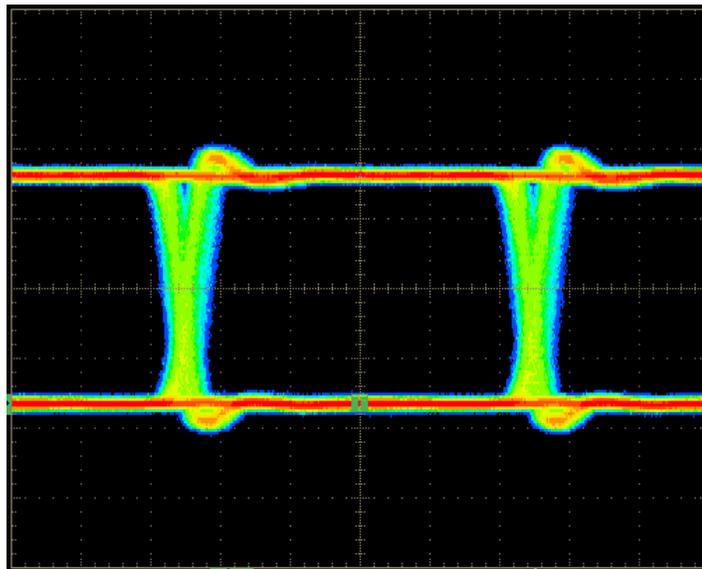


**Figure 4: Eye diagram – 100Mbps**

# 4    PCB Design
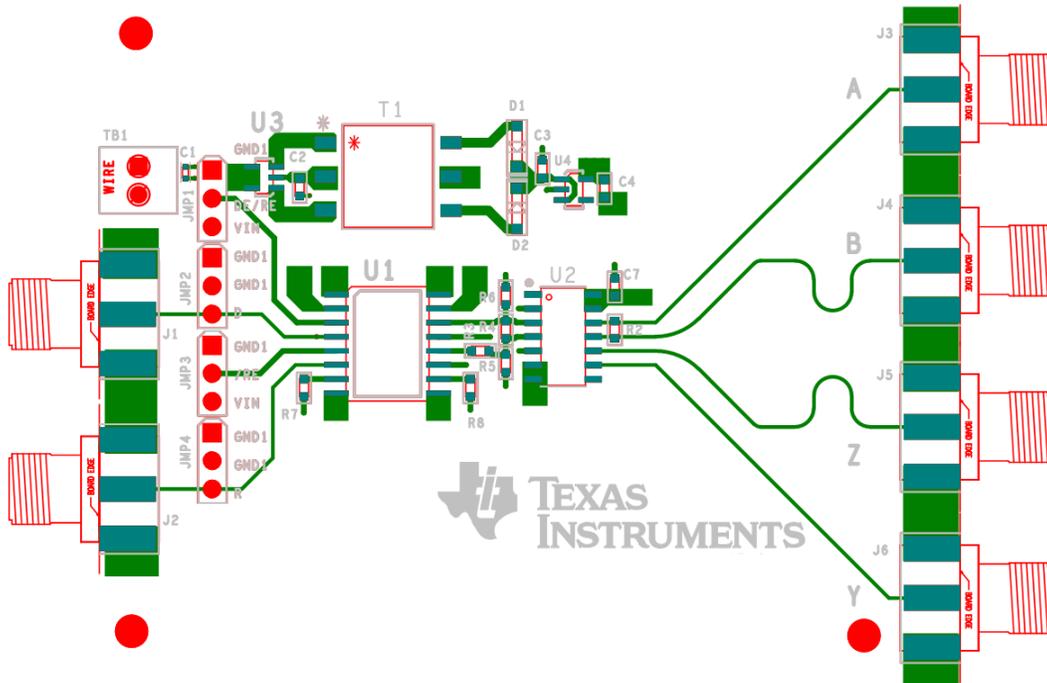


**Figure 6: PCB layout top**
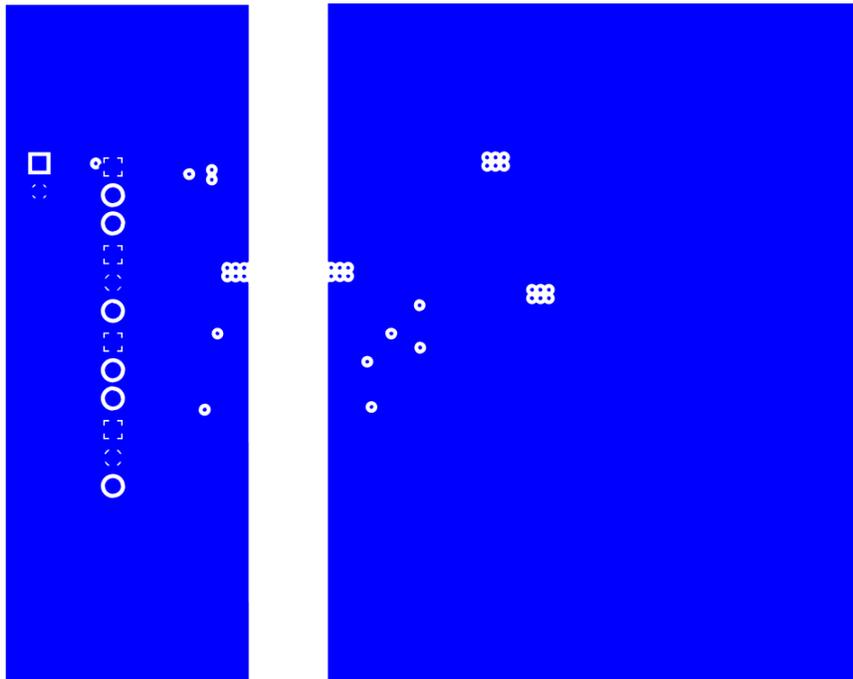


**Figure 7: PCB layout ground**

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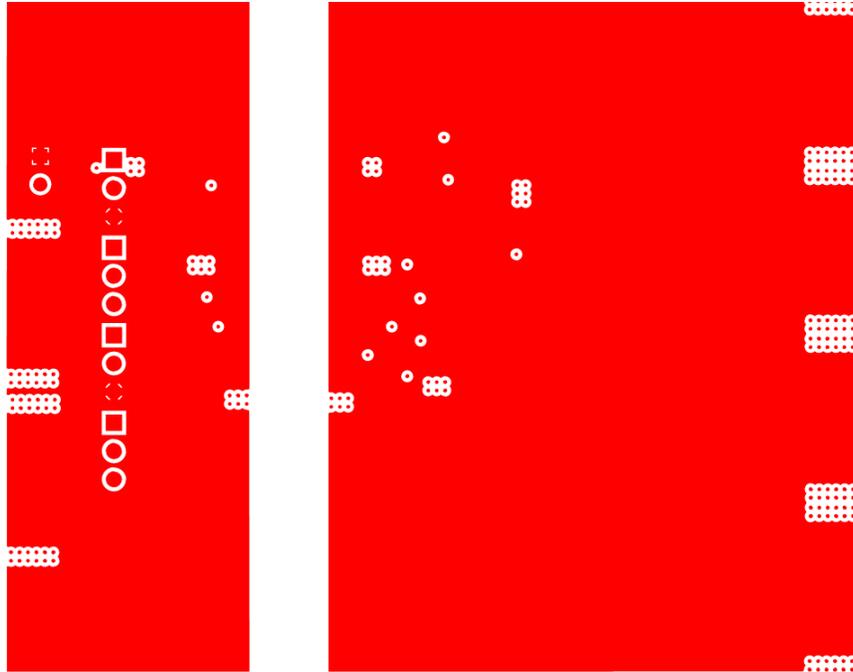
**Figure 8: PCB layout power**
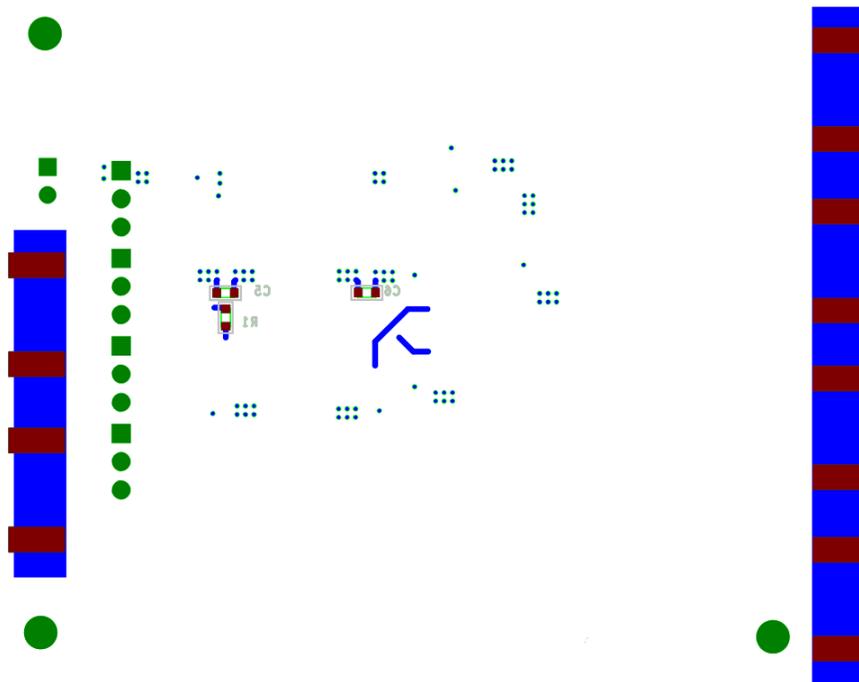


**Figure 9: PCB layout bottom**

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## 5 References

1. *LVDS Owner's Manual*, [SNLA187](SNLA187)

2. *Introduction to M-LVDS (TIA/EIA-899), Peffers 2013,* [SLLA108A](SLLA108A)

## 6 Appendix

### 6.1 *Schematic*
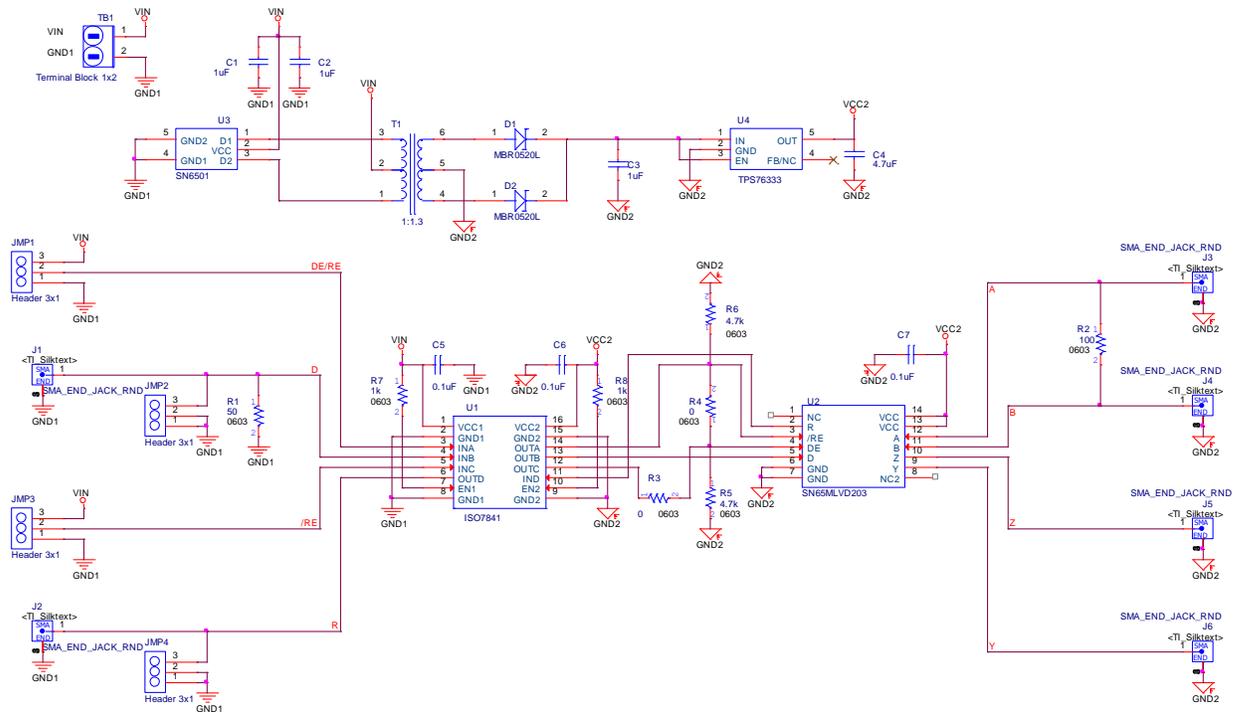


**Figure 10: Reinforced isolated MLVDS transceiver**

## 6.2 Bill of Materials

### Table 1: Isolated auto-polarity RS-485 transceiver Bill of Materials

| Item | Quantity | Reference | Part | Footprint | Manufacturer | Manufacturer Part Number |
|------|----------|-----------|------|-----------|--------------|--------------------------|
| 1 | 1 | C1 | 1uF | 0402 | Taiyo Yuden | LMK105BJ105KV-F |
| 2 | 2 | C2, C3 | 1uF | 0603 | TDK | C1608X7R1C105K |
| 3 | 1 | C4 | 4.7uF | 0603 | TDK | C1608X5R0J475K |
| 4 | 2 | C5, C6, C7 | 0.1uF | 0603 | | |
| 5 | 2 | D1, D2 | MBR0520L | SOD-123 | ON-Semi | MBR0520LT1G |
| 6 | 6 | J1, J2, J3, J4, J5, J6 | SMA_END_JACK_RND | | Johnson Components | 142-0701-801 |
| 7 | 4 | JMP1, JMP2, JMP3, JMP4 | Header 3x1 | | | |
| 8 | 1 | R1 | 50 | 0603 | | |
| 9 | 1 | R2 | 100 | 0603 | | |
| 10 | 1 | R3 | DNI | 0603 | | |
| 11 | 1 | R4 | 0 | 0603 | | |
| 12 | 2 | R5, R6 | 4.7k | 0603 | | |
| 13 | 2 | R7, R8 | 1k | 0603 | | |
| 14 | 1 | T1 | 1:1.3 | SMT | Wurth Electronics | 750313638 |
| 15 | 1 | TB1 | Terminal Block 1x2 | | | |
| 16 | 1 | U1 | ISO7842 | 16DW | Texas Instruments | ISO7842DW |
| 17 | 1 | U2 | SN65MLVD203 | SOIC-14 | Texas Instruments | SN65MLVD203DR |
| 18 | 1 | U3 | SN6501 | SOT-23 | Texas Instruments | SN6501DBVR |
| 19 | 1 | U4 | TPS76333 | SOT-23 | Texas Instruments | TPS76333DBVR |

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