

TI Designs

66AK2L06 DSP+ARM[®] Processor JESD204B Attach to Wideband ADCs and DACs Design Guide



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Design Resources

TIDEP0034	Tool Folder Containing Design Files
66AK2L06	Product Folder
ADC12J4000	Product Folder
DAC38J84	Product Folder



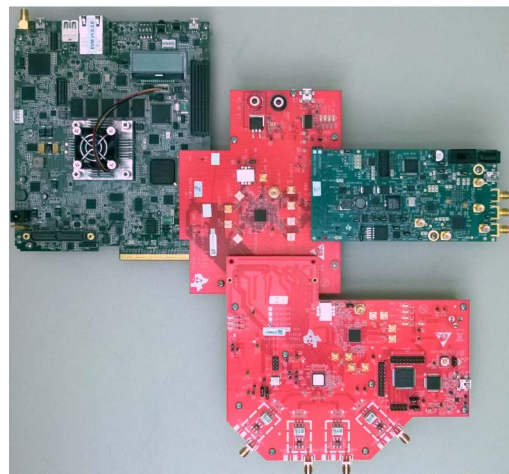
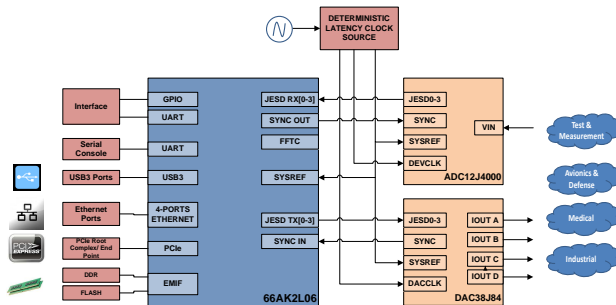
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Design Features

- Easy Integration of Signal Processor to Data Converters Over JESD204B
- Multichannel Sampling Rates up to 368 Msp/s With 150 MHz of Processing Bandwidth
- DFE Processing for Filtering, Down-sampling, or Up-sampling
- System Optimized for Test And Measurement and Defense Applications
- Wideband Sampling With JESD204B Attached Signal Processing Solution Including DSP, ADC and DAC Boards, Demo Software, Configuration GUIs, and Getting Started Guide
- A Robust Demonstration and Development Platform Including Three EVMs, a Deterministic Latency Card, Schematic, BOM, User Guide, Benchmarks, Software, and Demos

Featured Applications

- Test and Measurement
- Defense



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

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General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines



Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center <http://support.ti.com> for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.** If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety

- (a) Keep work area clean and orderly.
- (b) Qualified observer(s) must be present anytime circuits are energized.
- (c) Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
- (d) All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
- (e) Use stable and nonconductive work surface.
- (f) Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.

2. Electrical Safety

As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.

- (a) De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
- (b) With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
- (c) After EVM readiness is complete, energize the EVM as intended.

WARNING: WHILE THE EVM IS ENERGIZED, NEVER TOUCH THE EVM OR ITS ELECTRICAL CIRCUITS AS THEY COULD BE AT HIGH VOLTAGES CAPABLE OF CAUSING ELECTRICAL SHOCK HAZARD.

3. Personal Safety

- (a) Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1 System Description

The *66AK2L06 DSP+ARM Processor JESD204B Attach to Wideband ADCs and DACs Design Guide* demonstrates performance of the high-speed JESD204B connectivity between the 66AK2L06 System-on-Chip (SoC) with industry-leading high-speed data converters. This design also demonstrates the signal-processing power of 66AK2L06 hardware co-processors, DSP CorePacs, and control processing power using ARM® CorePacs. A high-level hardware block diagram shown in [Figure 1](#) explains high-level connectivity of the 66AK2L06 device with ADC12J4000 and DAC38J84 for different applications. The analog input comes from an ADC that best matches the requirements of each industry application. The analog input is sampled, digitized, and sent to the 66AK2L06 device over a JESD204B interface. The 66AK2L06 processes the received data using its internal hardware co-processors and sends the data out through any of the available interfaces including JESD204B, Ethernet, or PCIe. The JESD output from the 66AK2L06 can be sent over the JESD204B interface to DAC38J84 for converting digitized data to analog output.

The *66AK2L06 DSP+ARM Processor JESD204B Attach to Wideband ADCs and DACs Design* is well suited for applications such as:

- Communications test: Mobile handset testers, radio communication analyzer, base station analyzer, RF test cards
- General purpose test: Spectrum analyzers, vector or signal analyzer, vector or signal generator, oscilloscopes
- High-speed data acquisition and generation
- Electronic warfare and communications: Military radar, civilian radar, synthetic-aperture radar (SAR), signals Intelligence (SIGINT/ELINT), countermeasure
- Missiles and ground defense: Missile guidance and control systems, missile compute platforms, monitoring systems
- Military aircraft and general aviation: Unmanned systems, munitions, surveillance or mobility aircraft

2 Block Diagram

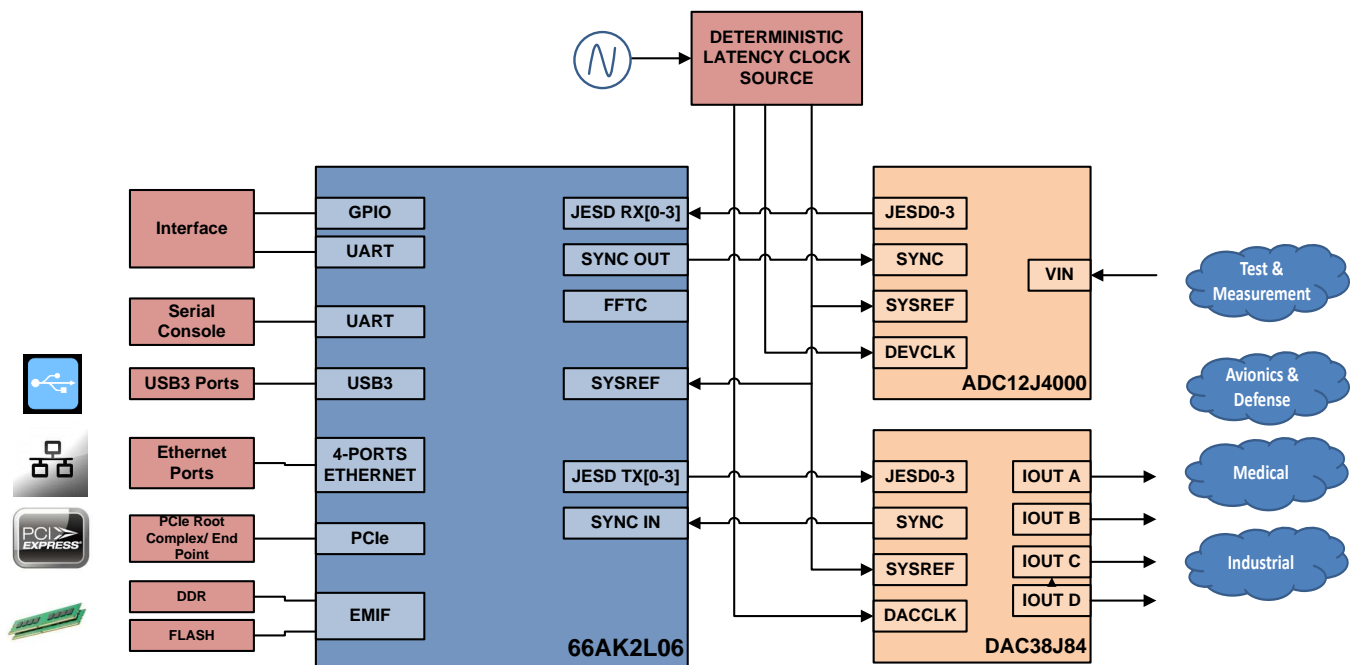


Figure 1. System Block Diagram

2.1 Highlighted Products

2.1.1 66AK2L06

The 66AK2L06 is a member of the C66x family based on TI's new Keystone™ II Multicore SoC architecture. The SoC is a lower power, smaller size, and lower-cost solution with eight integrated lanes of the JESD204B interface to meet the requirements of test and measurement, avionics and defense, and medical applications. The device's ARM and DSP cores deliver exceptional processing power for platforms needing high signal and control processing. The Keystone II architecture provides a programmable platform integrating various subsystems (ARM CorePacs, C66x CorePacs, DFE, FFTC, 4-Port Ethernet Switch, and so on) and uses a queue-based communication system that allows the SoC resources to operate efficiently and seamlessly. This unique SoC architecture also includes a TeraNet switch that enables a wide mix of system elements, from programmable cores to dedicated co-processors and high-speed I/O, to allow each of them to operate at maximum efficiency with no blocking and stalling. The 66AK2L06 SoC is part of TI's scalable multicore SoC architecture solution that provides developers with a range of software-compatible and hardware-compatible devices to minimize development time and maximize reuse across all applications. The following are some of the key features that enable the SoC to be used in the test and measurement, avionics and defense, medical, and industrial applications:

- JESD204A/B Compliant Four Tx and Four Rx lanes supporting speeds up to 7.37 Gbps
- Seamless connectivity with JESD204B-compliant data converters with support for alignment across multiple lanes within a single converter or multiple converters in the same device
- 2x FFT Co-processor with support for maximum FFT size 8192
- Four-Gigabit Ethernet SGMII ports
- Four C66x CorePacs and two ARM CorePacs operating up to 1.2 GHz

The 66AK2L06 product page, which has additional information on the 66AK2L06 family, is available at [66AK2L06](#). For more information, see [Figure 2](#).

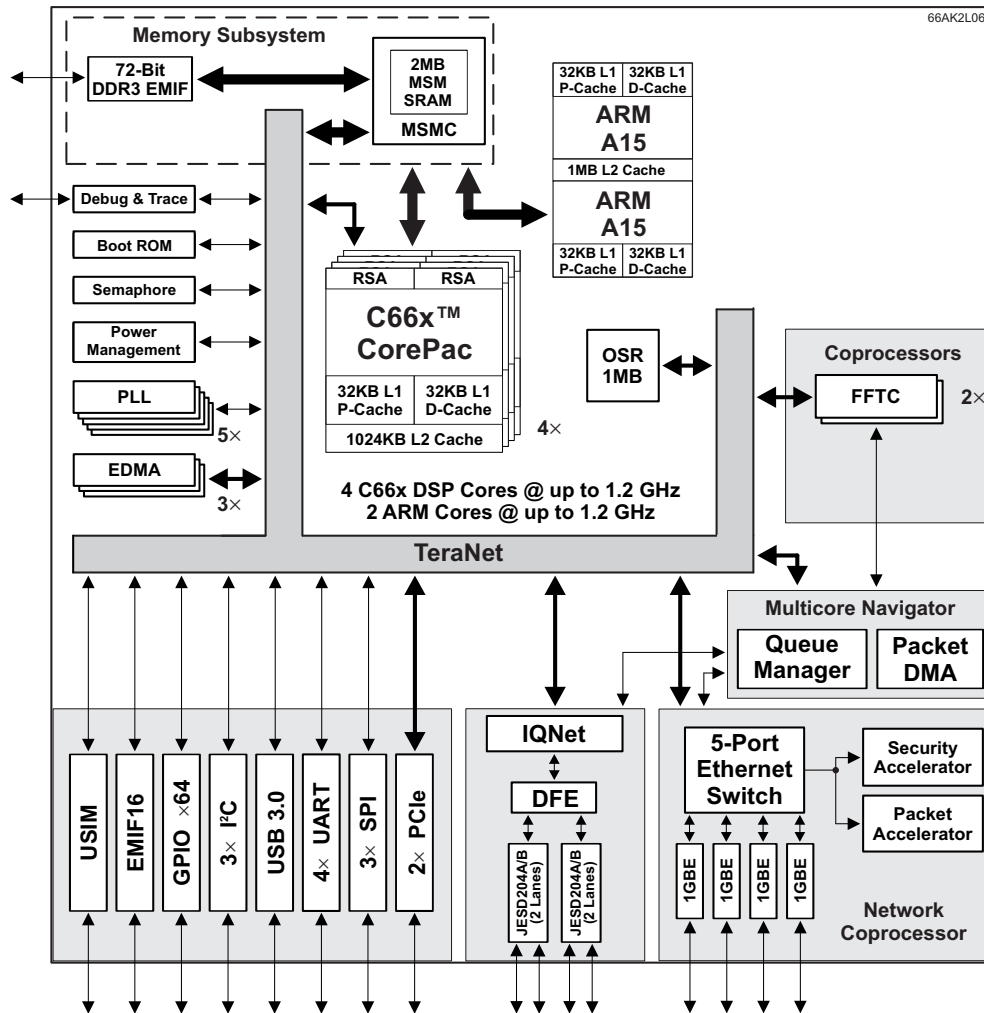


Figure 2. 66AK2L06 Block Diagram

2.1.2 ADC12J4000

ADC12J4000 is a wideband sampling and digital tuning device. TI's giga-sample analog-to-digital converter (ADC) technology enables a large block of frequency spectrum to be sampled directly at RF. An integrated DDC (Digital Down Converter) provides mixing, digital filtering, and down-conversion (decimation). The low-pin-count JESD204B Subclass-1-compliant eight-output serial lanes provides ease of board routing and connectivity. The ADC12J4000 supports maximum sampling rate of 4000 Msps.

The ADC12J4000 product page, which has additional information on the ADC12J4000, is available at [ADC12J4000](#).

2.1.3 DAC38J84

DAC38J84 is a low-power, 16-bit, quad-channel, 2.5-GSPS digital-to-analog converter (DAC) with a JESD204B interface. This device includes features that simplify the design of complex transmit architectures. Fully bypassable 2x-to-16x digital interpolation filters with over 90 dB of stop-band attenuation simplify the data interface and reconstruction filters. An on-chip 48-bit Numerically Controlled Oscillator (NCO) and independent complex mixers allow flexible and accurate carrier placement.

The DAC38J84 product page, which has additional information on the DAC38J84 family, is available at [DAC38J84](#).

3 System Design Theory

A wideband demonstration of the *66AK2L06 DSP+ARM Processor JESD204B Attach to Wideband ADCs and DACs Design* is available to evaluate the sampling of two 75-MHz channels. The following sections provide details of the data flow and processing path.

3.1 Input Data Stream

Pre-defined input data stream is stored in the DDR memory. Two options of pre-defined input data stream are available:

- Two dual-tone different amplitude data sampled at 92.16 Msps
- 240 single tones spread across 75-MHz bandwidth

3.2 Transmit Data from 66AK2L06 over JESD to DAC38J84

The packet (PktDMA) engine inside the I/Q Network (IQNet) module reads the pre-defined input data stream from DDR memory and transfers it to the Antenna Interface for DFE (AID) module. AID sends this data stream at a 92.16-Msps rate to 'Baseband' block inside Digital Front End (DFE) sub-system. The baseband block reformats and de-interleaves the data into I and Q streams and sends it to Digital Down Converter/Up Converter (DDUC). The DDUC block filters this stream, and up converts it. After DDUC, the sumchain combines DDUC channels into a stream. One channel is in each stream. Gain is applied, and CDFR (CFR DPD Fractional Resampler) interpolates this stream by four and mixes it with -43.5 MHz and 43.5 MHz, respectively. These I and Q channels are summed up into a single stream and resampled at 368.64 Msps. The Tx block passes the CDFR stream to the JESD block. The JESD block is configured as explained in detail in Section 3.4. JESD frames pass through the serializer/deserializer block (SERDES) on 66AK2L06 and output serially on two Transmit (Tx) lanes (Lane0 and Lane1). The SERDES is configured to operate at a link rate of 7.37 Gbps. The DAC38J84 receives this data and samples it using a sampling rate clock (DACCLK) of 368.64 MHz. A ratio of 2 interpolation is applied inside the DAC to generate the 737.28-Msps output data stream. The $F_s/4$ -course mixer is also enabled on the DAC, so the output data is centered at 184.32 MHz. For more information, see Figure 3.

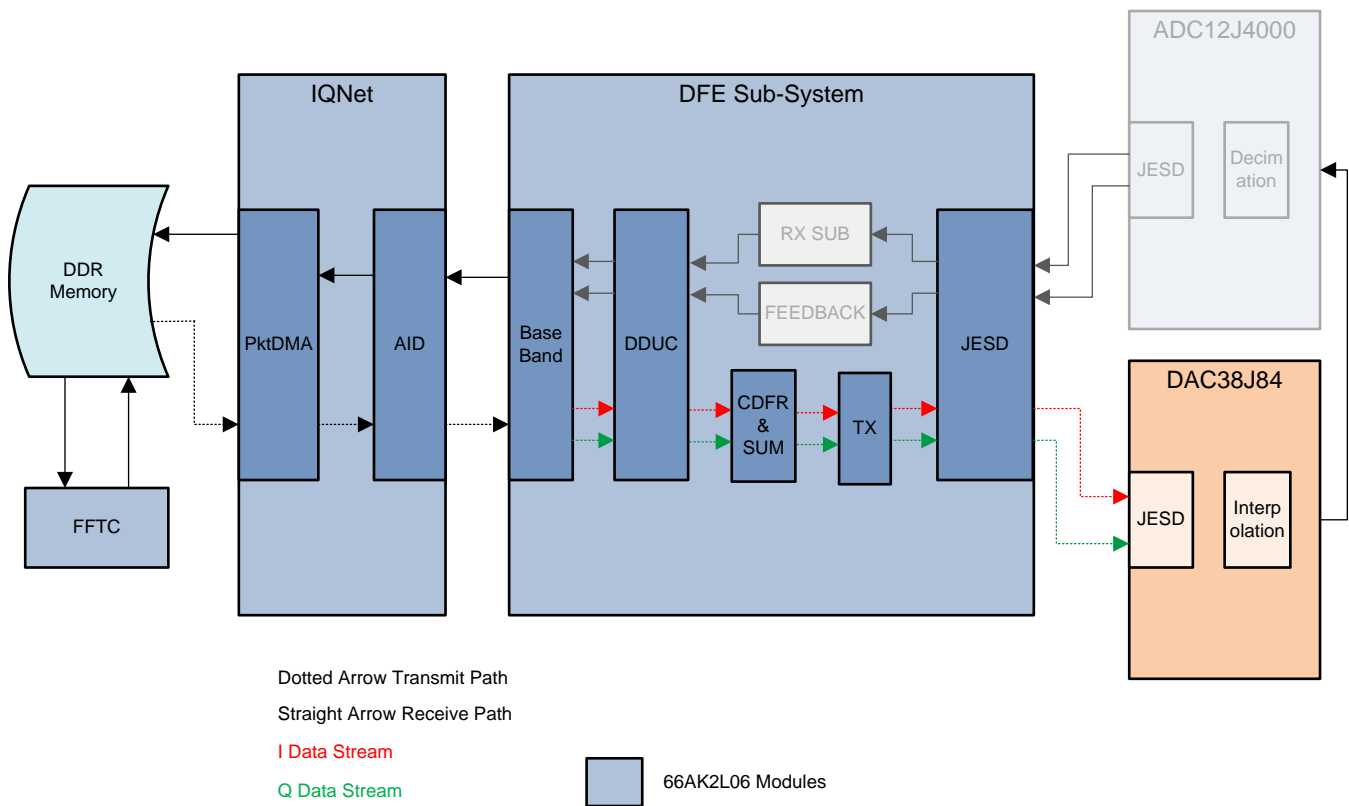


Figure 3. Tx Data Path

3.3 Receive Data from ADC12J4000 over JESD204B to 66AK2L06

The DAC output signal is looped back to the ADC12J4000's analog input channel 0 through an external low-pass filter and a balun card. The ADC12J4000 samples the analog input signal with a sampling frequency (DEVCLK) of 2949.12 MHz. The sampled data is mixed to -184.32 Mhz, resulting in OIF then the mixed output is filtered.. The filtered output is decimated by a factor of 8. The decimated data is sent to the JESD block inside the ADC, which sends the data out in IQ parallel format with a byte clock of 368.64 MHz. The JESD module is configured as explained in detail in [Section 3.4](#). The 66AK2L06 JESD module receives the data over Rx Lane0 and Lane1. The data is sent to the Rx sub-block and the feedback block inside the DFE module where the IQ stream is translated in frequency for the two channels to 43.5, and -43.5 Mhz. The Rx and Feedback block then decimates it by 2, to an 184.32 Mhz complex IQ rate.. The DDUC module filters both streams and provides output at 92.16 Msp/s to the baseband module, which transfers data to the IQNet. The PktDMA stores the data in DDR memory. This data is picked up by FFTC co-processor to perform 4096 point FFT and output data is stored to DDR memory. For more information, see [Figure 4](#).

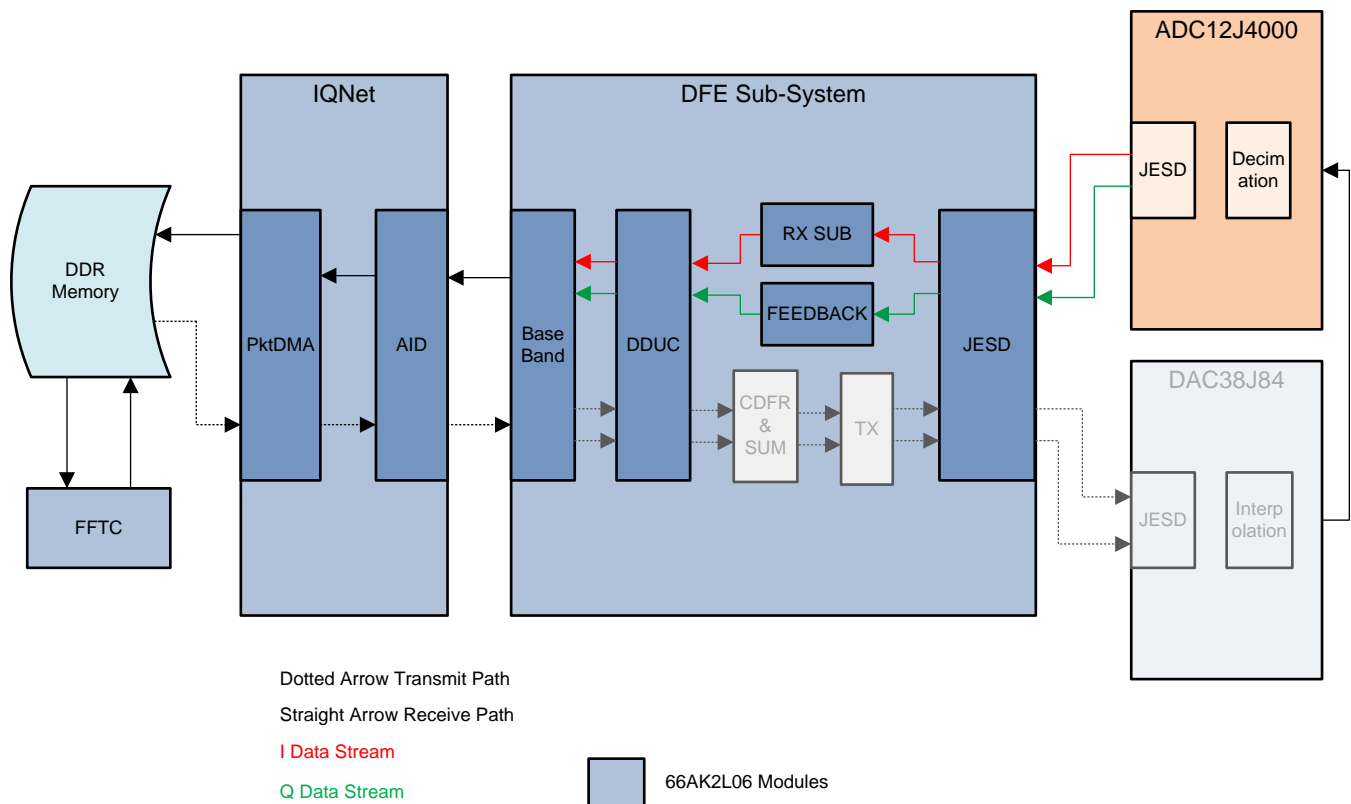


Figure 4. Rx Data Path

3.4 JESD204B Capabilities and Configurations

The JESD204B module is capable of the following:

- Four transmit lanes with up to 7.37 Gbps each
- Four receive lanes with up to 7.37 Gbps each
- Alignment across multiple lanes within a single converter or multiple converters in the same device
- Support for subclass 0 and 1

In the demo application, the 66AK2L06 communicates with the ADC12J4000 and the DAC38J84 over two lanes operating at a link rate of 7.37 Gbps. A JESD subclass 1 configuration is used with a SYSREF frequency of 368.64 MHz. Data scrambling is supported on the 66AK2L06 as well as the ADC12J4000 and the DAC38J84. For this application, scrambling is disabled on the lanes. [Table 1](#) shows the JESD link-parameters configuration.

Table 1. JESD Link Parameters

JESD PARAMETER	66AK2L06 CAPABILITY	PARAMETERS USED IN DEMONSTRATION	
		ADC12J4000 → 66AK2L06	66AK2L06 → DAC38J84
M - (Number of Converters per Device)	Depends on the Converter's capability. With 4 Tx and 4 Rx lanes and bit rate requirement maximum 4 converters can be supported in Tx direction and 4 in the Rx direction	1	2
N - (Resolution of Converters)	Depends on the Converter's capability.	12	16
N' - (JESD Word Size)	Depends on the Converter's capability.	16	16
L - (No of Lanes)	Total 8 lanes but Maximum 4 lanes in each direction	2	2
F - (No of Octets per Frame)	Calculated based on other parameters	2	2
K - (No of Multiframe)	Max 32	16	16
S - (Samples per Converter per Frame)	Depends on the Converter's capability.	1	1

3.5 FFT Processing

The FFT co-processor (FFTC) modules in 66AK2L06 provides the following features:

- IFFT and FFT operations
- Maximum FFT size of 8192
- Processing up to 1200 Msps for a FFT size of 1024
- 77-dB SNR—dynamic and programmable scaling modes
- Support for FFT shift (switch left and right halves)
- Support for cyclic prefix addition or removal

4 Getting Started Hardware

The *66AK2L06 DSP+ARM Processor JESD204B Attach to Wideband ADCs and DACs Design Development Kit* is an application development platform for evaluating the 66AK2L06 device's connectivity and performance with leading-edge ADC12J4000 and DAC38J84. As shown in [Figure 5](#), 66AK2L06 EVM, ADC12J4000 EVM, and DAC38J84 EVMs are connected through the K2L-HSP FMC adapter board that provides signal routing across the FMC interface and supports Deterministic Latency.

The purpose of the K2L-HSP FMC Adapter board is to generate sampling clocks for ADC12J4000 and DAC38J84. The card uses SYSCLK provided by 66AK2L06 as an input reference clock for generating sampling clocks. The card also generates a common SYSREF clock for deterministic latency using the common input SYSCLK. The K2L-HSP FMC Adapter board routes the JESD lanes and SYNC signals from one Lamarr FMC to 2 data converter FMC connectors, one for ADC and one for DAC. This process allows the 66AK2L06 EVM board to communicate with both ADC and DAC EVMs over the JESD204B interface.

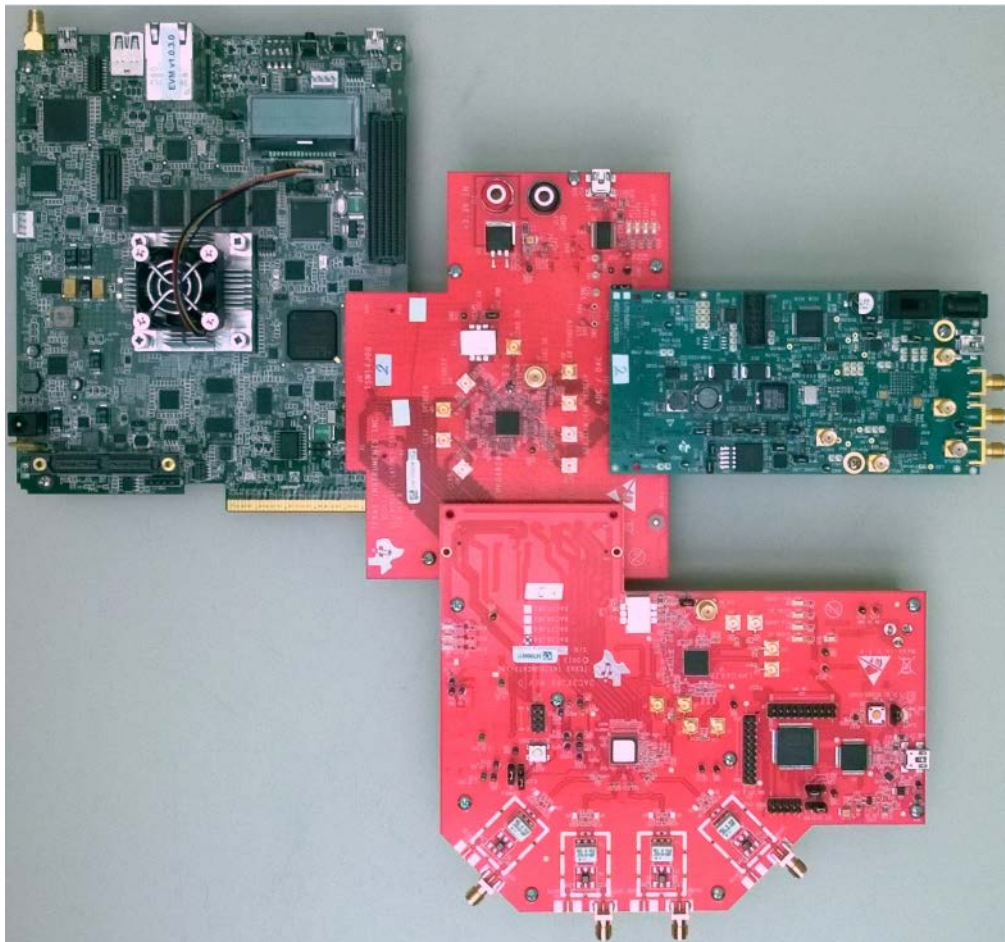


Figure 5. 66AK2L06 DSP+ARM Processor JESD204B Attach to ADC12J4000 / DAC38J84 Design Development Kit

Find additional information on the 66AK2L06 EVM at <http://ti.com/tool/xevmk2lx>.

Find additional information on ADC12J4000 EVM at <http://www.ti.com/tool/adc12j4000evm>.

Find additional information on DAC38J84 EVM at <http://www.ti.com/tool/dac38j84evm>.

5 Getting Started Software

The *66AK2L06 DSP+ARM Processor JESD204B Attach to Wideband ADCs and DACs Design* provides a Linux application developed using Software Development Kits available from Texas Instruments.

5.1 Multicore Software Development Kit (MCSDK)

The MCSDK provides foundational software for TI KeyStone II devices. The MCSDK encapsulates a collection of software elements and tools intended to enable customer application development and migration. The foundational components include:

- TI-RTOS real-time embedded operating system on DSP cores
- Linux high-level operating system running on ARM A15 cluster (SMP mode)
- DSP chip support libraries, DSP/ARM drivers, and basic platform utilities
- Interprocessor communication for communication across cores and devices
- Bootloaders and boot utilities, power-on-self test

5.2 RF Software Development Kit (RFSDK)

The RFSDK is an integrated software solution that simplifies leveraging all the components of the 66AK2L06 Digital-Front-End (DFE) module. The RFSDK aims to provide an integrated environment to transmit, receive, process, and visualize signals.

- Provides an integrated solution requiring a minimal amount of software development to enable JESD data converters.
- Provides tools for evaluation and debug of integrated solution with 66AK2L06 devices and data converters

5.3 Design Linux Application

The *66AK2L06 DSP+ARM[®] Processor JESD204B Attach to Wideband ADCs and DACs Design* Linux application has the following features:

- The application configures the operation of IQN2 and DFE (and required infrastructure such as Navigator, Serdes, DDR, and others) for Tx and Rx according to a particular configuration.
- Users can load pre-defined distinct signal patterns in the Tx buffers (DDR memory) to continuously transmit known data patterns on both carriers. Data patterns are 10msec (one frame) IQ samples and are loaded into memory from where they are played out.
- Tx data can be looped back to Rx at multiple loop points (IQN2, JESD, or external). External Rx data can also be supplied to the receiver to capture external Rx signal (e.g. from a signal generator)
- When requested, playback can capture 10msec worth of samples at a receiver-in-capture buffer in DDR.

6 Test Setup

Figure 6 shows the connectivity of the various boards. Find more information about the test setup in the *66AK2L06 DSP+ARM Processor JESD204B Attach to Wideband ADCs and DACs Design Getting Started Guide* available at <http://www.ti.com/tool/tidep0034>.

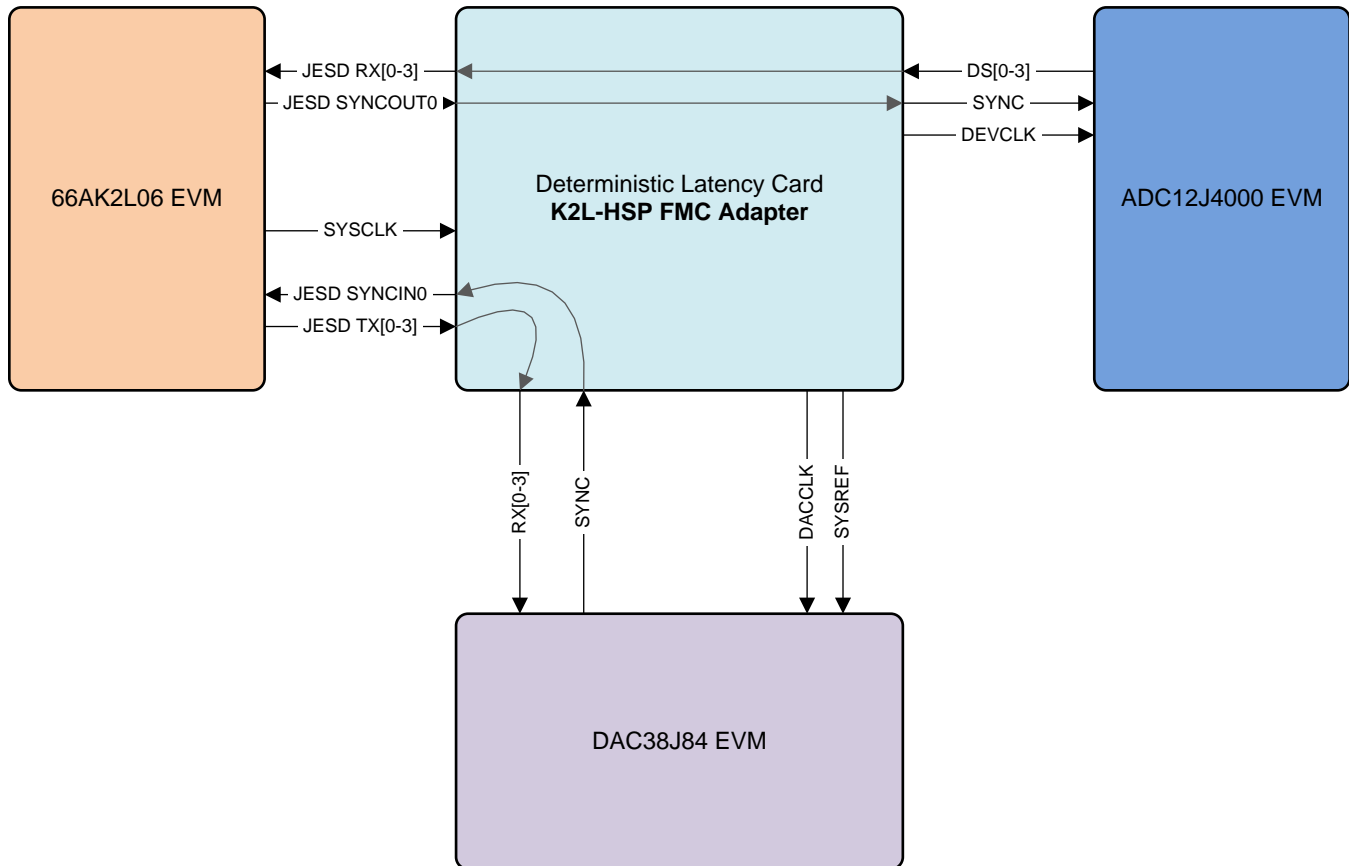


Figure 6. Hardware Connectivity Diagram

- JESD Tx[0-3] – Four 66AK2L06 JESD Transmit Lanes connecting with Rx[0-3] through DLC card
- Rx[0-3] – Four DAC38J84 JESD Input Lanes
- JESD Rx[0-3] – Four 66AK2L06 JESD Receive Lanes connecting with DS[0-3] through DLC card
- DS[0-3] – Four ADC12J4000 JESD output lanes
- JESD SYNCIN0 – 66AK2L06 SYNC Input connected with DAC38J84 SYNC through DLC card
- JESD SYNCOUT0 – 66AK2L06 SYNC Output connected with ADC12J4000 SYNC through DLC card
- SYSCLK – 122.88-MHz SYSCLK from 66AK2L06 routed through and back to DLC as clock input source for generating sampling clock and SYSREF clock for ADC and DAC
- DEVCLK – 2949.12-MHz Sampling Clock generated by DLC card for ADC12J4000
- DACCLK – 737.28-MHz Sampling Clock generated by DLC card for DAC38J84
- SYSREF – 23.04-MHz Clock for Synchronization generated by DLC card for DAC38J84

7 Test Data

7.1 Visualization of the Input, Tx, Rx Data

7.1.1 Tx Data

Figure 7 and Figure 8 show the Tx data captured with the RFSDK visualization tools. This data is the raw base band data that will be processed by the 66AK2L06 DFE and converted by the DAC. The two available data files consist of a dual-tone example and a multi-tone example. Each example consists of two 75-MHz bandwidth data files. The IQ data is sampled at 92.16 Msps (sets of dual tone or multitone signals).

TX Signal Capture @ DSP (4k FFT, Hanning)

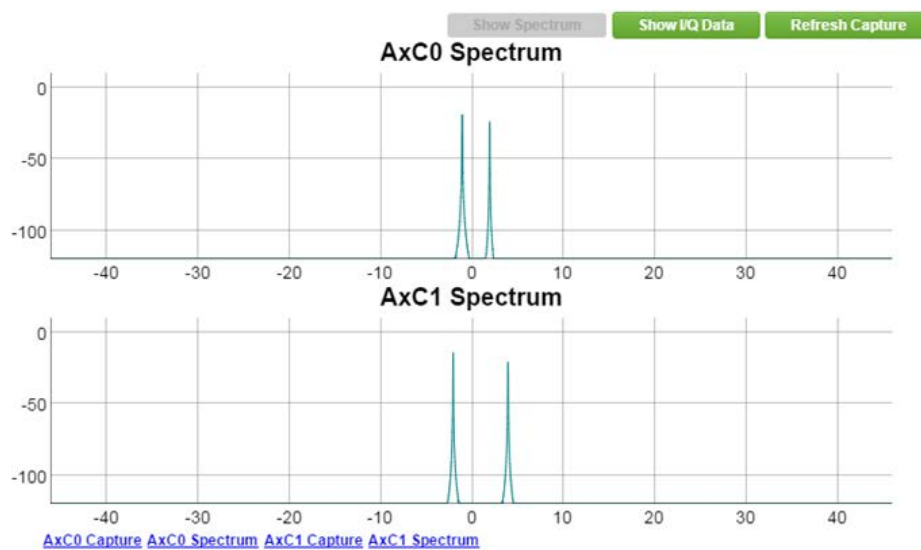


Figure 7. Tx Data - Dual Tone

TX Signal Capture @ DSP (4k FFT, Hanning)

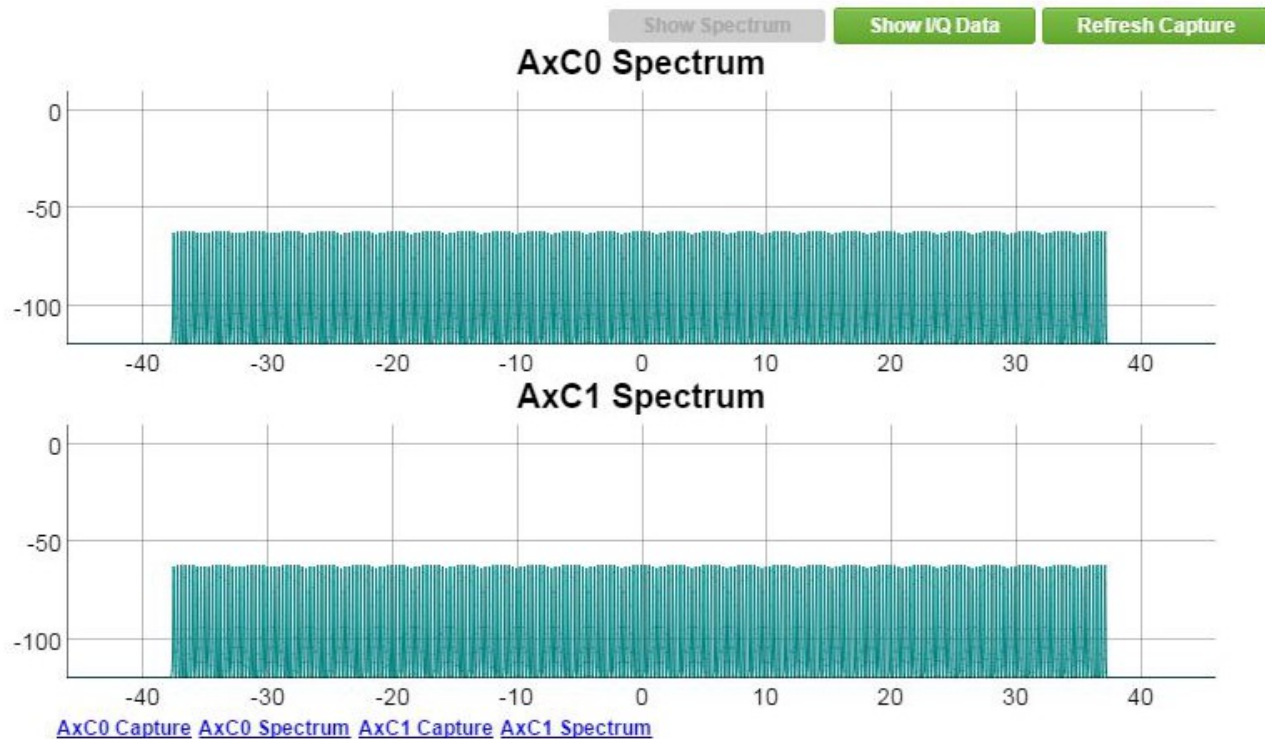


Figure 8. Tx Data - Multi Tone

7.1.2 Analog Output Data

[Figure 9](#) and [Figure 10](#) shows the Tx data captured with a spectrum analyzer. This data has been processed by the Tx path of the 66AK2L06 DFE and converted by the DAC. The data is captured at the output of the DAC. The two 75-MHz channels are frequency mixed and summed to a single output stream to represent a single 150-MHz channel.

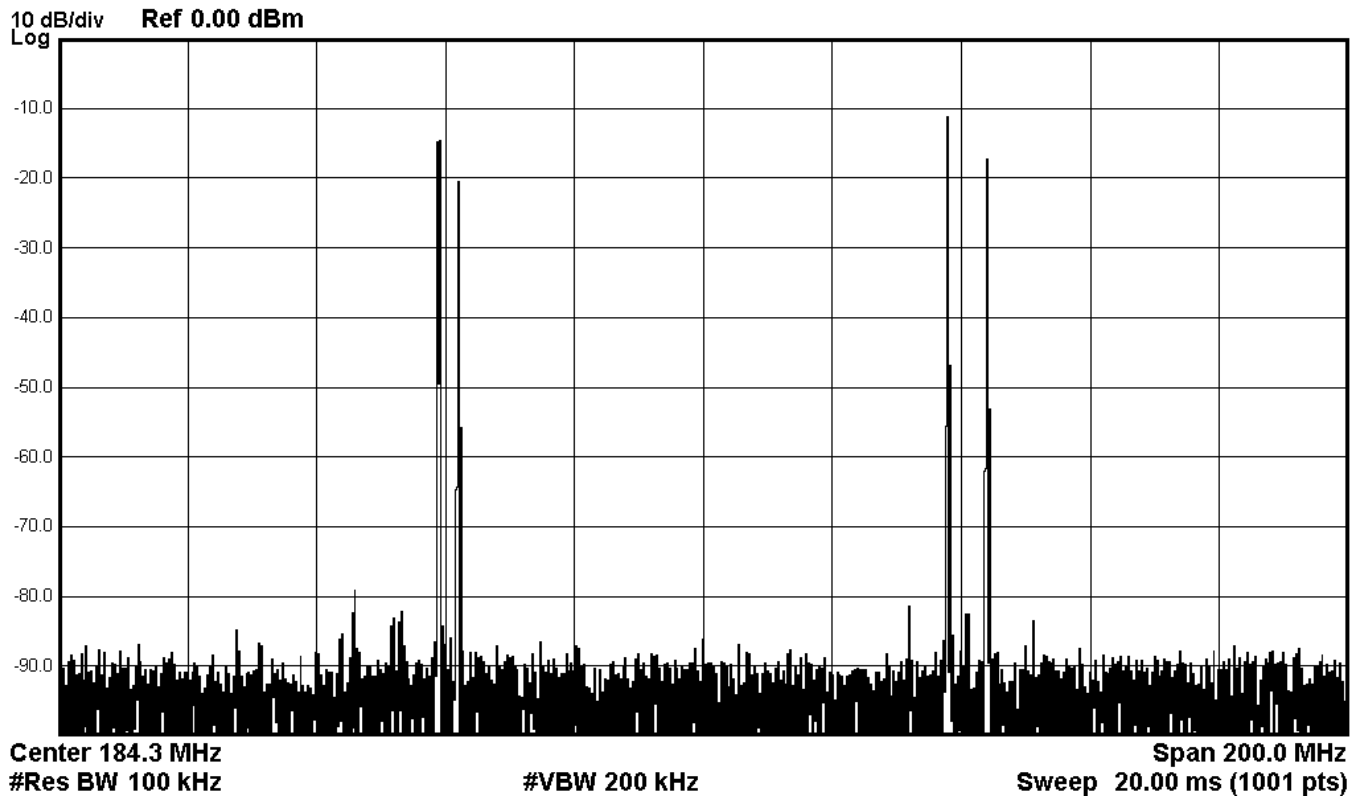


Figure 9. Analog Output Data – Dual Tone (–1.2-MHz and 2.4-MHz complex signals mixed to –43.5 and –43.5 MHz)

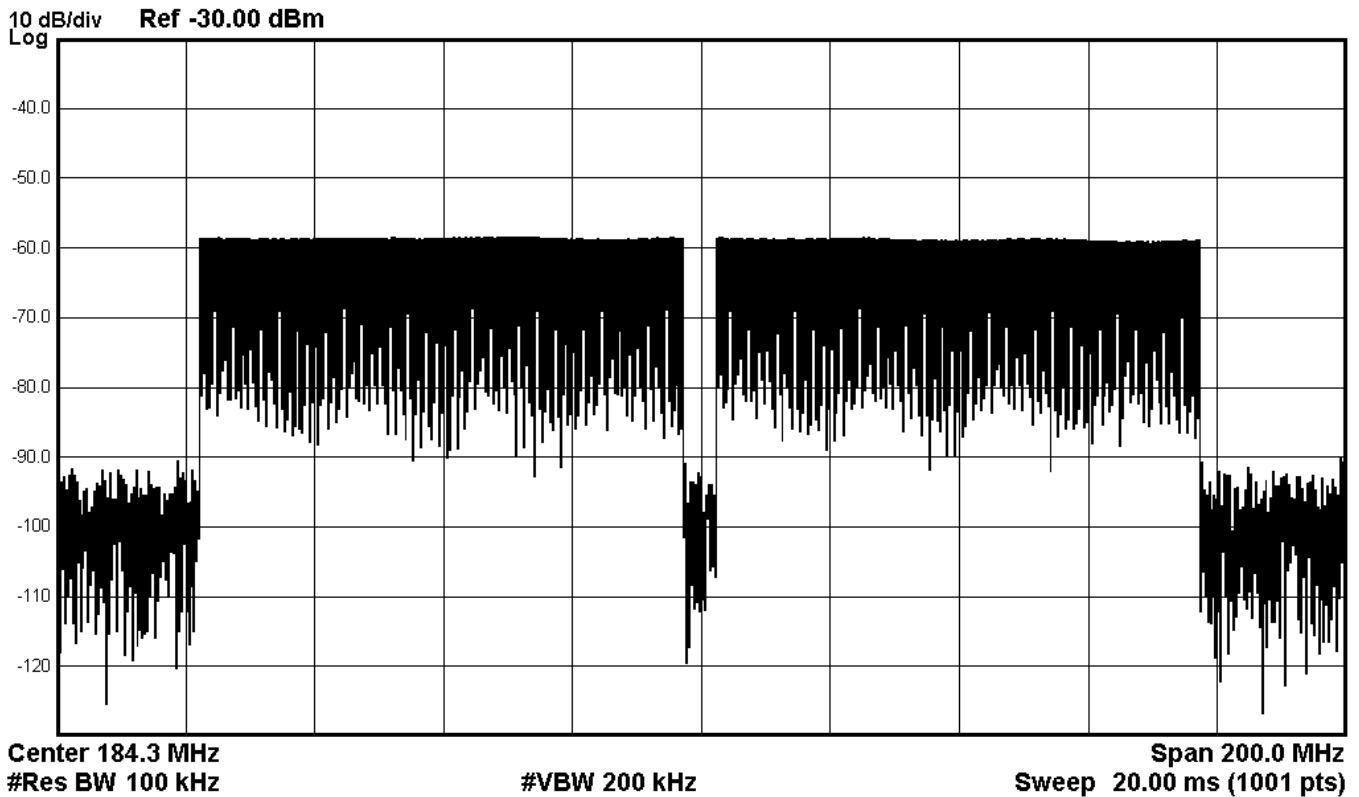


Figure 10. Analog Output Data – Multi Tone (240-tone signals mixed to -43.5 and 43.5 MHz)

7.1.3 Rx Data

Figure 11 and Figure 12 show the Rx data captured with the RFSDK visualization tools. This data is DAC output data that has been converted to digital format by the ADC and processed by the Rx path of the 66AK2L06 DFE. The data is captured in the 66AK2L06 DDR memory.

Combined RX Signal Capture @DSP

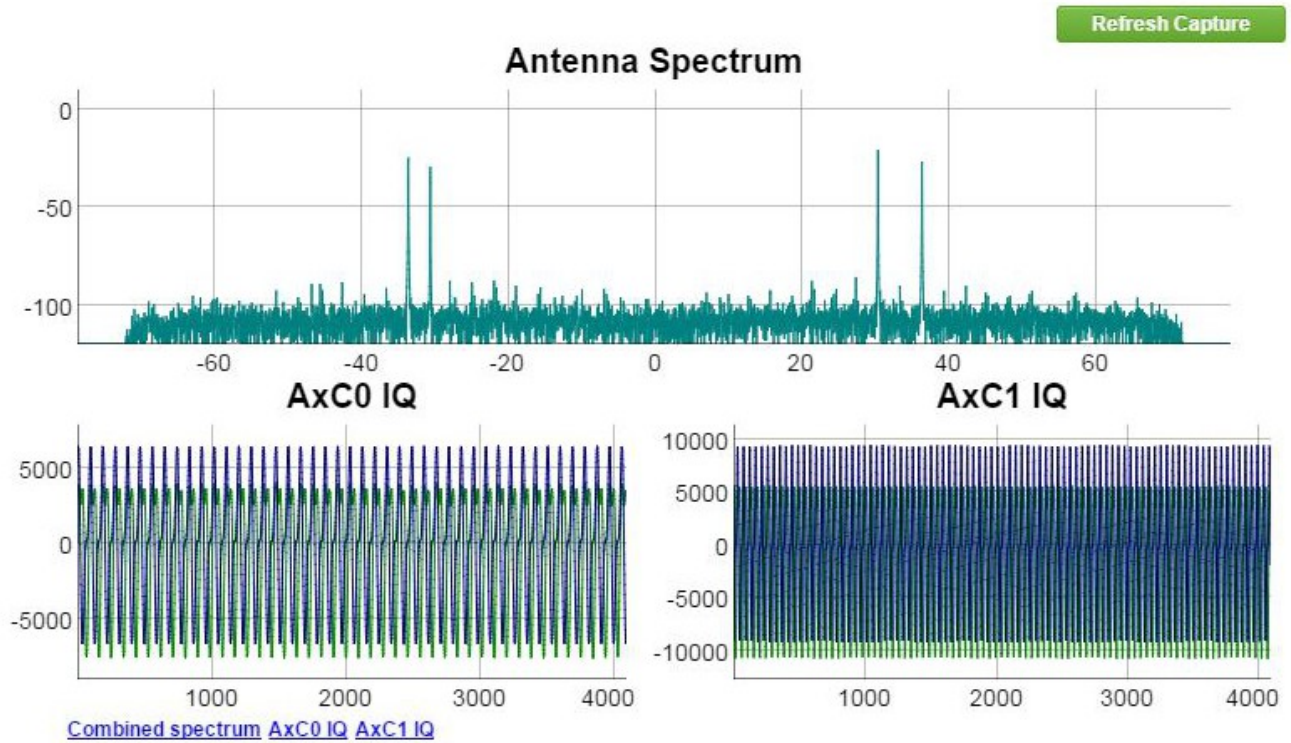


Figure 11. Rx Data - Dual Tone

Combined RX Signal Capture @DSP

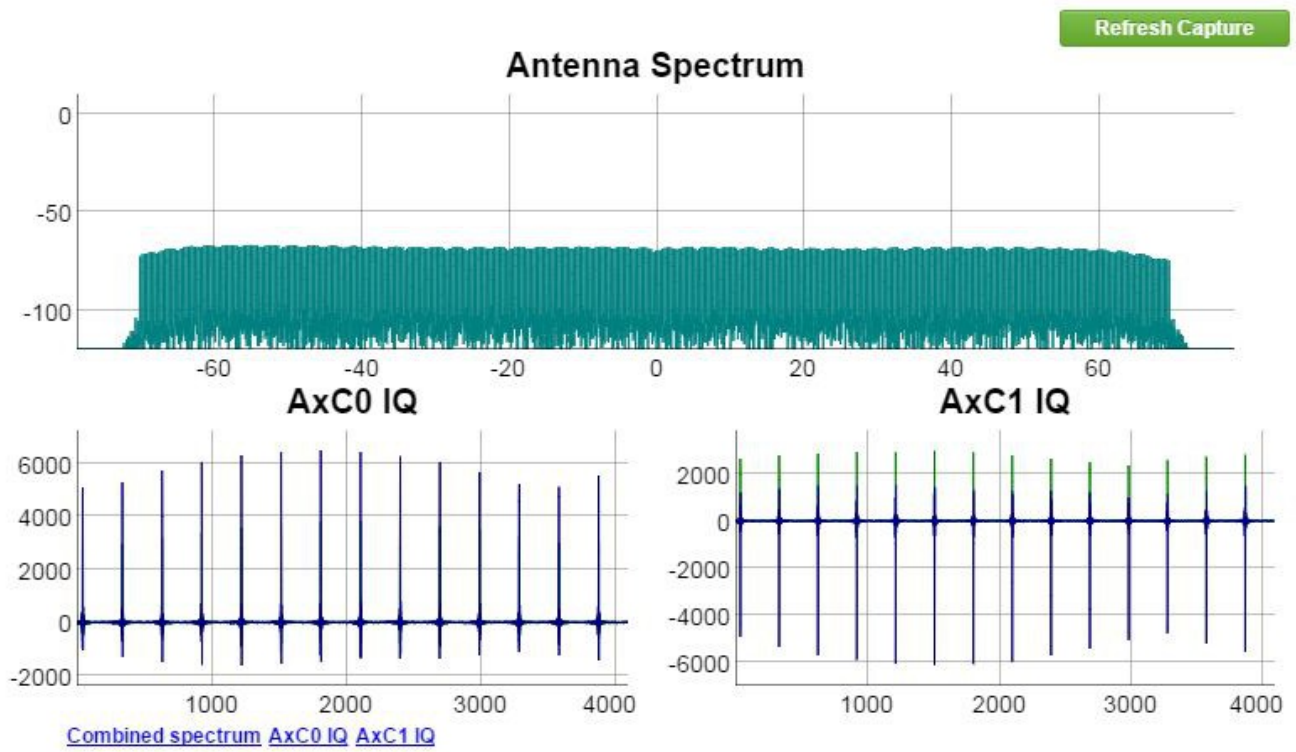


Figure 12. Rx Data - Multi Tone

7.2 Stress Testing

TI ran the demo for 17 hours. The DFE JESD status registers reported no errors.

8 Design Files

8.1 Schematics

To download the schematics for each board, see the design files at [TIDEP0034](#).

A reference schematic and Bill of Materials focus on the consolidated JESD204B interface and deterministic clocking solution between the 66AK2L06, ADC12J4000, and DAC38J84 devices. This reference design is based on the EVM environment previously described. This design consolidates the integration to demonstrate the fundamental interfaces between these devices without the existing EVM architecture. Because of this, the necessary JESD204B, SPI, GPIO, and clocking tree are simplified when compared to the EVM architecture.

Block diagrams are included with the schematic to provide an overall system context for the proposed consolidated design, however only the JESD204B, DAC, and ADC control and deterministic JESD clocking components are actually implemented in the schematic. For more information, see [Figure 13](#).

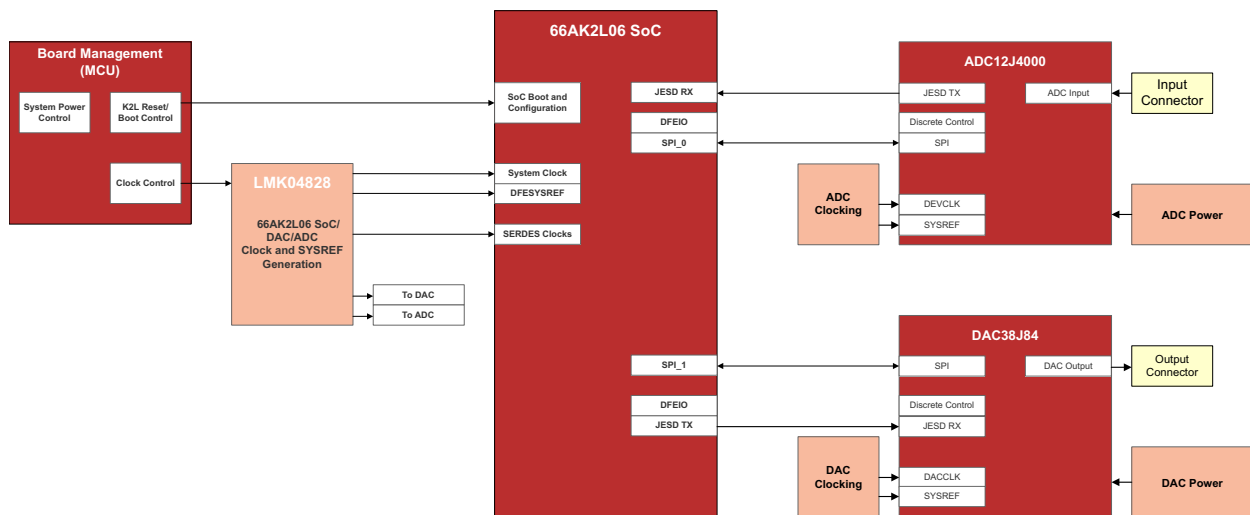


Figure 13. Schematic Diagram

The 66AK2L06 SoC masters the ADC12J4000 ADC through SPI port 0 and the dedicated DFEIO. Likewise, the 66AK2L06 SoC masters the DAC38K84 through SPI port 1. The use of dedicated SPI ports for both devices is for both signal integrity and SPI port bandwidth optimization. The use of the DFEIO programmable I/O allows the system designer to use both the dedicated DFE sub-system interrupts or the general-purpose GPIO system interrupts to control and respond to events from the ADC and DAC devices.

The 66AK2L06 JESD204B SERDES transmit channels are routed to the DAC38J84 SERDES receiver channels. The ADC12J4000 JESD204B SERDES transmit channels are routed to the 66AK2L06 SERDES receiver channels.

Although the current demonstration scenario only uses JESD Tx/Rx Lane 0 and Lane 1, the ADC and DAC devices include up to eight JESD204B SERDES channels. [Figure 13](#) shows the use of all four 66AK2L06 JESD Tx lanes and all four JESD Rx lanes as a proposed channel utilization scheme to aid in both initial system debug and bandwidth per SERDES channel optimization.

The LMK04828 JESD204B clock synthesizer is used to provide the device clock and periodic SYSREF pulses for the 66AK2L06, ADC12J4000, and DAC38J84 devices. The LMK04828 is also used to provide the SERDES reference clocks for the 66AK2L06. The LMK04828's dual PLL architecture and high-output frequency limit, along with a programmable SYSREF and delayed reference clocks, allows this single device to provide a low-jitter, deterministic-reference-clock source to all data acquisition and processing elements, SERDES transmitters, receivers, and baseband processing elements within this JESD204B system.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDEP0034](#).

8.3 PCB Layout Recommendations

- Refer to 66AK2L06 JESD204B specific section in the *KeyStone II Architecture Serializer/Deserializer (SerDes) User Guide* ([SPRUHO3](#)).
- Refer to 66AK2L06 JESD204B specific section in the *Hardware Design Guide for KeyStone II Devices* ([SPRABV0](#)).
- Refer to Layout section of *ADC12J4000 12-Bit 4 GSPS ADC With Integrated DDC* ([SLAS989B](#)).
- Refer to Layout section of *DAC3xJ84 Quad-Channel, 16-Bit, 1.6/2.5 GSPS, Digital-to-Analog Converters with 12.5 Gbps JESD204B Interface* ([SLASE17B](#)).
- Refer to Layout section of *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs* ([SNAS605AQ](#)).

8.4 Software Files

To download the software files, see the design files at [TIDEP0034](#).

- The MCSDK can be downloaded from [bioslinuxmcsdk](#).
- The RFSDK can be downloaded from [rfsdk](#).

9 References

1. *KeyStone II Architecture Digital Radio Front End User's Guide* ([SPRUHX8](#))
2. *KeyStone II Architecture Serializer/Deserializer (SerDes) User Guide* ([SPRUHO3](#))
3. *Hardware Design Guide for KeyStone II Devices* ([SPRABV0](#))

Revision History

Changes from Original (April 2015) to A Revision	Page
• Changed from 66AK2L06 JESD Attach to ADC12J4000 / DAC38J84 Design Guide throughout document	1
• Changed from 120 MHz to 150-MHz of Processing Bandwidth.....	1
• Changed from JESD throughout document.....	1
• Replaced block diagram.....	1
• Changed from 60-MHz channels to 75-MHz channels	6
• Added "sampled at 92.16 Msps"	6
• Deleted 60-MHz LTE data channel	6
• Changed from 196 to 240 single tones.....	6
• Changed from 60-MHz bandwidth to 75-MHz bandwidth	6
• Added "After DDUC, the sumchain combines DDUC channels into a stream. One channel is in each stream."	7
• Changed from –35 MHz to –43.5 MHz	7
• Changed from 35 MHz to 43.5 MHz	7
• Changed from 245.7 Msps to 368.64 Msps	7
• Deleted "This IQ data stream is sent to the JESD block." Replaced with "The Tx block passes the CDFR stream to the JESD block."	7
• Changed from 4.91 Gbps to 7.37 Gbps	7
• Changed from 245.7 MHz to 368.64 MHz of a sampling rate clock (DACCLK)	7
• Changed from 491.52 Msps to 737.28-Msps output data stream	7
• Changed from 122.88 MHz to 184.32 MHz.....	7
• Changed from 2457.6 MHz to 2949.12 MHz of sampling frequency	8
• Replaced "–122.88 MHz, then the mixed output is filtered to 0 IF." with "–184.32Mhz, resulting in 0IF then mixed output is filtered."	8
• Changed from 10 of factor to 8 of factor	8
• Changed from 245.76 MHz to 368.64 MHz of byte clock.....	8
• Replaced "where I and Q channels convert to 0 IF" with "where the IQ stream, is translated in frequency for the two channels to 43.5 and –43.5 Mhz. The Rx and Feedback block then decimates it by 2, to an 184.32 Mhz complex IQ rate."	8
• Changed from 4.91 Gbps to 7.37 Gbps	9
• Replaced "via a deterministic latency card" with "the K2L-HSP FMC adapter board that provides signal routing across the FMC interface and supports Deterministic Latency"	10
• Replaced "deterministic latency card" with "the K2L-HSP FMC Adapter board" throughout document	10
• Replaced "one FMC connector to two other FMC connectors" with "one Lamarr FMC to 2 data converter FMC connectors, one for ADC and one for DAC.".....	10
• Added DSP+ARM Processor JESD204B.....	10
• Changed from 2457.6 to 2949.12-MHz sampling clock for ADC12J4000.....	12
• Changed from 245.76 to 737.28-MHz sampling clock for DAC38J84	12
• Changed from 245.76 to 23.04-MHz clock for synchronization.....	12
• Changed from three to two available data files	13
• Changed from 60 to 75-MHz bandwidth data files	13
• The IQ data is sampled at 92.16 Msps (sets of dual tone or multitone signals).....	13
• Changed from 60-MHz channels to 75-MHz channels	14
• Changed from 120-MHz channel to 150-MHz channel	14
• Added "–1.2-MHz and 2.4-MHz complex signals mixed to –43.5 and –43.5 MHz" to Analog Output Data Dual Tone Figure.....	15
• Added "(240-tone signals mixed to –43.5 and 43.5 MHz)" to Analog Output Data Multi Tone Figure	16

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