TIDA-00425 12 Gbps SAS-3 Link Extender

Silicon Valley Analog Datapath Solutions
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ABSTRACT

Storage applications utilizing the SAS-3 standard often involve physically large systems and long cables. This reference design can be used to compensate for some of the attenuation effects seen in these areas. A critical part of the SAS-3 operation at 12 Gbps is link training. During link training the SAS-3 Transmitter and Receiver communicate with each other to optimize the signal integrity on the channel. With the DS125BR401A in the channel helping to compensate for a portion of the overall channel attenuation, the channel appears “shorter” to the Receiver. This allows a larger range of channels to support SAS-3 communication at 12 Gbps.

The DS125BR401A SAS-3 reference design provides a high band-width platform which highlights the signal integrity and signal conditioning capabilities of the *DS125BR401A* as it relates to the SAS-3 12 Gbps standard. MiniSAS-HD connectors are used as the input and output connections to this board. This allows standard external miniSAS-HD cables to connect to existing SAS-3 systems. The DS125BR401A SAS-3 board can be controlled via jumpers or via the SMBus with the aid of the graphic user interface based tool SigCon Architect. The ‘DS125BR401A’ device profile within this GUI can be used to read and write register setting

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1. Features

- 4 Lane Repeater with Equalization up to 12 Gbps
- Linear Equalization allows for Link Training protocol for SAS3
- B-Side: Receive Equalization up to 24 dB at 6 GHz
- B-Side: Transmit de-emphasis driver >10 dB
- B-Side: Transmit voltage control: 700 – 1300 mV
- A-Side: Receive Equalization up to 10 dB at 6 GHz
- A-Side: Linear output driver
- A-Side: Maximum output voltage range over 1200 mV
- Programmable by Pin selection (Pin Mode) or SMBus interface
- Single supply operation: VIN = 3.3V±10% or VDD = 2.5V±5%
- -40°C to +85°C Operation
- 4 kV HBM ESD rating
- High speed signal flow–thru pin-out package: 54-pin WQFN (10 mm x 5.5 mm, 0.5 mm pitch)

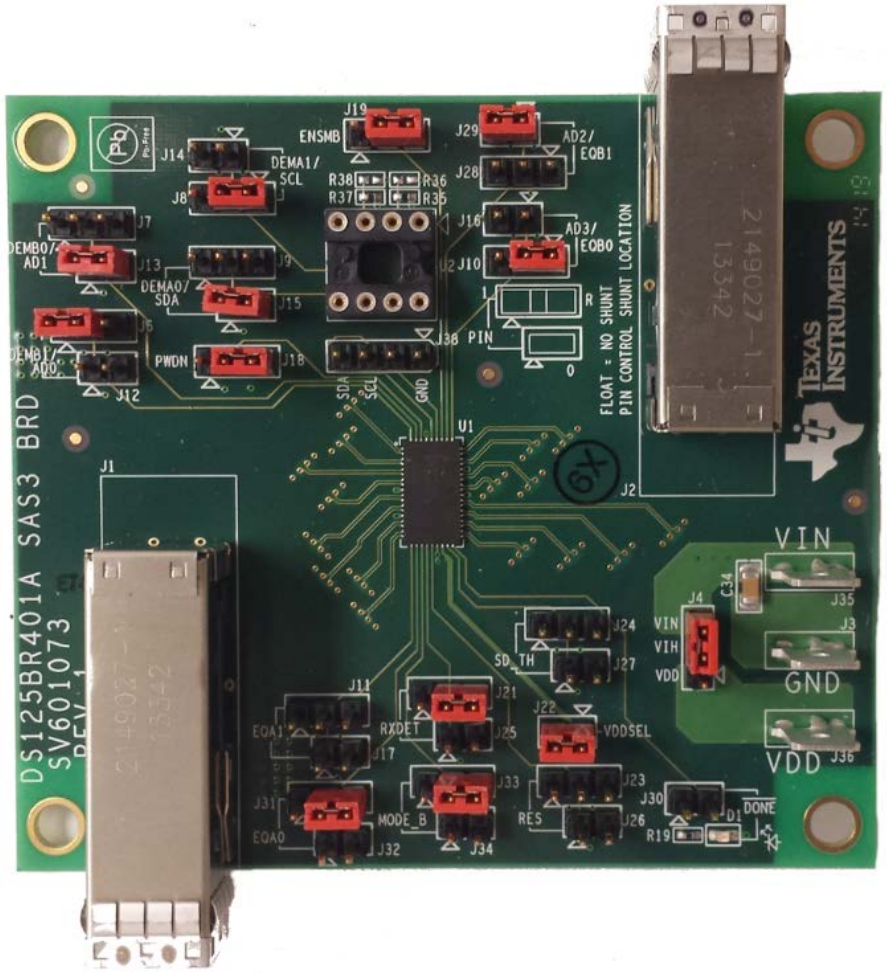


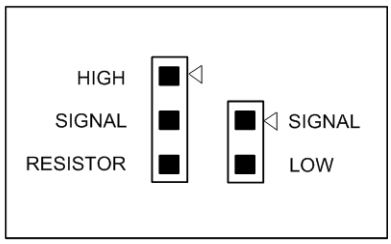
Figure 1: 12 Gbps SAS-3 Link Extender Board

2. Hardware Description and Setup

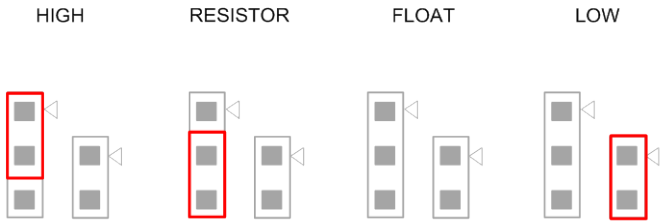
2.1 4-Level IO Control

The 4-level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30K pull-up and a 60K pull-down connected to the pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Figure 2: Header Pin Description



4-LEVEL CONTROL



PIN HEADER CONNECTION

Table 1: Jumpers to set the 4-Level input control pins

	4-Level IO Settings	Jumper Setting
0	1K to GND	Pin 1 – Pin 2 on Header_2
R	20K to GND	Pin 2 – Pin 3 on Header_3
F	FLOAT (open)	No Jumper
1	1K to VIH	Pin 1 – Pin 2 on Header_3

NOTE: Only 1 of the signal pins at a time should be tied to another pin with a jumper. Using a jumper on both signal pins simultaneously results in an indeterminate voltage level.

2.2 Jumper Connection Overview

Table 2: Control Pin Definitions and Jumper Connections

Component	Name	Function
J1	IA0+, IA0-, IA1+, IA1-, IA2+, IA2-, IA3+, IA3- OB0+, OB0-, OB1+, OB1-, OB2+, OB2-, OB3+, OB3-	High-speed differential inputs/outputs
J2	OA0+, OA0-, OA1+, OA1-, OA2+, OA2-, OA3+, OA3- IB0+, IB0-, IB1+, IB1-, IB2+, IB2-, IB3+, IB3-	High-speed differential inputs/outputs
J4	VIH	VIN (3.3V) or VDD (2.5V) to VIH power
J22	VDD_SEL	F = 2.5V mode (internal LDO disabled) 0 = 3.3V mode (internal LDO enabled)
J30	$\overline{\text{DONE}}$	Valid Register Load Status Output RED = External EEPROM load failed or incomplete GREEN = External EEPROM load passed
J24, J27	SD_TH	SD_TH – Signal detect threshold level for Channel B (F = Default level)
J23, J26	RES	Reserved – This input must be left Floating
J21, J25	RX_DET	RX_DET – Controls the receiver detect function (1 = Default level for SAS)
J33, J34	MODE_B	MODE_B controls output driver characteristics for channel B 0 = SAS 1,2 R = SAS3 without De-emphasis (Default level) 1 = SAS3 with De-emphasis
J11, J17	EQA1	PIN MODE – EQ control for channel A inputs
J31, J32	EQA0	PIN MODE – EQ control for channel A inputs
J19	ENSMB	ENSMB = 0 – PIN MODE ENSMB = 1 – SMBus (Slave Mode) ENSMB = F – SMBus (Master Mode – load configuration from EEPROM)
J18	PWDN	1 = Low power – power down 0 = Normal operation (Default level)
J38	SDA, SCL	Optional SMBus access pins. See the datasheet for additional information on SMBus

Jumper Connection Overview (continued)

Component	Name	Function
U2	EEPROM	Socket for optional EEPROM
J28, J29	EQB1 or AD2	PIN MODE – EQ control for channel B inputs SMBus Mode – Device address bit 2
J10, J16	EQB0 or AD3	PIN MODE – EQ control for channel B inputs SMBus Mode – Device address bit 3
J9, J15	DEMA0 or SDA	PIN MODE – DEM control for channel A outputs SMBus Mode – ENSMB = 1
J8, J14	DEMA1 or SCL	PIN MODE – DEM control for channel A outputs SMBus Mode – ENSMB = 1
J6, J12	DEMB1 or AD0	PIN MODE – DEM control for channel B outputs SMBus Mode – Device address bit 0
J7, J13	DEMB0 or AD1	PIN MODE – DEM control for channel B outputs SMBus Mode – Device address bit 1

Jumper Connection Overview

1. Connect J22 (VDD_SEL):

- **FOR 3.3V MODE:**
  Tie pin 1 to pin 2 (VDD_SEL tied to GND) on J22.
- **FOR 2.5V MODE:**
  Do not connect a jumper (VDD_SEL left OPEN).

2. Connect J4 (VIH):

- **FOR 3.3V MODE:**
  Tie pin 2 to pin 3 (VIH tied to VIN).
- **FOR 2.5V MODE:**
  Tie pin 1 to pin 2 (VIH tied to VDD).

3. Set the control jumpers for normal operation:

- **J33 – MODE_B = R (SAS3 without de-emphasis)**
- **J21 – RXDET = 1 (Input termination always 50Ω)**
- **J18 – PWDN = 0 (Tie pin 2 to pin 3 for normal operation)**

4. Pin Mode - Set the input equalization level:

- **For external pin mode control of the equalization level:**
- **J19 – Set ENSMB = 0 (Tie pin 2 to pin 3)**
- **J10, J16, J28, J29 – EQB – Refer to Table 5 in the DS125BR401A datasheet.**
- **J11, J17, J31, J32 – EQA – Refer to Table 6 in the DS125BR401A datasheet.**
- **Refer to Table 1 for information on the 4 level settings.**

5. Pin Mode - Set the output VOD and De-emphasis level:

- **For external pin mode control for the VOD and De-emphasis level:**
- **J19 – Set ENSMB = 0 (Tie pin 2 to pin 3)**
- **J11, J17, J31, J32 – EQA – Refer to Table 6 in the DS125BR401A datasheet.**
- **J6, J7, J12, J13 – DEMB – Refer to Table 7 in the DS125BR401A datasheet.**
- **J8, J9, J14, J15 – DEMA – Refer to Table 8 in the DS125BR401A datasheet.**
- **Refer to Table 1 for information on the 4 level settings.**

6. SMBus Slave Mode - Set the EQ, VOD, De-emphasis level:

- **For SMBus mode control of the EQ, VOD and DEM level:**
- **J19 – Set ENSMB = 1 (Tie pin 1 to pin 2)**
- **J8 – Set SCL = 1 (Tie pin 1 to pin 2)**
- **J9 – Set SDA = 1 (Tie pin 1 to pin 2)**
- **Connect SDA, SCL and GND to J38.**
  Refer to datasheet EQ, VOD and DEM register information.

3. Test Data and Recommended SAS-3 Settings

The following EQ, VOD, and DEM settings have been tested for SAS-3 12 Gbps compliance with a SAS-3 expander ASIC. The cable lengths tested ranged from 1 – 12 meters with no more than 7 meters on one side of the DS125BR401A. Refer to Table 3 for recommended settings over the specified cable length. A portion of the test data is shown below in Table 4.

Figure 3: SAS-3 Test Setup

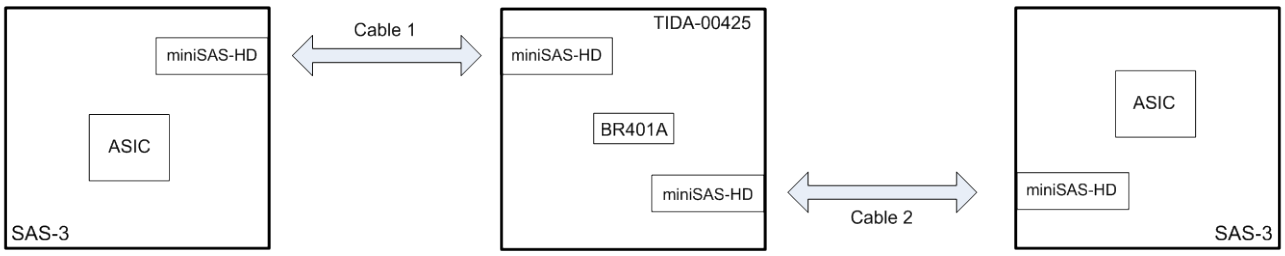


Table 3: SAS-3 System Test Data with DS125BR401A

Cable Lengths		DS125BR401A Settings						BER Testing Result
Cable1	Cable 2	CH-A EQ	CH-A VOD	CH-A DEM	CH-B EQ	CH-B VOD	CH-B DEM	
2m	**7m**	0x03'h	110'b	0x00'h	0x03'h	1.4Vpp	0x00'h	**Pass**
3m	**7m**	0x03'h	110'b	0x00'h	0x03'h	1.4Vpp	0x00'h	**Pass**
5m	**7m**	0x03'h	110'b	0x00'h	0x03'h	1.4Vpp	0x00'h	**Pass**
7m	**2m**	0x03'h	110'b	0x00'h	0x00'h	1.4Vpp	0x00'h	**Pass**
7m	**3m**	0x03'h	110'b	0x00'h	0x00'h	1.4Vpp	0x00'h	**Pass**
7m	**5m**	0x03'h	110'b	0x00'h	0x00'h	1.4Vpp	0x00'h	**Pass**

NOTE: Channel-A DEM is listed as VOD_DB in the device datasheet

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NOTE: The mini-SAS HD cable running from the system ASIC to the DS125BR401A (Table 4, Column 2) connects to the top connector on the DS125BR401A SAS board given the orientation shown in Figure 1. The mini-SAS HD cable running from the DS125BR401A to the system ASIC (Table 4, Column 4) connects to the bottom connector.

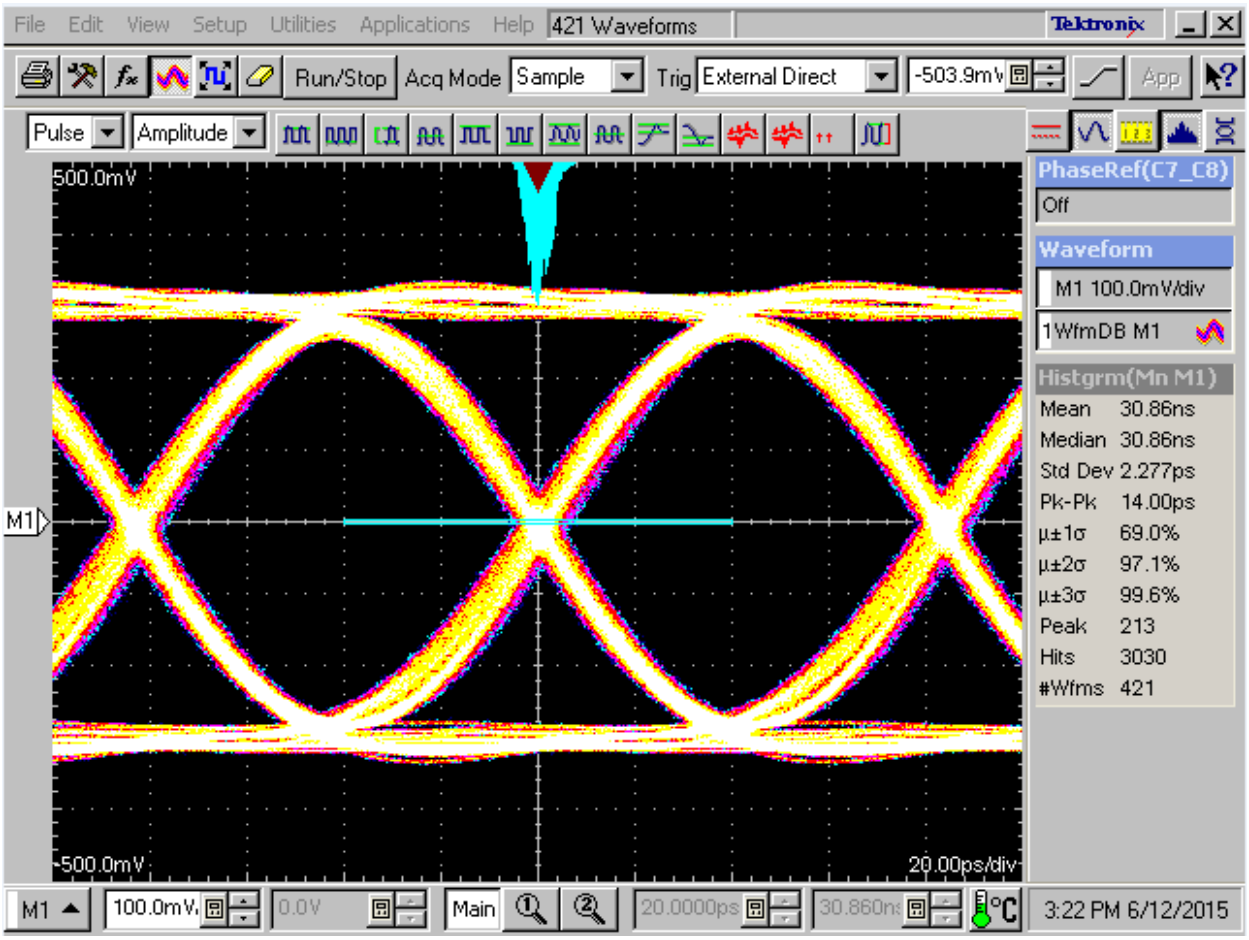
Table 4: Recommended SAS-3 EQ, VOD, and De-Emphasis Settings

	A Channels	B Channels
Equalization Level	0x01'h – 0x03'h	0x00'h – 0x03'h
VOD Level	110'b (1:1 ratio Vi/Vo)	1.4 Vpp
De-Emphasis Level	0x00'h	0x00'h

Although testing was completed with DS125BR401A CTLE = 0x03'h for Channel A, lower equalization levels are often used if the attenuation between SAS-3 Tx and the DS125BR401A is less than -8 dB.

With the miniSAS-HD cables removed and the "SAS-3 Link Extender" design is tested directly, high quality waveforms are observed on the output ports.

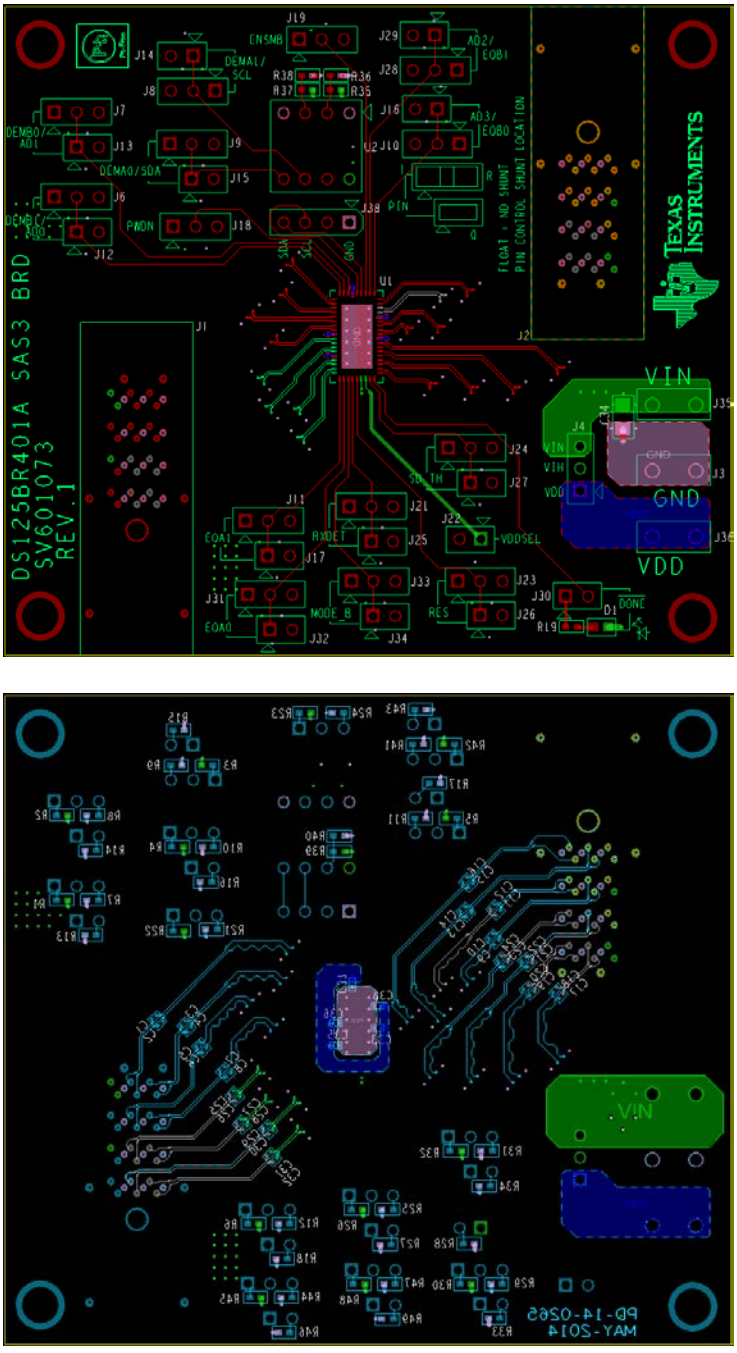
Figure 4: 12 Gbps SAS-3 Output Waveform



4. Layout

The following Figures show the DS125BR401A SAS3 board layout. The evaluation board controls signal integrity functions via jumpers. The DS125BR401A is very compact and low power. The WQFN package offers an exposed thermal pad to enhance electrical and thermal performance. This must be soldered to the copper landing on the PCB.

Figure 5: Top and Bottom PCB Assembly



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