TI Design: TIDA-00394
Dual Power Path Multiplexer Reference Design

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Circuit Description

Many systems require a backup battery to provide power in the event of a power outage. Switching between the main power and the backup battery power without incurring significant efficiency degradation or cost is a tricky challenge. TIDA-00394 provides a high accuracy, low current solution for systems using a 12 V rail at a lower cost than most existing devices. The primary rail is intended to be the main power supply for the system, and is selected when the rail voltage is above the programmed under-voltage (UVLO) minimum, regardless of the other rail's status. When the primary rail goes below the UVLO minimum, the circuit will switch to the secondary (battery backup) rail if the secondary rail is above its programmed UVLO minimum. When both rails are below the UVLO minimum, neither rail is selected. The back-to-back PMOS switches allow for the input voltages of either rail to be higher than the opposite rail without any risk of conduction.

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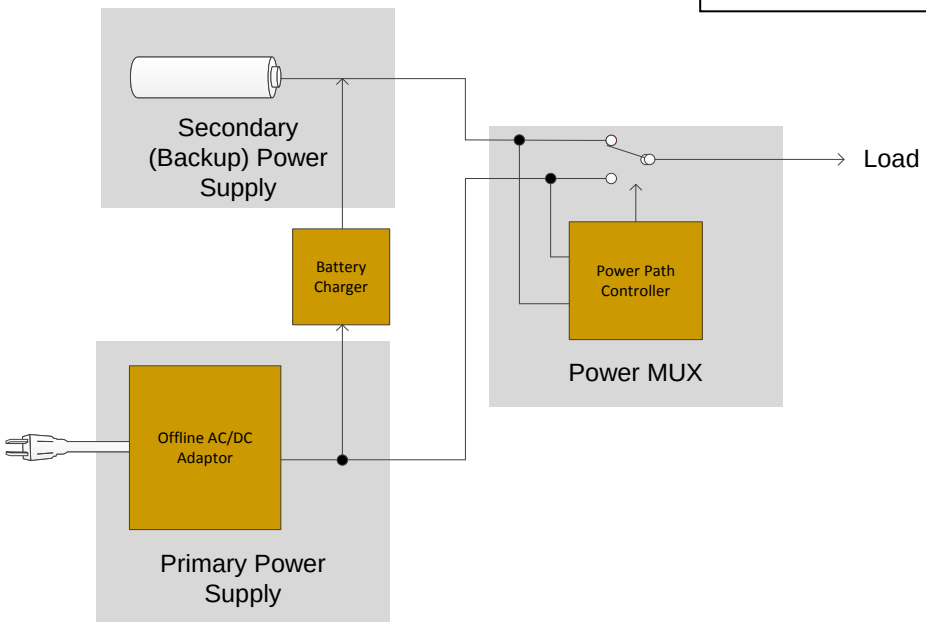

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1 Design Summary

The design requirements are as follows:

- Primary Power Rail Input Voltage: 12 V ± 10 %
- Secondary Battery Backup Rail Input Voltage: 14.4 V – 12.6 V
- Primary Power Rail Under Voltage Lockout Threshold: 10.8 V ± 2 %
- Secondary Battery Backup Rail Under Voltage Lockout Threshold: 12.6 V ± 2 %
- Maximum Rail Current: 200 mA
- Multiplexer Current Consumption During Battery Selection Mode: 50 µA max.

Parameters	Goal	Measured
Primary Rail UVLO Threshold, $V_{UVLOPRI}$	10.8 V	10.86 V
Secondary Rail UVLO Threshold, $V_{UVLOSEC}$	12.6 V	12.66 V
Secondary Iq (Secondary VIN = 13.5 V, Primary = 0 V)	50 µA	28 µA
Secondary Iq (Secondary VIN = 13.5 V, Primary = 12 V)	300 µA	278 µA

Table 1: Comparison of Design Goals and Measured Performance

2 Theory of Operation

The ubiquitous method for power rail selection between two separate power rails, i.e. a primary power supply and a battery backup, has traditionally been done with two diodes in series from each supply, or, power supply “OR-ing”. OR-ing diodes provide an easy solution for the rail selection; however, poor efficiency performance and no enable/disable functionality make basic OR-ing hardly useful for many applications. Additionally, in circuits where the desired rail is not necessarily the highest voltage, such as some battery backup systems, basic OR-ing is not feasible because the battery can continuously back-feed the primary supply.

Offline systems that require constant power through power outages often use a battery for backup power when the primary (offline) power source goes down. **Figure 1** shows a common approach for backup multiplexer power – a charging circuit is used from the primary supply to ensure the battery is constantly charged during primary power operation. When the primary power falls below the minimum acceptable supply voltage, the backup battery is switched in to provide power to the load by a Power MUX and the battery charger is disabled. The Power MUX must switch the loads without allowing the supply voltage to the load to drop below critical levels, and operate at very low bias currents when the battery is in use in order to maximize the battery lifetime during power outages.

The TPS3701 is a high voltage window comparator well suited to provide the signal detection required for the power path controller circuitry. Its high voltage capability (36 V max.) yields a robust voltage range for 12 V to 24 V systems. The low Iq (7 µA nominal) makes it capable of providing detection with minimal current consumption.

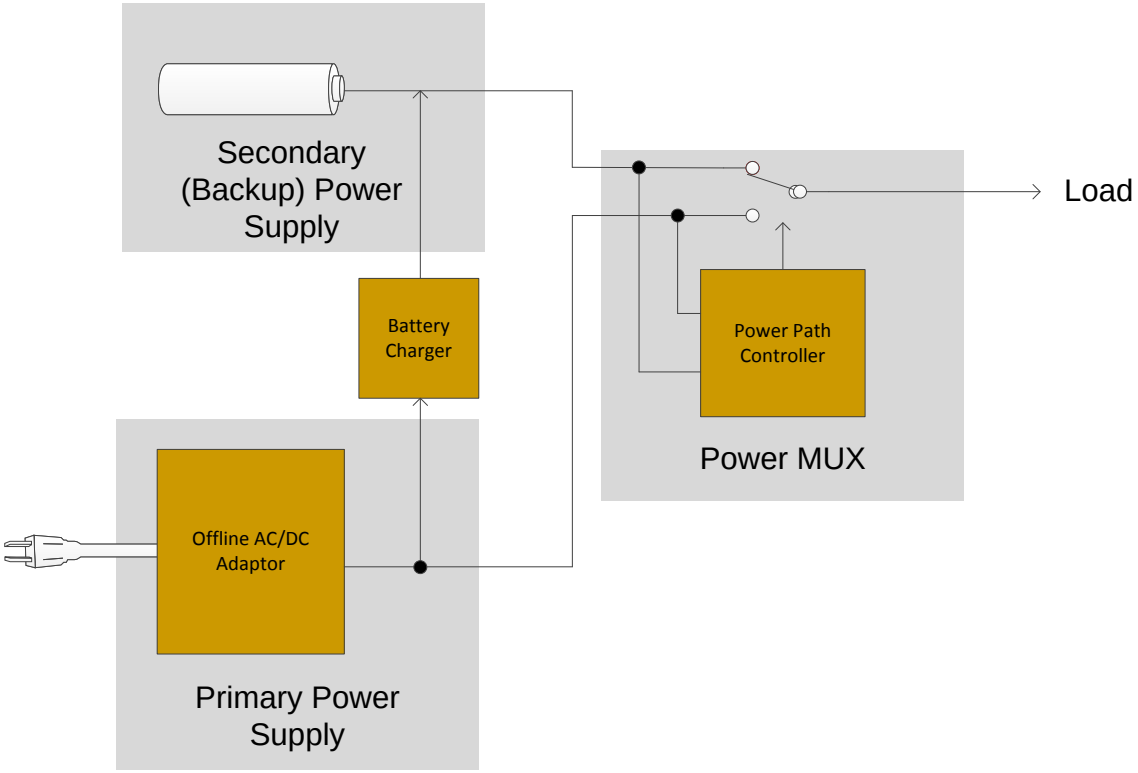

Figure 1: Battery Backup Block Diagram

The implementation architecture for the power multiplexer can be seen in **Figure 2**. The switches are implemented with dual P-type MOSFETS with the sources connected to block any positive or negative current flow when the V_{GS} voltage of the MOSFET is higher than the respective device threshold. The TPS3701 is used to detect the voltages at the primary and secondary rails. The outputs of the voltage supervisor, along with additional circuitry, will control the gates of the switches, ensuring that only one channel is connected at a time and the desired priority logic is enforced.

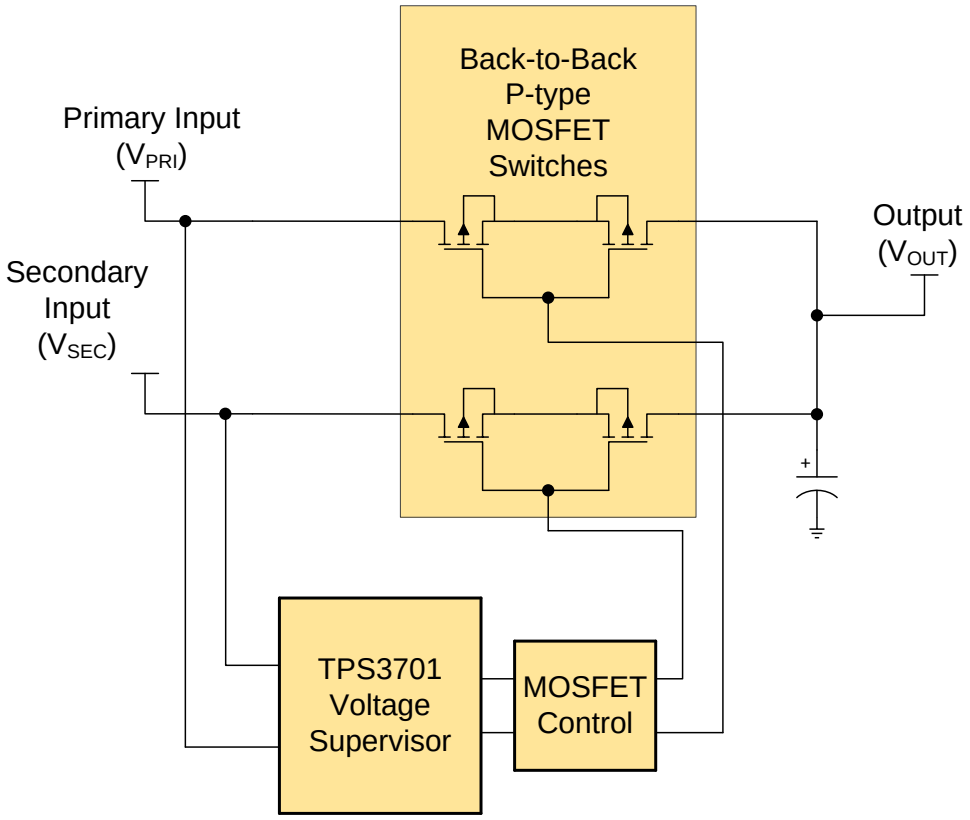

Figure 2: Power Multiplexer Block Diagram

This simple approach can offer a lower current consumption and higher threshold accuracy than other more expensive solutions. The low nominal Iq of the TPS3701 (7 µA) with the additional resistor current consumption of 21 µA, gives a total current of only 28 µA when the secondary input is selected. The threshold accuracy of the TPS3701 is 0.75%, and assuming 1% resistors are used for the sense resistor divider, the total accuracy of the threshold voltages are approximately 1.75%.

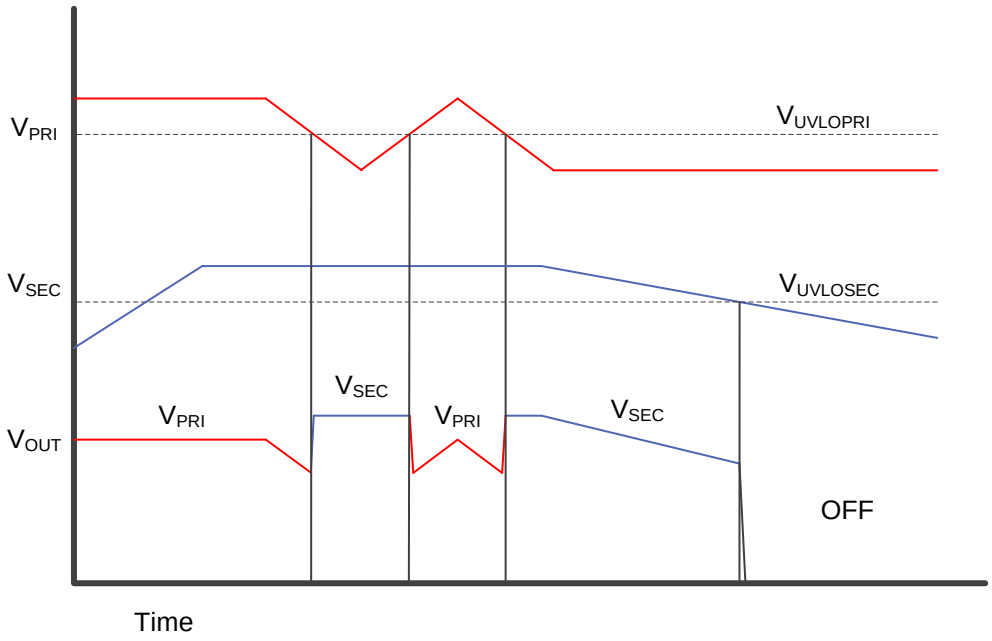

Figure 3: Functional Timing Diagram

The dual power path multiplexer presented in this design features the ability to allow either supply (battery or primary) to operate at a higher voltage. **Figure 3** shows the behavior of the circuit when the V_{PRI} or V_{SEC} voltages cross the UVLO threshold voltages. The rail selection is determined by the programmed UVLO threshold voltage levels at each rail with the primary rail given priority; see **Table 2** for the logic states.

Primary Power Supply	Secondary Power Supply	Power to Load (V_{OUT})
$V_{PRI} > V_{UVLOPRI}$	$V_{SEC} > V_{UVLOSEC}$	V_{PRI}
$V_{PRI} > V_{UVLOPRI}$	$V_{SEC} < V_{UVLOSEC}$	V_{PRI}
$V_{PRI} < V_{UVLOPRI}$	$V_{SEC} > V_{UVLOSEC}$	V_{SEC}
$V_{PRI} < V_{UVLOPRI}$	$V_{SEC} < V_{UVLOSEC}$	Disconnect

Table 2: Power MUX Rail Selection Truth Table

3 Component Selection

See the schematic in section 4 for the reference designators of each component.

3.1 Threshold Selection

The UVLO threshold voltages are determined by selecting the resistor values for the divider network created by R1/R2 for the primary rail and R3/R4 for the secondary rail. Selecting high value resistors helps reduce the overall current consumption. For this design, R1 and R3 were chosen to be 2 MΩ and R2 and R4 were calculated from equation 1 below:

$$R_{2,4} = \frac{2\ M\Omega \cdot V_{IT}}{V_{UVLO} - V_{IT}}$$

Where

$R_{2,4}$ = Resistance value of R2 for primary rail or R4 for secondary rail

V_{IT} = Input threshold voltage for the TPS3701. For the primary rail, V_{IT} rising is 0.400 V. For the secondary rail, V_{IT} rising is 0.405 V

V_{UVLO} = Desired undervoltage lockout threshold for primary or secondary rail.

Equation 1

For additional information on the TPS3701 voltage window comparator, see SBVS240.

3.2 Pullup/Pulldown Resistor Selection

Resistors are required to discharge the PMOS gate to source voltage when the corresponding rail is turned off. Referring to Figure 4, R5, R6 and R7 pull up the gates of Q1, Q2 and Q3, respectively. R8 is used as a "pulldown" resistor – it slows the time that the gate of Q3 is pulled low, or, ON. In addition to current consumption, the timing of the switches are controlled by the pullup/pulldown resistors. A critical timing consideration occurs in the case that the primary rail shuts off and the secondary rail is turning on. In light load conditions, when $V_{SEC} > V_{PRI}$, both channels can be turned on simultaneously (known as "cross-conduction"), which can result in V_{PRI} being pulled high by V_{SEC}, and ultimately resulting in an oscillation. Selecting R8 to be at least a factor of 10 higher than R5 allows the enhancement of Q3 to be sufficiently delayed, eliminating any cross-conduction in this situation.

Note that delaying the switch conduction will result in a period of time where both switches are off, creating a "break-before-make" condition. During this time, all current to the load must be provided by the output capacitor, C1. C1 must be properly selected to ensure that the load voltage does not drop below the minimum required voltage at the maximum load during these events. Equation 2 can be used to approximate the time required for the secondary switch to enable.

$$t_{EN} = -\frac{R_1 R_2 C_{iss}}{R_1 + R_2} \ln\left(\frac{-2V_{th}}{V_{SEC}} - 1\right)$$

Where

t_{EN} = Time from threshold detection to Q3 conduction.

C_{ISS} = Input capacitance parameter of Q3

V_{TH} = Minimum threshold voltage of Q3 (for SI3993 max = -1.0 V, min = -3.0 V)

Equation 2

For this design, t_{EN} is calculated to be 65 µs. Equation 3 gives an approximation of how much output capacitance is necessary to maintain the output voltage within a specified drop for a given t_{EN}. Note equation 3 assumes a resistive load.

$$C_L = -\frac{t_{EN}}{R_L}\frac{1}{\ln(1-\frac{\%Drop}{100})}$$

Where

t_{EN} = Time from threshold detection to Q3 conduction.

C_L = Output Capacitance (C1)

R_L = Output Load Resistance

%Drop = Percentage of output voltage drop that can be tolerated during t_{EN}

Equation 3

For this design (t_{EN} = 65 µs, R_L = 65 Ω), a 2.5% drop in VOUT during this time period results in a required 40 µF of capacitance; a 47 µF capacitor was selected.

3.3 Power Transistor Selection

Q1 and Q3 are required to conduct the full load current when their respective channels are selected, therefore the power loss associated with the resistance of the FET when fully enhanced (R_{DSON}) must be considered when making the FET selection. The devices selected for this design yield a good compromise between size and R_{DSON}. In addition to R_{DSON}, the maximum and minimum V_{GS} and V_{DS} voltage rating of the device must exceed the maximum input voltage requirement. Devices that tolerate VIN_MAX for the minimum V_{DS} rating are common; devices with higher V_{GS} ratings are less common. This is required for the primary channel because the gate will be pulled to ground when it is enabled, and with the source at VIN. The V_{GS} min./max. rating for Q1 and Q3 is ±20 V.

3.4 Logic Transistor Selection

Q2 provides the logic selection of the primary rail, forcing a NAND operation between OUTA and OUTB with the output on the gate of Q3. This ensures that the secondary rail only turns on when both OUTA and OUTB are high. A dual small-signal FET with V_{GS} and V_{DS} ratings that exceed VIN_MAX is suitable for this device; using a low-R_{DSON} FET (i.e. a typical power FET) may have high output capacitance, or, C_{OSS}, which will slow the response of the gate signal on Q3. No significant current carrying capability is required for Q2.

3.5 Diode Selection

D1 provides the highest voltage between the primary or secondary rail to the TPS3701 and the gate pullup resistors. This is required to ensure Q1 and Q3 turn fully off when the opposite channel is enabled. In the case where a high voltage is selected on one channel (i.e. 14.4 V on V_{SEC}) and the other channel is at a lower voltage (i.e. 10 V on V_{PRI}) , the gate pullup resistor must be pulled to the highest voltage because the source voltage on the disabled channel will track VOUT via the body diode of the disabled pass device.

The requirements of D1 are minimal. A small, low cost Shottky diode pair with connected cathodes and a maximum reverse voltage higher than the maximum input voltage is recommended.

4 Verification & Measured Performance

4.1 Schematic

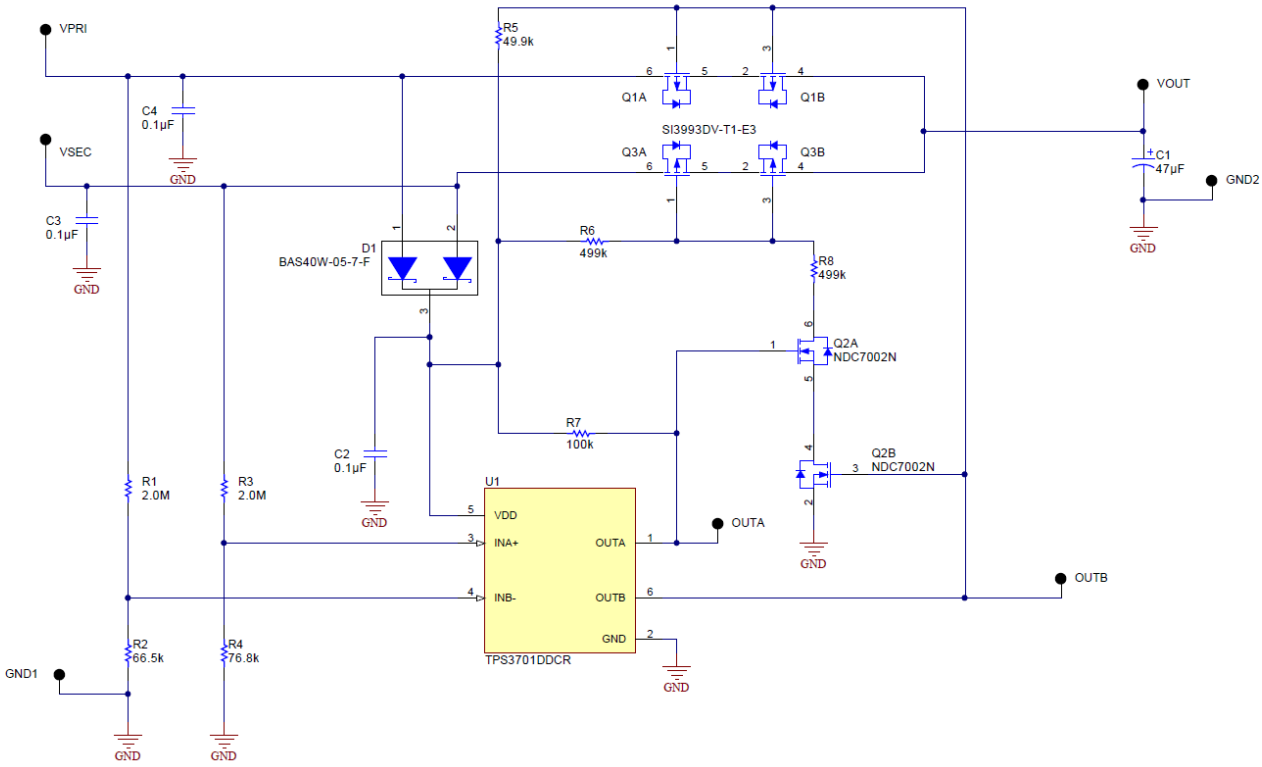

Figure 4: Schematic

4.2 Scope Plots

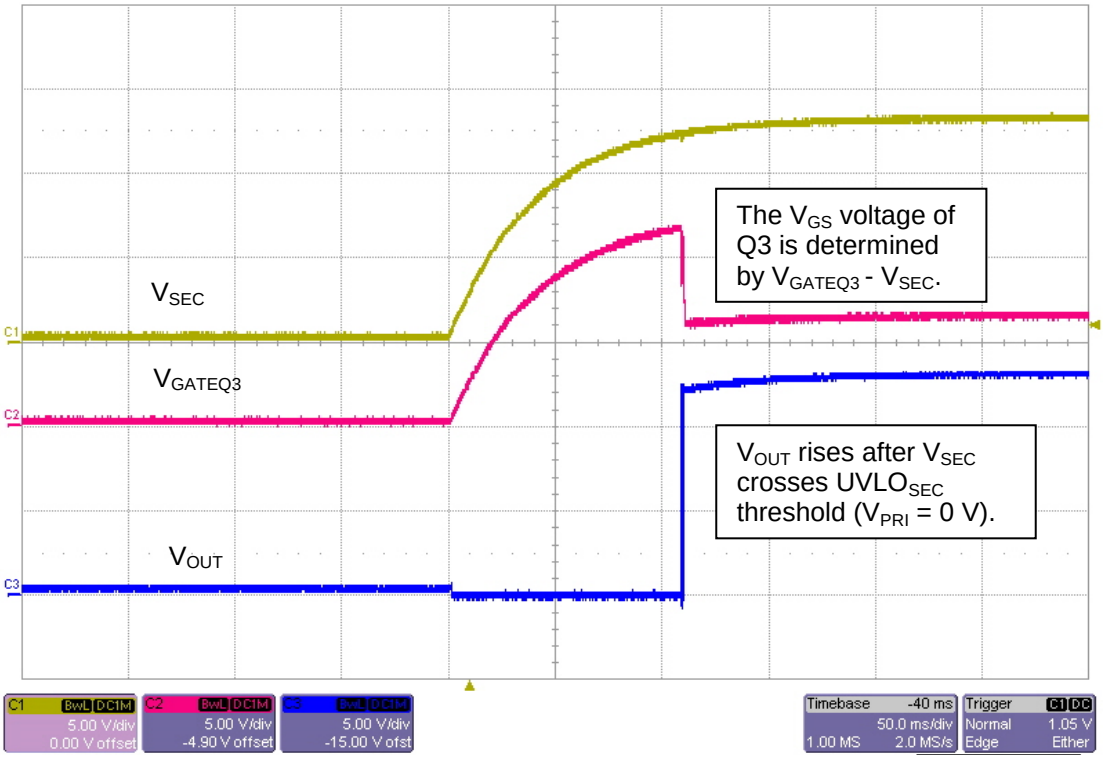

FIGURE 5: V_{SEC} Startup. V_{PRI} = 0 V, Load = 65 Ω

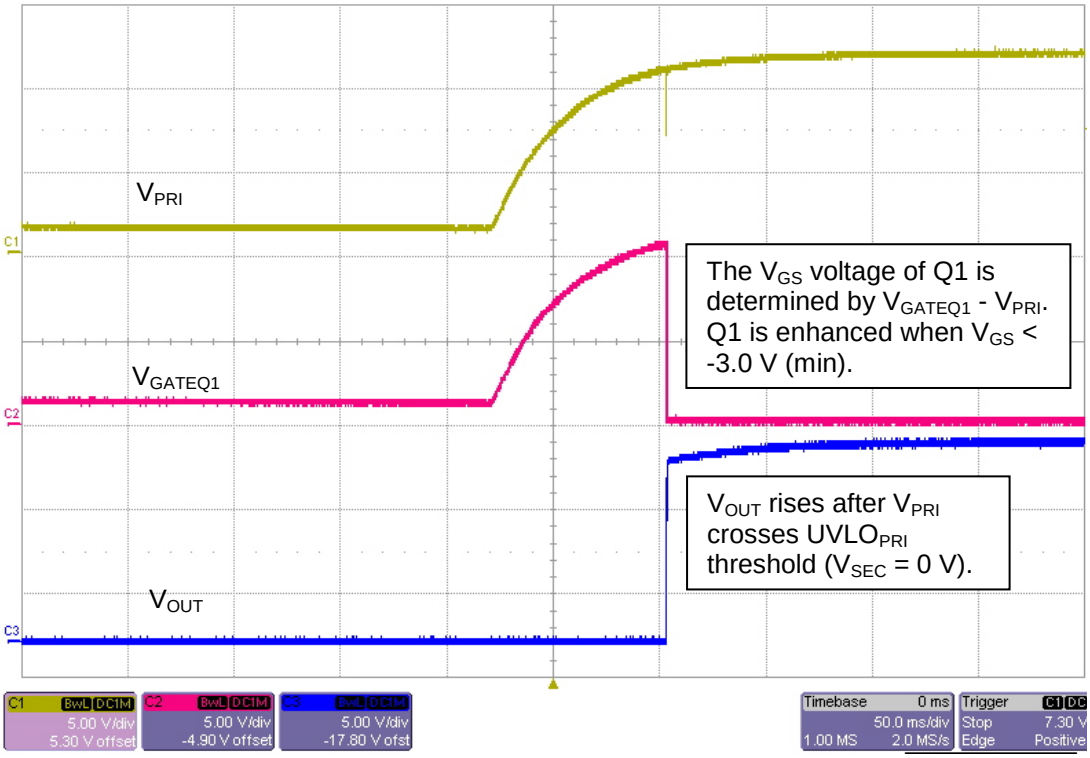

FIGURE 6: V_{PRI} Startup. V_{SEC} = 0 V, Load = 65 Ω

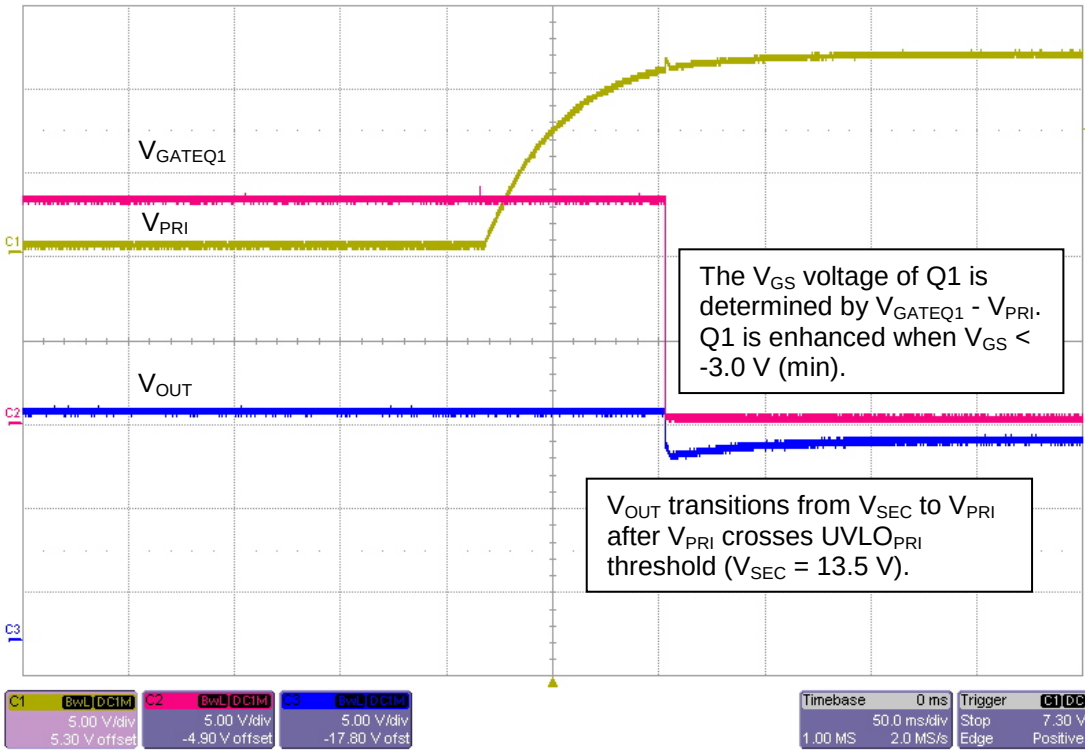

FIGURE 7: V_{PRI} Startup. V_{SEC} = 13.5 V, Load = 65 Ω

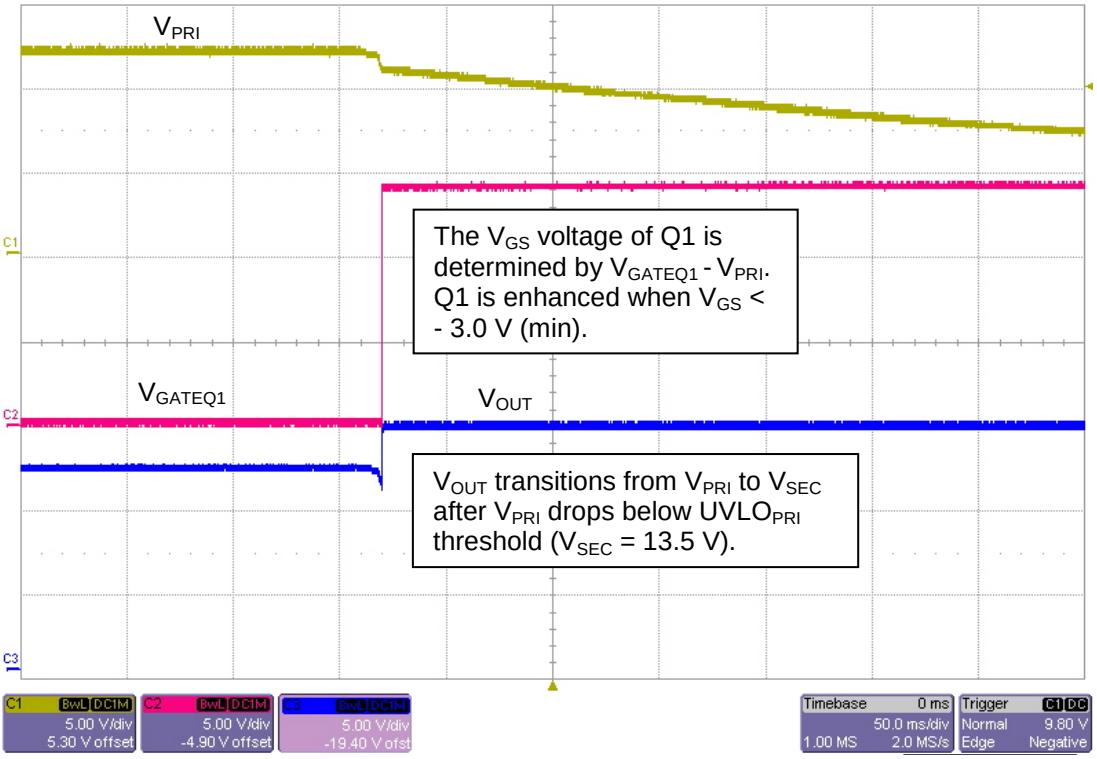

FIGURE 8: V_{PRI} Falling. V_{SEC} = 13.5 V, Load = 65 Ω

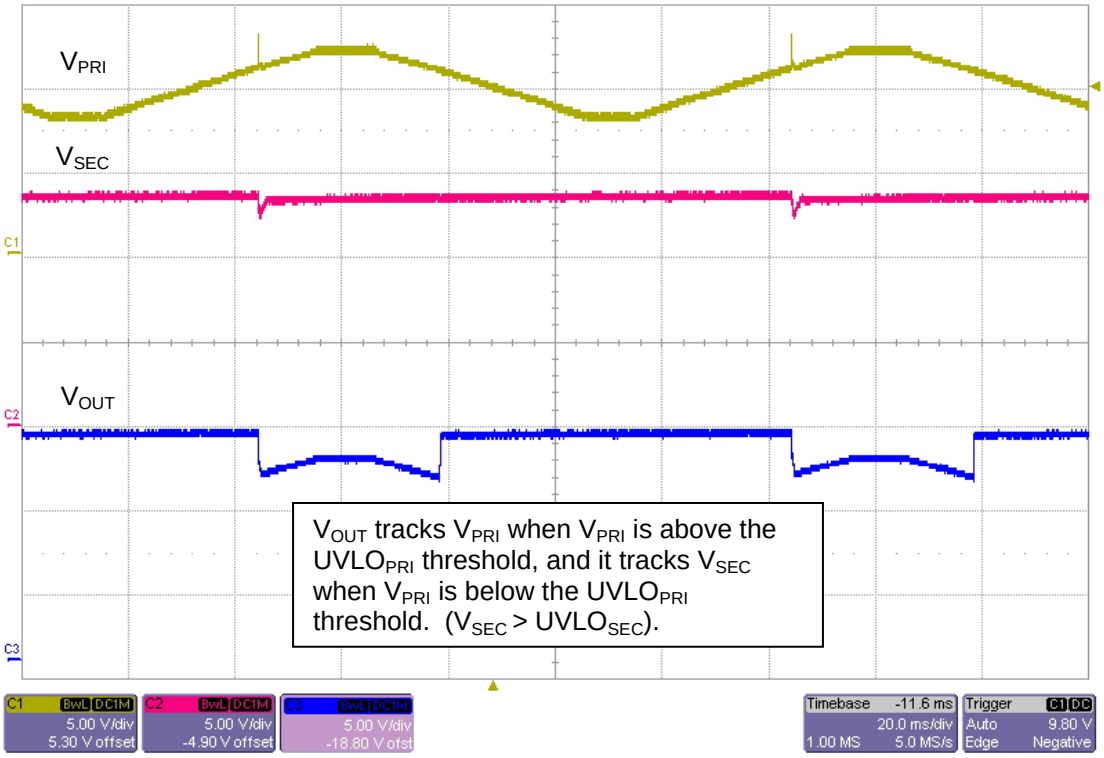

FIGURE 9: V_{PRI} Ramp. V_{SEC} = 13.5 V, Load = 65 Ω

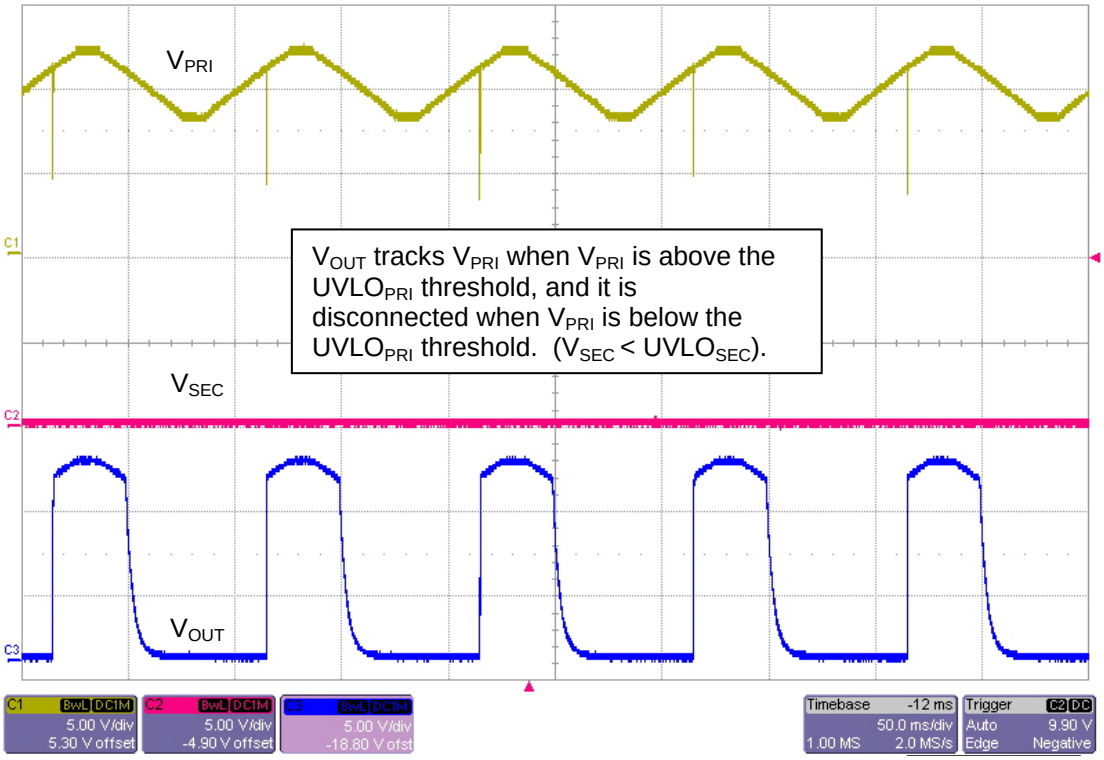

FIGURE 10: V_{PRI} Ramp. V_{SEC} = 0 V, Load = 65 Ω

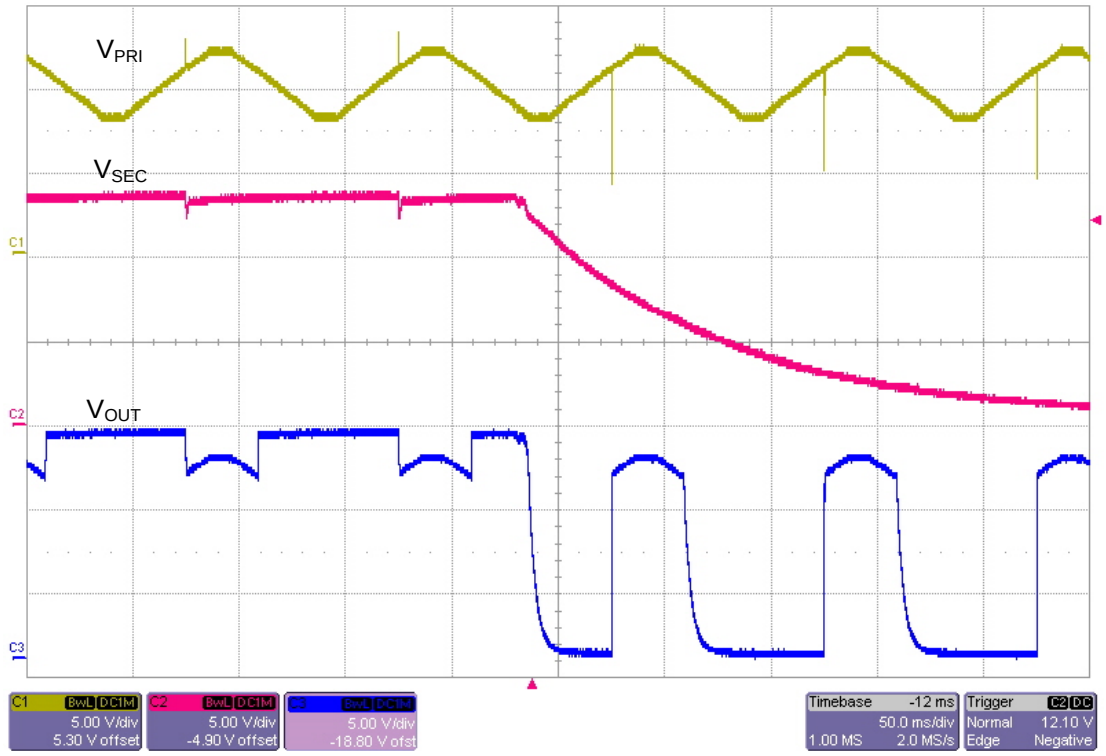

FIGURE 11: V_{PRI} Ramp. V_{SEC} = 13.5 to 0 V, Load = 65 Ω

4.3 BOM

Bill of Materials

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Item	Designator	Description	RoHS	Manufacturer	PartNumber
1	C1	CAP, AL, 47 µF, 25 V, +/- 20%, 0.3 ohm, TH	Y	Panasonic	EEU-FM1E470
2	C2	CAP, CERM, 0.1 µF, 50 V, +/- 10%, C0G/NP0, 0402	Y	TDK	C1005X7R1H104K
3	C3	CAP, CERM, 0.1 µF, 50 V, +/- 10%, C0G/NP0, 0402	Y	TDK	C1005X7R1H104K
4	C4	CAP, CERM, 0.1 µF, 50 V, +/- 10%, C0G/NP0, 0402	Y	TDK	C1005X7R1H104K
5	D1	Diode, Schottky, 40 V, 0.2 A, SOT-323	Y	Diodes Inc.	BAS40W-05-7-F
6	Q1	MOSFET, P-CH, -30 V, -1.8 A, TSOP-6	Y	VISHAY	SI3993DV-T1-E3
7	Q2	MOSFET, 2N-CH, 50 V, 0.51 A, SSOT-6	Y	Fairchild Semiconductor	NDC7002N
8	Q3	MOSFET, P-CH, -30 V, -1.8 A, TSOP-6	Y	VISHAY	SI3993DV-T1-E3
9	R1	RES, 2.0 M, 5%, 0.063 W, 0402	Y	Vishay-Dale	CRCW04022M00JNED
10	R2	RES, 66.5 k, 1%, 0.063 W, 0402	Y	Vishay-Dale	CRCW040266K5FKED
11	R3	RES, 2.0 M, 5%, 0.063 W, 0402	Y	Vishay-Dale	CRCW04022M00JNED
12	R4	RES, 76.8 k, 1%, 0.063 W, 0402	Y	Vishay-Dale	CRCW040276K8FKED
13	R5	RES, 49.9 k, 1%, 0.063 W, 0402	Y	Vishay-Dale	CRCW040249K9FKED
14	R6	RES, 499 k, 1%, 0.063 W, 0402	Y	Vishay-Dale	CRCW0402499KFKED
15	R7	RES, 100 k, 5%, 0.063 W, 0402	Y	Vishay-Dale	CRCW0402100KJNED
16	R8	RES, 499 k, 1%, 0.063 W, 0402	Y	Vishay-Dale	CRCW0402499KFKED
17	U1	36V Window Comparator with Internal Reference for Over and Under Voltage Detection, DDC0006A	Y	Texas Instruments	TPS3701DDCR

5 About the Author

Mike Hartshorne is an applications engineer in the Linear Power business unit. He has worked as an applications engineer in various power product lines and Analog-to-Digital Converter product lines. Mike received a BSEE from the University of San Diego and an M. Eng. from the University of Arizona.

6 References

1) TPS3701 Data Sheet

2) SI3993DV Data Sheet

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