Test Report

TIDUAZ9A – November 2015 – Revised January 2017

TIDA-00431 RF Sampling 4-GSPS ADC With 8-GHz DC-Coupled, Fully-Differential Amplifier Reference Design

Wideband radio frequency (RF) receivers allow greatly increased flexibility in radio designs. The wide, instantaneous bandwidth allows flexible tuning without changing hardware and the ability to capture multiple channels at widely separated frequencies. This reference design describes a wideband RF receiver utilizing a 4-GSPS analog-to-digital converter (ADC), with an 8-GHz, DC-coupled, fully differential amplifier front end. The amplifier front end provides signal gain and allows capture of signals down to DC, which is not possible with a balun-coupled input.

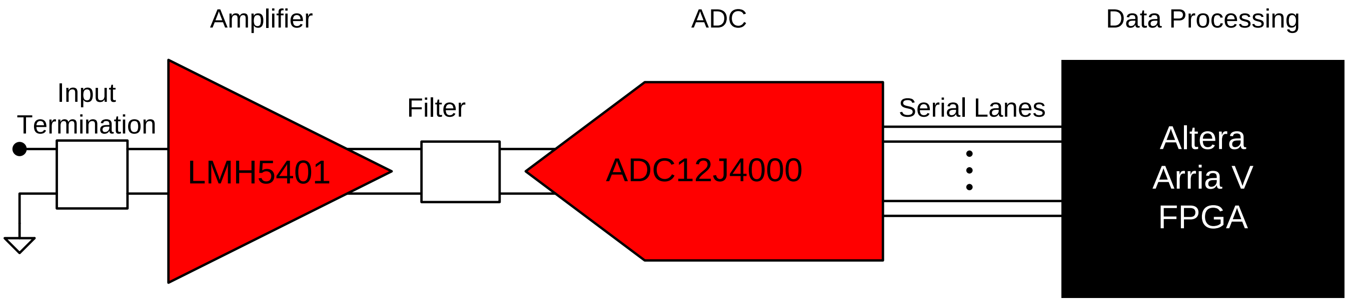

Figure 1. Simplified Block Diagram of RF Sampling ADC With DC-Coupled Front End

1 Introduction

This design describes an RF sampling solution including a high-bandwidth, high-sample rate ADC and a wide-bandwidth, low-distortion fully differential amplifier.

2 Design Steps

2.1 ADC Selection

For wide bandwidth signals, a high sampling rate is desired. The ADC sampling rate must be greater than two times the required signal bandwidth. In addition, the ADC sampling rate must be selected so that the input signal range is entirely in one Nyquist zone. Refer to Section 2.4 for further details on this topic.

For high-frequency signals, a high-input bandwidth is also necessary. In general, the –3-dB bandwidth of the ADC input must be higher than the maximum signal frequency. At higher input frequencies the sampled signal suffers from more attenuation as frequency increases. For a wideband signal, this variable attenuation or "tilt" may be challenging to compensate for. Operating the ADC input beyond the –3-dB point may be possible, because the amount of 'tilt' is limited over the small frequency range of interest.

2.2 Amplifier Selection

For high-frequency signals, a high bandwidth is desired. As for the ADC, the amplifier front end must also have a wide signal bandwidth capability. This capability is important both in terms of gain flatness and acceptable distortion performance. The distortion performance of amplifiers generally diminishes as the signal frequency increases. For this reason a very high-performance, high bandwidth amplifier is necessary for an RF sampling application.

For applications requiring amplification or buffering of the DC portion of the signal, a DC-coupling capability is necessary.

The power of the input signal and the full-scale range of the ADC determine how much amplifier gain is required.

2.3 Filter Design

In most applications using a high speed amplifier, a low-pass or band-pass filter is added to constrain the signal to the bandwidth of interest and attenuate any noise or distortion products that are above the frequency range of interest. For this design, a Butterworth filter topology is used. The Butterworth filter topology has the benefits of a good gain flatness in the pass-band, adequate roll-off, reasonable phase response, and is tolerant of component variations.

2.4 ADC Configuration

The ADC sample rate must be selected so that the entire signal bandwidth is within one Nyquist zone. This means that the rate must be within 0 to Fs/2, or Fs/2 to Fs, or Fs to 3Fs/2, and so forth. Consider the following example: If the signal frequency range is from 1000 MHz to 1400 MHz, one possible sampling rate is 3000 MSPS. In this case, the signal is entirely in the first Nyquist zone (0 MHz to 1500 MHz). Alternately, with a sampling rate of 1800 MSPS, the signal is entirely in the second Nyquist zone (900 MHz to 1800 MHz).

Some ADC or communication receiver products may contain an ADC front end followed by a digital down converter (DDC). The DDC usually consists of a digital numerically-controlled oscillator (NCO) and mixer followed by decimation filters. When configuring such a device there are two requirements:

1. The combination of the ADC sampling rate and decimation factor must be selected to ensure the alias protected bandwidth is sufficient to pass the desired signals.
2. The NCO frequency must be set to center the down-converted spectrum at the output of the mixer within the frequency limits of the decimation filter.

3 TSW12J54EVM Device Description

The TSW12J54EVM is an RF sampling system with a DC-coupled, fully differential amplifier front end. This system is implemented as an FPGA mezzanine card (FMC) for compatibility with Texas Instruments (TI) capture and source solutions like the TSW14J56, as well as other high pin-count (HPC) FMC carrier boards. The following Figure 2 shows a diagram of the TSW12J54EVM signal path.

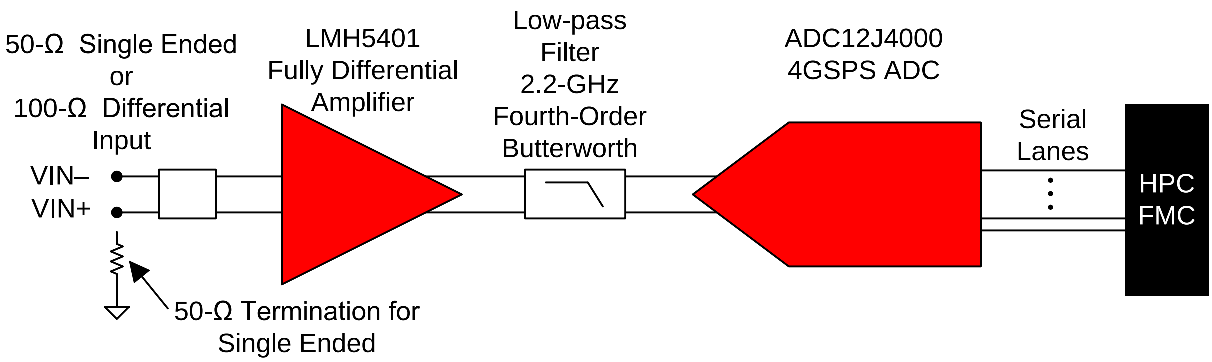

Figure 2. TSW12J54EVM Signal Path

See the related schematic, layout, and other documentation for the EVM details.

This solution has the following features and specifications:

- A useful F_{min} = 0 Hz.
- A useful F_{max} ≥ 1750 MHz.
- The ADC maximum sampling frequency is 4000 MSPS, which enables a maximum Nyquist bandwidth of 2000 MHz. The front end circuitry allows signals from 0 MHz to 1750 MHz to pass with good performance; therefore, the maximum useful bandwidth is 1750 MHz.

The following list describes the details of this solution, starting with the analog input signal conditioning:

- LMH5401—Fixed-Gain, Fully Differential, DC-coupled Amplifier Front End
  – Excellent linearity performance from DC to 2 GHz
  – 50-Ω SE input mode functions as active balun
  – Configured for 6-dB gain
  – Allows operation with DC- or AC-coupled input
  – Post-amplifier 2-GHz low-pass filter
    - Fourth-order Butterworth low-pass
    - F_c ≈ 2.2 GHz
    - Z_{in} = 100-Ω differential
    - Z_{out} = 100-Ω differential
    - Design tool: http://www.tonnesoftware.com/elsie.html
- ADC12J4000—12-bit, 4-GSPS ADC
  – High sampling rate provides 2-GHz Nyquist bandwidth
  – Raw 12-bit data mode provides ultra-wide bandwidth signal capture
  – Digital down converter (DDC) modes provide flexible tuning and decimation of 4x to 32x
  – DDC provides reduced sample rate and output signal bandwidth to ease downstream processing
- TRF3765—Low-noise phase-locked loop (PLL) with integrated VCO
  – Provides flexible ADC sample rates from 1 GSPS to 4 GSPS
- FMC mezzanine card format enables operation with the TSW14J56EVM from Texas Instruments and other compatible FMC carrier boards

The following Figure 3 shows a top and bottom view of the TSW12J54EVM.

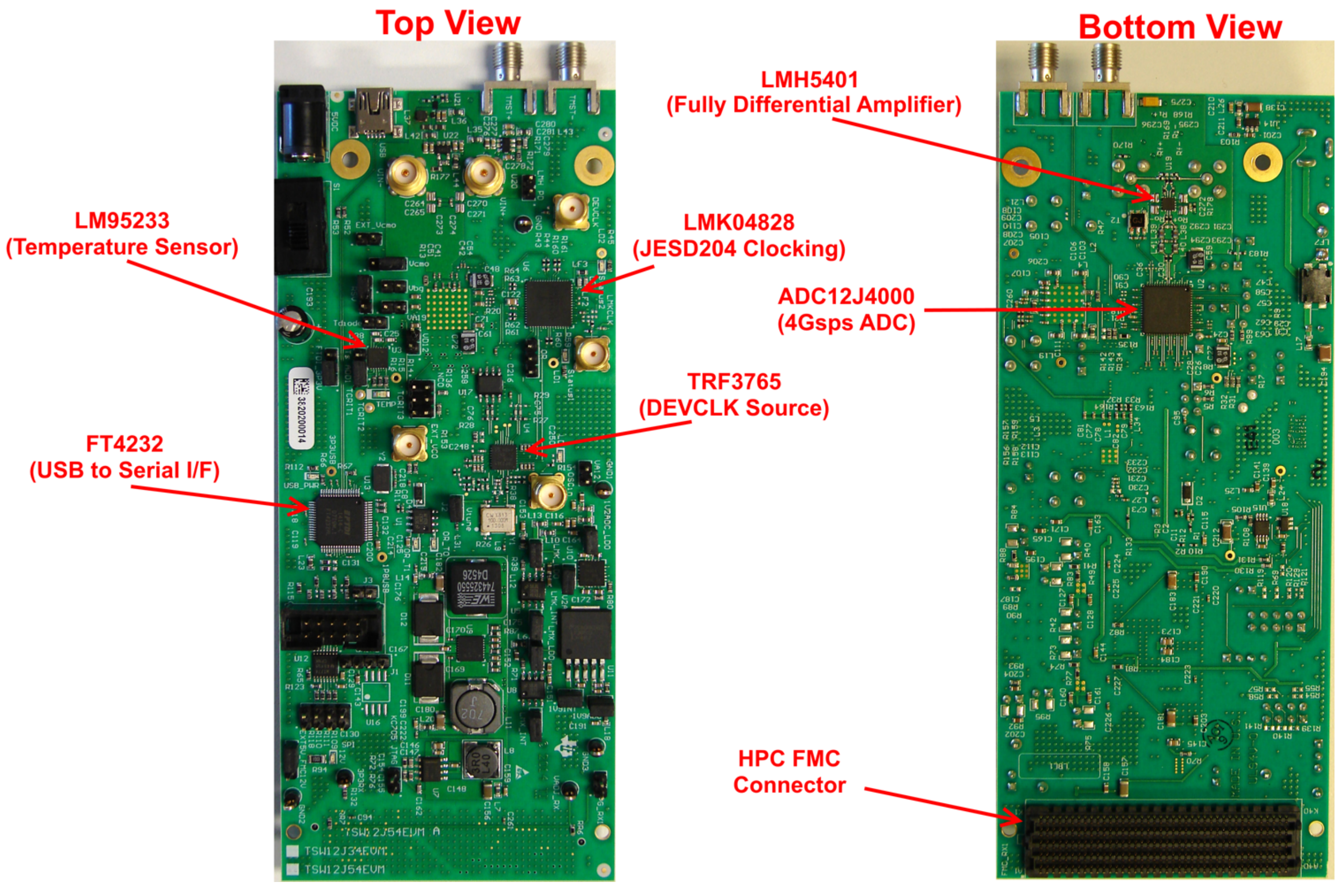

Figure 3. EVM Board Photos

4 Experimental Results

The LMH5401 and ADC12J4000 data capture system is configured with a +6-dB gain. Performance has been evaluated using input frequencies between 48 MHz to 1998 MHz.

The following Figure 4 shows a typical spectral plot:

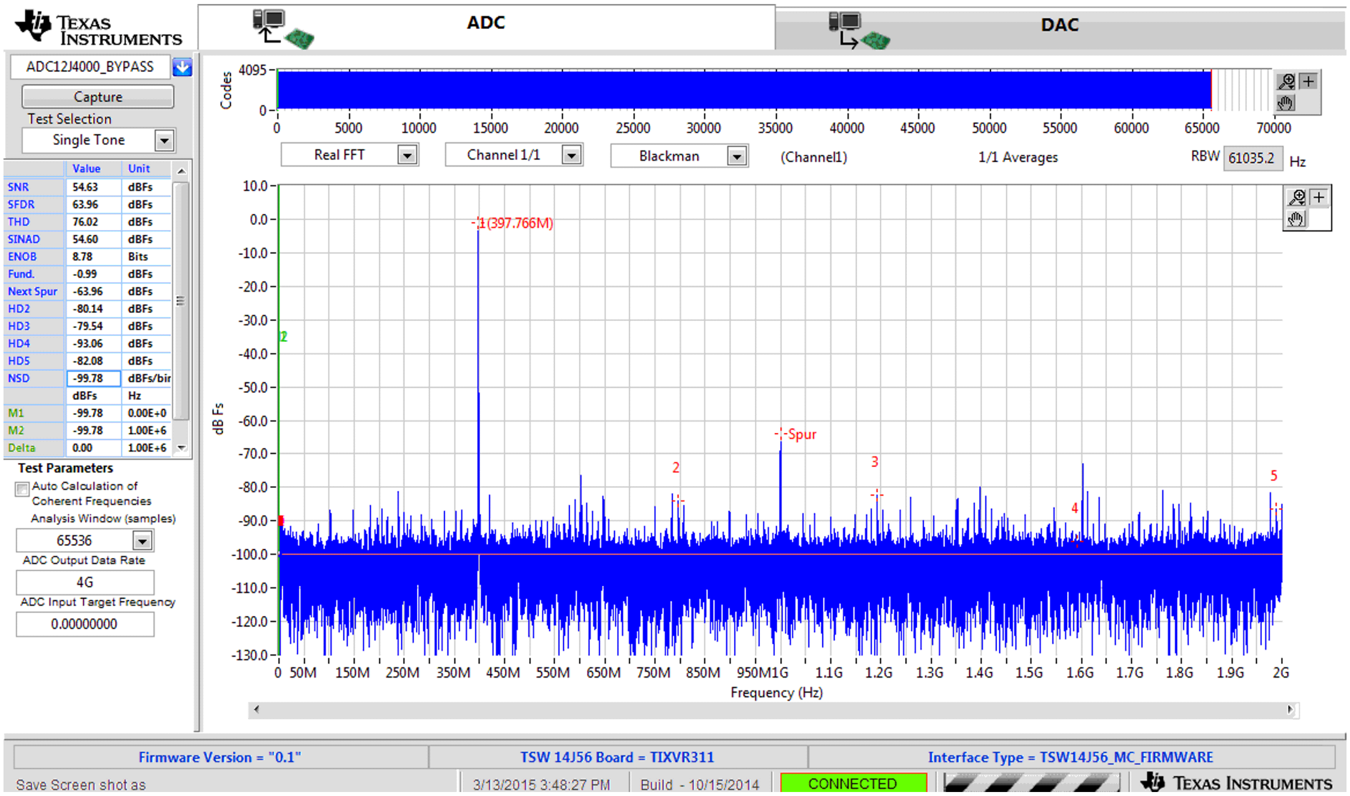

Figure 4. FFT at 397.7-MHz Input

Table 1 shows the tabular results of this testing. The RF generator amplitude has been set to achieve an input power of –1 dBFS:

Table 1. Testing Results

APPLIED FREQ.(MHz)	APPLIED GENERATOR POWER (dBm)	SNR (dBFs)	SINAD (dBFs)	SFDR (dBFs)	THD (dBFs)	HD2 (dBFs)	HD3 (dBFs)	HD4 (dBFs)	HD5 (dBFs)	ENOB (Bits)	FUND (dBFs)	NEXT SPUR (dBFs)	NSD (dBFs/Hz)
47.77	–4.5	53.64	53.56	66.32	–70.83	–90.85	–71.31	–80.43	–88.72	8.61	–1.02	–66.32	–98.79
97.77	–4.35	53.91	53.83	69.1	–71.01	–77.61	–72.25	–87.31	–88.11	8.65	–1.01	–69.1	–99.06
197.77	–4.35	53.74	53.65	67.34	–70.46	–73.54	–73.9	–83.79	–84.25	8.62	–1.01	–67.34	–98.89
297.77	–4.4	53.83	53.65	68.22	–67.62	–68.22	–79.54	–82.7	–82.42	8.62	–1	–72.12	–98.98
397.77	–4.5	53.13	52.97	61.8	–67.22	–67.8	–81.45	–75.19	–85.75	8.51	–1.03	–61.8	–98.29
497.77	–3.75	53.61	53.1	63.03	–62.57	–63.03	–75.1	–78.74	–84.76	8.53	–1	–72.4	–98.76
747.77	–4.2	52.86	52.34	62.38	–61.76	–62.38	–70.72	–79.21	–89.71	8.4	–1.02	–65.45	–98.02
997.77	–4.7	52.52	51.42	57.99	–57.94	–57.99	–79.28	–75.08	–85.48	8.25	–1.01	–67.32	–97.67
1247.77	–3.83	51.59	51.49	64.74	–67.77	–70.76	–70.2	–86.83	–83.37	8.26	–1	–64.74	–96.74
1497.77	–3.35	51.06	50.87	63.64	–64.45	–65.92	–69.81	–86.4	–86.13	8.16	–1	–63.64	–96.21
1747.77	–2.6	50.77	50.37	61.01	–60.95	–61.01	–74.41	–83.8	–84.51	8.08	–1.02	–63.16	–95.92
1997.77	2.12	49.67	46.19	48.78	–48.78	–48.78	–72.43	–80.68	–79.33	7.38	–1	–61.95	–94.82

Figure 5 shows a plot of the SNR, SINAD, and SFDR performance.

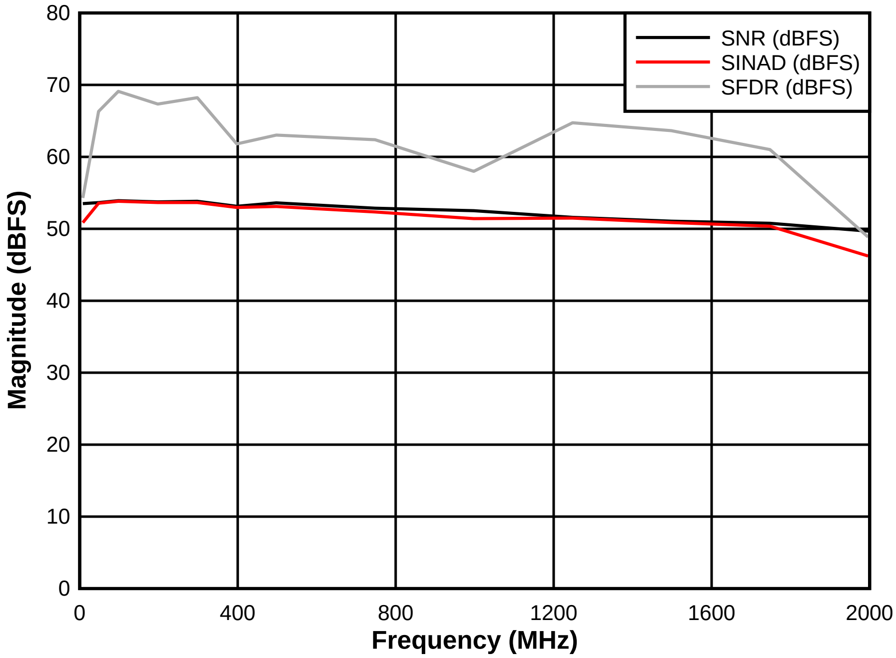

Figure 5. SNR, SINAD, and SFDR Performance

Figure 6 shows a plot of the harmonic distortion performance.

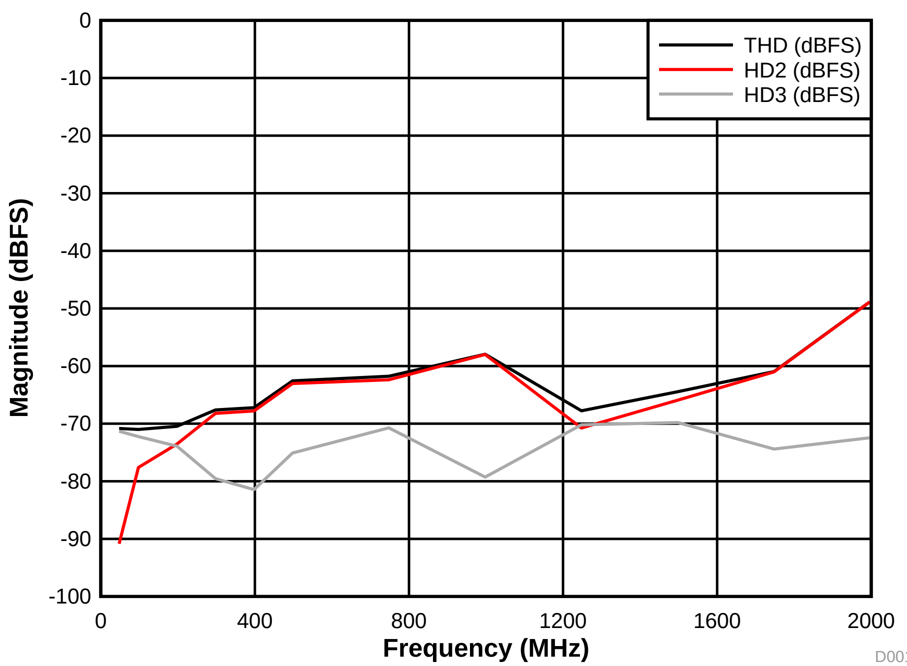

Figure 6. THD Performance

Figure 7 compares the TSW12J54EVM SFDR to that of the ADC12J4000EVM.

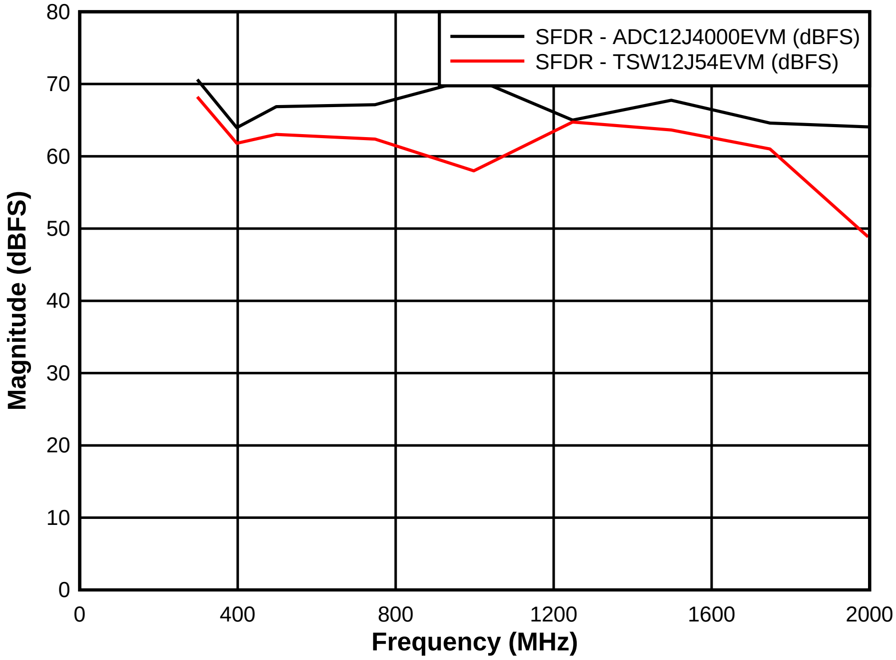

Figure 7. Comparison Between TSW12J54EVM and ADC12J4000EVM

5 About the Author

JIM BRINKHURST graduated from the University of Saskatchewan, where he earned a Bachelor of Science in Electrical Engineering. He is a senior Applications Engineer in the Texas Instruments High Speed Data Converter product line.

6 References

1. Texas Instruments, *Wideband RF Receiver Reference Design*, TSW12J54EVM Tool Folder (http://www.ti.com/tool/tsw12j54evm)
2. Texas Instruments, *ITSW14J56EVM Evaluation Module*, TSW14J56EVM Tool Folder (http://www.ti.com/tool/tsw14j56evm)
3. Texas Instruments, *High Speed Data Converter Pro Software*, DATACONVERTERPRO-SW Tool Folder (http://www.ti.com/tool/dataconverterpro-sw)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2016) to A Revision	Page
• Changed caption to specify TSW12J54EVM instead of TSW14J56EVM	7

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