TI Designs

Automotive Power Design for Front Camera Systems using Single Core Voltage Application Processors

Design Overview

This TI Design provides a broadly applicable automotive power solution for a variety of Advanced Driver Assistant Systems (ADAS) processors, focusing on front camera and surround view applications. The design supports an input range of 4 V to 48 V to supply common processor power rails through discrete components, which adds to the versatility of the design while providing designers with more flexibility and scalability in terms of power, layout, thermal, and EMI and EMC optimization to achieve automotive compliance for regulatory requirements associated with producing an automotive electronic subsystem.

Design Resources

TIDA-00803	Design Folder
LM3880-Q1	Product Folder
TPS22966-Q1	Product Folder
SN74AHC1G32-Q1	Product Folder
SN74LVC1G08-Q1	Product Folder
TPS54362-Q1	Product Folder
TPS57114-Q1	Product Folder
TPS61170-Q1	Product Folder
TPS62261-Q1	Product Folder
TPS71718-Q1 and TPS71728-Q1	Product Folder

Design Features

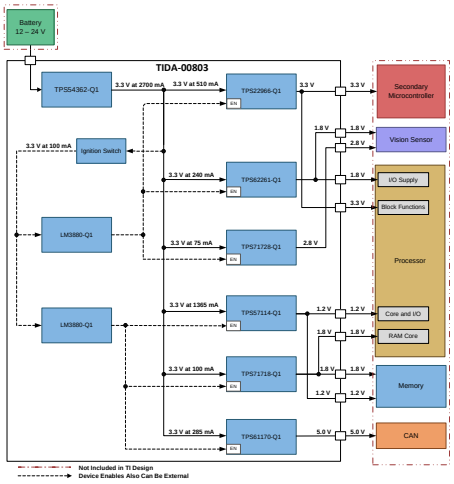
- Power Solution for Wide Array of ADAS Processors
- Designed for Wide-V_{IN} and Cold-Crank Conditions
- Size-Optimized Design (83.0 mm × 57.0 mm)
- Supports Peripheral Power Supply Needs [CMOS Sensor, Inputs and Outputs (I/Os), Memory, and Secondary Microcontroller (MCU)]
- Uses an Input Filter for Improved EMI and EMC Performance

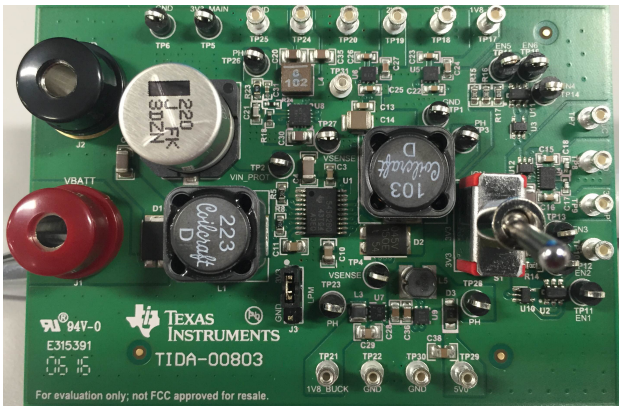
Featured Applications

- ADAS — Front-View Cameras
- Surround View Systems

TI E2E™ Community

ASK Our E2E Experts





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 Key System Specifications

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
SYSTEM INPUT					
V_{IN} Input Voltage	Battery Voltage Range (DC)	4	13	48	V
OUTPUT VOLTAGES					
3.3 V Main	Main Supply Rail	3.2	3.3	3.4	V
3.3 V µC	Microcontroller Supply Rail	3.2	3.3	3.4	V
3.3 V µP	Processor Supply Rail	3.2	3.3	3.4	V
1.8 V LDO	Processor and Memory Rail	1.7	1.8	1.9	V
1.8 V BUCK	Processor and Vision Sensor Rail	1.7	1.8	1.9	V
5.0 V	CAN Supply Rail	4.8	5	5.2	V
1.2 V	Processor and Memory Rail	1.15	1.2	1.25	V
2.8 V	Vision Sensor	2.73	2.8	2.87	V
OUTPUT CURRENTS (ONLY SHOWING MAX CURRENT for SYSTEM CONFIGURATION)					
3.3 V Main	Main Supply Rail			3	A
3.3 V µC	Microcontroller Supply Rail			0.5	A
3.3 V µP	Processor Supply Rail			0.1	A
1.8 V LDO	Processor and Memory Rail			0.1	A
1.8 V BUCK	Processor and Vision Sensor Rail			0.3	A
5.0 V	CAN Supply Rail			0.3	A
1.2 V	Processor and Memory Rail			1.5	A
2.8 V	Vision Sensor			0.1	A

Table 1. Sequencing

EN SIGNAL	RAIL NAME	DEVICE	RAMP START	STABLE TIME	UNIT
V_{IN}	3.3 V Main	TPS54362-Q1	0	2.4	ms
EN1	1.2 V	TPS57114-Q1	4.4	5.48	ms
EN2	1.8 V LDO	TPS71718-Q1	6.4	6.535	ms
EN3	1.8 V BUCK	TPS62261-Q1	8.4	8.65	ms
EN4	3.3 V µC	TPS22966-Q1	10.4	10.55	ms
EN5	2.8 V	TPS71728-Q1	12.4	12.535	ms
EN6	5.0 V	TPS61170-Q1	21	22	ms

2 System Description

This system design is for a complete power solution for a variety of ADAS processors, including key peripheral power (CAN, Memory, CMOS Sensor, and secondary MCU). This reference design uses an input connected to a car battery and provides common voltage rails to the point of load in an ADAS front-camera system.

The design utilizes the TPS54362-Q1 as a pre-regulator, which provides a main 3.3-V rail to power additional regulators and the sequencing mechanism. Common ADAS Front-View camera-system power rails are supplied via two Buck converters, two low-dropouts (LDOs), one Boost converter, and a load switch. To increase versatility, the sequencing, layout, and design allows for the addition, subtraction, or replacement of any output regulator to provide a different voltage output to the system. The design also has the following:

- Operates over the full range of battery conditions (4 V to 48 V)
- Provides a basic sequencing solution for both power up and power down of an ADAS processor
- Mitigates EMI and EMC issues with pre-regulator filter solution
- Provides power for key peripherals such as CAN PHY, Memory, and CMOS Vision Sensor
- Optimizes the individual blocks and layout for a small solution while maintaining high performance

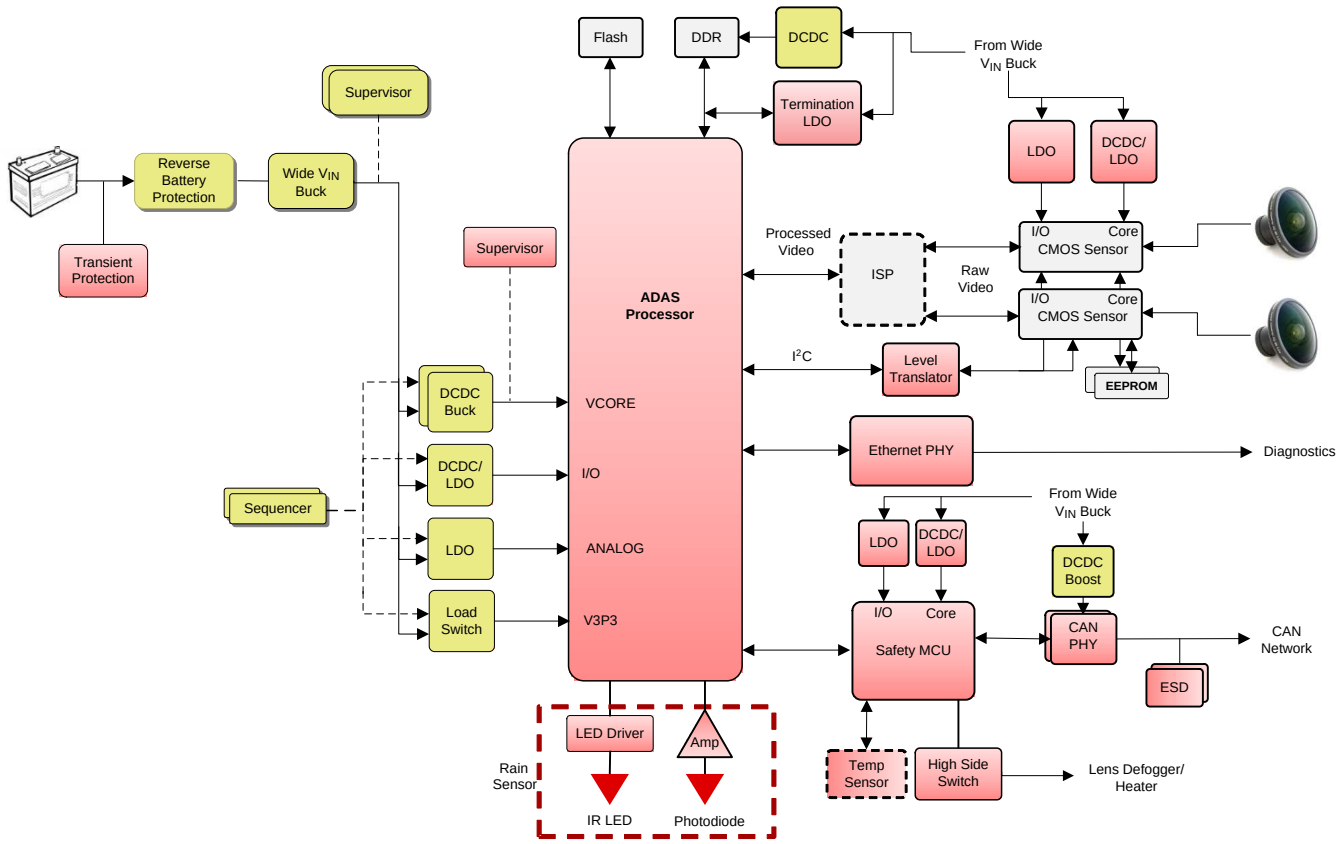


Figure 1. System Configuration

The yellow blocks are all components found on the TIDA-00803 board, covering nearly all monitoring, sequencing, and power requirements of the example system (as our design is not application-specific, power for a CMOS imaging sensor or other application-specific blocks is not included).

2.1 LM3880-Q1

The LM3880-Q1 Simple Power Sequencer offers the easiest method to control power up and power down sequencing of multiple Independent voltage rails. By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in a 6-pin SOT-23-6 package, the Simple Sequencer contains a precision enable pin and three open-drain output flags. When the LM3880-Q1 is enabled, the three output flags will sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags will follow a reverse sequence during power down to avoid latch conditions.

EPROM capability allows every delay and sequence to be fully adjustable. Contact Texas Instruments if a nonstandard configuration is required.

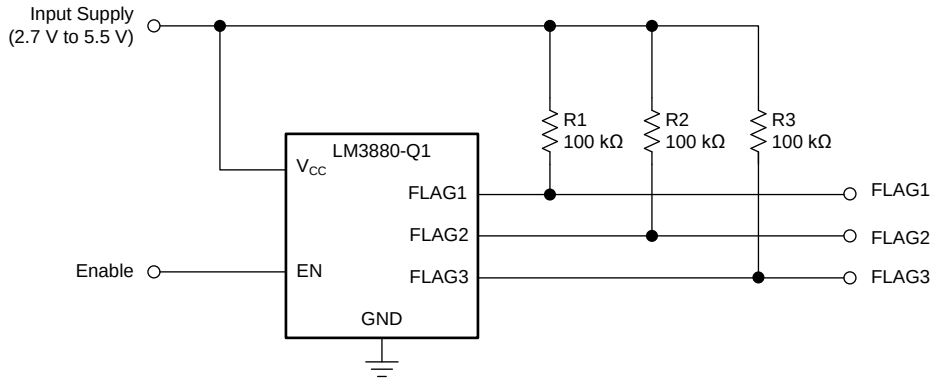


Figure 2. LM3880-Q1

2.2 TPS22966-Q1

The TPS22966-Q1 device is a small, ultralow R_{ON}, dual-channel load switch with adjustable rise time. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of up to 4 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. The TPS22966-Q1 includes a 230-Ω on-chip resistor for quick output discharge when the switch is turned off.

The TPS22966-Q1 is available in a small, space-saving 2-mm × 3-mm 14-SON package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 105ºC.

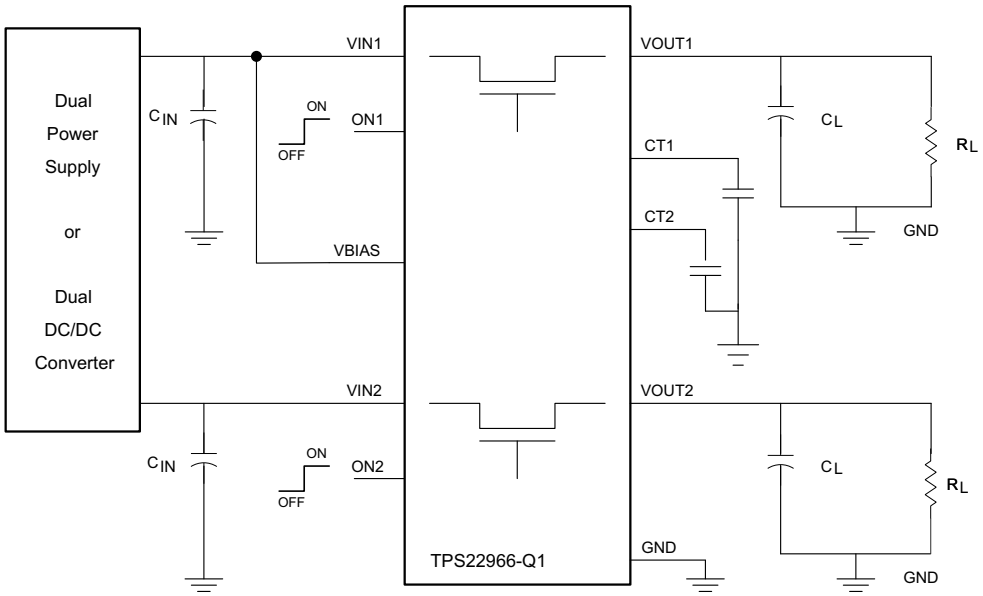


Figure 3. TPS22966-Q1

2.3 TPS54362-Q1

The TPS54362-Q1 device is a step-down switch-mode power supply with a low-power mode and a programmable voltage supervisor. Integrated input voltage-line feed-forward topology improves line transient regulation of the voltage-mode buck regulator. The regulator has a cycle-by-cycle current limit. Pulse-skip mode operation under no load reduces the supply current to 65 µA. Using the enable pin reduces the supply shutdown current to 1 µA.

An open-drain reset signal indicates when the nominal output drops below the threshold set by an external resistor-divider network. A soft-start capacitor controls the output voltage start-up ramp. The device activates an internal undervoltage shutdown when the input supply ramps down to 2.6 V.

Frequency foldback operation protects the device during an overload conditions on the output. The device also has thermal shutdown protection due to excessive power dissipation.

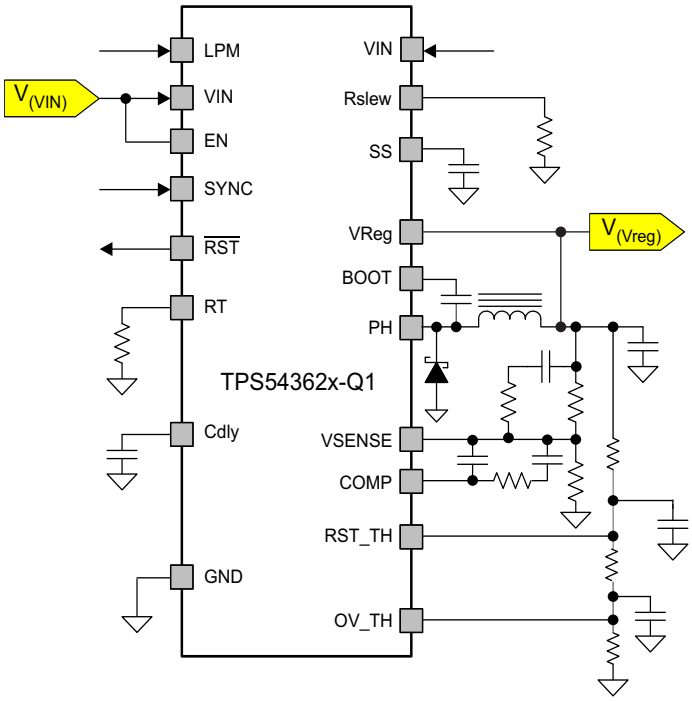


Figure 4. TPS54362-Q1

2.4 TPS57114-Q1

The TPS57114-Q1 device is a full-featured 6-V, 4-A, synchronous step-down current-mode converter with two integrated MOSFETs.

The TPS57114-Q1 device enables small designs by integrating the MOSFETs, implementing current-mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced QFN package.

The TPS57114-Q1 device provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{ref}) over temperature.

Efficiency is maximized through the integrated 12-mΩ MOSFETs and 515-µA typical supply current. Using the enable pin, shutdown supply current is reduced to 5.5 µA by entering a shutdown mode.

The internal undervoltage lockout setting is 2.45 V, but programming the threshold with a resistor network on the enable pin can increase the setting. The slow-start pin controls the output-voltage start-up ramp. An open-drain power-good signal indicates the output is within 93% to 107% of its nominal voltage.

Frequency foldback and thermal shutdown protect the device during an overcurrent condition.

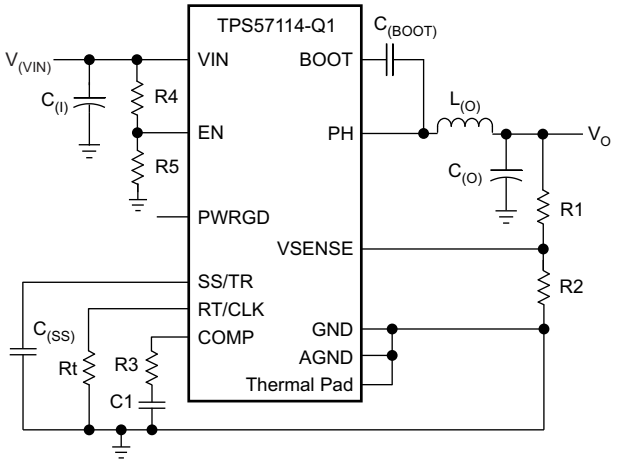


Figure 5. TPS57114-Q1

2.5 TPS61170-Q1

The TPS61170-Q1 device is a monolithic, high-voltage switching regulator with integrated 1.2-A, 40-V power MOSFET. The device can be configured in several standard switching-regulator topologies, including boost and SEPIC. The device has a wide input-voltage range to support applications with input voltage from multicell batteries or regulated power rails.

The TPS61170-Q1 operates at a 1.2-MHz switching frequency, allowing the use of low-profile inductors and low-value ceramic input and output capacitors. External loop compensation components give the user flexibility to optimize loop compensation and transient response. The device has built-in protection features, such as pulse-by-pulse overcurrent limit, soft start, and thermal shutdown.

The FB pin regulates to a reference voltage of 1.229 V. The reference voltage can be lowered using a 1-wire digital interface (EasyScale™ protocol) through the CTRL pin. Alternatively, a pulse width-modulation (PWM) signal can be applied to the CTRL pin. The duty cycle of the signal reduces the feedback reference voltage proportionally.

The TPS61170-Q1 is available in a 6-pin 2-mm × 2-mm SON package, allowing a compact power-supply solution.

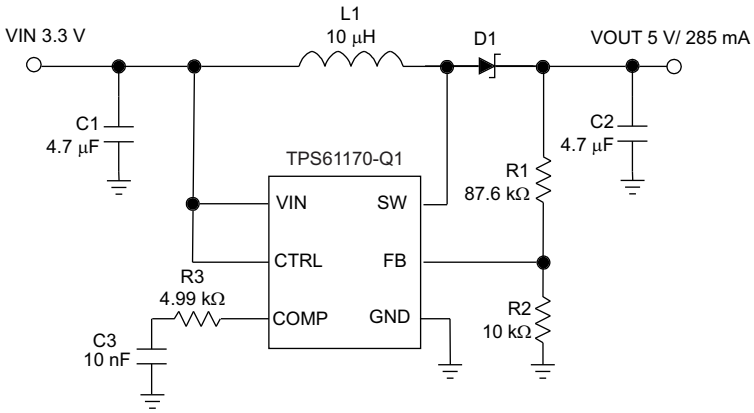


Figure 6. TPS61170-Q1

2.6 TPS62261-Q1

The TPS6226x-Q1 devices are high-efficiency synchronous step-down dc-dc converters optimized for battery-powered applications. The devices provide up to 600-mA output current from a single Li-Ion cell and are ideal to power mobile phones and other portable applications.

With a wide input voltage range of 2 V to 6 V, the device supports applications powered by Li-Ion batteries with extended voltage range, two- and three-cell alkaline batteries, 3.3-V and 5-V input voltage rails.

The TPS6226x-Q1 devices operate at 2.25-MHz fixed switching frequency and enter power-save-mode operation at light load currents to maintain high efficiency over the entire load-current range.

The power-save mode is optimized for low output-voltage ripple. For low-noise applications, the devices can be forced into fixed-frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS6226x-Q1 devices allow the use of small inductors and capacitors to achieve a small solution size.

All of the TPS6226x-Q1 devices are available in a very small 2-mm × 2-mm × 0.8-mm WSON (DRV) package.

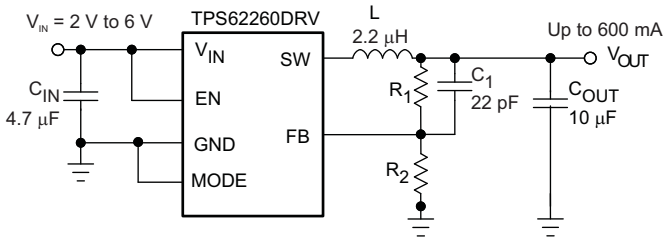


Figure 7. TPS62261-Q1

2.7 TPS717XX-Q1

The TPS717XX-Q1 family of low-dropout (LDO), low-power linear regulators offers very high power-supply rejection (PSRR) and maintains very low 45-µA ground current in an ultra-small, five-pin SOT package. The family uses an advanced BiCMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717XX-Q1 is stable with a 1-µF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. The device family is fully specified from T_J, T_A = –40°C to 125°C and is offered in a small SOT (SC70-5) package, a 2-mm × 2-mm WSON-6 package with a thermal pad, and a 1.5-mm × 1.5-mm WSON-6 package, which are ideal for small form-factor portable equipment (such as wireless handsets and PDAs). The TPS717XX-Q1 family of LDOs is qualified for AEC-Q100 grade 1.

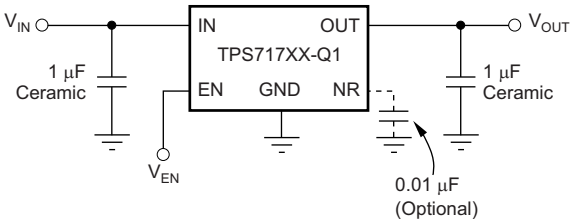
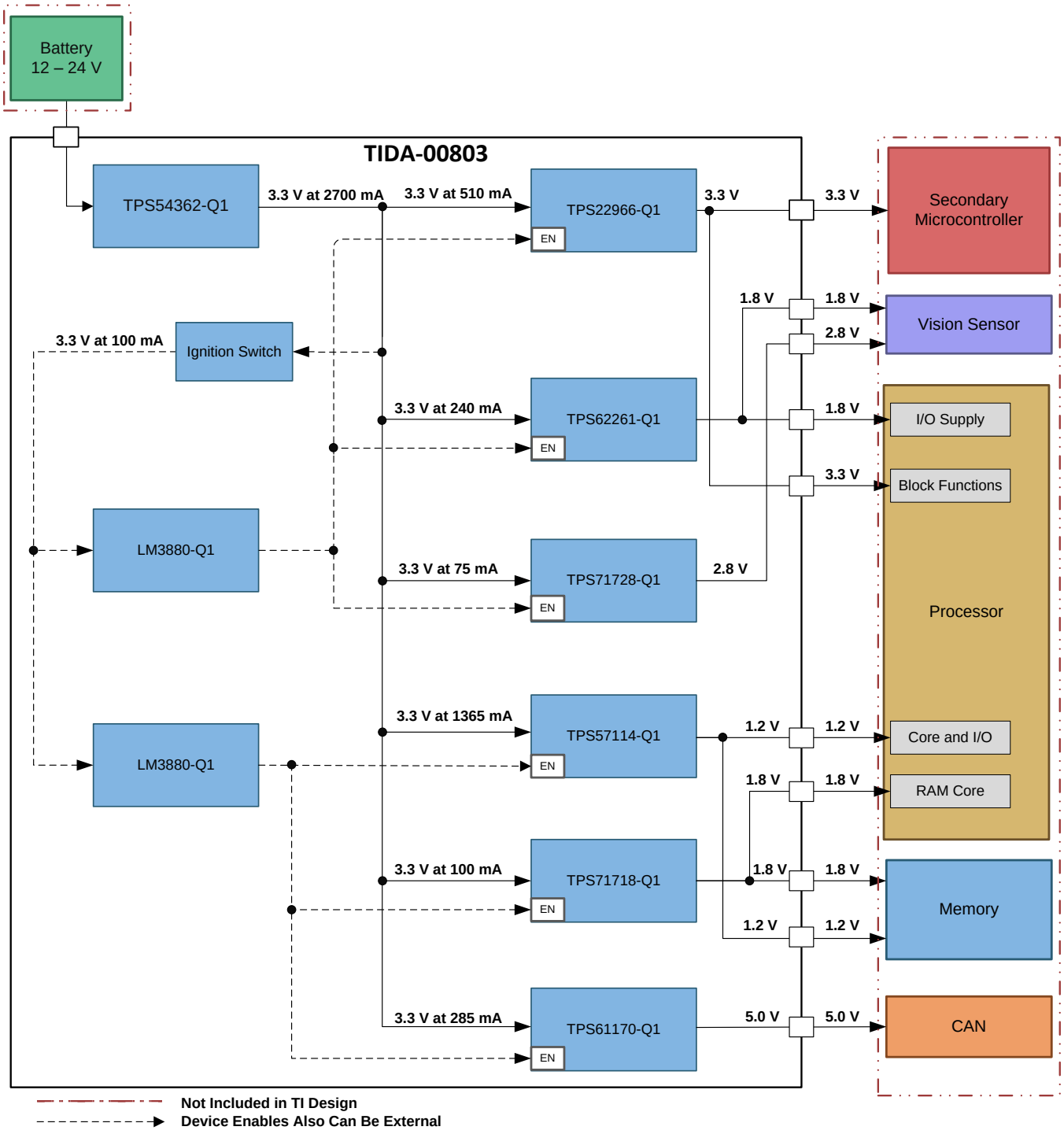


Figure 8. TPS717XX-Q1

3 Block Diagram



4 Highlighted Products

The Reference Design features the following devices:

- LM3880-Q1
- TPS22966-Q1
- TPS54362-Q1
- TPS57114-Q
- TPS61170-Q1
- TPS62261-Q1
- TPS71718-Q1
- TPS71728-Q1

All the above devices are qualified for automotive applications and for more information on each of these devices, see the respective product folders at www.TI.com.

4.1 LM3880-Q1 Features

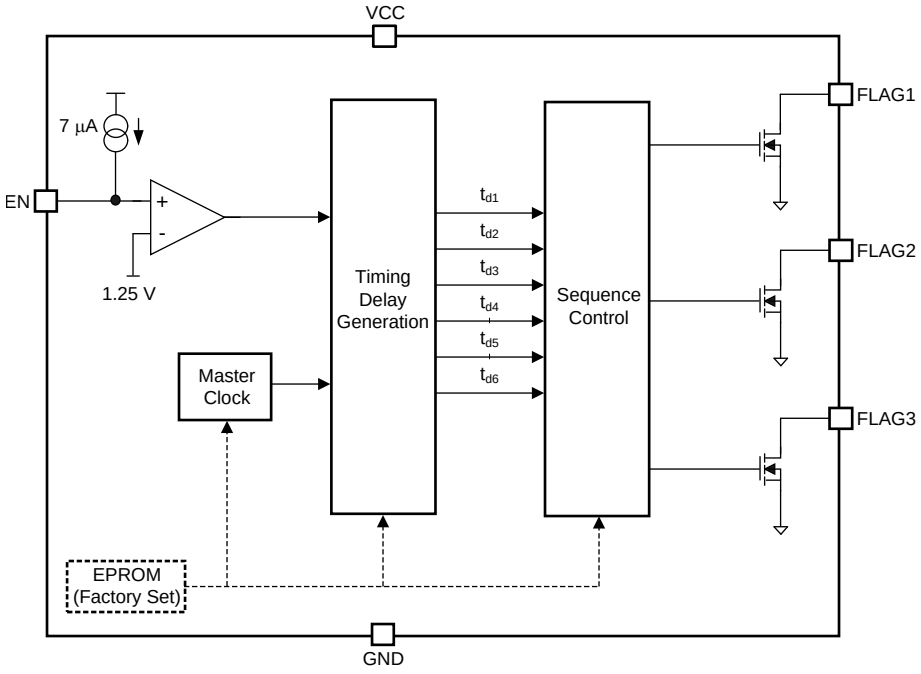


Figure 9. LM3880-Q1 Block Diagram

- Easiest Method to Sequence Rails
- Power-Up and Power-Down Control
- Tiny Footprint
- Low Quiescent Current of 25 µA
- Input Voltage Range of 2.7 V to 5.5 V
- Standard Timing Options Available
- Customization of Timing and Sequence Available Through Factory Programmability

4.2 TPS22966-Q1 Features

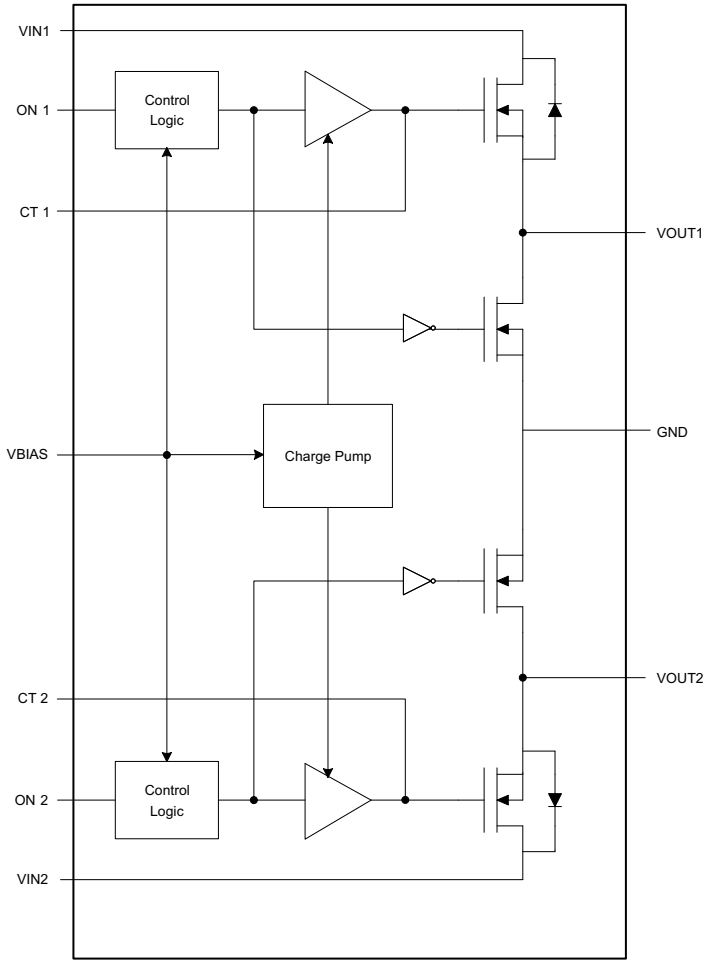


Figure 10. TPS22966-Q1 Block Diagram

- Integrated Dual-Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- Ultralow ON-Resistance (R_{ON})
  - R_{ON} = 16 mΩ at V_{IN} = 3.3 V (V_{BIAS} = 5 V)
- 4-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - 80 µA (Both Channels)
  - 80 µA (Single Channel)
- Low Control Input Threshold Enables Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Configurable Rise Time
- SON 14-Pin Package With Thermal Pad

4.3 TPS54362-Q1 Features

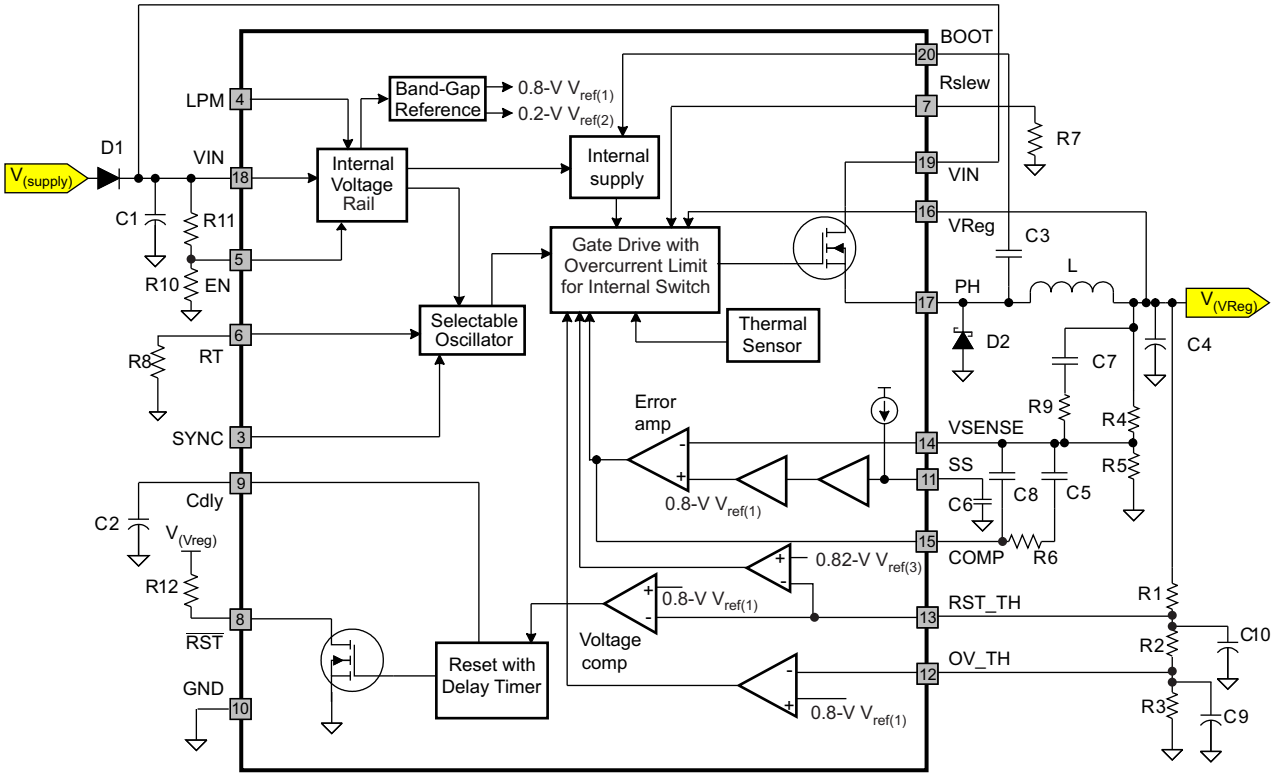


Figure 11. TPS54362-Q1 Block Diagram

- Withstands Transients up to 60 V With an Operating Range of 3.6 V to 48 V and Load Current up to 3 A
- 200-kHz to 2.2-MHz Switching Frequency
- High-Voltage-Tolerant Enable Input for ON and OFF State
- Soft Start on Enable Cycle
- Slew-Rate Control on Internal Power Switch
- External Clock Input for Synchronization
- Pulse-Skip Mode (PFM) During Light Output Loads With Quiescent Current = 65 µA Typical (LPM Operation)
- Internal Undervoltage Lockout, UVLO
- Programmable Reset Power-On Delay
- Reset-Function Filter Time for Fast Negative Transients
- Programmable Overvoltage Output Monitoring
- Programmable Undervoltage Output Monitoring, Issuance of Reset if Output Falls Below Threshold
- Switch Current-Limit Protection
- Short-Circuit and Overcurrent Protection of FET
- 20-Pin HTSSOP PowerPAD™ Package

4.4 TPS57114-Q1 Features

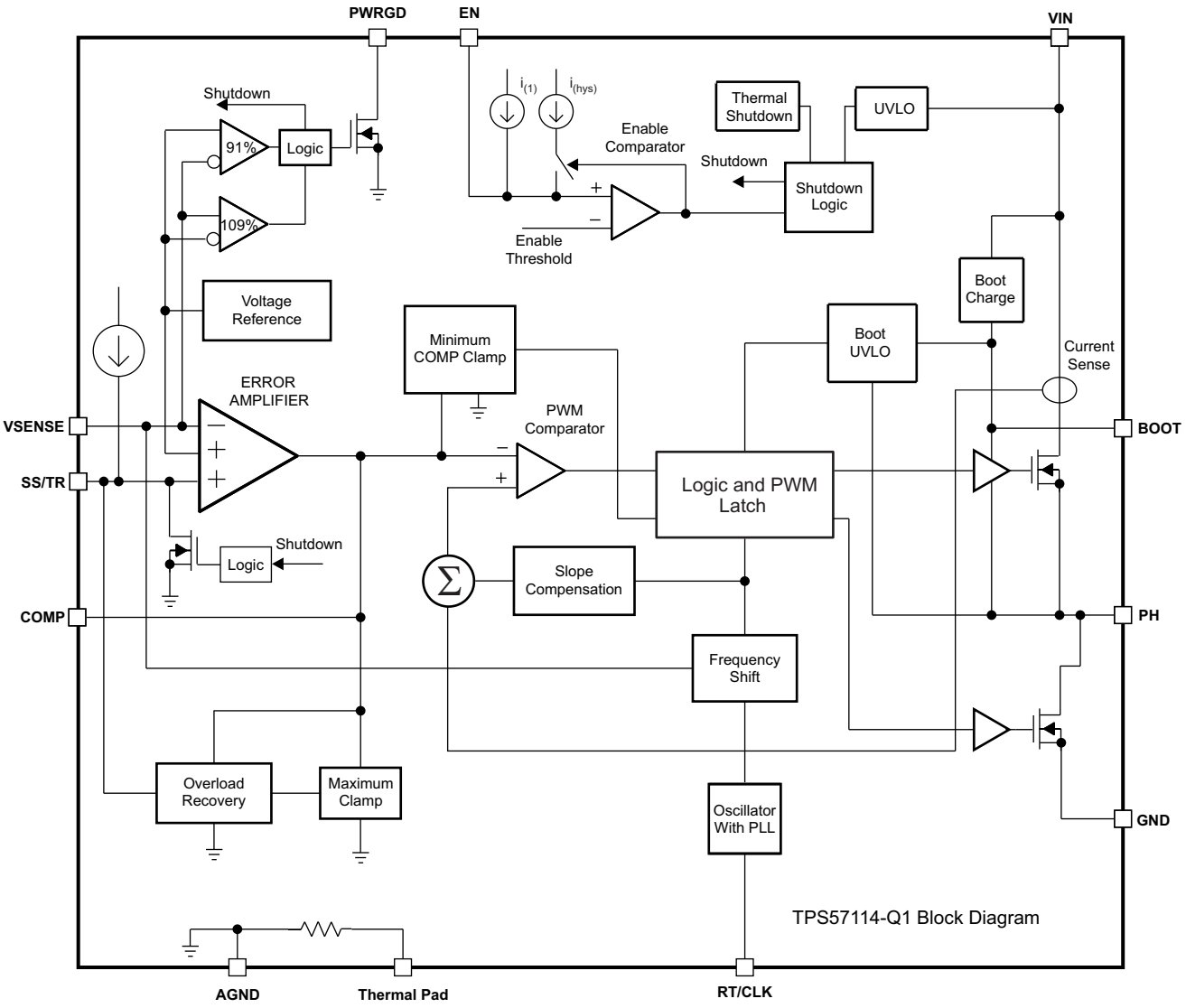


Figure 12. TPS57114-Q1 Block Diagram

- Two 12-mΩ (typical) MOSFETs for High Efficiency at 4-A Loads
- 200-kHz to 2-MHz Switching Frequency
- Synchronizes to External Clock
- Adjustable Slow Start and Sequencing
- UV and OV Power-Good Output
- Thermally Enhanced 3-mm × 3-mm 16-Pin QFN
- Pin-Compatible to TPS57112-Q1/TPS54388-Q1 devices

4.5 TPS61170-Q1

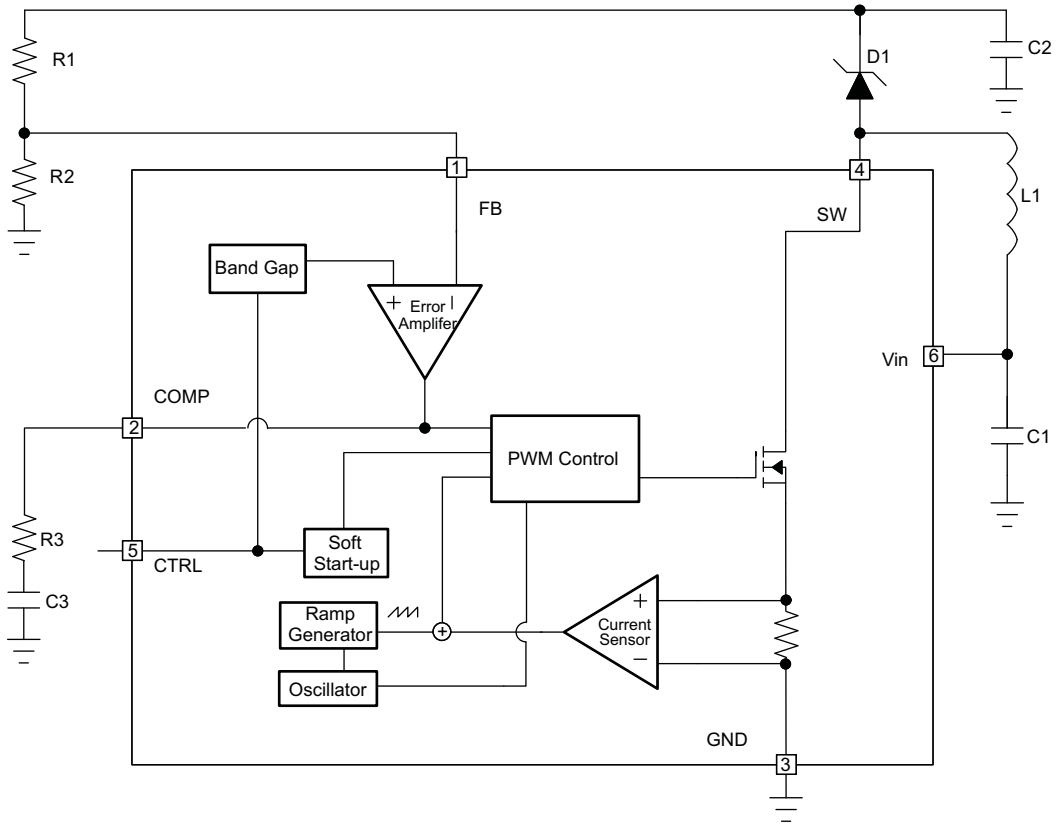


Figure 13. TPS61170-Q1 Block Diagram

- 3-V to 18-V Input Voltage Range and output voltage up to 38 V
- 1.2-A Integrated Switch
- 1.2-MHz Fixed Switching Frequency
- Up to 93% Efficiency
- *On-The-Fly* Output Voltage Reprogramming
- Skip-Switching Cycle for Output Regulation at Light Load
- Built-in Soft Start
- 6-Pin, 2-mm × 2-mm SON Package

4.6 TPS62261-Q1

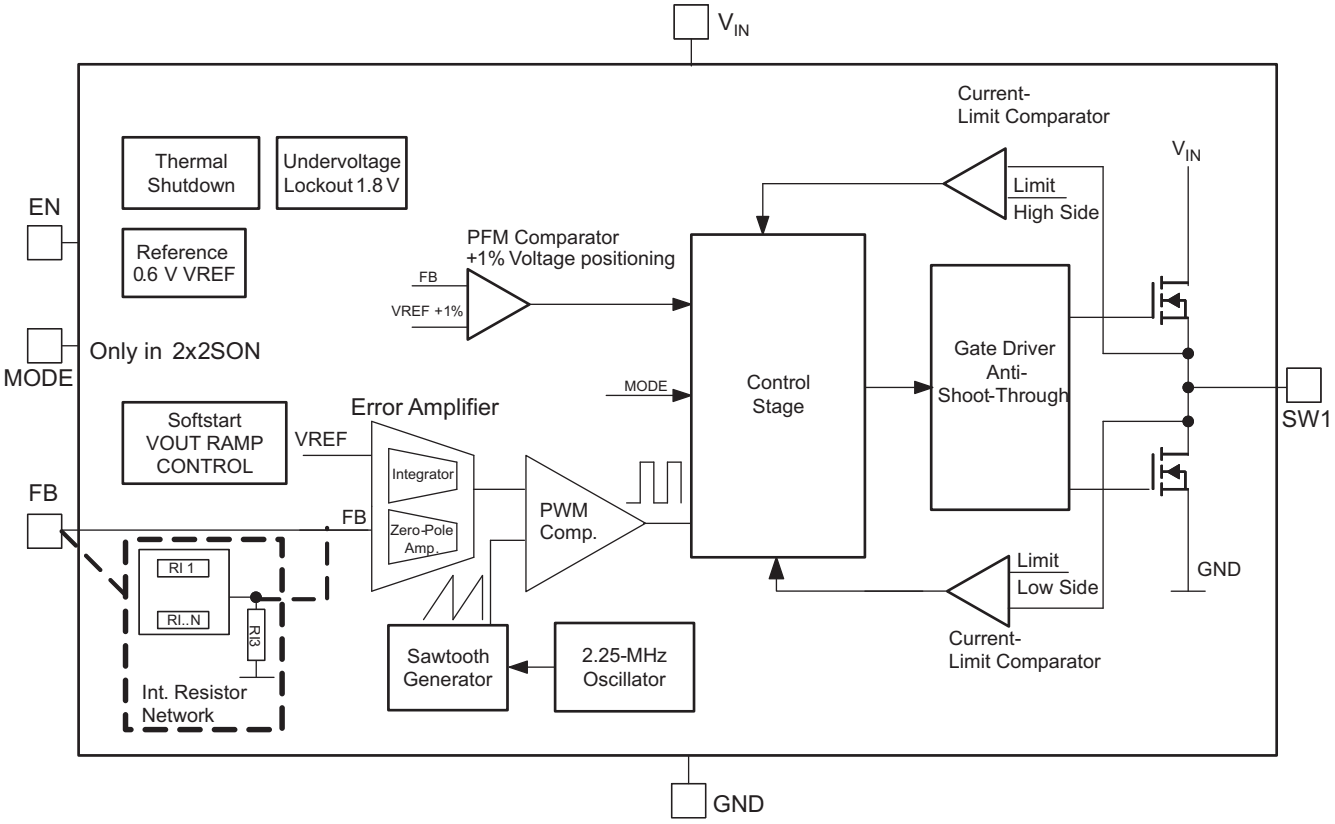


Figure 14. TPS62261-Q1 Block Diagram

- High-Efficiency Step-Down Converter with V_{IN} Range from 2 V to 6 V and output current up to 600 mA
- 2.25-MHz Fixed-Frequency Operation
- Power-Save Mode at Light-Load Currents
- 15-µA (Typ) Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Soft Start
- Voltage Positioning at Light Loads
- Available in a Small 2-mm × 2-mm × 0.8-mm SON (DRV) Package and SOT23-5 (DDC) Package
- Allows <1-mm Solution Height

4.7 TPS717XX-Q1

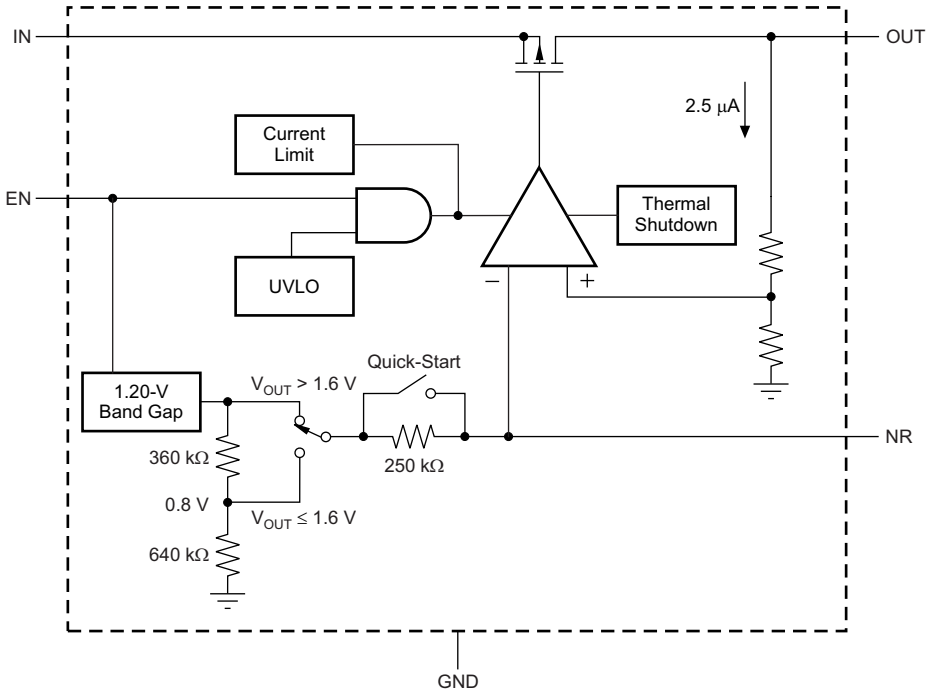


Figure 15. Fixed Voltage Versions Block Diagram

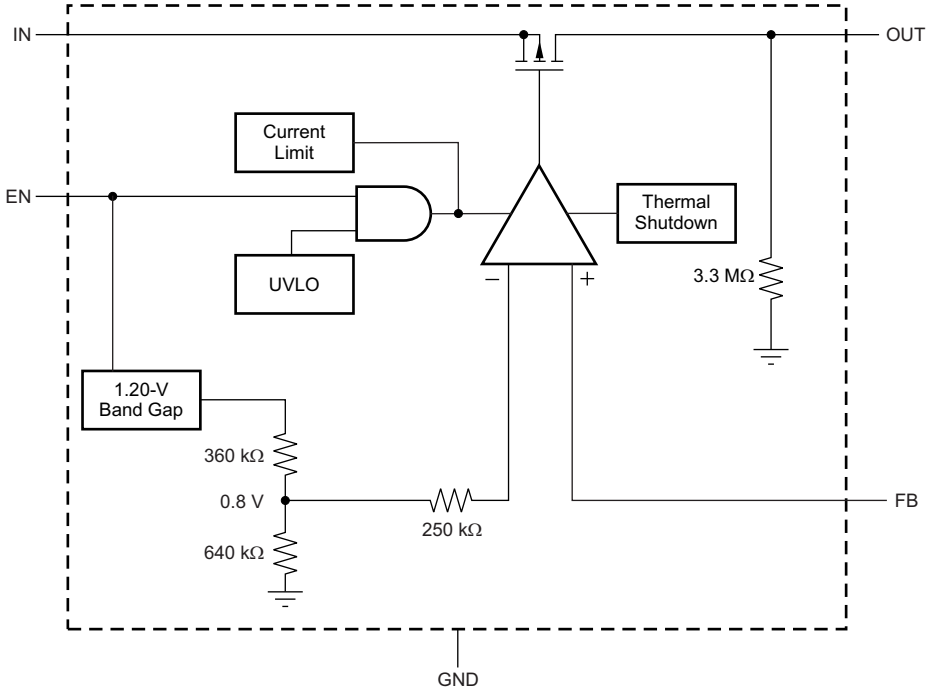


Figure 16. Adjustable Voltage Version Block Diagram

- Input Voltage: 2.5 V to 6.5 V
- Available in Multiple Output Versions:
  - Fixed Output with Voltages from 0.9 V to 5 V
  - Adjustable Output Voltage from 0.9 V to 6.2 V

- Ultra-High PSRR:
  - 70 dB at 1 kHz, 67 dB at 100 kHz, and 45 dB at 1 MHz
- Excellent Load and Line Transient Response
- Very Low Dropout: 170 mV typical at 150 mA
- Low Noise: 30 μV_{RMS} typical (100 Hz to 100 kHz)
- Small 5-pin SOT, 2-mm × 2-mm WSON-6, and 1.5-mm × 1.5-mm WSON-6 Packages

5 System Design Theory

The following sections detail the design considerations for each part of the system.

5.1 Printed Circuit Board (PCB) and Form Factor

This design does not fit any particular form-factor. The only goal of the PCB design is for as compact of a solution as possible while still providing a reasonable way to test the performance of the board. Large clip-on connectors provide access to the main voltage rails while smaller-looped test points are available to access key measurement signals. Banana connecters are for the battery input to connect to the board, which increases ease of use and protects against high current draws. See Figure 17 and Figure 18 for a 3D rendering of the board.

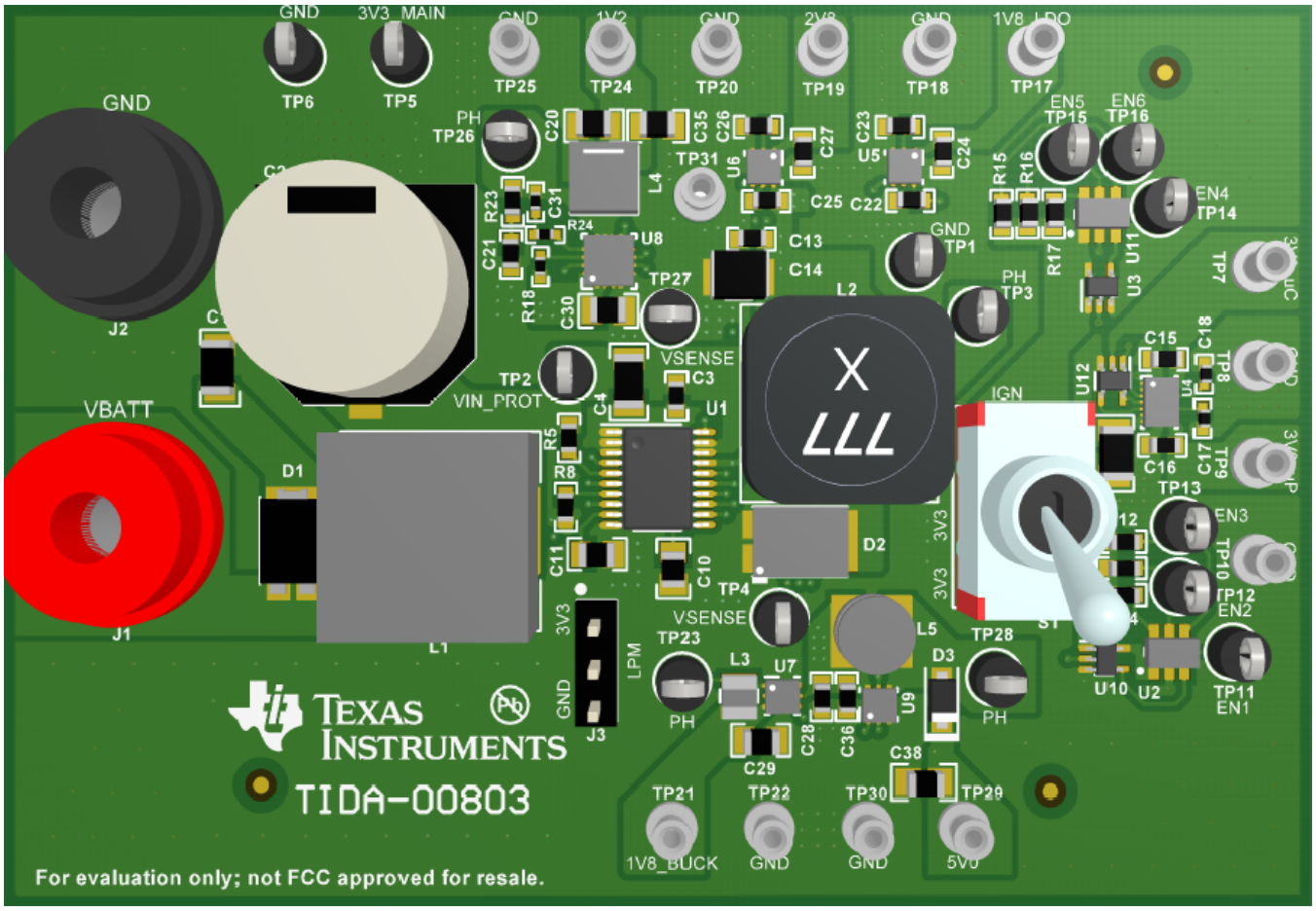


Figure 17. Printed Circuit Board Top View

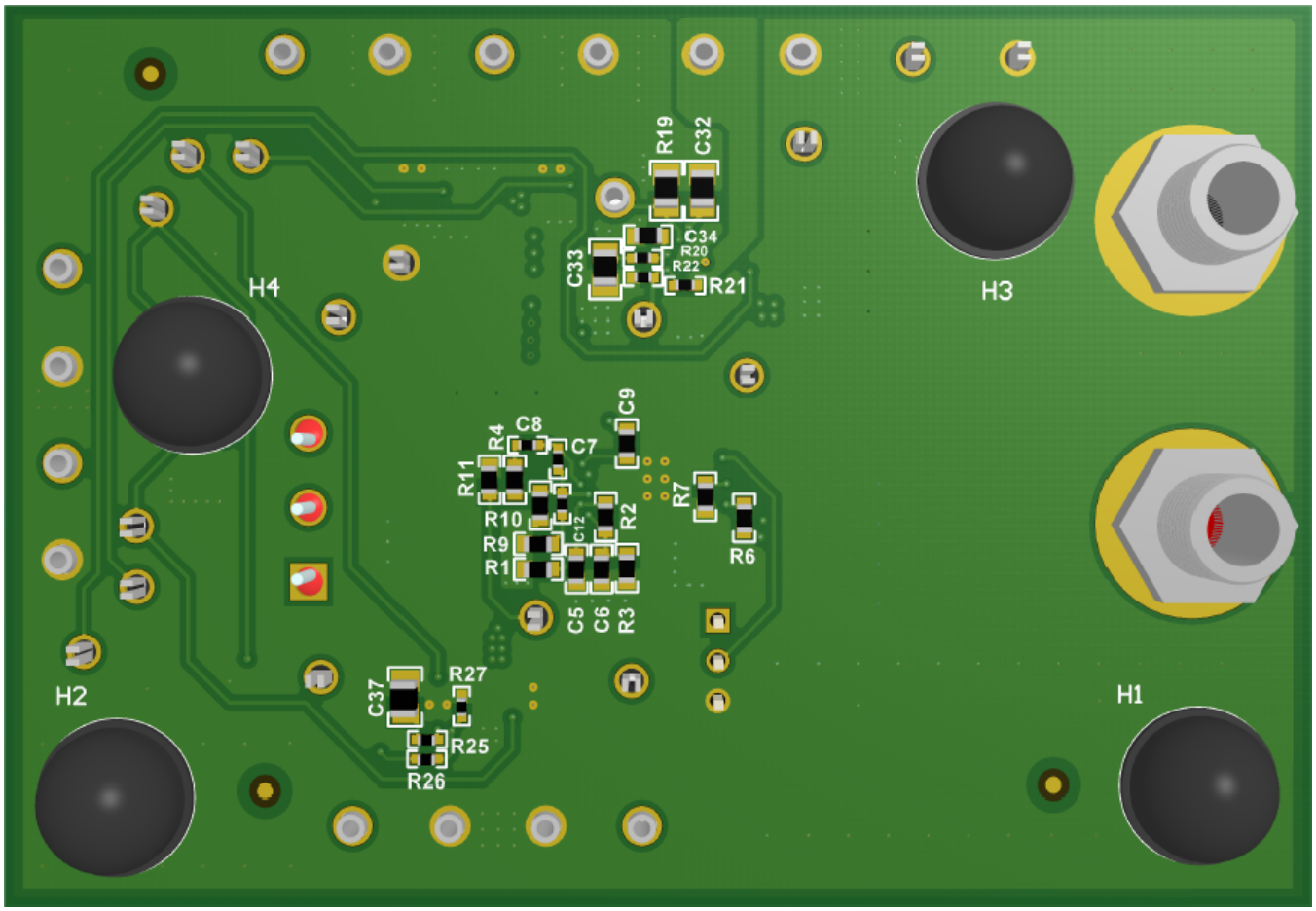


Figure 18. Printed Circuit Board Bottom View

In a final production-quality version of this design, there are several techniques that can reduce the size of the solution.

- Remove test points, headers, standoffs, ignition switch, and banana plugs in final version
- Optimize with regards to the number, size, and value of capacitors in the system
- Adjust distance of discrete regulators closer to component that the regulator supplies

5.2 Input Protection and EMI and EMC Input Filter

Nearly every electronic subsystem of a vehicle requires reverse battery protection, both by original equipment manufacturer (OEM) and ISO 16750-2, an international standard pertaining to supply quality, standards. To satisfy this requirement, this design has a traditional diode-rectifier solution for reverse battery protection that uses a PDS360-13 Schottky diode rated to handle up to 60-V transients, see Figure 19.

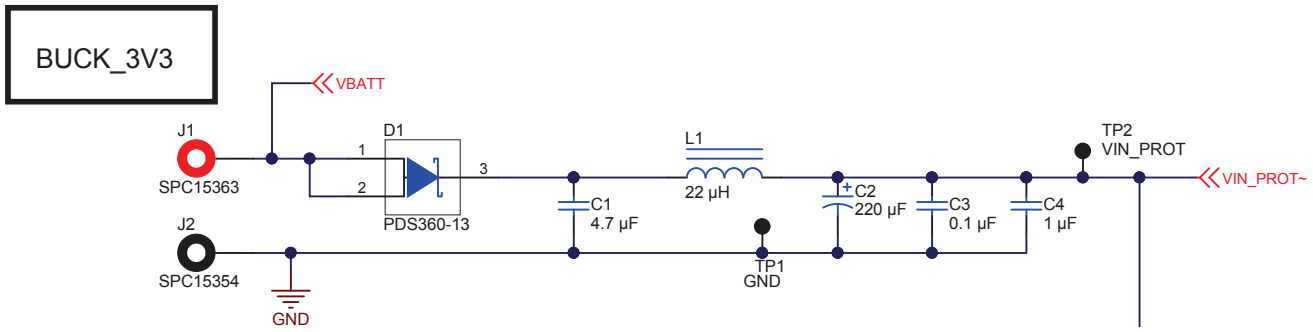


Figure 19. Input Protection and EMI and EMC Input Filter Schematic

To help mitigate EMI and EMC issues inherent to switching power supplies, there is a filter at the input to the buck pre-regulator. This filter design with the pre-regulator switching frequency, 500 KHz, reduces the radiated and conducted emissions at the input. This filter also helps resolve the issue of noise from the power supply with the combination of capacitors.

5.3 Wide-V_{IN} Buck Pre-Regulator

The TPS54362-Q1 is an AEC-Q100 qualified, Wide-V_{IN} buck regulator for use as a front-end supply to provide a 3.3-V system voltage for the solution. Input voltage range (4 V to 48 V nominally, and transients up to 60 V) can continue operation through most battery conditions (start-stop, cold-crank, load dump, and so forth).

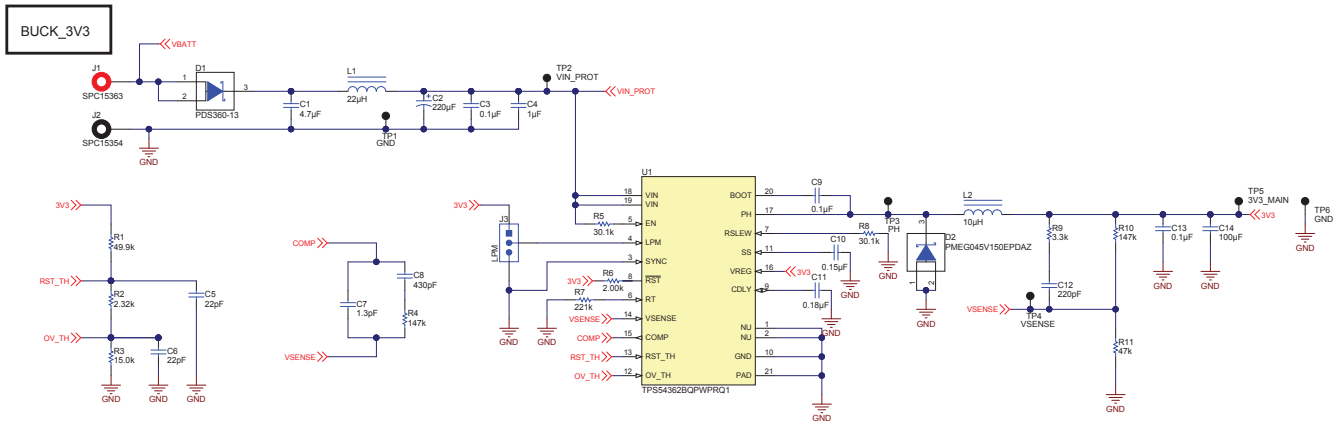


Figure 20. Wide-V_{IN} Buck Pre-Regulator Schematic

The device has an output-current limit of 3 A. A switching frequency of 500 KHz, using a resistor on the RT pin, limits switching losses and keeps the device out of the AM-frequency band. To vary the switching frequency between 200 KHz and 2.2 MHz, change the resister on the RT pin. However, the Type-III configuration and selection of the compensation components are optimized for a switching frequency of 500KHz. The TPS54362 has overvoltage and undervoltage protection, with the thresholds set at 3.59 V

and 3.18 V, respectively. To configure the device for normal or low-power operating modes, enable by using the “LPM” jumper. Connecting pins 2 and 3 enables the device to go into low-power mode when necessary, while connecting pins 1 and 2 inhibits low-power mode operation. Set the output voltage of 3.3 V using a resistor divider on VSENSE and the selection of low ESR-output capacitors improves voltage ripple and voltage drop during transients.

- Using the most stringent outcome of the equations in the *Output Capacitor (C_O)* section of data sheet SLVS845, a 100-µF output capacitor was selected and placed in parallel with a 0.1–µF capacitor to filter high-frequency noise.
- A 10-µH inductor was chosen by first calculating the minimum allowable value when evaluating ripple current, switching frequency, output voltage, minimum input voltage and maximum input voltage. The equations in the *Output Inductor Selection (L_O)* section of data sheet SLVS845 are used for these calculations.
- TI recommends that a Flyback Schottky diode must have the appropriate power rating and be placed between the PH pin and the power ground termination. Equation 29 in the datasheet determines the power the diode will be subject.
- This solution requires an input ceramic-decoupling capacitor, with type X5R or X7R dielectric, and a bulk capacitance to minimize input ripple voltage. It is imperative that the input capacitors be rated to the maximum input voltage. This solution uses 4.7 µF, 220 µF, 0.1 µF and 1 µF capacitors as part of an input filter for EMI mitigation. If no input filter is desired, consult the equations in the *Input Capacitor, $C_{(I)}$* section of data sheet SLVS845.
- A comprehensive guide to selecting the correct compensation components for the Type-III compensation network can be found in the *Loop-Control Frequency Compensation*, *Guidelines for Compensation Components*, and *Compensation* sections of data sheet SLVS845.

5.4 TPS62261-Q1 Buck Converter

The TPS62261-Q1 Step-Down Converter was chosen to supply the 1.8-V rail for the common input-output processor needs and a low-noise rail to the CMOS vision sensor peripheral. This solution was chosen due to the small package size, low-quiescent current, and high efficiency.

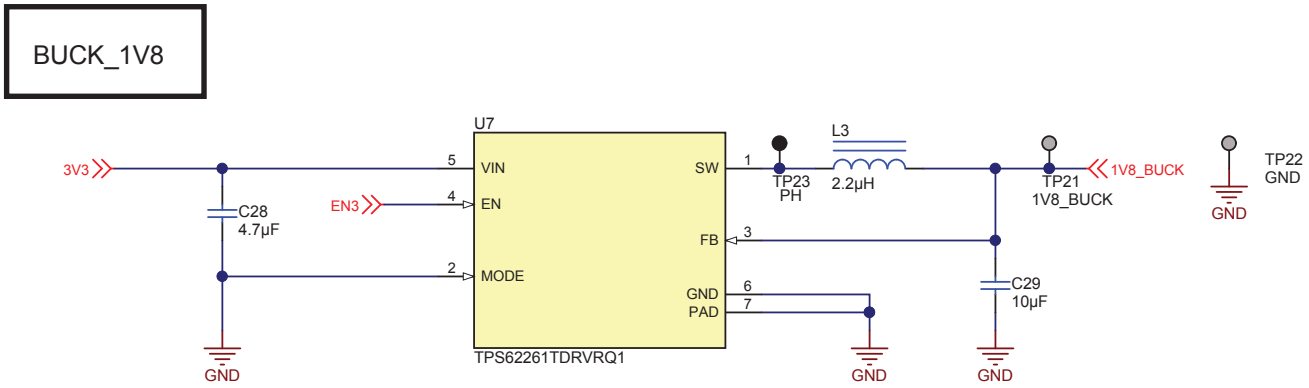


Figure 21. TPS62261-Q1 Buck Converter Schematic

An input voltage range of 2 V to 6 V gives healthy margins of error for the main 3.3-V rail and with a switching frequency of 2.25 MHz, and any EMI does not interfere with the AM band. Integrated FETs greatly reduce the solution size and BOM cost. Selecting the fixed 1.8-V solution reduces the number of external components needed. Connecting the MODE pin to ground enables the Power Save Mode with automatic transition from PFM mode to fixed-frequency PWM mode, which helps with efficiency.

- An input capacitor of 4.7 µF mitigates any noise on the 3.3-V main rail caused by high input voltage spikes
- A 2.2-µH inductor, with a saturation current of 1A, handles the entire range of loads
- An output capacitor of 10 µF helps improve load transient performance

5.5 TPS57114-Q1 Buck Converter

The TPS57114-Q1 synchronous step-down switcher was selected to provide the high-current 1.2-V rail for the processor core and memory peripheral. The device is AEC-Q100 qualified. Covering a possible input range of 2.95 V to 6 V with a configurable output voltage that can provide up to 4A, the TPS57114-Q1 device is very useful for low voltage, high-current applications. To help comply with EMI and EMC requirements by avoiding the AM band, using an 82.5-kΩ resistor chooses a switching frequency of 2 MHz. The addition of an RC-snubber circuit improves EMI and EMC quality. Although the solution does include internal FETs, the design does require an external compensation network.

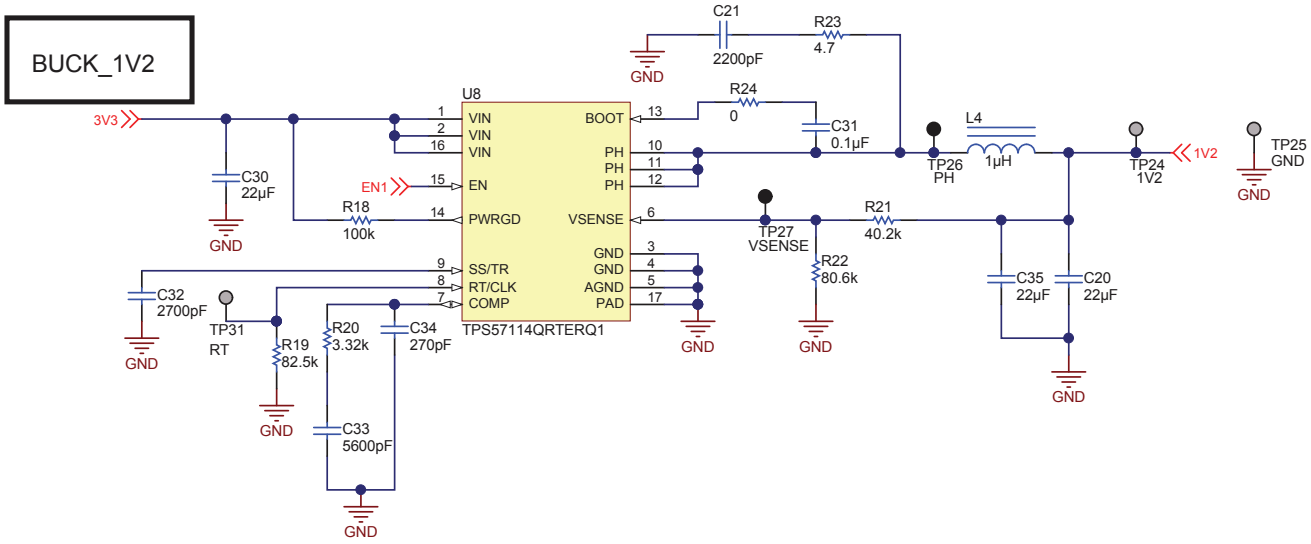


Figure 22. TPS57114-Q1 Buck Converter Schematic

Consulting the application section of the datasheet is helpful when calculating the output circuitry and compensation components, consulting the applications section of the datasheet is helpful. For this design, the following considerations were used when selecting the output components:

- A 1-µH inductor with a 5.4-A saturation-current rating was chosen based upon calculations for ripple current, peak current, and transient conditions. See the equations in the *Output Inductor Selection* section in datasheet SLVSAH5.
- Two 22-µF, ceramic, X7S capacitors were chosen and placed in series to represent a 44-µF output capacitor. Three main factors were used to determine the output capacitor: determining the modulator pole, the output-voltage ripple, and how the regulator responds to a large change in load current. The ESR of the capacitor plays a large role in the placement of the modulator pole and the output-voltage ripple, while the overall capacitance value affects the response to transients. See the equations in the *Output Capacitor* section in data sheet SLVSAH5 to help determine the correct selection.
- The output voltage must be selected using a resistor-divider pair. Use the equations in the *Output-Voltage And Feedback-Resistor Selection* section in data sheet SLVSAH5 to select the resistor-divider pair.

Selecting the correct type of compensation network and the necessary compensation components within that network can be difficult. However, the compensation section in the datasheet does a good job of describing the process. For this design, a type-2A compensation network was used.

5.6 TPS61170-Q1 Boost Converter

The TPS61170-Q1 High-Voltage Boost Converter was used to provide the 5.0-V rail that is commonly used for CAN transceivers in ADAS systems. Operating at 1.2-MHz switching frequency allows the use of low-profile inductors, low-value ceramic input capacitors, and output capacitors that reduce overall solution size. This device requires a simple RC-compensation network, a voltage divider to determine the output voltage, and typical output-filter components.

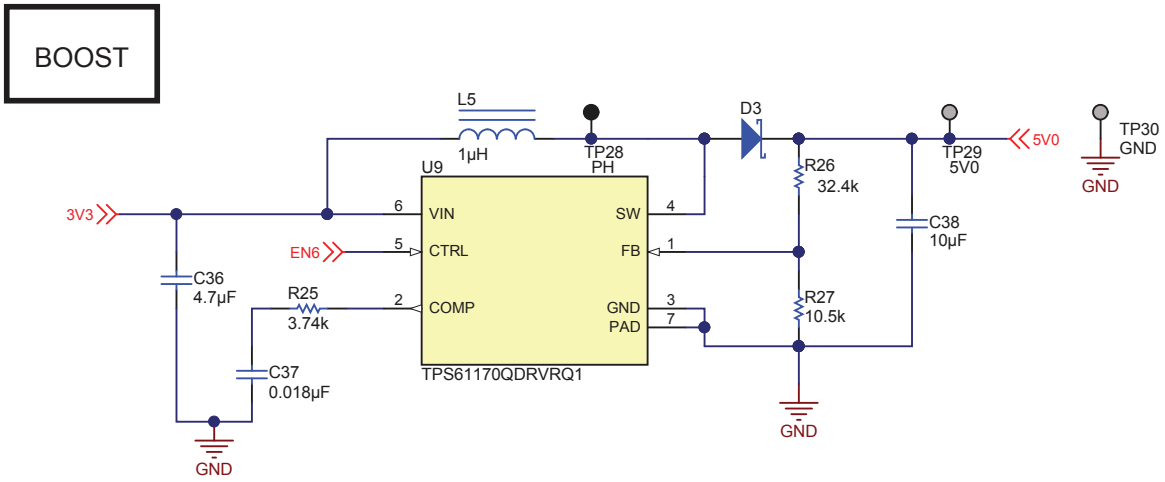


Figure 23. TPS61170-Q1 Buck Converter Schematic

The output components were selected using the Application and Implementation section of the datasheet:

- A 1-µH inductor with 3.8-A saturation current was selected according to the requirements of the three main factors: inductor value, DC resistance (DCR), and saturation current.
- The high-switching frequency of the TPS61170-Q1 demands a high-speed rectifying switch. Ensuring that the average-current and peak-current ratings of the diode exceed the average-output current and peak-inductor current is a must. Schottky diodes are the most common selections. This design uses a PMEG2010AED Schottky diode with a 1-A average-current rating and 9-A peak-current rating.
- A 10-µF, ceramic, X7R-output capacitor was selected using the equations in the *Input and Output Capacitor Selection* section in data sheet SLVSAX2.
- An external resistor and ceramic capacitor are connected to the COMP pin to provide a pole and zero. This pole and zero, along with the inherent pole of a current-mode control-boost converter, determine the closed-loop frequency response. This is important to converter stability and transient response. Following the *Compensation Capacitor Selection* section inSLVSAX2 helps determine these components for the design solution.

5.7 TPS71728-Q1 and TPS71718-Q1 LDOs

LDOs are commonly used in applications that require very little noise on the voltage rail. In this solution, the TPS71718-Q1 provides a low-noise 1.8-V rail for the CMOS image sensor and the TPS71728-Q1 provides the low-noise 2.8-V rail for the same CMOS image sensor. Both LDOs are fixed volta ge and use the same output components.

- A low-ESR, 2.2-µF, ceramic–output capacitor increases the bandwidth of the control loop, which increases the response time to changes in load.
- A 0.1-µF input capacitor was implemented in the design to help dampen any noise from the other regulators on the 3V3-main rail.
- To reduce the output noise even further, a 0.1-µF capacitor was connected to the noise reduction pin, which is only available on the fixed voltage configurations of the TPS717xx-Q1.

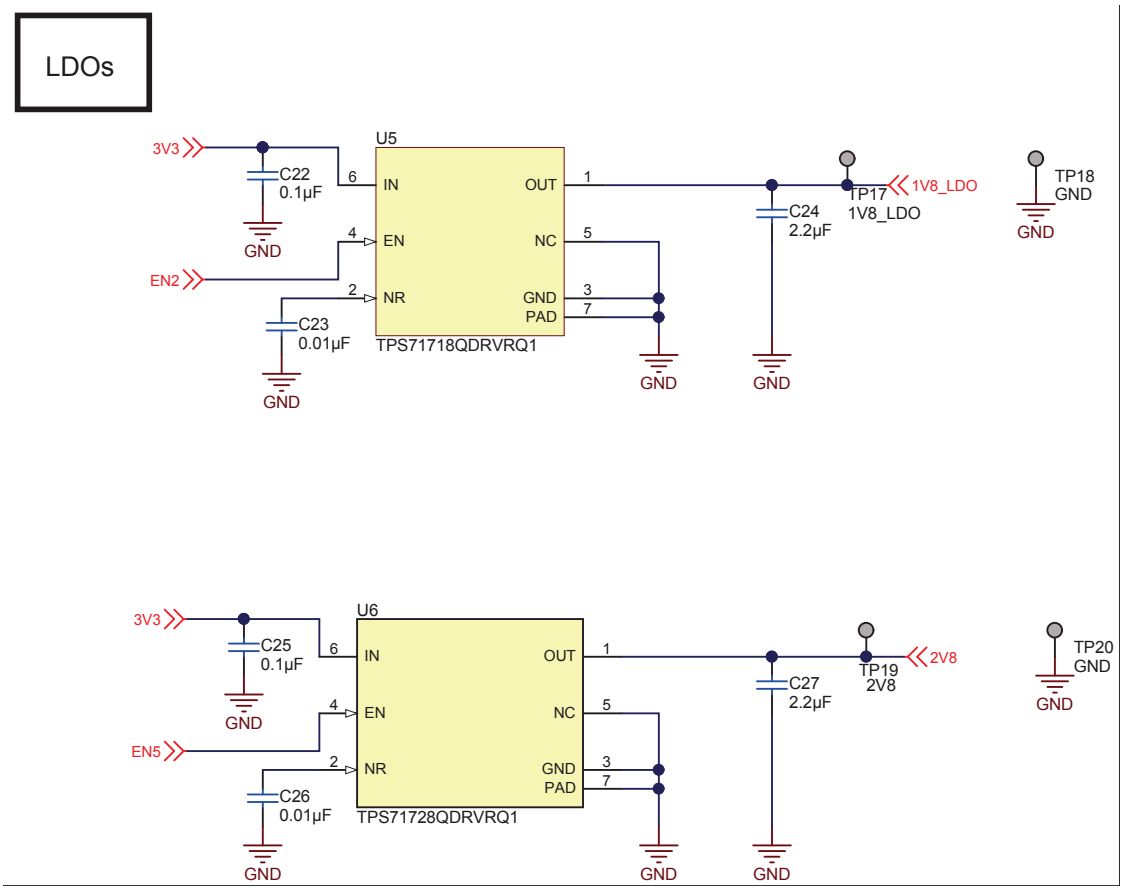


Figure 24. TPS71728-Q1 and TPS71718-Q1 LDOs

5.8 General Power Supply Design Considerations

Choose inductors for DC-DC converters such that:

- The ripple current is between 20% to 40% of the load current ILOAD (with the given F_{SW}, V_{IN}, and V_{OUT}). For this design, 40% was used.
- The temperature ratings are appropriate for an automotive application, typically –40°C to +125°C for ADAS applications.
- Saturation current is chosen per the following equation for peak current, plus additional margin: ISAT ≥ (ILOAD + 0.5 × IRIPPL) × 1.2

For ADAS applications, it is recommended that all ceramic capacitors use X7R dielectric material, which ensures minimum capacitance variation over the full temperature range. The voltage rating of the capacitors should be greater than the maximum voltage they could see, and two times the typical voltage seen to avoid DC-bias effects. The amount of output capacitance to use depends on output ripple and transient response requirements and there are many equations and tools available online to help estimate these. Power supplies in this solution were designed for a ±2.5% (5%) total–transient response. To reduce ripple, low-ESR ceramic capacitors were used exclusively. For internally compensated supplies, please see device-specific datasheets, as there may be limitations on acceptable LC-output filter values. Devices should always be qualified per AEC-Q100. TI parts, which are qualified, will typically end their part numbers with Q1. For improved accuracy, all FB-resistor dividers should use components with 1% or better tolerance.

5.9 Voltage Sequencing

The solution for sequencing uses two cascaded LM3880-Q1 three-channel sequencers, in conjunction with some logic and a battery-supply supervisor. The order in which the LM3880-Q1 enables or disables its outputs, and delays associated with power-up and power-down, is different between several orderable part numbers. In this design case, they sequence up 1->2->3, and down 3->2->1, with equal 2-mS delays between each. The solution requires external logic to properly execute power-down sequencing.

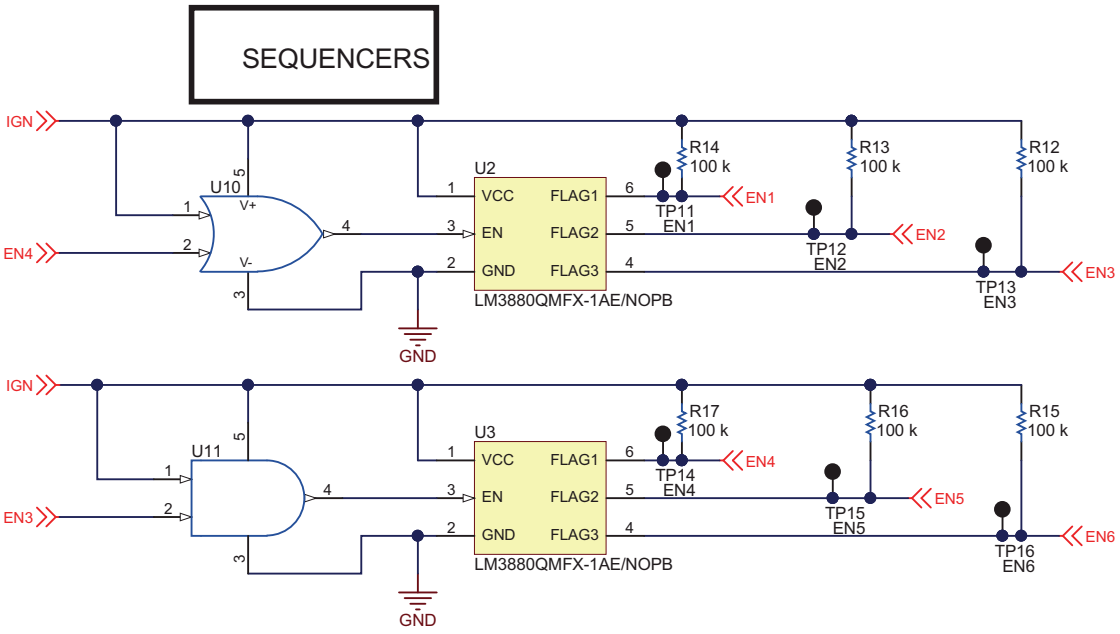


Figure 25. Sequencing Schematic

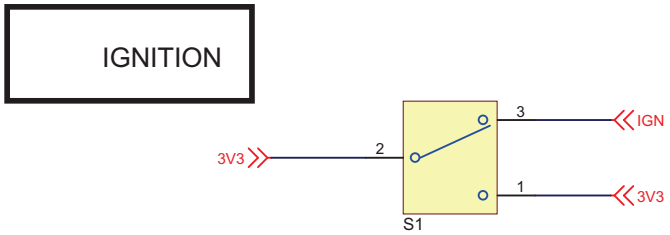


Figure 26. Ignition Switch

Sometimes there are multiple power rails in a system, which have the same voltage, but need to be sequenced or controlled separately. A load switch allows the use of the same LDO or DC-DC for both rails, while having independent control over each. In this case, 3V3_uC and 3V3_uP are both 3.3-V rails that are sourced from the TPS54362-Q1, but can be sequenced independently. For this solution, instead of providing two separate enable signals to the TPS22966-Q1 load switch, discrete logic delays the sequencing of the 3V3_uP rail until the 3V3_uC rail is powered on.

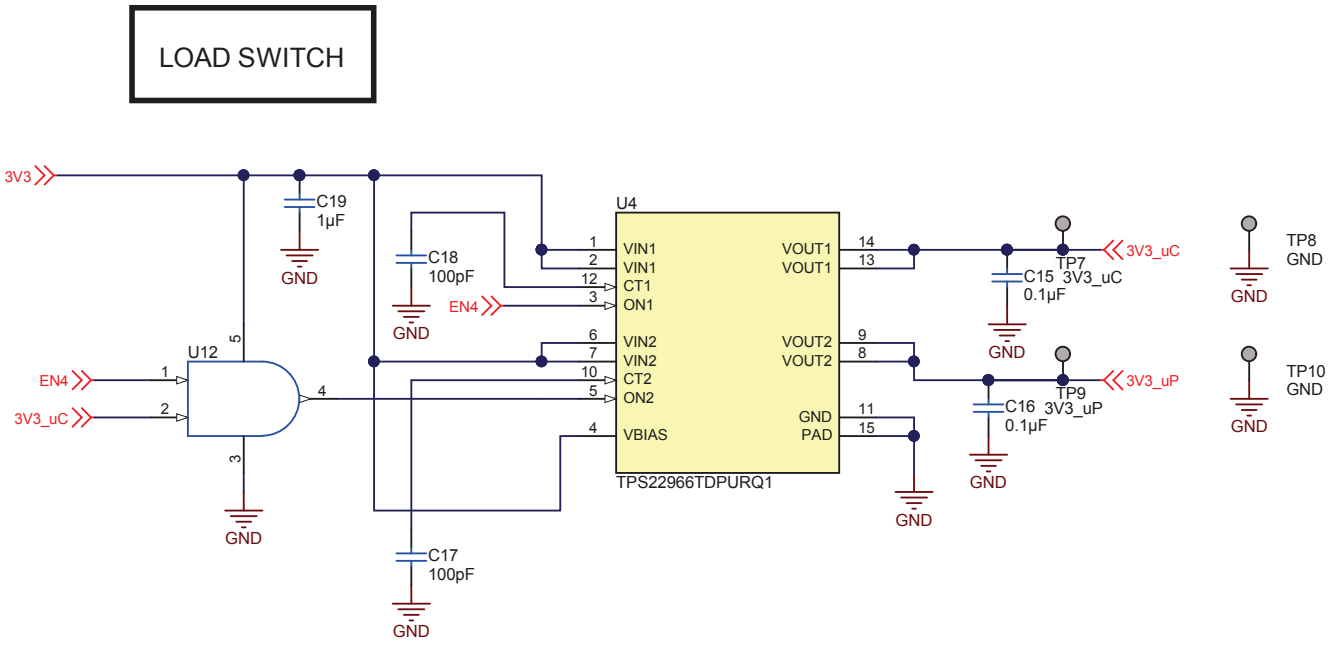


Figure 27. TPS22966-Q1 Load Switch

6 Getting Started

6.1 Hardware

The TIDA-00803 is easy to set up. Please refer to Figure 28 for component locations.

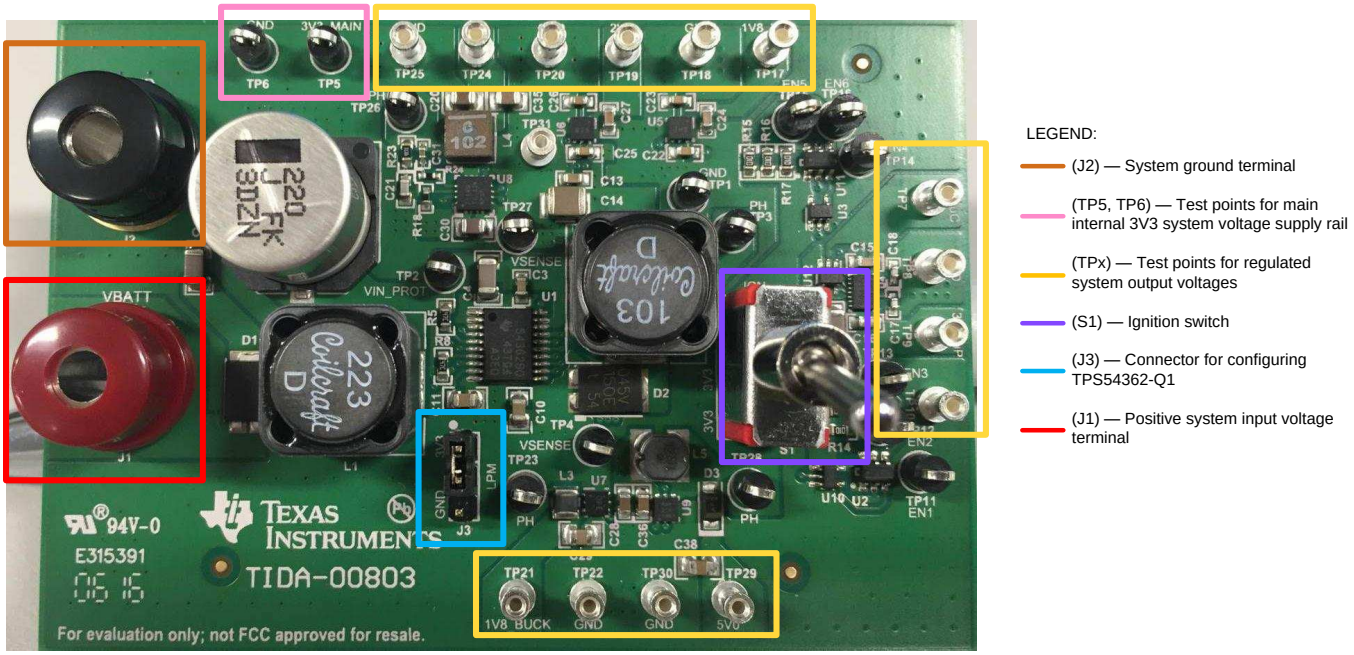


Figure 28. Hardware

- Red Box (J1): The connecter J1 is for the positive input voltage to the system. This is a female receptacle for standard banana plugs. Acceptable limits for input voltage are 4 V to 48 V and set a 3 A limit on the power supply if possible.
- Brown Box (J2): The connector J2 is the ground connection for the system and it is a receptacle for a standard banana plug.
- Blue Box (J3): The jumper J3 configures the TPS54362-Q1 Pre-Regulator low-power mode. Connecting pins 1 and 2 forces the device to operate in normal mode at a fixed frequency. Leaving the jumper open or connecting pins 2 and 3 allows the device to change automatically between normal and low-power mode depending on load current.
- Purple Box (S1): The switch S1 is the ignition switch. The top position is OFF and the bottom position is ON. To enable the voltage rail sequencers, the switch must be in the bottom (ON) position. TIDA-00803 can be powered on with the switch in either position.
- Yellow Box (TPx): The connectors boxed in yellow are the regulated output voltages of the system. Each voltage rail is paired with a ground connector for easy testing.
- Pink Box (TP5, TP6): The test points, TP5 and TP6, boxed in pink are the main internal 3V3-voltage supply rail of the system.
- Other test points monitor switching nodes, enable signals, and sense voltage lines placed throughout the design for evaluation purposes.

6.1.1 Hardware Setup

Before starting, connect a power-supply with sufficient output power using banana-jack cables to J1 (VBATT) and J2 (GND). If desired, apply loads to the outputs. Consider the total current available from the pre-regulator when determining loads. Consult the *Key System Specifications* section for the maximum current that each component should provide for correct values.

6.1.1.1 Power Up

The design configuration powers up the pre-regulator, which supplies the main 3V3 rail as soon as the user applies power to the board. To enable the remaining voltage rails through the predetermined power-up sequence, the ignition switch must be switched to the bottom position (closest to TP28). Placing the ignition switch in the top position at any time disables all voltage rails, except the main 3V3 rail.

6.1.1.2 Power Down

There is no pre-determined power-down sequence for this design. Simply switch the ignition switch to the top position to disable all voltage rails, but the 3V3 main rail, or remove the input voltage to disable the whole system.

7 Test Setup

The following sections show the test setups for the corresponding tests and test data.

7.1 Load Regulation Test Setup

To test how well each voltage rail behaves under loading, see the setup in Figure 29. A DC-power supply with a setting of 13 V was the input power to the system. A voltmeter was placed across the output connecters of each output and the electronic load in use had an internal Ammeter monitoring the load current. The electronic load was applied at the output connectors of each voltage rail. Using an oscilloscope, V_{OUT}, Load CurrentV, and the Switching Node (PH) waveforms were captured. For the LDOs, output-voltage noise was monitored instead of ripple voltage and there was no PH waveform to capture. The outputs were monitored with no load, a light load, and maximum load. Intermittent load steps were also observed to determine how well the output was regulated and provide the information in the Load Regulation graphs in the *Test Data* section.

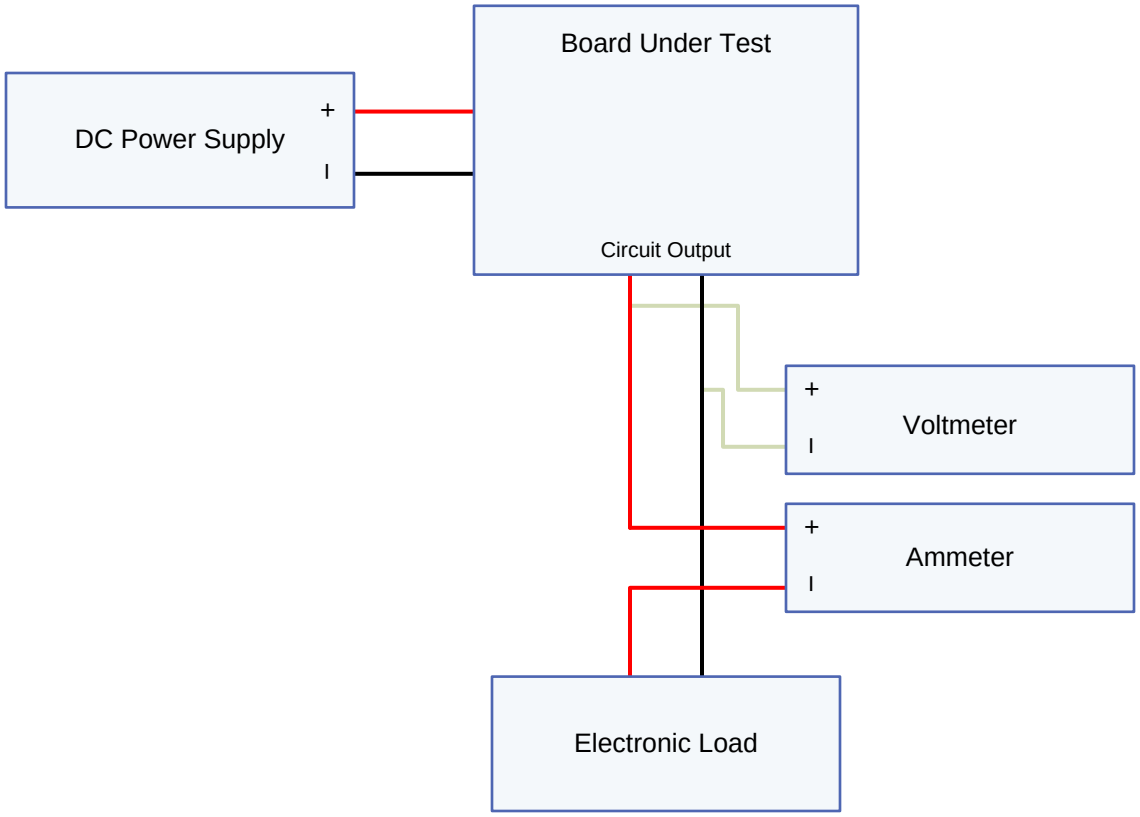


Figure 29. Setup for Measuring Load Regulation of Voltage Rails

7.2 Output Ripple Voltage Test Setup

The output ripple voltage of each voltage rail was observed using the setup in Figure 30. A DC-power supply with a setting of 13 V was the input power to the system. An electronic load was applied across the output connectors of each voltage rail. An oscilloscope, placed directly across the output capacitor and set to AC coupling, captured the output voltage ripple. The Load Current was also monitored via a current probe. Plots were taken showing the voltage-rail ripple voltage under minimum-load current and maximum-load current per the *Key System Specifications* section.

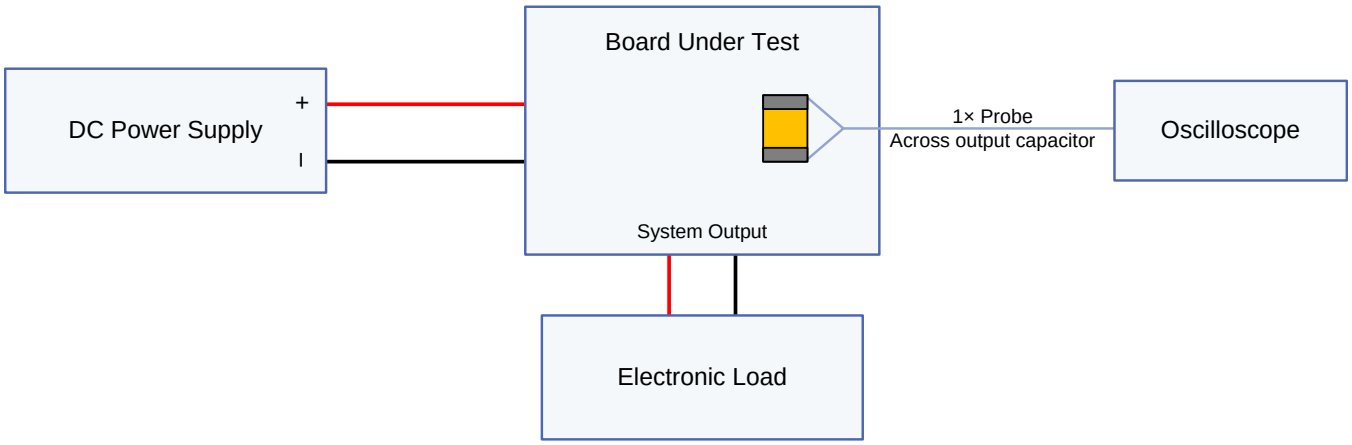


Figure 30. Setup for Measuring Output Ripple Voltage of Voltage Rails

7.3 Load Transient Test Setup

Using the setup in Figure 31, a load transient was applied to each output to determine how well the voltage rail responds to drastic changes in load. A DC-power supply with a setting of 13 V was the input power to the system. An AC-coupled oscilloscope probe placed directly across the output capacitor of the respective voltage rail captured the changes in V_{OUT} due to the applied load setup. To apply a load setup, an electronic load was connected across the output, and was controlled by an external FET. When the FET was ON, the load was the load determined by the electronic load. When the FET was OFF, there was no load. The FET switching frequency was determined by a square wave from a function generator. The load and frequency varied depending on the voltage rail under test.

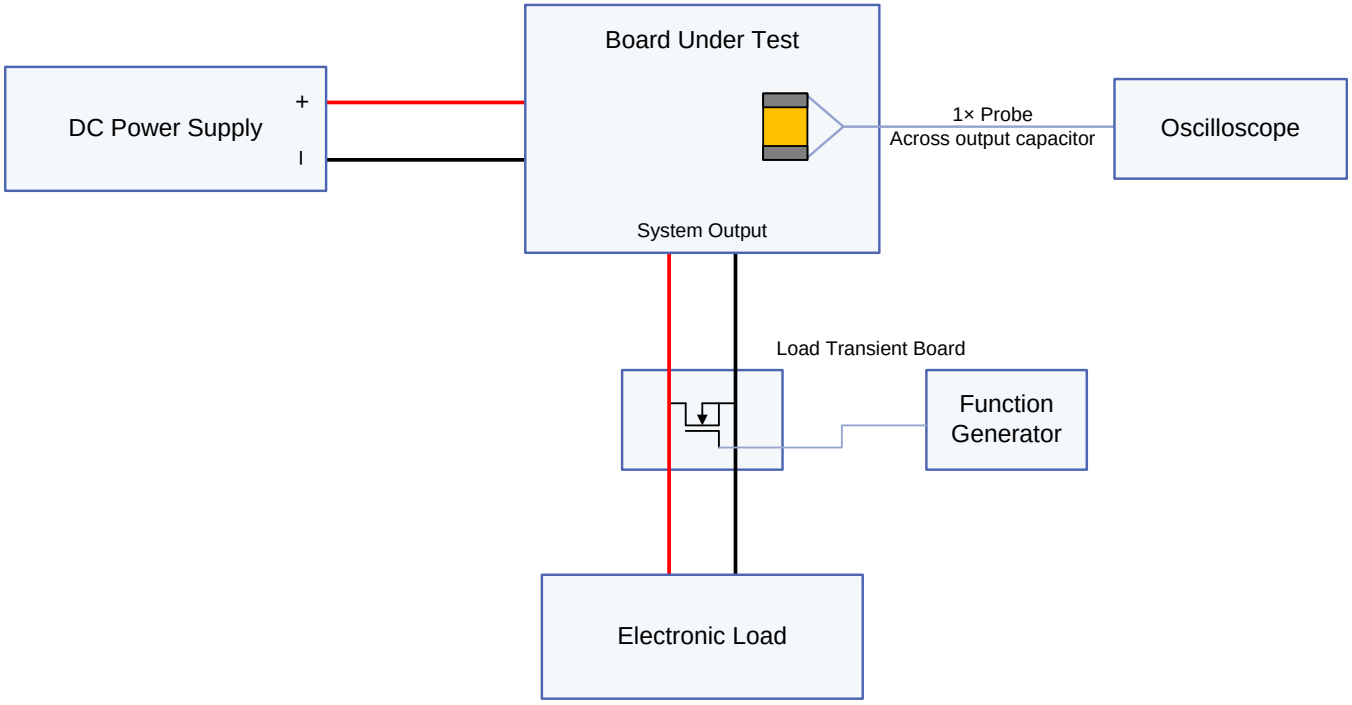


Figure 31. Setup for Measuring Load Transients on Voltage Rails

7.4 Efficiency Test Setup

Due to the layout of the design, determining the efficiency of each individual regulator was not feasible. However, an approach was taken so that the system efficiency of each regulator could be captured. Using the setup in Figure 32, the efficiency graphs shown in the Efficiency sections of *Test Data* were created. Rather than applying an discrete input voltage to each regulator and monitoring the output, the system-input voltage of 13 V was applied by a DC power supply, and the 3.3-V main rail was used as the input voltage to the regulator under test. The system-input voltage as well as the system-input current was monitored in addition to the output voltage and output current of the voltage rail being tested. Although this does not give the strict efficiency of each regulator, it shows, at a system level, how efficient each regulator is as load current from the electronic load is increased.

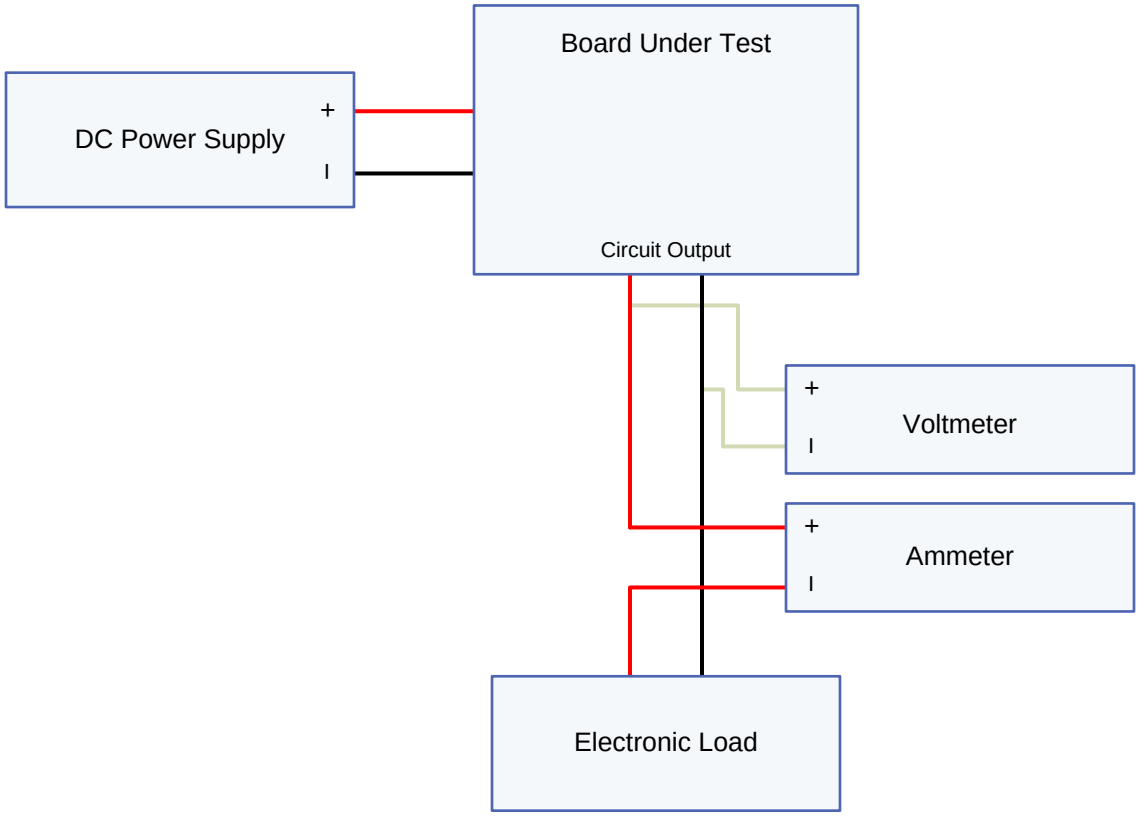


Figure 32. Setup for Measuring System Efficiency of Voltage Rails

7.5 Sequencing Test Setup

To observe the power-up sequencing of the voltage rails. A DC-power supply of 13 V was applied at the system input and no loads were connected to any of the voltage rails. Using an oscilloscope, four voltage rails were monitored at a time and the rails were cycled through to show the ramp timing for all outputs. Setup behavior was captured with the ignition switch both in the ON position at the time V_{IN} was applied, showing the ramping of the 3.3-V main rail with respect to the other output voltage rails, and the OFF position, showing the ramping of the output voltage rails once the 3.3-V main rail had already been stabilized.

8 Test Data

The following section show the test data from characterizing the switching power supplies in the system.

8.1 TPS54362-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.1.1 Load Regulation

The plots in Figure 33 and Figure 34 show the behavior of the 3.3-V main rail provided by the TPS54362-Q1 device.

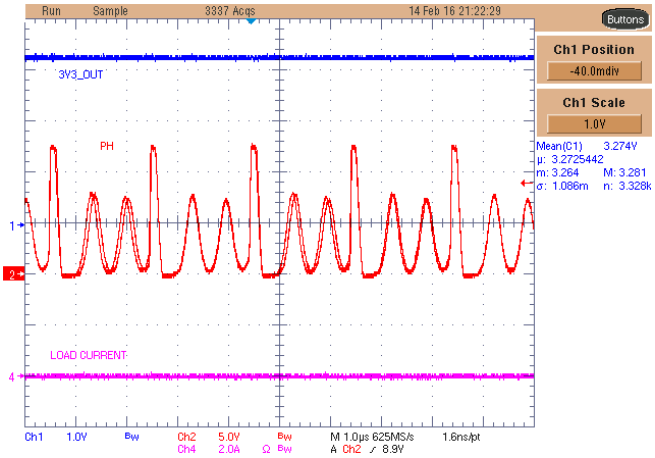


Figure 33. TPS54362-Q1 3.3-V Main Rail With No Load

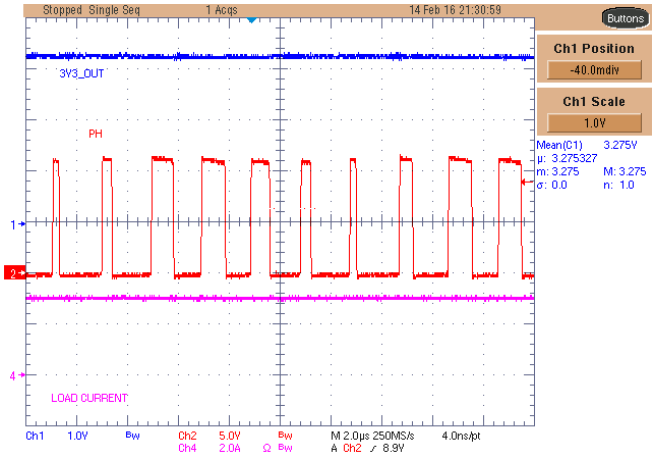


Figure 34. TPS54362-Q1 3.3-V Main Rail With 3-A Load

8.1.2 Output Ripple Voltage

The plots in Figure 35 and Figure 36 show the ripple voltage of the 3.3-V main rail provided by the TPS54362-Q1 device.

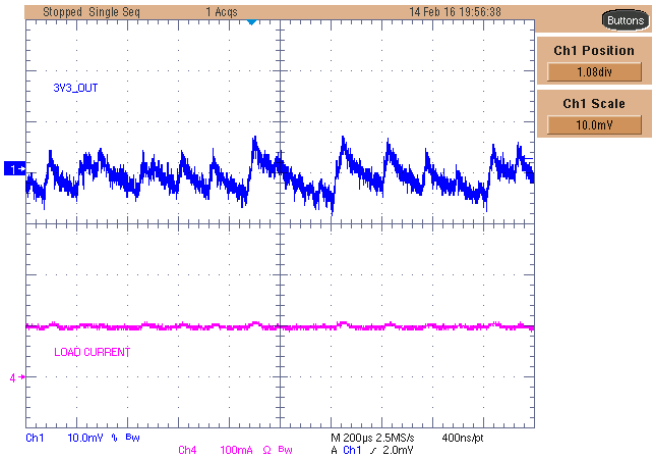


Figure 35. TPS54362-Q1 3.3V-Main Rail Ripple Voltage With 100-mA Load

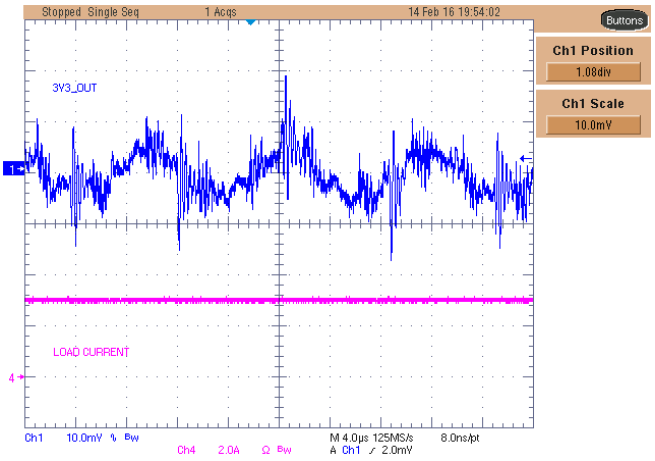


Figure 36. TPS54362-Q1 3.3V-Main Rail Ripple Voltage With 3-A Load

8.1.3 Load Transient

The plot in Figure 37 shows a 3-A load transient on the main 3.3-V rail provided by the TPS54362-Q1 device.

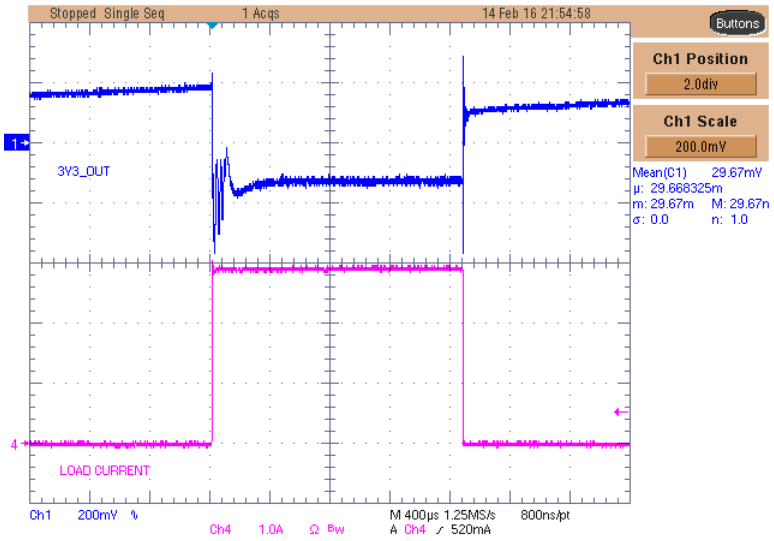


Figure 37. TPS54362-Q1 3.3-V Main Rail Voltage With 3-A Load Transient

8.1.4 Efficiency

The plot in Figure 38 shows the system efficiency of the TPS54362-Q1 main 3.3-V rail. This efficiency was determined with all other rails powered off and the load placed directly on the main 3.3-V rail.

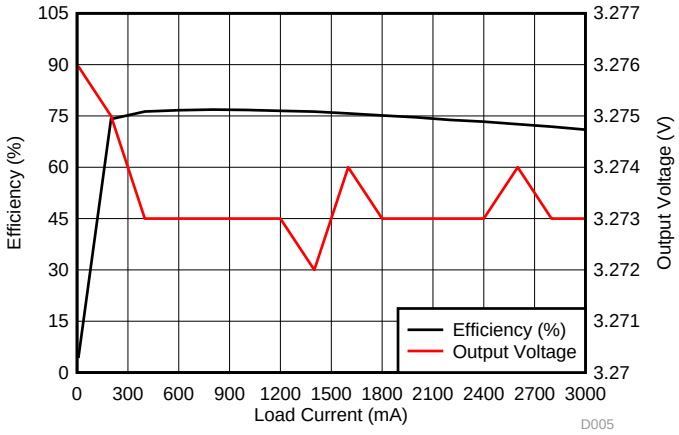


Figure 38. Efficiency of TPS54362-Q1 Main 3.3-V Rail

8.2 TPS62261-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.2.1 Load Regulation

The plots in Figure 39 and Figure 40 show the behavior of the 1V8_BUCK rail provided by the TPS62261-Q1 device.

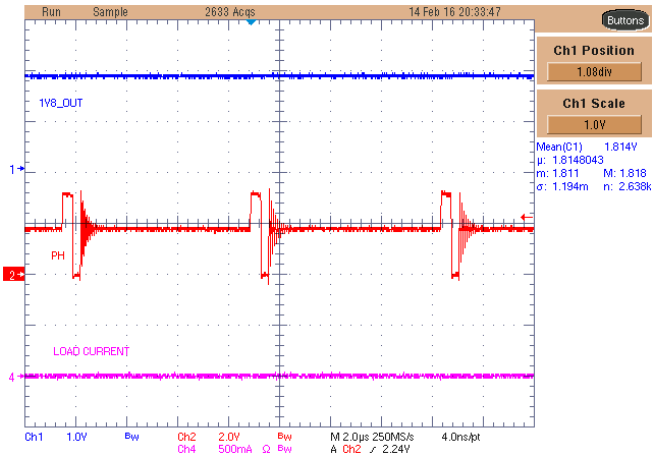


Figure 39. TPS62261-Q1 1V8_BUCK Rail With No Load

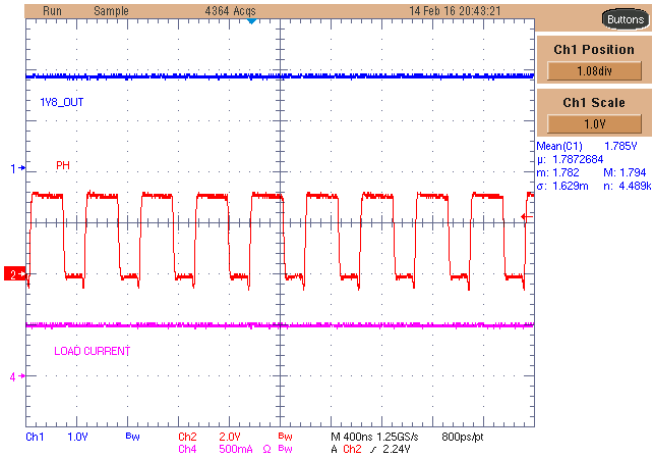


Figure 40. TPS62261-Q1 1V8_BUCK Rail With 500-mA Load

8.2.2 Output Ripple Voltage

The plots in Figure 41 and Figure 42 show the ripple voltage of the 1V8_BUCK rail provided by the TPS62261-Q1 device.

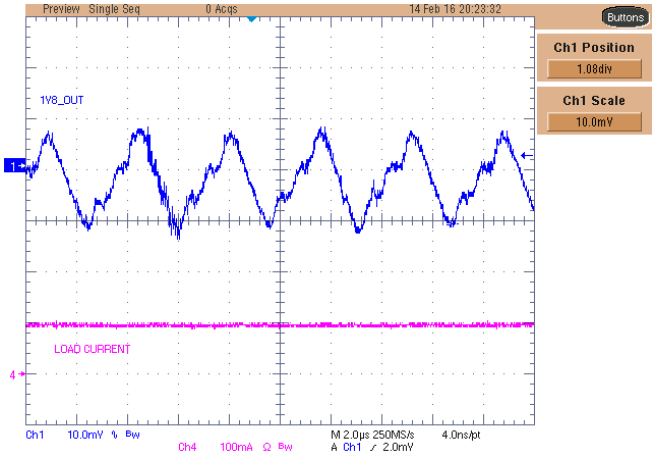


Figure 41. TPS62261-Q1 1V8_BUCK Rail Ripple Voltage With 100-mA Load

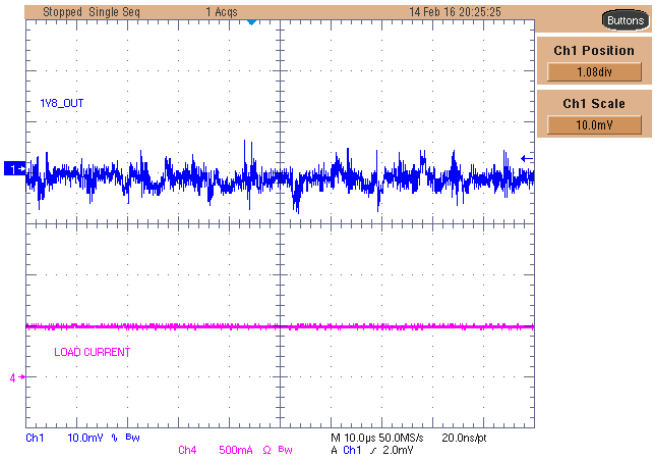


Figure 42. TPS62261-Q1 1V8_BUCK Rail Ripple Voltage With 500-mA Load

8.2.3 Load Transient

The plot in Figure 43 shows a 500-mA load transient on the 1V8_BUCK rail provided by the TPS62261-Q1 device.

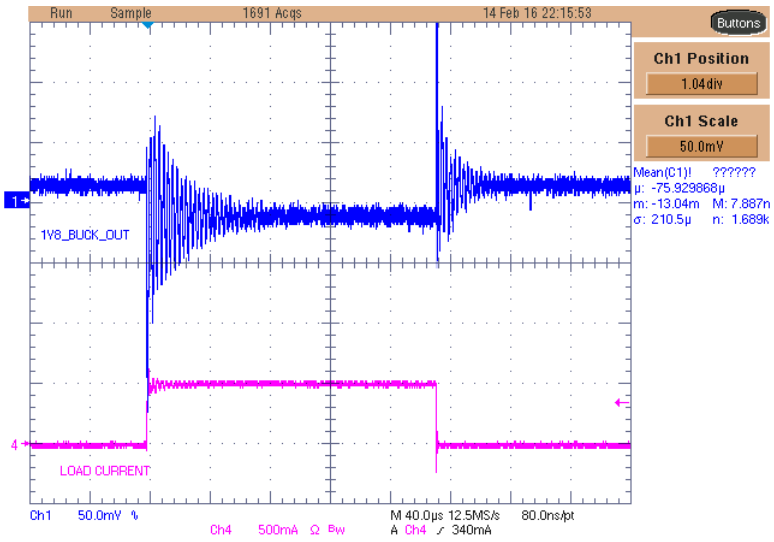


Figure 43. TPS62261-Q1 1V8_BUCK Rail Voltage With 500-mA Load Transient

8.2.4 Efficiency

The plot in Figure 44 shows the system efficiency of the TPS62261-Q1 1V8_BUCK rail. This efficiency was determined with all other rails powered on.

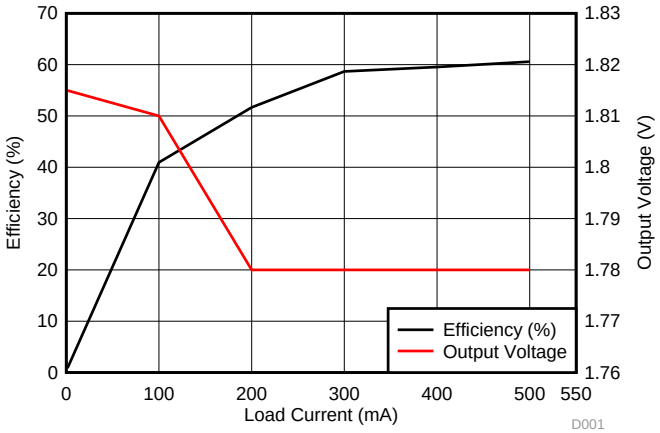


Figure 44. Efficiency of TPS62261-Q1 1V8_BUCK Rail

8.3 TPS57114-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.3.1 Load Regulation

The plots in Figure 45 and Figure 46 show the behavior of the 1.2-V rail provided by the TPS57114-Q1.

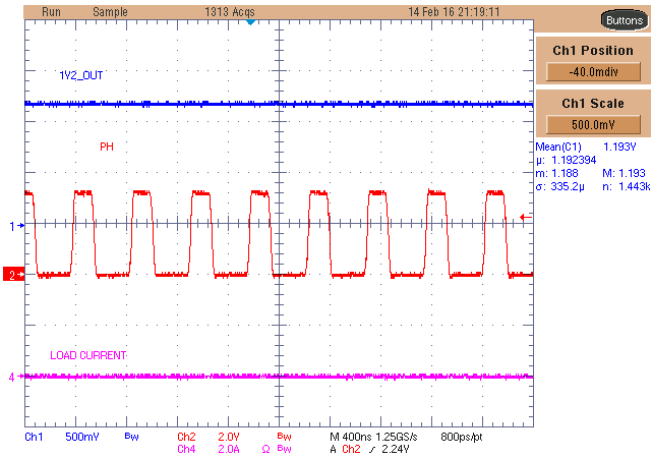


Figure 45. TPS57114-Q1 1.2-V Rail With No Load

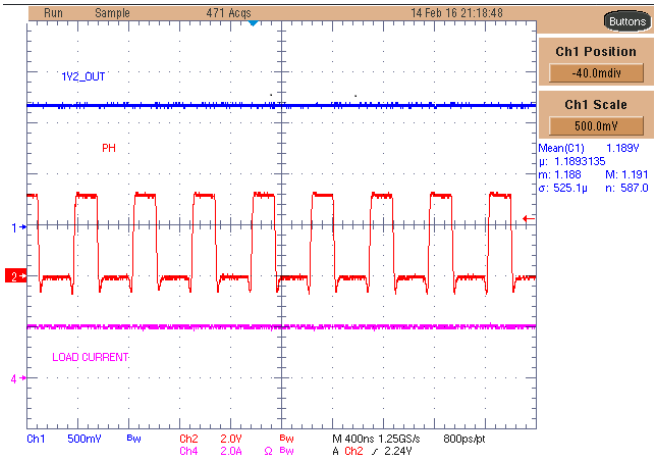


Figure 46. TPS57114-Q1 1.2-V Rail With 2-A Load

8.3.2 Output Ripple Voltage

The plots in Figure 47 and Figure 48 show the ripple voltage of the 1.2-V rail provided by the TPS57114-Q1 device.

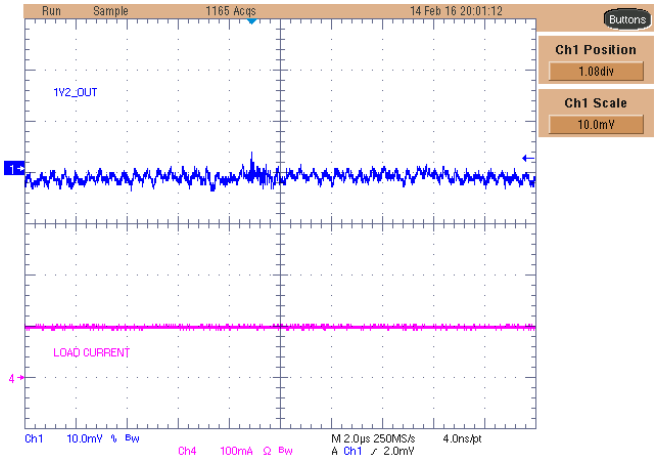


Figure 47. TPS57114-Q1 1.2-V Rail Ripple Voltage With 100-mA Load

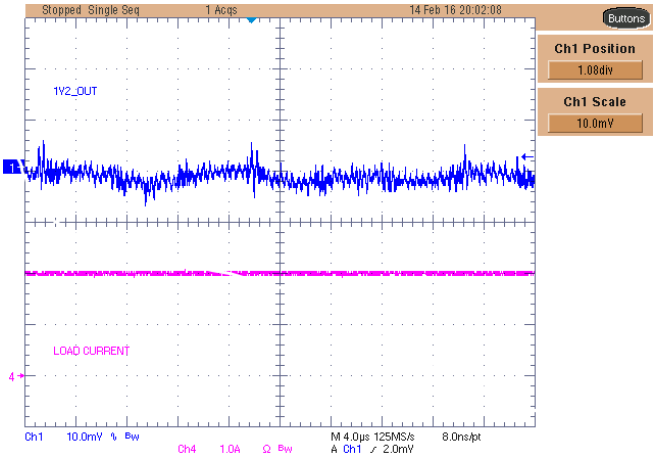


Figure 48. TPS57114-Q1 1.2-V Rail Ripple Voltage With 2-A Load

8.3.3 Load Transient

The plot in Figure 49 shows a 2-A load transient on the 1.2-V rail provided by the TPS57114-Q1 device.

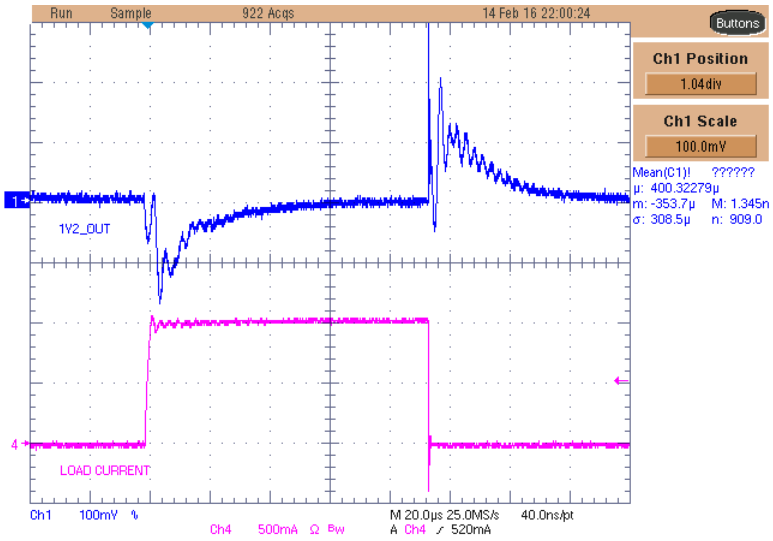


Figure 49. TPS57114-Q1 1.2-V Rail Voltage With 2-A Load Transient

8.3.4 Efficiency

The plot in Figure 50 shows the system efficiency of the TPS57114-Q1 1.2-V rail. This efficiency was determined with all other rails powered on.

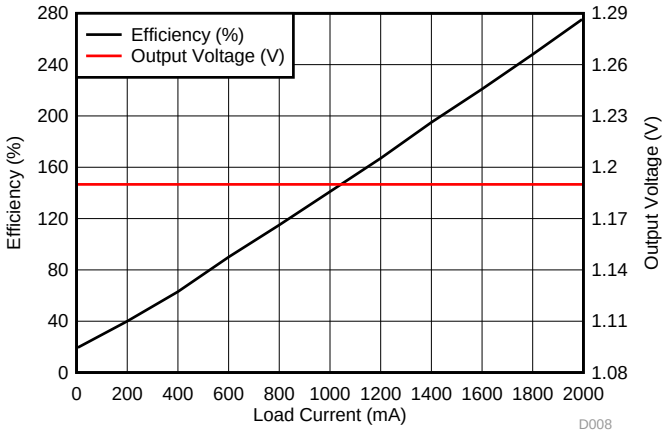


Figure 50. Efficiency of TPS57114-Q1 1.2-V Rail

8.4 TPS61170-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.4.1 Load Regulation

The plots in Figure 51 and Figure 52 show the behavior of the 5.0-V rail provided by the TPS61170-Q1.

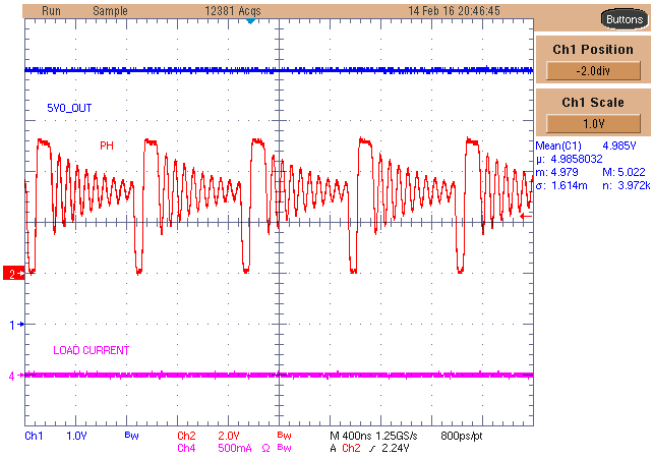


Figure 51. TPS61170-Q1 5.0-V Rail With No Load

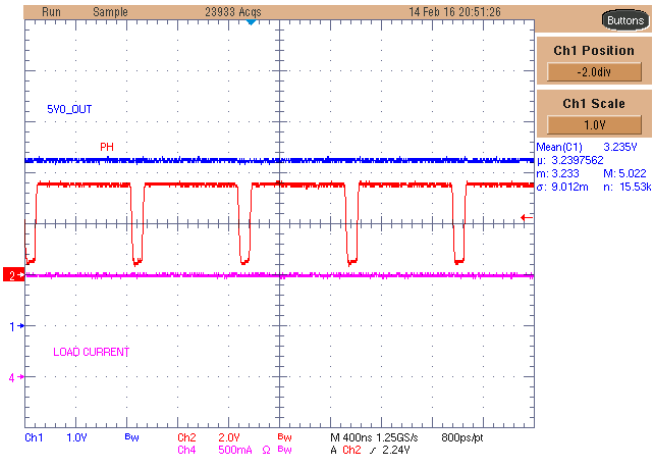


Figure 52. TPS61170-Q1 5.0-V Rail Ripple Voltage With 1-A Load

8.4.2 Output Ripple Voltage

The plots in Figure 53 and Figure 54 show the ripple voltage of the 5.0-V rail provided by the TPS61170-Q1 device.

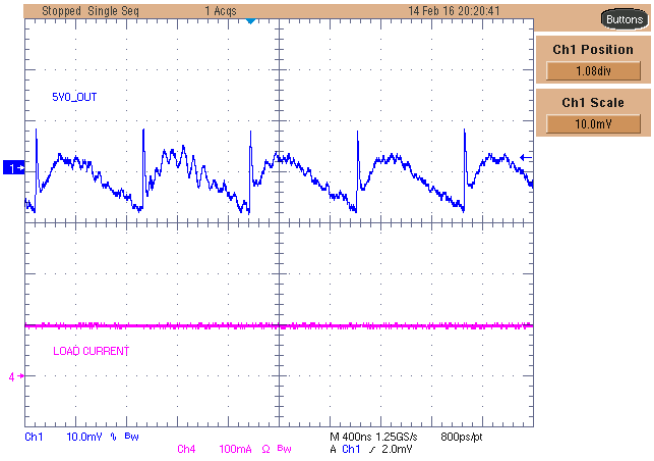


Figure 53. TPS61170-Q1 5.0-V Rail Ripple Voltage With 100-mA Load

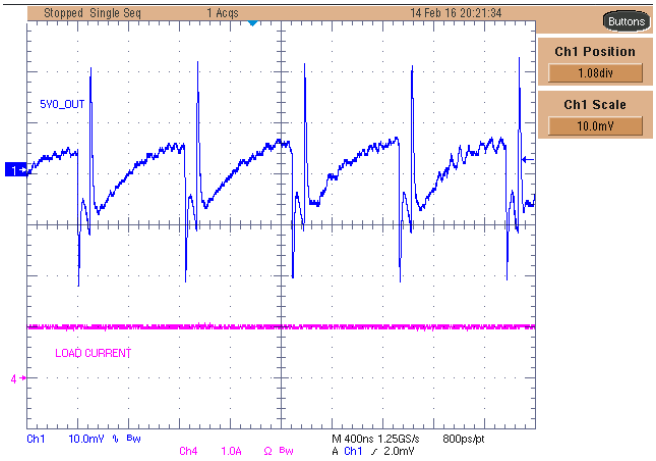


Figure 54. TPS61170-Q1 5.0-V Rail Ripple Voltage With 1-A Load

8.4.3 Load Transient

The plot in Figure 55 shows a 2-A load transient on the 1.2-V rail provided by the TPS57114-Q1 device.

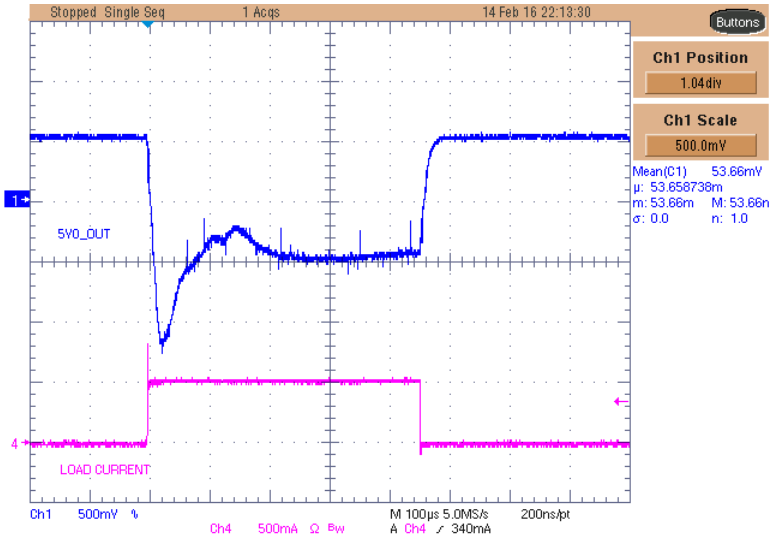


Figure 55. TPS61170-Q1 5.0-V Rail Voltage With 500-mA Load Transient

8.4.4 Efficiency

The plot in Figure 56 shows the system efficiency of the TPS61170-Q1 5.0-V rail. This efficiency was determined with all other rails powered on.

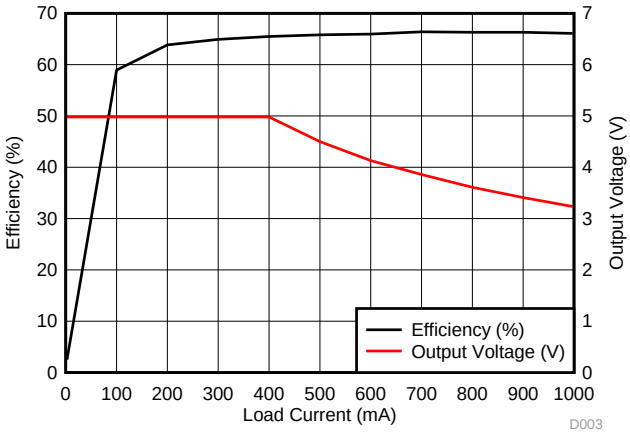


Figure 56. Efficiency of TPS61170-Q1 5.0-V Rail

8.5 TPS71718-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.5.1 Load Regulation

The plots in Figure 57 and Figure 58 show the behavior of the 1V8_LDO rail provided by the TPS71718-Q1.

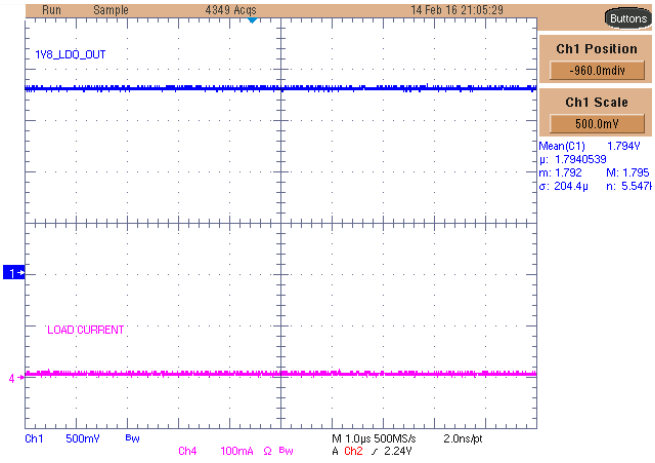


Figure 57. TPS71718-Q1 1V8_LDO Rail With No Load

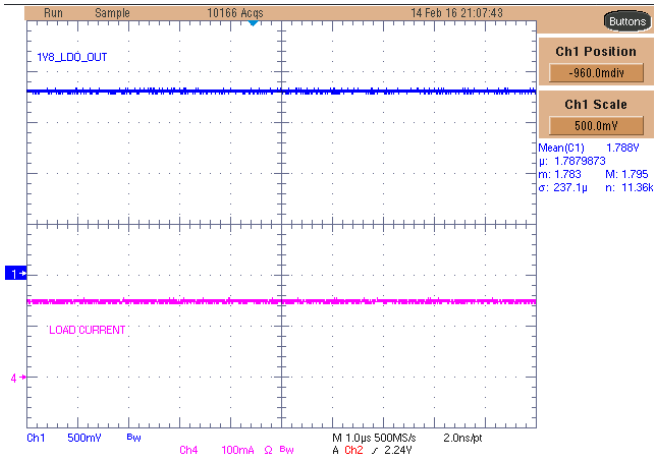


Figure 58. TPS71718-Q1 1V8_LDO Rail With 150-mA Load

8.5.2 Output Ripple Voltage

The plot in Figure 59 shows the ripple voltage of the 1V8_LDO rail provided by the TPS71718-Q1 device.

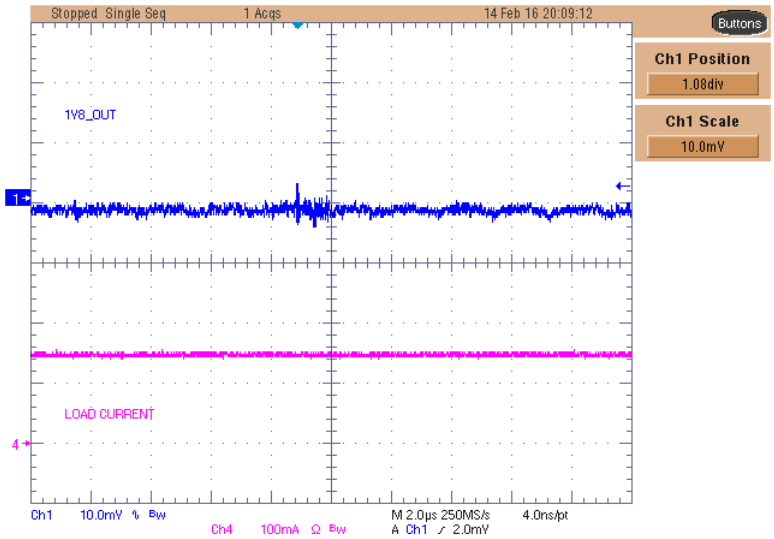


Figure 59. TPS71718-Q1 1V8_LDO Rail Ripple Voltage With 150-mA Load

8.5.3 Load Transient

The plot in Figure 60 shows a 150-mA Load Transient on the 1V8_LDO rail provided by the TPS71718-Q1 device.

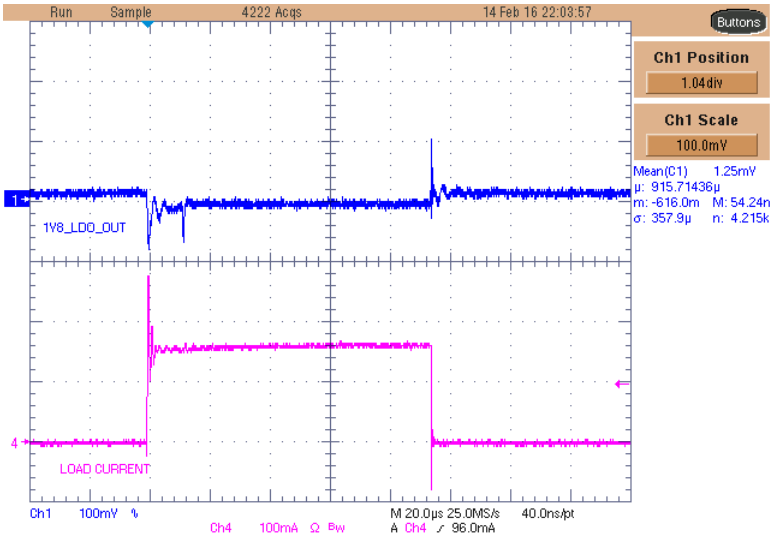


Figure 60. TPS71718-Q1 1V8_LDO Rail Voltage With 150-mA Load Transient

8.5.4 Efficiency

The plot in Figure 61 shows the system efficiency of the TPS71718-Q1 1V8_LDO rail. This efficiency was determined with all other rails powered on.

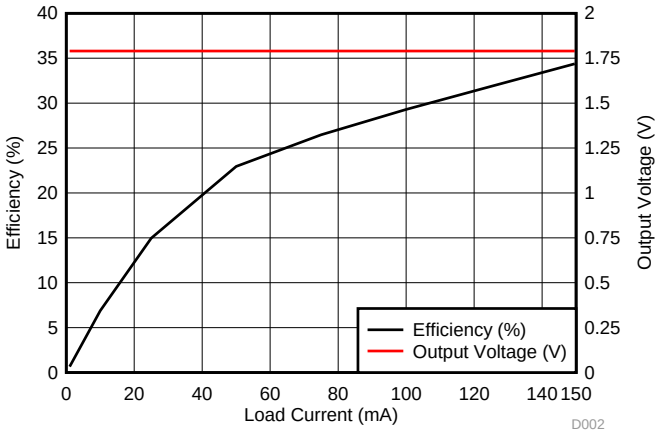


Figure 61. Efficiency of TPS71718-Q1 1V8_LDO Rail

8.6 TPS71728-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.6.1 Load Regulation

The plots in Figure 62 and Figure 63 show the behavior of the 2.8-V rail provided by the TPS71728-Q1.

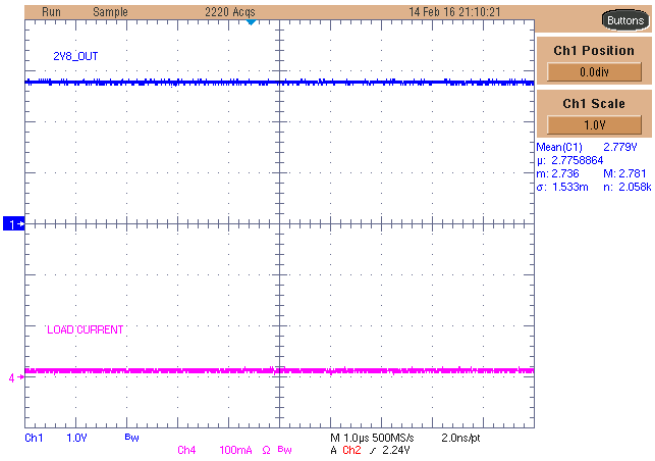


Figure 62. TPS71728-Q1 2.8-V Rail With No Load

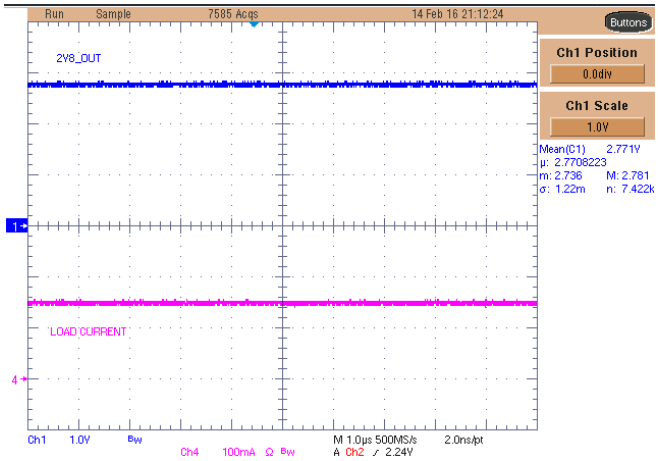


Figure 63. TPS71728-Q1 2.8-V Rail With 150-mA Load

8.6.2 Output Ripple Voltage

The plot in Figure 64 shows the ripple voltage of the 2.8-V rail provided by the TPS71728-Q1 device.

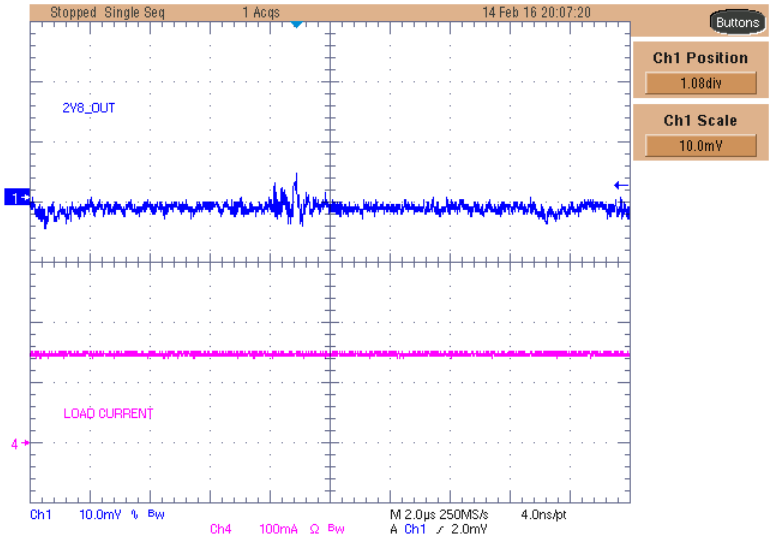


Figure 64. TPS71728-Q1 2.8-V Rail Ripple Voltage With 150-mA Load

8.6.3 Load Transient

The plot in Figure 65 shows a 150-mA Load Transient on the 2.8-V rail provided by the TPS71728-Q1 device.

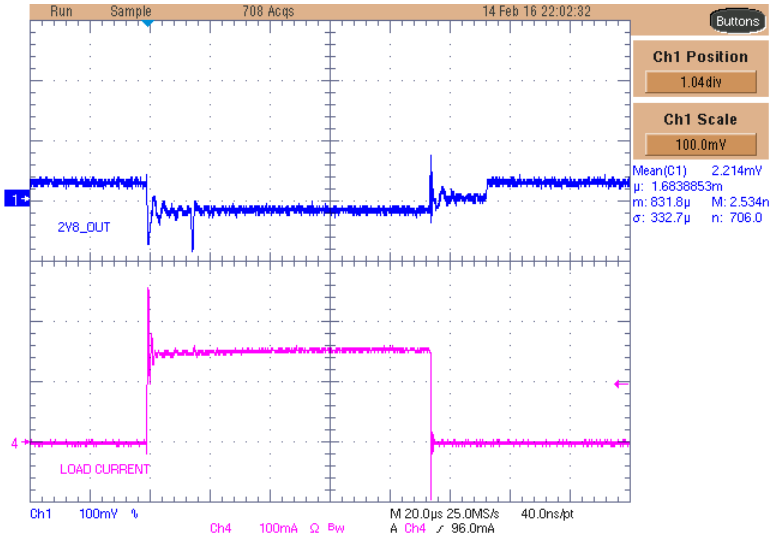


Figure 65. TPS71728-Q1 2.8-V Rail Voltage With 150-mA Load Transient

8.6.4 Efficiency

The plot in Figure 66 shows the system efficiency of the TPS71728-Q1 2.8-V rail. This efficiency was determined with all other rails powered on.

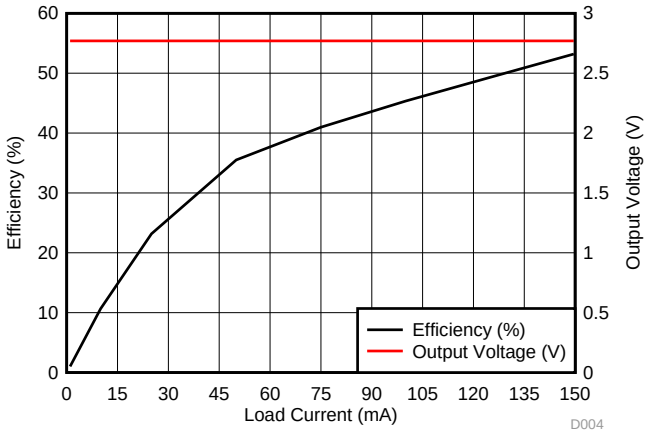


Figure 66. Efficiency of TPS71728-Q1 2.8-V Rail

8.7 TPS22966-Q1 Test Data

The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.

8.7.1 Load Regulation

The plots in Figure 67 and Figure 68 show the behavior of the 3.3-V rail provided by the TPS22966-Q1.

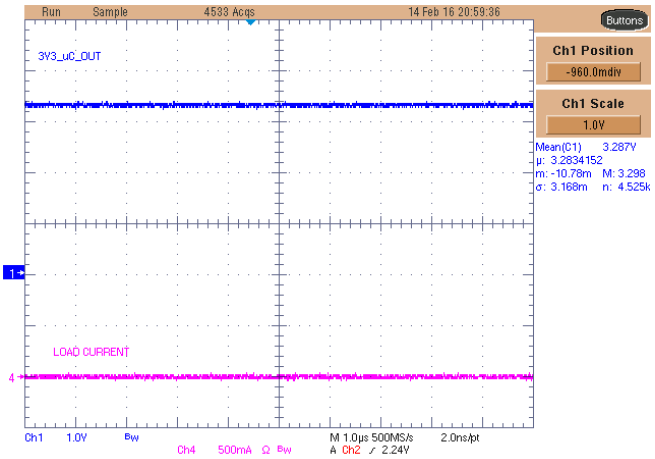


Figure 67. TPS22966-Q1 3V3_uC Rail With No Load

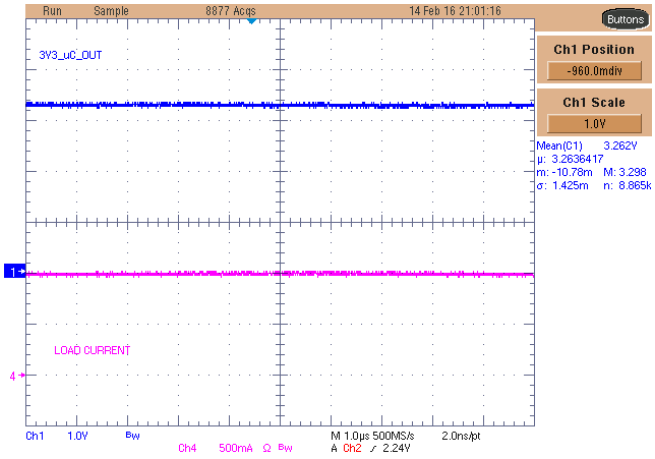


Figure 68. TPS22966-Q1 3V3_uC Rail With 1-A Load

8.7.2 Output Ripple Voltage

The plots in Figure 69, Figure 70, Figure 71, and Figure 72 show the ripple voltage of the 3.3-V rail provided by the TPS22966-Q1 device.

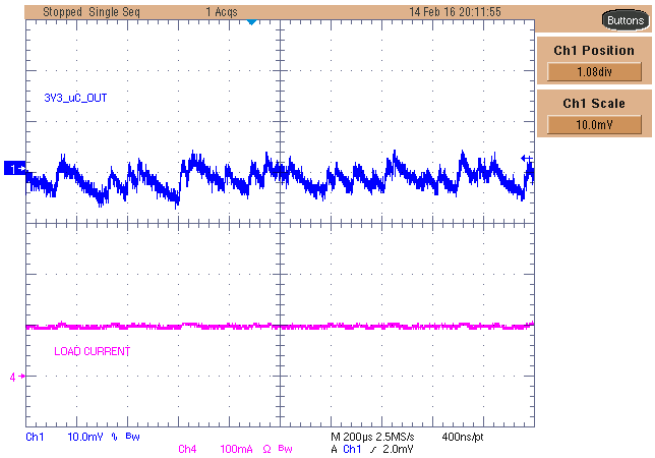


Figure 69. TPS22966-Q1 3V3_uC Rail Ripple Voltage With 100-mA Load

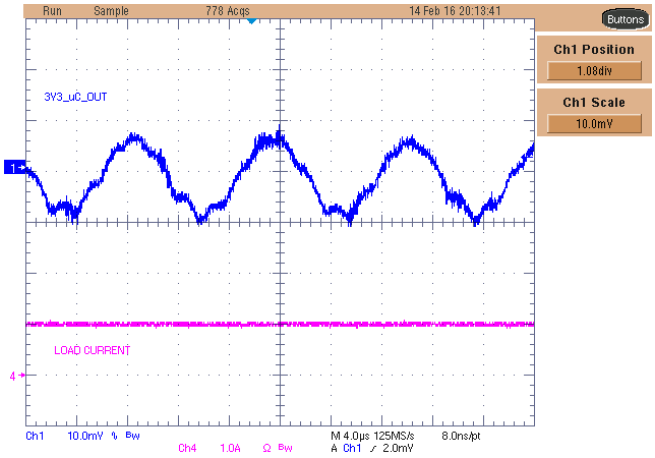


Figure 70. TPS22966-Q1 3V3_uC Rail Ripple Voltage With 1-A Load

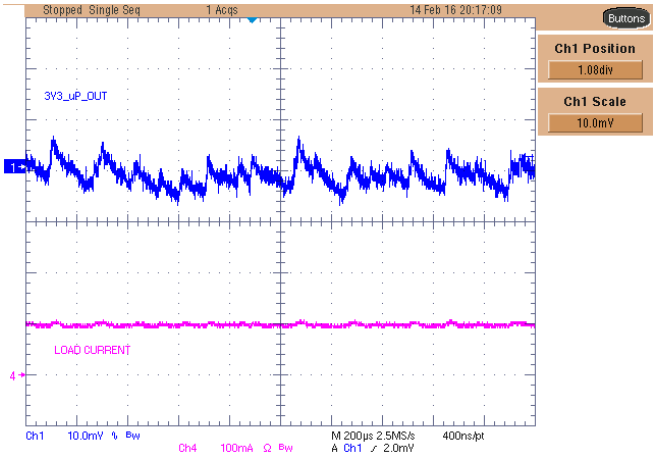


Figure 71. TPS22966-Q1 3V3_uP Rail Ripple Voltage With 100-mA Load

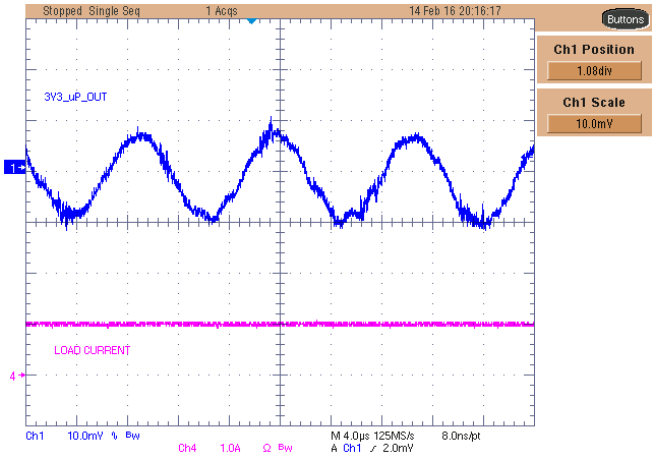


Figure 72. TPS22966-Q1 3V3_uP Rail Ripple Voltage with 1-A Load

8.7.3 Load Transient

The plots in Figure 73 and Figure 74 show a 1-A Load Transient on the 3.3-V rail provided by the TPS22966-Q1 device.

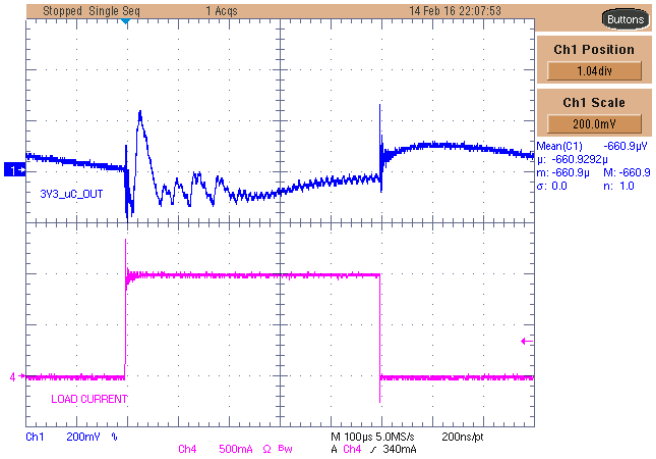


Figure 73. TPS22966-Q1 3V3_uC Rail Voltage With 1-A Load Transient

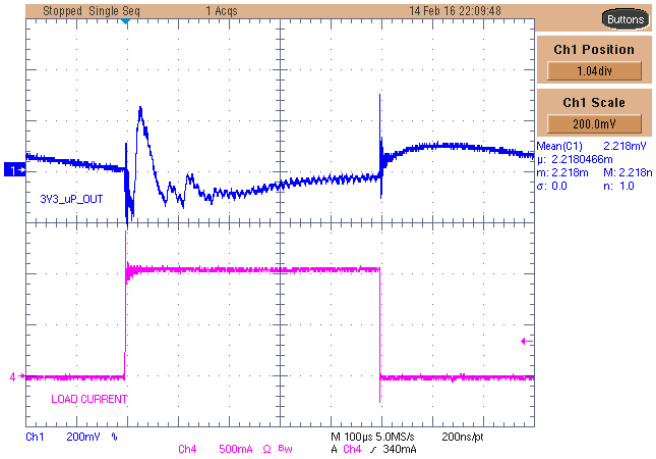


Figure 74. TPS22966-Q1 3V3_uP Rail Voltage With 1-A Load Transient

8.7.4 Efficiency

The plots in Figure 75 and Figure 76 show the system efficiency of the TPS22966-Q1 3.3-V rails. This efficiency was determined with all other rails powered on.

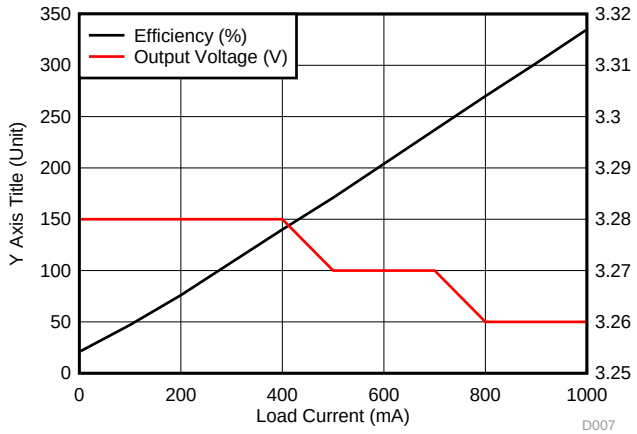


Figure 75. Efficiency of TPS22966-Q1 30V3_uC Rails

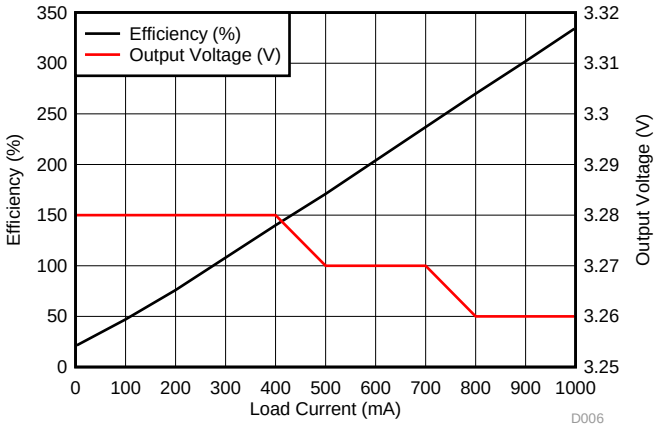
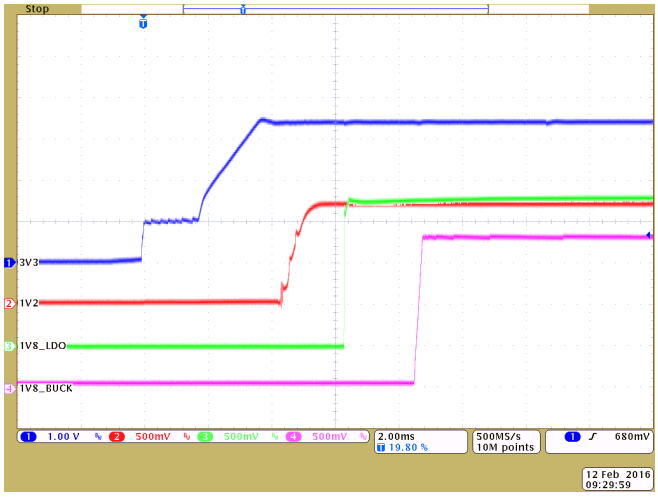


Figure 76. Efficiency of TPS22966-Q1 3V3_uP Rails

8.8 Sequencing Test Data

Figure 77 through Figure 81 show the power-up sequencing of the TIDA-00803 voltage rails. The sequencing was configured to use two LM3880-Q1 sequencers to control the enable signals of the regulators, LDOs, and load sSwitches. The following tests were conducted at a temperature of 25°C with an input voltage of 13 V.



Ignition Switch is ON when VIN applied

Figure 77. Startup Behavior of 3V3 Main Rail, 1V2, 1V8_LDO, and 1V8-BUCK

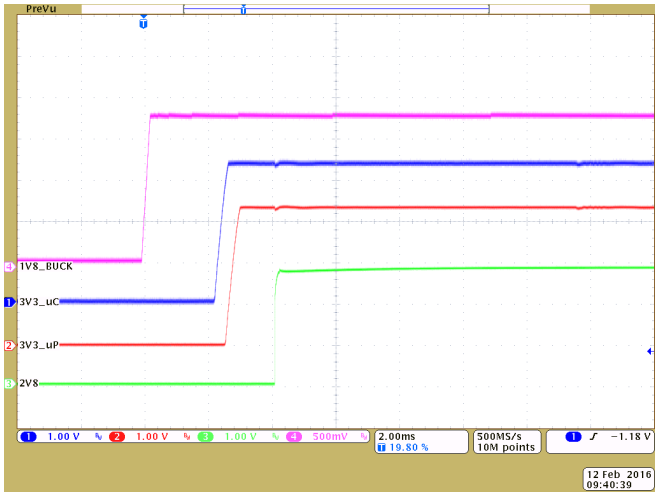


Figure 78. Startup Behavior of 1V8_BUCK, 3V3_uC, 3V3_uP, and 2V8 Rails

NOTE: Because 5V0 is a Boost regulator rail, the 5V0 is already 3.3 V before becoming enabled and rising to 5.0 V

Figure 79. Startup Behavior of 3V3_uC, 3V3_uP, 2V8, and 5V0 rails.

Figure 80. Startup Behavior of 1V2, 1V8_LDO, and 1V8_BUCK When Activated By Ignition Switch With 3V3 Main Rail Already Powered On

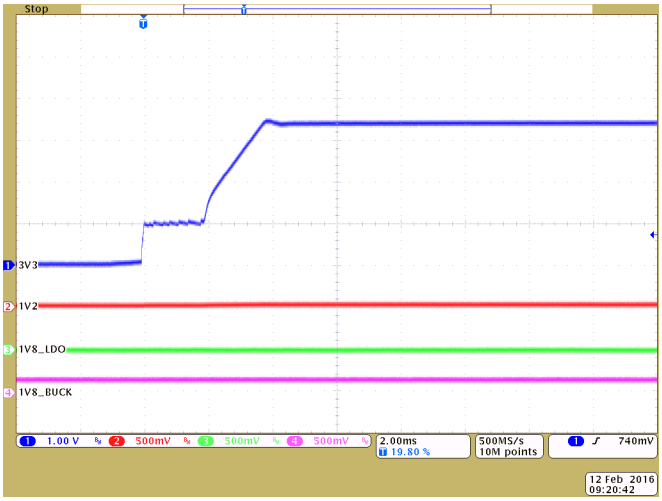


Figure 81. Startup Behavior of Main 3V3 Rail With Ignition Switch OFF

9 Design Files

9.1 Schematics

To download the schematics for each board, see the design files at http://www.ti.com/tool/TIDA-00803.

9.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00803.

9.3 Layer Plots

To download the layer plots for each board, see the design files at TIDA-00803.

9.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00803.

9.5 Layout Guidelines

9.5.1 LM3880-Q1 Layout Guidelines

- Pullup resistors should be connected between the flag output pins and a positive input supply, usually VCC. An independent flag supply may also be used. These resistors should be placed as close as possible to the Simple Power Supply Sequencer and the flag supply. Minimal trace length is recommended to make the connections. A typical value for the pullup resistors is 100kΩ.
- For very tight sequencing requirements, minimal and equal trace lengths should be used to connect the flag outputs to the desired inputs. This will reduce any propagation delay and timing errors between the flag outputs along the line.

9.5.2 LM3880-Q1 Layout Example

Figure 82 and Figure 83 are layout examples for the LM3880 and LM3880-Q1. These examples are taken from the LM3880EVAL.

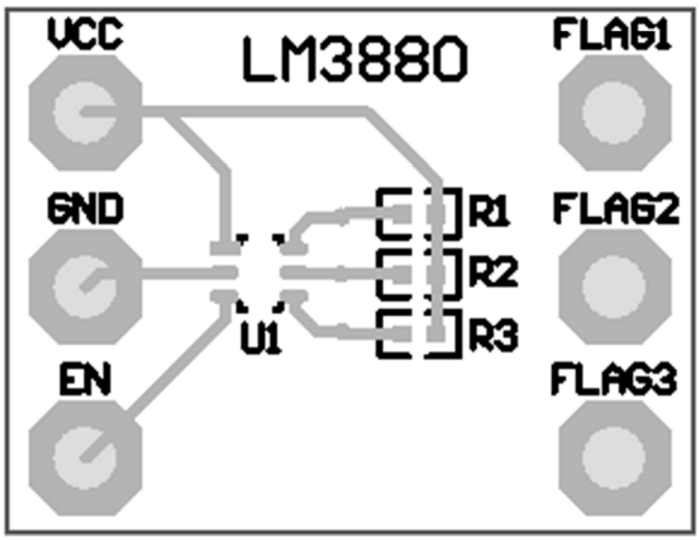


Figure 82. LM3880-Q1 Top

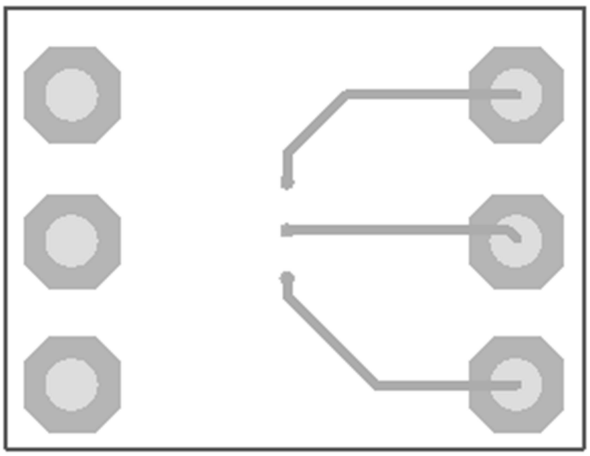


Figure 83. LM3880-Q1 Bottom

9.5.3 TPS22966-Q1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (1)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22966-Q1)
- T_A = ambient temperature
- Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

Figure 84 shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

9.5.4 TPS22966-Q1 Layout Example

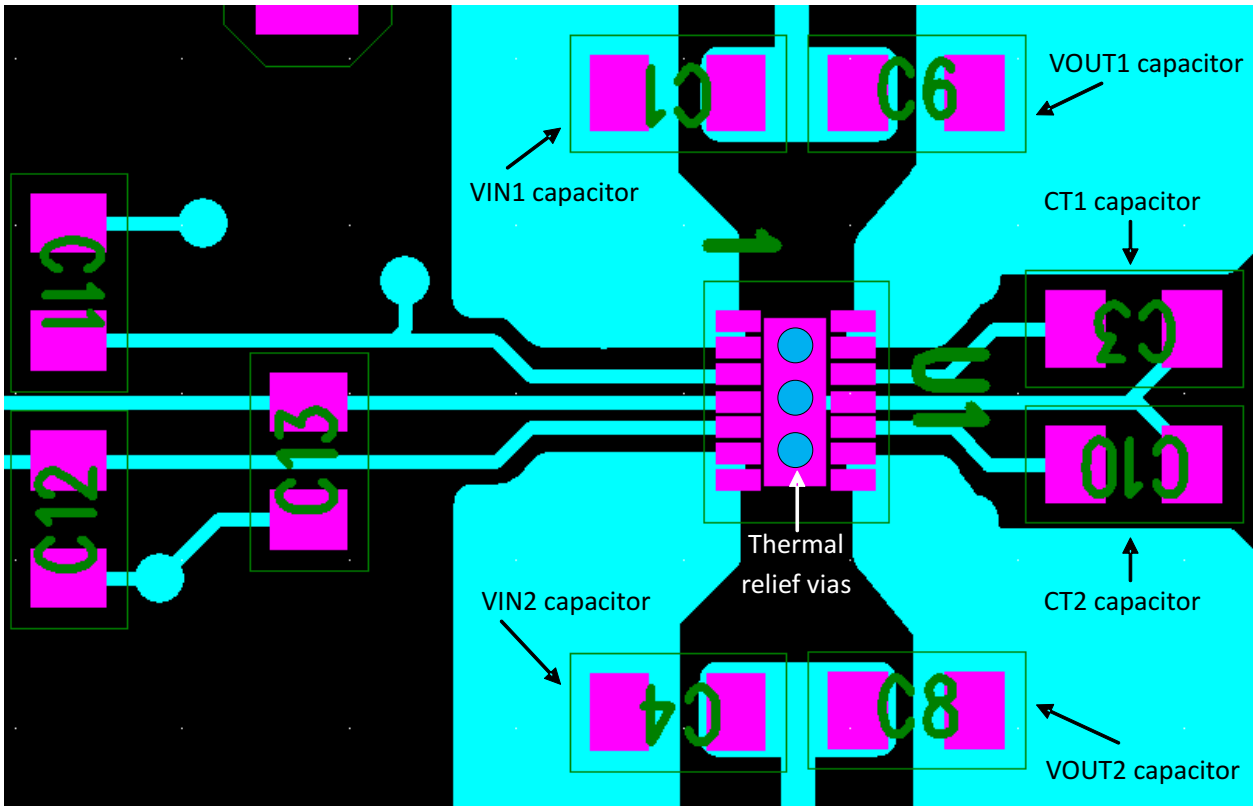


Figure 84. Layout Example

9.5.5 TPS22966-Q1 Layout Guidelines

TI recommends the following guidelines for PCB layout of the TPS54362-Q1 device.

9.5.5.1 Inductor

Use a low-EMI inductor with a ferrite-type shielded core. Other types of inductors may be used; however, they must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.

9.5.5.2 Input Filter Capacitors

Input ceramic filter capacitors should be located in close proximity to the VIN pin. TI recommends surface-mount capacitors to minimize lead length and reduce noise coupling.

9.5.5.3 Feedback

Route the feedback trace such that there is minimum interaction with any noise sources associated with the switching components. Recommended practice is to place the inductor away from the feedback trace to prevent EMI noise.

9.5.5.4 Traces and Ground Plane

All power (high-current) traces should be thick and as short as possible. The inductor and output capacitors should be as close to each other as possible. This reduces the EMI radiated by the power traces due to high switching currents.

In a two-sided PCB, TI recommends having ground planes on both sides of the PCB to help reduce noise and ground-loop errors. Connect the ground connection for the input and output capacitors and IC ground to this ground plane.

In a multilayer PCB, the ground plane separates the power plane (where high switching currents and components are placed) from the signal plane (where the feedback trace and components are) for improved performance.

Also, arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction the current path is in the same direction. Doing so prevents magnetic field reversal caused by the traces between the two half cycles, helping to reduce radiated EMI.

9.5.6 TPS22966-Q1 Layout Example

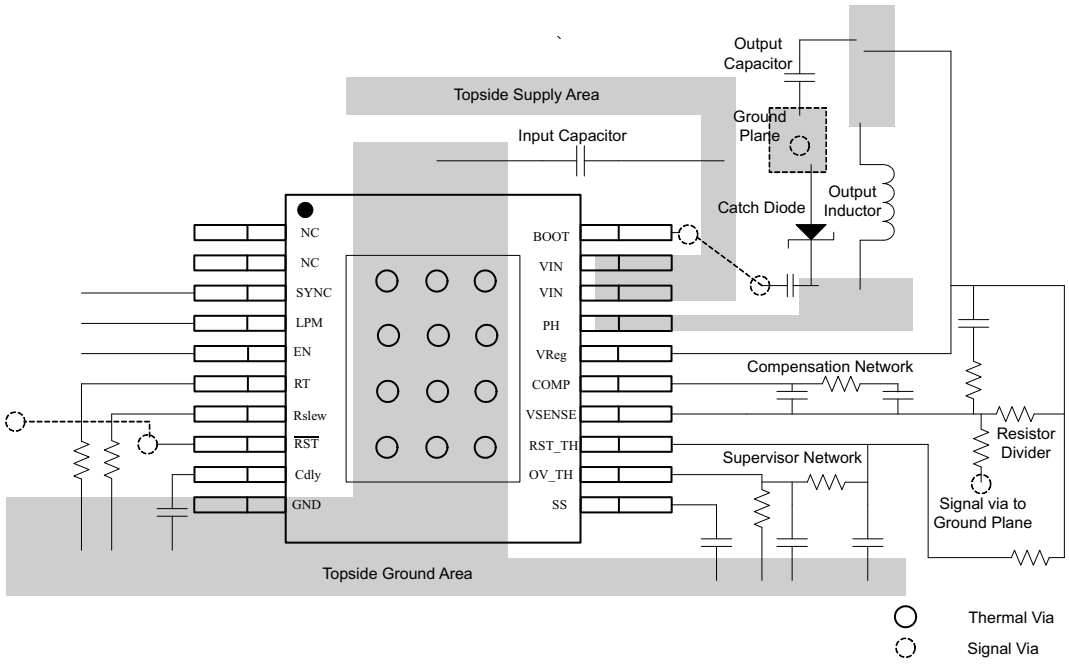


Figure 85. TPS22966-Q1 PCB Layout Example

9.5.7 TPS57114-Q1 Layout Guidelines

Layout is a critical portion of good power-supply design. There are several signal paths which conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. Take care to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 86 for a PCB layout example. Tie the GND pins and AGND pin directly to the thermal pad under the IC. Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC. Use additional vias to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full-rated load, the top-side ground area along with any additional internal ground planes must provide adequate heat-dissipating area.

Locate the input bypass capacitor as close to the IC as possible. Route the PH pin to the output inductor. Because the PH connection is the switching node, locate the output inductor close to the PH pins, and minimize the area of the PCB conductor to prevent excessive capacitive coupling. Also, locate the boot capacitor close to the device. Connect the sensitive analog ground connections for the feedback voltage divider, compensation components, slow-start capacitor, and frequency-set resistor to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise, so locate the Rt resistor as close as possible to the IC and connect it with minimal lengths of trace. Place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternative PCB layout. However, this layout, meant as a guideline, produces good results.

9.5.8 TPS57114-Q1 Layout Example

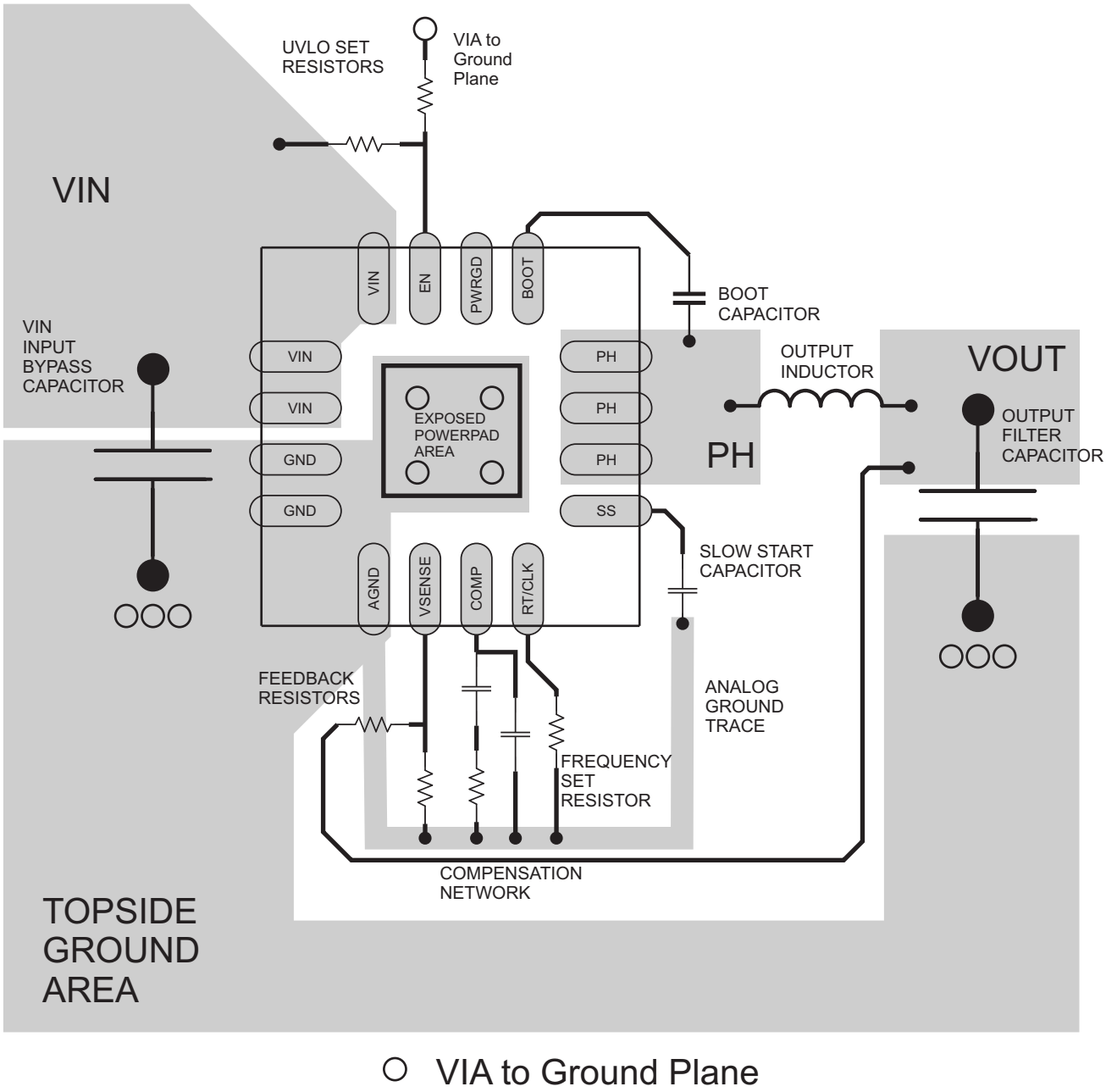


Figure 86. TPS57114-Q1 PCB Layout Example

9.5.9 PS61170-Q1 Layout Guidelines

As for all switching power supplies, especially those switching at high frequencies or providing high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times should be as short as possible. To reduce radiation of high-frequency switching noise and harmonics, proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch, Schottky diode, and output capacitor, contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin to reduce the IC supply ripple. Figure 87 shows a sample layout.

9.5.10 TPS61170-Q1Layout Example

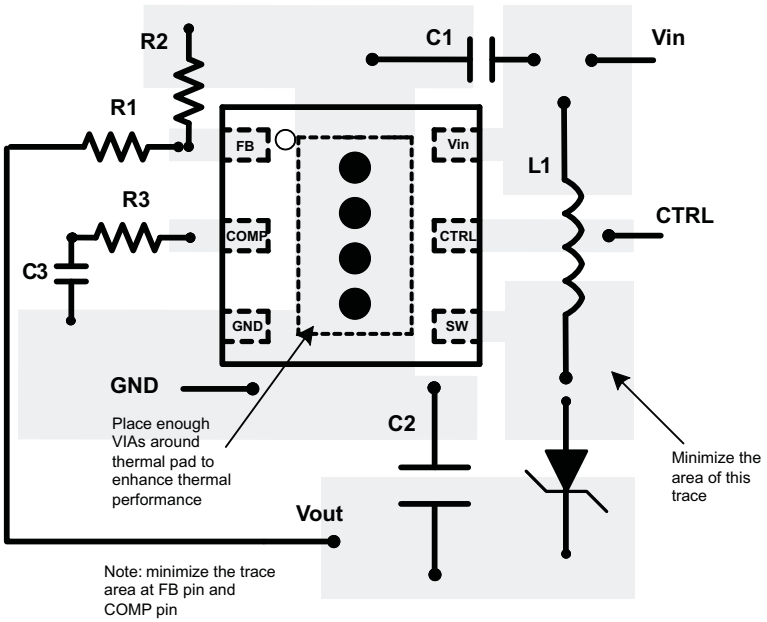


Figure 87. TPS61170-Q1 PCB Layout Recommendation

9.5.11 TPS6226x-Q1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line or load regulation, stability issues as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the thermal-pad land of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the thermal-pad land (star point) underneath the IC. Keep the common path to the GND pin, which returns the small-signal components and the high current of the output capacitors, as short as possible to avoid ground noise. The FB line should be connected directly to the output capacitor and routed away from noisy components and traces (for example, the SW line).

9.5.12 TPS6226x-Q1 Layout Examples

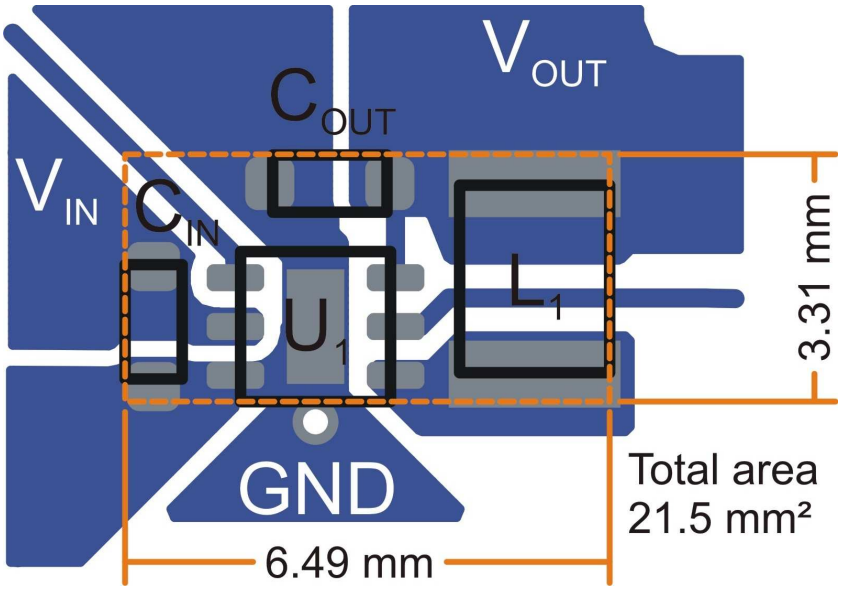


Figure 88. Suggested Layout for Fixed Output Voltage Options

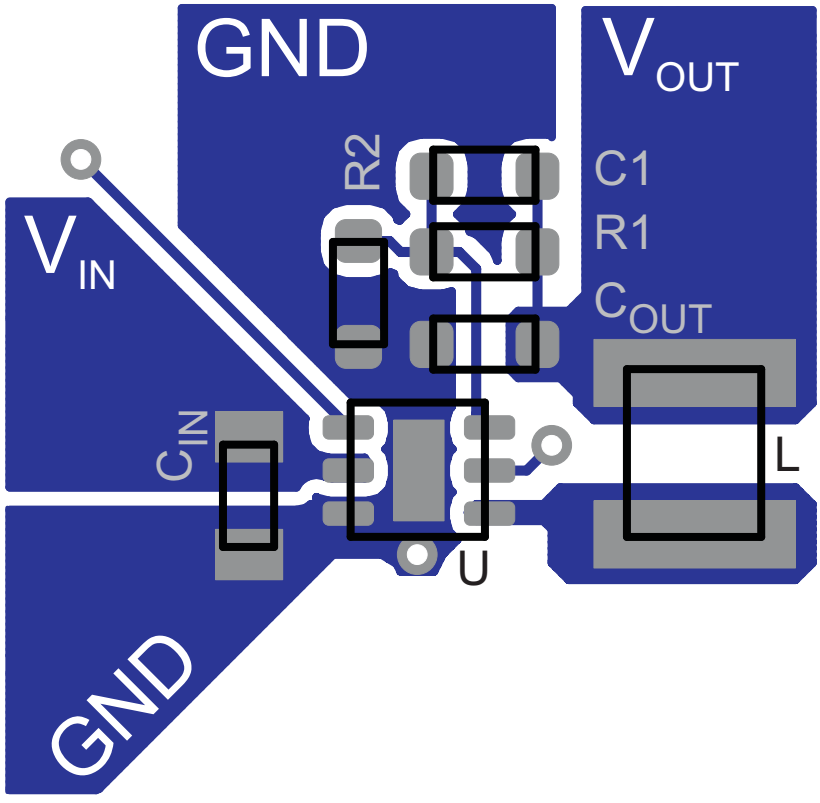


Figure 89. Suggested Layout for Adjustable Output Voltage Version

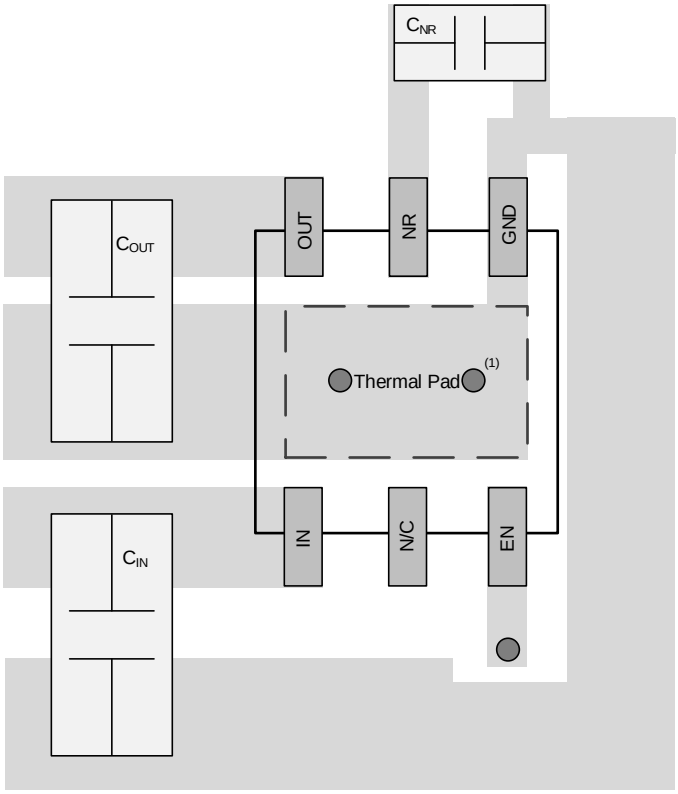
9.5.13 TPS717xx-Q1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to the GND pin as possible, connected by wide, component-side, copper surface area. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and functions similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

9.5.13.1 TPS717xx-Q1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

9.5.14 TPS717xx-Q1 Layout Example



(1) Circles within thermal pad area indicate vias to other layers on the board.

Figure 90. Fixed Voltage Layout

10 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00803.

11 References

1. Texas Instruments, *TPS57114-Q1 2.95-V to 6-V Input, 4-A Output, 2-MHz, Synchronous Step-Down SWIFT™ Switcher*, Data Sheet, SLVSAH5
2. Texas Instruments, *TPS61170-Q1 1.2-A High-Voltage Boost Converter in 2-mm × 2-mm SON Package*, Data Sheet, SLVSAX2
3. Texas Instruments, *TPS717xx-Q1 Low-Noise, High-Bandwidth PSRR, Low-Dropout, 150-mA Linear Regulator*, Data Sheet, SLVSBM4
4. Texas Instruments, *TPS22966-Q1 Dual-Channel, Ultralow Resistance Load Switch*, Data Sheet, SLVSC71
5. Texas Instruments, *2.25-MHz 600-mA Step-down Converters*, Data Sheet, SLVSA16
6. Texas Instruments, *LM3880/-Q1 Simple Power Sequencer*, Data Sheet, SNVS451
7. Texas Instruments, *TPS54362-Q1 3-A, 60-V Step-Down DC-DC Converter With Low $I_{(q)}$*, Data Sheet, SLVS845

12 About the Author

HAYDEN HAST joined Texas Instruments as an Application Engineer in 2015 after earning his Bachelor of Science in Electrical Engineering from Valparaiso University. As a member of the Mixed Signal Automotive – Automotive Safety and Power team, Hayden focuses on creating collateral and supporting top automotive OEM and Tier 1 customers regarding Buck, Boost, and Buck-Boost power topologies.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265