TI Designs

PMP9801 Reference Design 5-V Output, 4000-V Isolated Voltage Power Supply for RS485 Applications

Description

The PMP9801 is an isolated Flyback DC-DC converter reference design based on the TPS61046. The input voltage ranges from 5 V to 20 V. The output voltage is set to 5 V. The output current can be up to 250 mA at 10-V input condition. The isolation voltage of the transformer is 4000-V DC. Both primary-side and secondary-side regulation solutions are introduced in the reference design.

Resources

PMP9801	Design Folder
TPS61046	Product Folder

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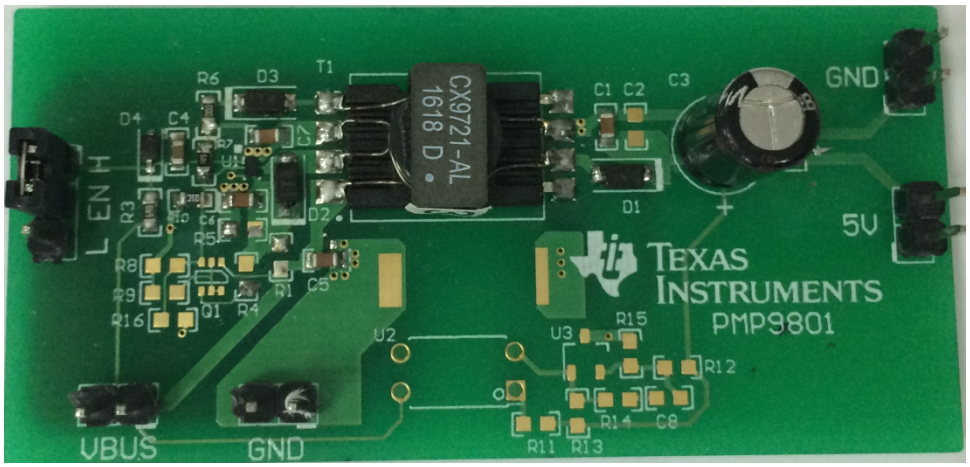
Features

- 5-V to 20-V Input Voltage Range
- 5-V Output Voltage With Up to 250-mA Output Current
- Primary-Side Regulation to Reduce Cost
- Secondary-Side Regulation for Excellent Load Regulation
- Circuit Tested With Evaluation Board

Applications

- Appliances
- Grid Infrastructure



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1 System Overview

1.1 System Description

This reference design demonstrates an isolated flyback DC-DC converter based on the boost converter IC TPS61046. Two control methods are used to regulate the output voltage, one is the primary-side regulation using an auxiliary wind, and the other is the secondary-side regulation using an optocoupler and a shunt voltage reference IC TL431. The primary-side regulation solution is low cost and easy to achieve; while the secondary-side regulation solution has much better output voltage regulation. Section 2 and Section 3 focus on the primary-side regulation solution. Section 4 focuses on the secondary-side regulation solution. Section 5 contains the bill of materials of both solutions.

1.2 Key System Specifications

Table 1 provides the electrical specification of the reference design. Operation conditions outside the range of the table are also possible if the electrical specification is within the value specified in the TPS61046 data sheet (SLVSCQ7).

Table 1. Electrical Specification Summary

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{BUS}, Input voltage	5	10	20	V
V_{OUT}, Output voltage	4.5	5	5.5	V
I_{OUT}, Output current	—	—	250 (1)	mA
Isolation voltage	4000	—	—	V

(1) Users must ensure the peak current flowing through the primary-side of the transformer is not higher than the current limit of the TPS61046.

2 System Design Theory

2.1 Operating Principle and Circuit Implementing

Figure 1 shows the schematic of the reference design. The design is a flyback topology DC-DC converter based on the TPS61046. The operating principle of the flyback converter is similar to the boost converter. When the low-side MOSFET is on, the SW-node voltage is approximately zero, and the current flowing through the primary-side of the transformer increases linearly. When the low-side MOSFET is off, the energy stored in the primary-side winding releases to the secondary-side and also to the auxiliary winding. The output voltage of the auxiliary winding is in proportion to the secondary-side winding, so it can be used to regulate the V_{OUT} to avoid adding a sensing circuit at the secondary side.[1]

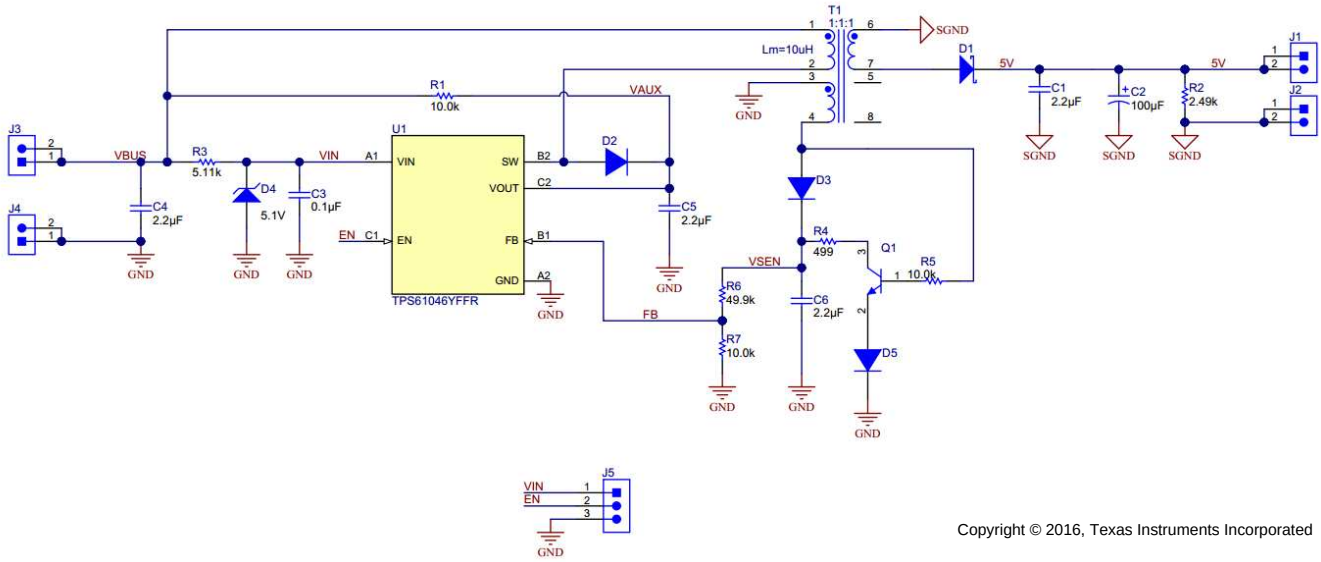


Figure 1. Reference Design Schematic

2.2 Transformer Design

Assuming the turn ratio of the primary winding to the secondary winding is n, and the transformer is ideal, Equation 1 defines the voltage stress of the Schottky diode D1, and Equation 2 defines the voltage stress of SW node.

$$V_{D1\_R} = \frac{V_{IN}}{n} + V_{OUT} \quad (1)$$

$$V_{SW} = V_{IN} + n \cdot (V_{OUT} + V_{D1\_F}) \quad (2)$$

where

- V_{D1_F} = forward voltage of the Schottky diode, approximately 0.5 V

The maximum voltage of the TPS61046 SW pin should be lower than 32 V. So, n is set to 1. For an ideal transformer, the voltage of the SW pin is approximately 25.4 V when V_{IN} = 20 V. In real application, the voltage spike at the SW pin is higher because of the leakage inductance of the transformer. The turnings of the auxiliary winding are set to the same as the secondary-side winding. In CCM, the current ripple of the primary-side inductor can be calculated through Equation 3.

$$\Delta I_T = \frac{1}{f_{SW}} \frac{(V_{OUT} + V_{D1\_F}) \cdot V_{IN}}{(V_{OUT} + V_{D1\_F} + V_{IN}) \cdot L_T} \quad (3)$$

where

- f_{sw} = the switching frequency of the TPS61046 in CCM, 1 MHz

- L_T = the primary-side inductance of the transformer

The current ripple can be set to 40% of the current limiting value of the TPS61046. So the inductance L_T is approximately 10 µH when V_{IN} = 10 V. Higher inductance helps to improve the output current capability, but the transformer is be larger.

TI recommends that the inductance of the primarily-side winding is in the range recommended by the data sheet, 1 µH to 22 µH, as listed in Table 2.

Table 2. TPS61046 Recommended Operating Condition

	MIN	TYP	MAX	UNIT
V_{IN} Input voltage range	1.8	—	5.5	V
V_{OUT} Output voltage range	4.5	—	28	V
L Effective inductance range	1.0 × 0.7	10	22 × 1.3	µH
C_{IN}	0.22	1.0	—	µF
C_{OUT}	0.22	1.0	10	µF
T_J	–40	—	125	°C

The saturation current of the transformer should be higher than the current limiting value of the TP61046, which is typical 0.9 A.

2.3 V_{OUT} Regulation Circuit

Figure 1 shows the primary-side regulation solution. To sense the secondary-side voltage easily, an auxiliary winding with the same turnings as the secondary winding is used. TI recommends using the rectifier D3 as a fast switching diode, such as 1N4148. Equation 4 defines the relationship of the feedback resistors.

$$R_7 = R_6 \cdot \left(\frac{V_{OUT} + V_{D1\_F} - V_{D3\_F}}{V_{REF}} - 1 \right) \quad (4)$$

where

- V_{D3_F} = the forward voltage of the D3, approximately 0.7 V if using 1N4148
- V_{REF} = the reference voltage for the TPS61046 FB pin, 0.8 V

2.4 TPS61046 Input Pin

The V_{IN} pin of the TPS61046 must be lower than 5.5 V, even when the input voltage V_{BUS} is 20 V. A 5.1-V Zener diode D4 and a 5.1-kΩ current limiting resistor R3 are used to limit the voltage below 5.5 V, shown in Figure 1. A larger current limiting resistor can also be used if the minimum input voltage is higher. Ensure that the V_{IN} pin voltage of the TPS61046 is higher than 1.8 V during start-up and normal operation. After finishing start-up the internal circuit of the TPS61046 is powered by the V_{OUT} pin. So D2 and C5 must be placed.

2.5 Dummy Load

Because the transformer is not ideal, the leakage inductance of the transformer causes the VSEN to be out of proportion to V_{OUT}. The V_{OUT} is be too high at light load condition and too low at heavy load condition. Instead of the fixed dummy load in the *Low Cost 1-W Isolated Power Supply Solution With TPS61085* application report [1], a self-adaptive dummy load circuit is proposed to improve load regulation.

The circuit composes of a NPN Q1, a diode D5, and two resistors, as shown in Figure 1. The purpose of the circuit is to adjust its dummy load according to the output current. The NPN Q1 only conducts when the Schottky diode D1 is on. At this period, the energy of the transformer is transferred to the second side. Before the flyback enters CCM, the I_{OUT} is proportional to the length of this period. The dummy load increases with the I_{OUT}, which improves the load regulation and efficiency of the boost converter.

Besides the self-adaptive dummy load circuit, R2 is also the dummy load, which is used to reduce the V_{OUT} at no-load condition. The following two steps optimize resistors R4 and R2.

1. Set the V_{IN} to typical value and I_{OUT} to full load (V_{IN} = 10 V and I_{OUT} = 250 mA in this reference design), then decrease the resistance of R4 until V_{OUT} is acceptable.
2. Set the V_{IN} to typical value and I_{OUT} to zero, then decrease the resistance of R2 until V_{OUT} is acceptable.

Table 3 lists the test results.

Table 3. Dummy Load Optimization at V_{IN} = 10 V

STEPS TO OPTIMIZE DUMMY LOAD	DUMMY LOAD (Ω)		V_{OUT} (V)	
	R4	R2	I_{OUT} = 0 mA	I_{OUT} = 250 mA
Step 1	499	∞	6.4	4.87
Step 2	499	2.49 K	5.2	4.86

R1 between V_{BUS} and V_{AUX} is also the dummy load, but it does not help much to improve load regulation. R1 is used to prevent V_{AUX} from rising too high and triggering OVP at the V_{BUS} = 20 V condition.

3 Test Results

Figure 2 shows the load regulation of the reference design at different V_{BUS} conditions.

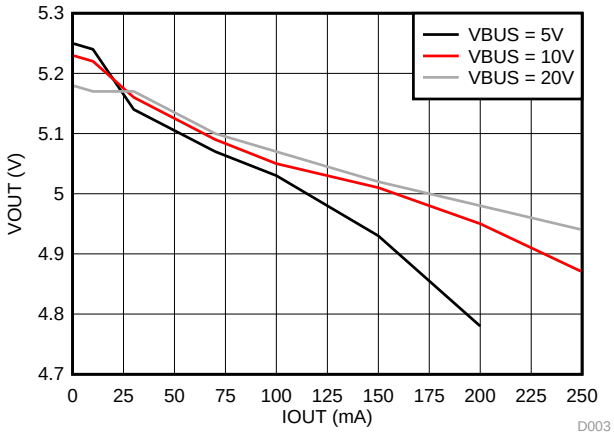


Figure 2. Load Regulation of Primary-Side Regulation Solution (V_{OUT} = 5 V)

Figure 3 shows the efficiency at different V_{BUS} and I_{OUT} conditions.

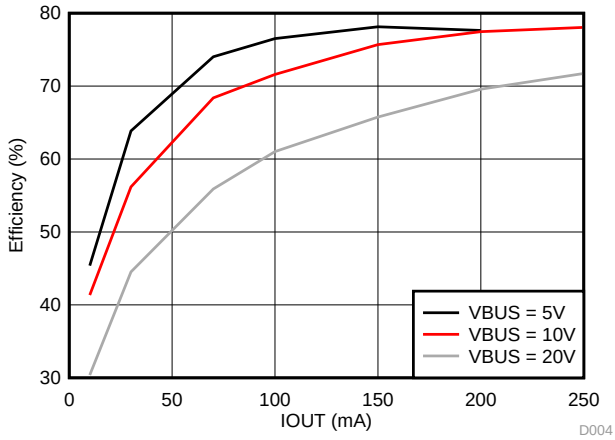


Figure 3. Efficiency of Primary-Side Regulation Solution

Figure 4 shows the start up waveform.

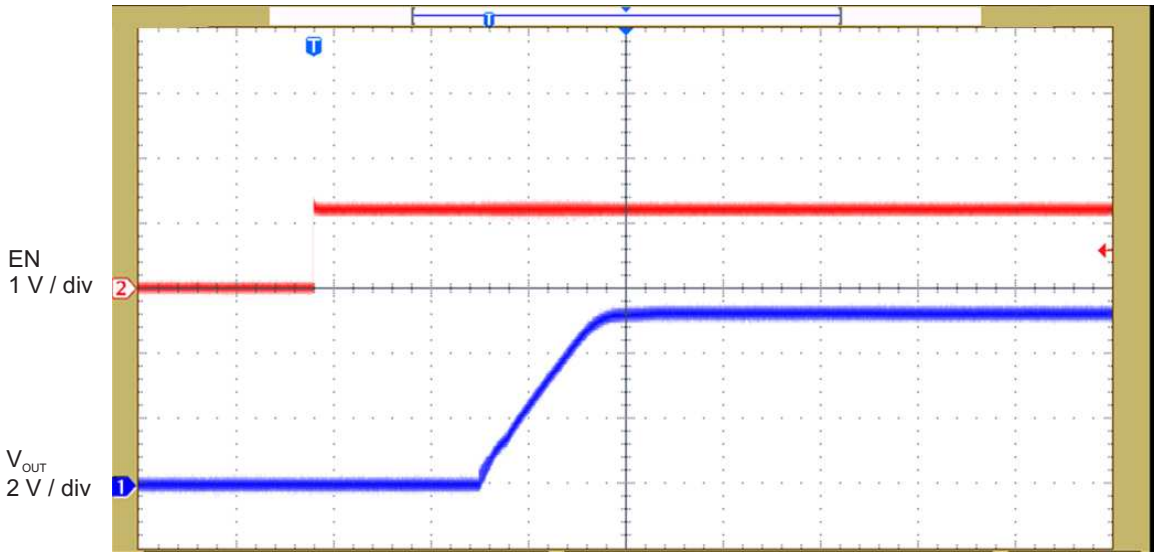


Figure 4. Start Up By EN Pin (V_{BUS} = 10 V, I_{OUT} = 10 mA)

Figure 5 shows the output voltage ripple at a V_{BUS} = 10 V and I_{OUT} = 250 mA condition.

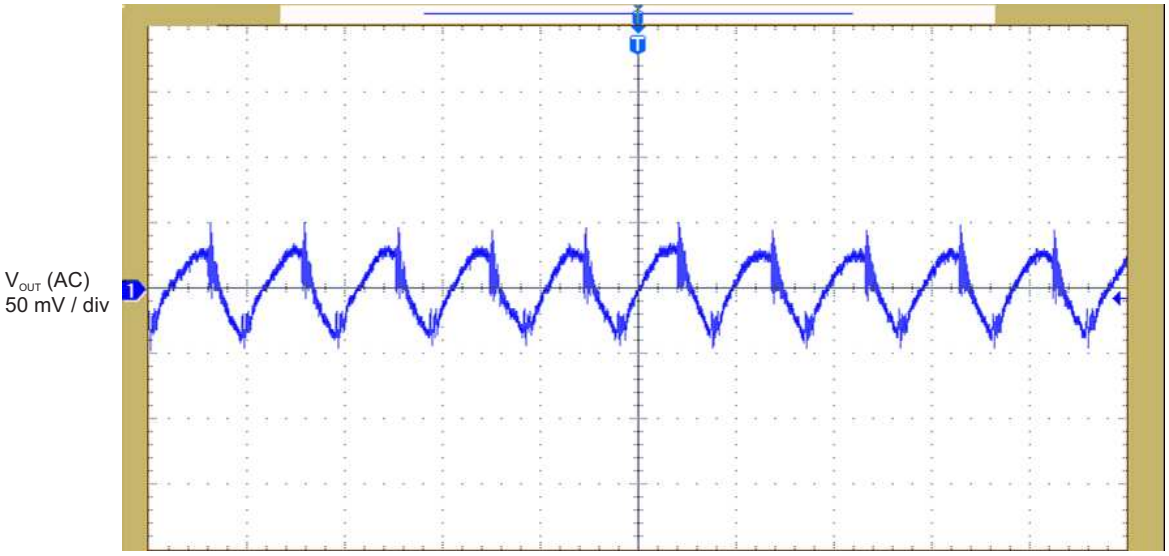
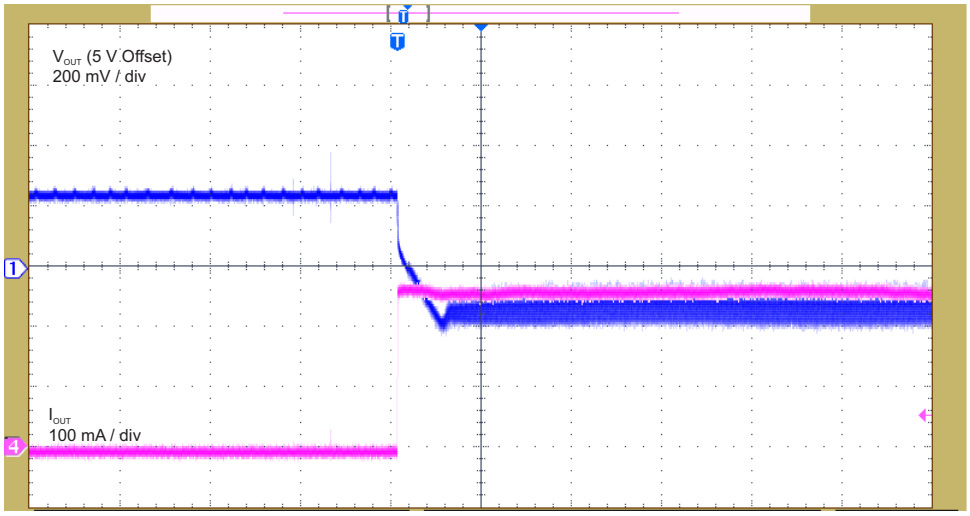
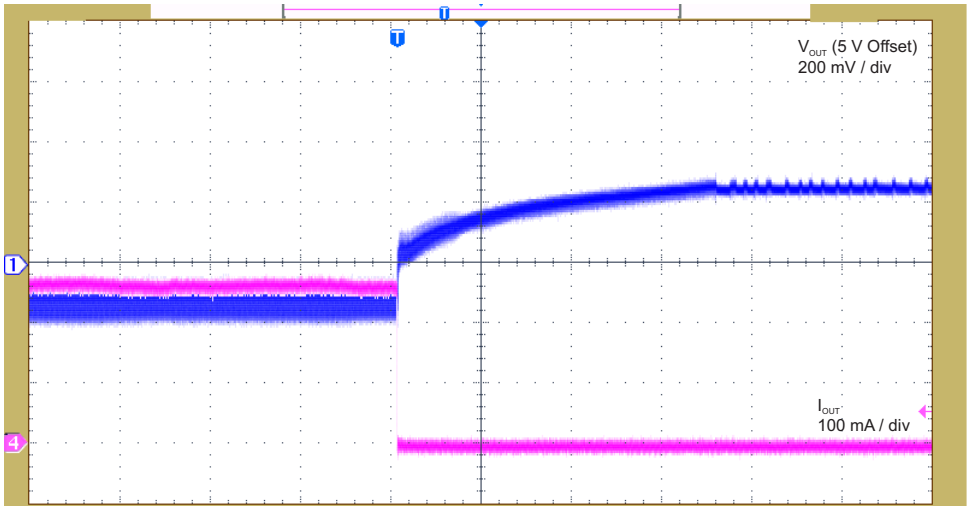


Figure 5. V_{OUT} Ripple at V_{IN} = 10 V and I_{OUT} = 250 mA

Figure 6 shows the 0- to 250-mA load transient waveform (a) and the 250- to 0-mA load transient waveform (b) at V_{BUS} = 10 V.



(a) 0 mA to 250 mA



(b) 250 mA to 0 mA

Figure 6. V_{OUT} Ripple at Load Transient

4 Secondary-Side Regulation Solution

To avoid using the auxiliary winding and achieve better load regulation, users can use secondary side regulation solution as shown in Figure 7. The V_{OUT} is sensed and regulated by U4 (ATL431) in the secondary side. The linear optocoupler U3 is used to transfer the signal to the primary side. A linear regulator based on U2 is used to power the optocoupler U3 and the voltage reference U4. The linear regulator aims to ensure that the gain of the feedback circuit is only determined by R9, C6, and R6.

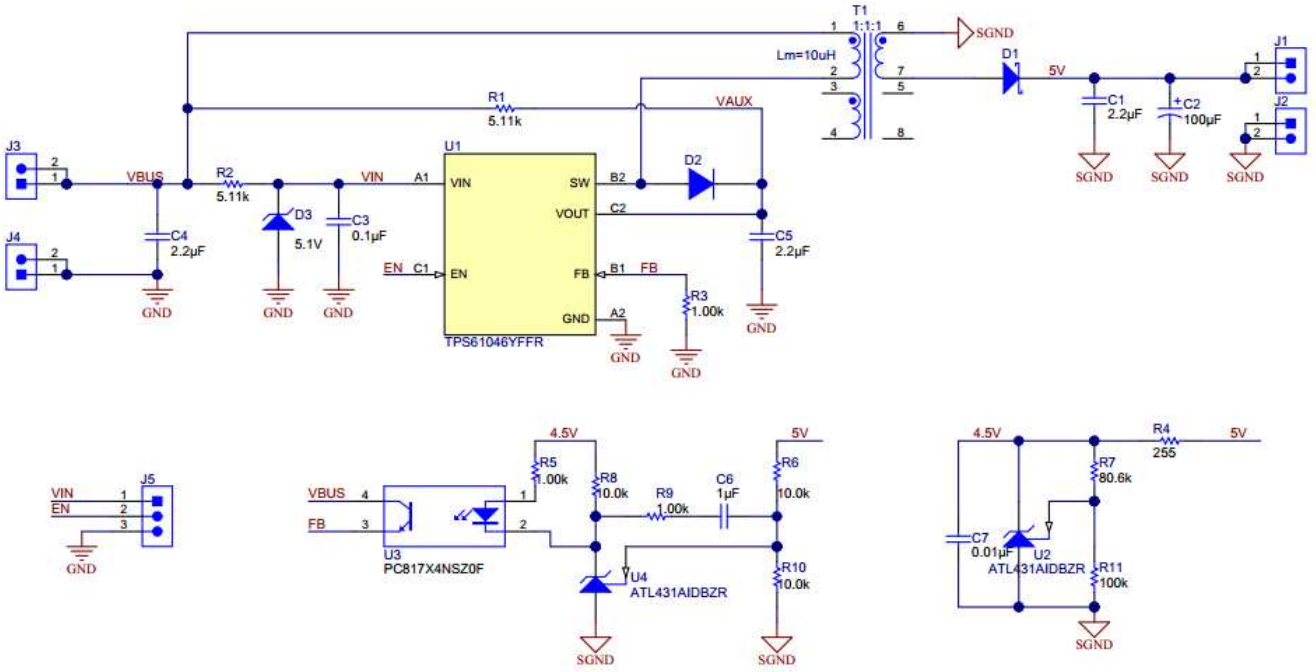


Figure 7. Secondary-Side Regulation Solution

To stabilize the flyback converter, TI recommends that the time constant of R9 and C6 must be higher than 1 ms. The gain of the feedback circuit at the frequencies higher than 1 kHz is defined by R9 and R6. Higher R9 and R6 values improves the load transient, but the converter tends to be unstable, while lower R9 and R6 help to stabilize the converter.

Figure 8 shows the load regulation. With the secondary-side regulation solution, V_{OUT} is almost unchanged from no load to full load.

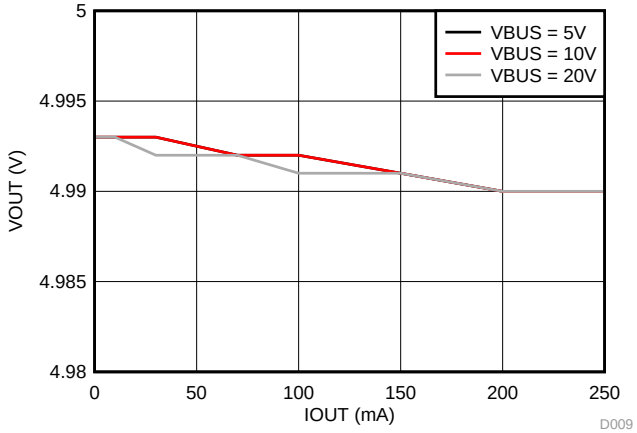


Figure 8. Load Regulation of Secondary-Side Regulation Solution

Figure 9 shows the efficiency of Figure 7.

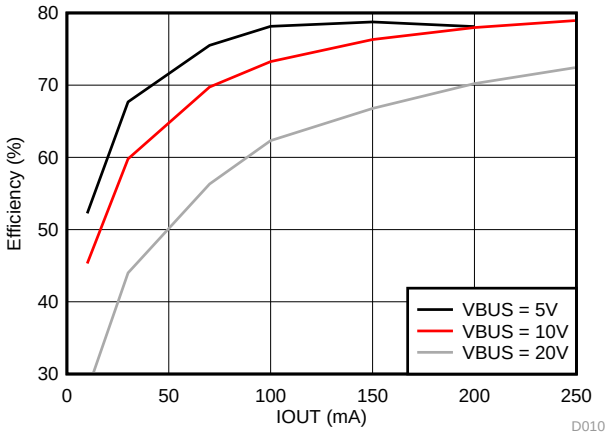


Figure 9. Efficiency of Secondary-Side Regulation Solution

Figure 10 shows the start-up waveform of the secondary-side regulation solution at I_{OUT}= 10 mA and V_{BUS}= 10 V.

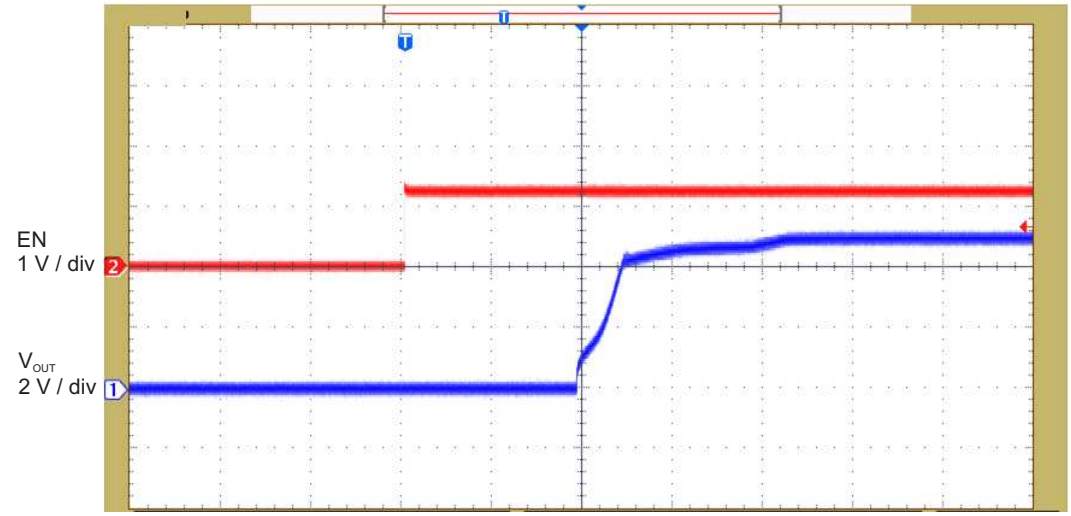


Figure 10. Start-Up Waveform of Secondary-Side Regulation Solution

Figure 11 shows the output voltage ripple of the secondary-side regulation solution at I_{OUT} = 10 mA and V_{BUS} = 10 V.

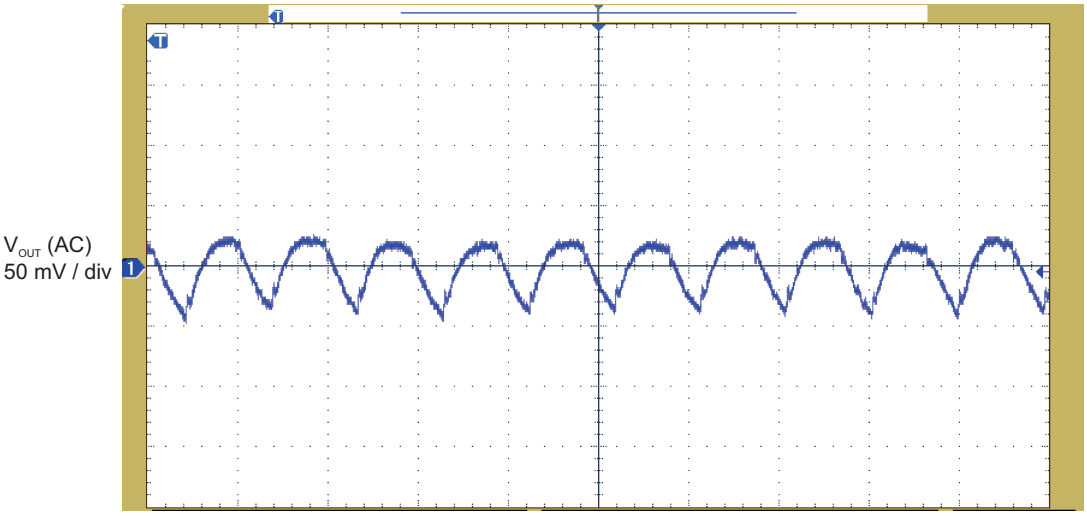


Figure 11. V_{OUT} Ripple of Secondary-Side Regulation Solution

Figure 12 shows the 0-mA to 250-mA load transient waveform (a) and the 250-mA to 0-mA load transient waveform (b) at V_{BUS} = 10 V.

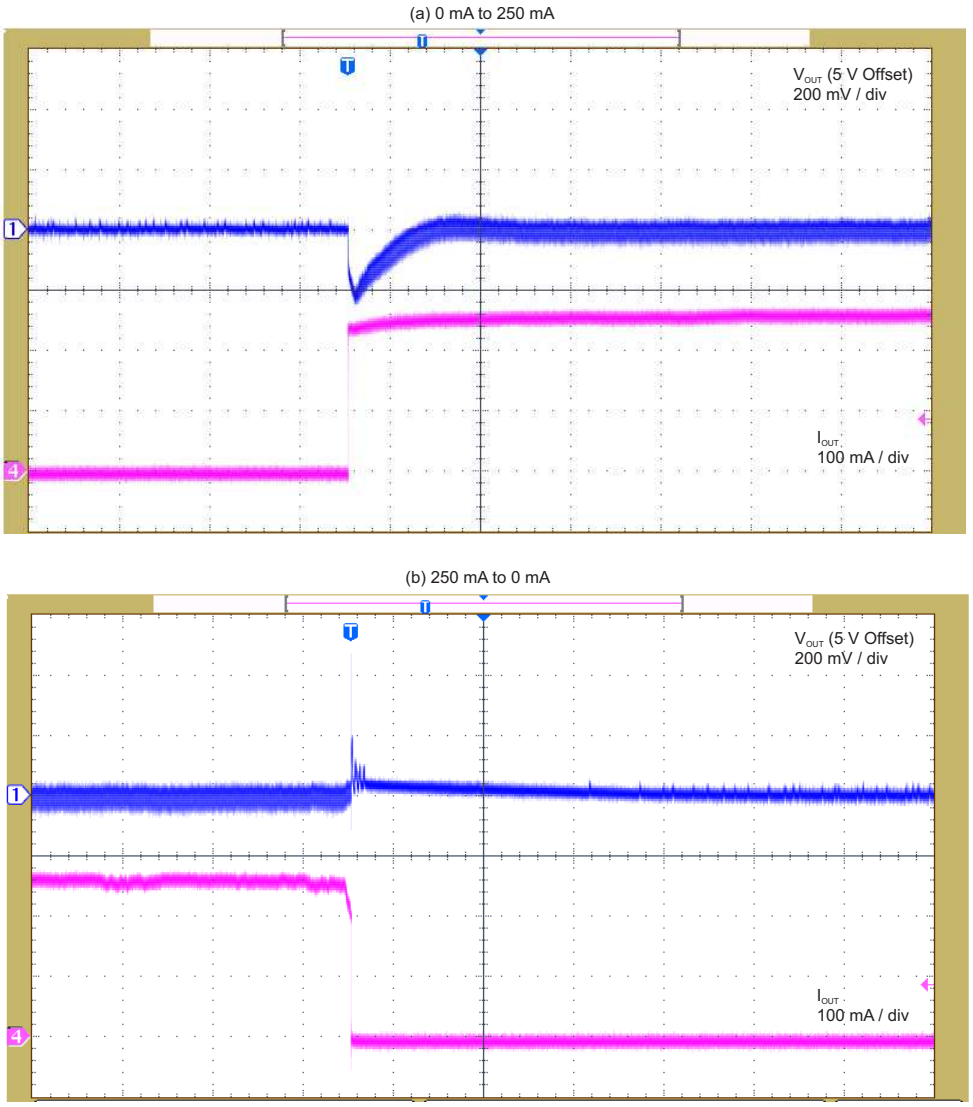


Figure 12. Load Transient of Secondary-Side Regulation Solution

5 Design Files

5.1 Schematics

To download the schematics, see the design files at http://www.ti.com/tool/PMP9801

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at http://www.ti.com/tool/PMP9801.

5.3 PCB Layout Recommendations

To download the PCB Layout Recommendations, see the design files at http://www.ti.com/tool/PMP9801

5.4 Altium Project

To download the Altium Project, see the design files at http://www.ti.com/tool/PMP9801

5.5 Gerber Files

To download the Gerber files, see the design files at http://www.ti.com/tool/PMP9801

6 Reference

1. Texas Instruments, *Low Cost 1W Isolated Power Supply Solution with TPS61085*, Application Report (SLVA496).

7 About the Author

JASPER LI is a Power Application Engineer for the Texas Instruments Boost Converter Solution Group. In this role, he supports worldwide customers, writes application notes, and develops reference designs. Since 2013 his focus has been on ultra-low-power applications. Jasper received his master's degree in Power Electronics in 2013 at Zhejiang University in China.

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