TI Designs

18-V/1-kW, 160-A_{PEAK}, >98% Efficient, High Power Density Brushless Motor Drive Reference Design

1 Description

The TIDA-00774 is a 1-kW power stage for a three-phase brushless DC (BLDC) motor in power tools operating from a 5-cell Li-ion battery with a voltage up to 21 V. The design is a 65-mm×60-mm compact drive, implementing sensor-based trapezoidal control. The design takes advantage of TI's MOSFET Power Block technology, which integrates two FETs in half-bridge configuration into a single SON 5×6 package, enabling very high power density. The design uses two power blocks in parallel and delivers 50-A_{RMS} continuous (120-A peak for 3 seconds, 160-A peak for 1 second) winding current. The MOSFET power block with minimum parasitic inductance and the current controlled gate driver with slew rate control helps in effective MOSFET paralleling and reduces switching spikes. The current sensing is done by monitoring MOSFET VDS. The board provides cycle-by-cycle overcurrent and short-circuit protection.

2 Resources

TIDA-00774	Design Folder
CSD88584Q5DC	Product Folder
DRV8323	Product Folder
MSP430F5132	Product Folder
TPS54061	Product Folder
LMT87	Product Folder

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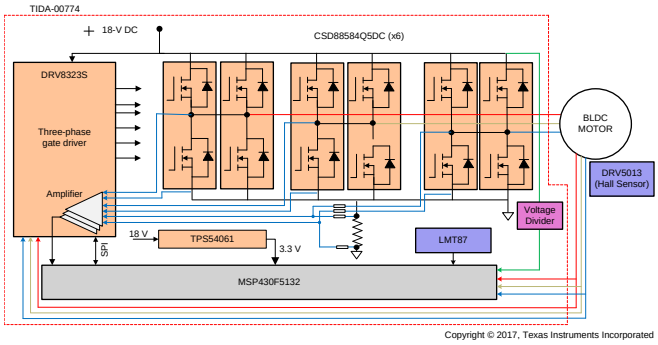
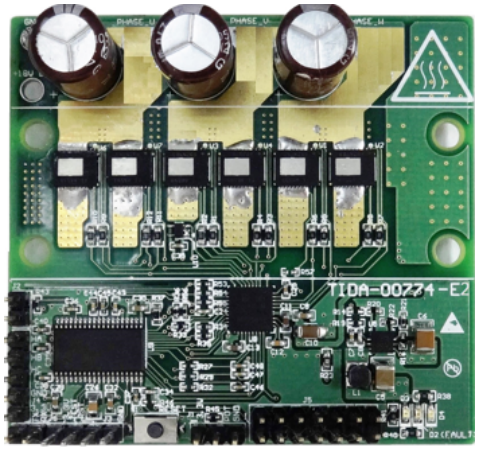
3 Features

- 1-kW Drive for BLDC Motor Supporting Sensor-Based Trapezoidal Control
- Designed to Operate From 6 to 21 V
- Continuous Output Current up to 50-A_{RMS}
- Peak Current Capability of 120 A for 3 Seconds and 160 A for 1 Second
- Small PCB Form Factor of 65-mm×60-mm Using 40-V/400-A_{PEAK}, 1-mΩ R_{DS_ON}, SON5×6 Package Half-Bridge Power Blocks
- 18-V/680-W, 33-A_{RMS} Without Heat Sink
- Motor Current Sensing by Monitoring the VDS of MOSFETs, Enables Elimination of Shunt Resistor
- Cycle-by-Cycle Overcurrent and Motor Stall Current Non-Latching Limit and Short-Circuit Latch Protection by VDS Sensing
- Shoot-Through, Undervoltage, Over-Temperature, and Blocked Rotor Protection
- Effective MOSFET Paralleling With Excellent Dynamic Current Sharing
- Option for Single PWM Control
- Operating Ambient: –20°C to 55°C

4 Applications

- Cordless Power Tools
- Cordless Garden Tools
- E-Bikes





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5 System Overview

5.1 System Description

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden tools, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air. Power tools can be either corded or cordless (battery powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors.

Most of the cordless tools use lithium-ion batteries, the most advanced in the industry. Lithium-ion batteries have high energy density, low weight, and greater life. These batteries have relatively low self-discharge (less than half that of nickel-based batteries) and can provide a very high current for applications like power tools.

Power tools are available in different power levels and battery voltage levels. Power tools such as cordless chain saws and cordless circular saws and different garden tools like cordless wood and branch cutters require very high torque and need very high peak current.

Cordless tools use brushed or brushless DC (BLDC) motors. The BLDC motors are more efficient and have less maintenance, low noise, and longer life. Power tools have requirements on form factor and thermal performance. Therefore, high-efficient power stages with a compact size are required to drive the power tool motor. The small form factor of the power stage enables flexible mounting, better PCB layout performance, and low-cost design. High efficiency provides maximum battery duration and reduces cooling efforts. The high-efficiency requirement in turn asks for switching devices with a low drain-to-source resistance (R_{DS_ON}). The power stage should also take care of protections like motor stall or any other chances of high current.

This TI Design uses the CSD88584 NexFET power block featuring a very low R_{DS_ON} of 1 mΩ in a SON5×6 SMD package. The power block with high-side and low-side FETs in single package helps to achieve very small form factor and better switching performance. The three-phase gate driver DRV8323 is used to drive the three-phase MOSFET bridge, which can operate from 6 to 60 V and support programmable gate current with maximum setting of 2-A sink / 1-A source. The DRV8323 includes three current shunt amplifiers, which helps in measuring and amplifying the VDS of the FET for accurate current measurements that support bidirectional current sensing with adjustable gain and eliminates the use of shunt. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for the current shunt amplifier, slew rate control of the gate drivers, and various protection features.

The LMT87 temperature sensor is used to sense the FET temperature and the results is used to calibrate the current sensing by VDS monitoring. The MSP430F5132 microcontroller is used to implement the control algorithm.

The test report evaluates the RMS current capability, peak current capability, and thermal performance of the board and overcurrent protection features such as cycle-by-cycle control and latch control of the DRV8323. The test results also show the improved RMS current capability of the board with different air flow.

5.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	18-V DC (6-V min to 21-V max) – 5-cell Li-Ion
Rated output power	1 kW
RMS winding current	50A
Peak winding current	120 A for 3 seconds, 160 A for 1 second
Control method	Sensor-based trapezoidal
Inverter switching frequency	20 kHz (adjustable from 5k to 100k)
Feedback signals	DC bus voltage, Hall sensor, inverter leg currents, low-side DC bus current
Protections	Cycle-by-cycle overcurrent, input undervoltage, over temperature, and blocked rotor
Cooling	With and without heat sink
Operating ambient	–20°C to 55°C
Board specification	65 mm × 60 mm, 4-layer, 2-oz copper
Efficiency	> 98.5%

5.3 Block Diagram

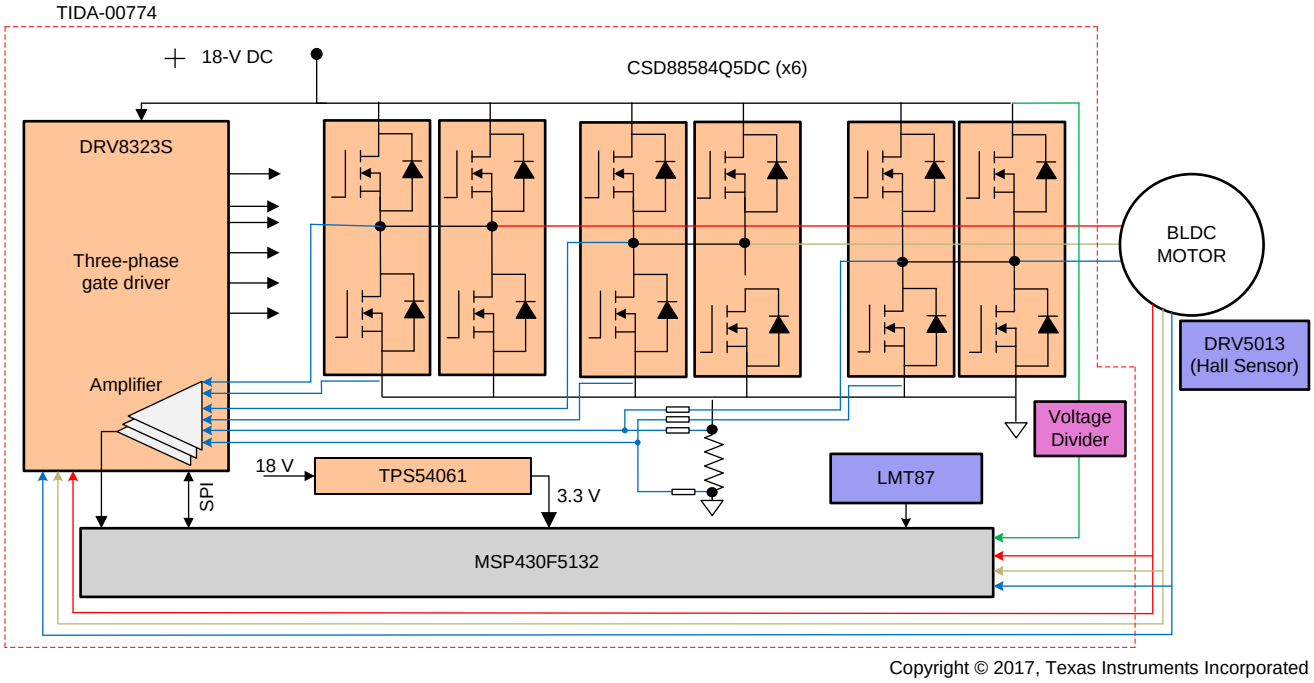

Figure 1. Block Diagram of TIDA-00774

5.4 Highlighted Products

5.4.1 CSD88584Q5DC

The CSD88584Q5DC 40-V Power Block is an optimized design for high-current motor control applications such as handheld, cordless garden and power tools. This device uses TI's patented stacked die technology in order to minimize parasitic inductances while offering a complete half bridge in a space saving thermally enhanced DualCool™ 5×6-mm package. With an exposed metal top, this power block device allows for simple heat sink applications to draw out heat through the top of the package and away from the PCB, for superior thermal performance at the higher currents demanded by many motor control applications.

5.4.2 DRV8323

The DRV8323 is a gate driver IC for three phase motor drive applications. The device provides three half-bridge drivers, each capable of driving one high-side and one low-side N-channel MOSFET. The DRV832x generates the proper gate voltage drive for both the high-side and low-side FETs using a charge pump. The DRV832x supports up to 1-A source and 2-A sink peak gate drive current capability. The DRV832x can operate from a single power supply and supports a wide input supply range from 6 to 60 V. The DRV8323 includes three current shunt amplifiers for accurate current measurements, supports 100% duty cycle, and has multiple levels of protection. The gate driver is programmable through SPI.

5.4.3 MSP430F5132

The TI MSP430™ family of ultra-low-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The architecture is combined with five low-power modes. The device features a powerful 16-bit reduced instruction set computing (RISC) CPU, 16-bit registers, and constant generators that contribute to the maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs.

The MSP430F51x2 series are microcontroller configurations with two 16-bit high-resolution timers, two universal serial communication interfaces (USCIs) USCI_A0 and USCI_B0, a 32-bit hardware multiplier, a high-performance 10-bit 200-ksps analog-to-digital converter (ADC), an on-chip comparator, a three-channel direct memory access (DMA), 5-V tolerant I/Os, and up to 29 I/O pins. The timer event control module connects different timer modules to each other and routes the external signals to the timer modules. The device is capable of working up to a system frequency of 25 MHz. The operating temperature of the device is –40°C to 85°C.

5.4.4 TPS54061

The TPS54061 device is a 60-V, 200-mA, synchronous step-down DC-DC converter with integrated high-side and low-side MOSFETs. Current mode control provides simple external compensation and flexible component selection. The non-switching supply current is 90 µA. Using the enable pin, shutdown supply current is reduced to 1.4 µA.

Undervoltage lockout is internally set at 4.5 V, but can be increased using two resistors on the enable pin. The output voltage startup ramp is controlled by the internal slow-start time. The adjustable switching frequency range allows efficiency and external component size to be optimized. The TPS54061 enables small designs by integrating the MOSFETs, boot recharge diode, and minimizing the IC footprint with a small 3.00-mm×3.00-mm thermally enhanced VSON package.

5.4.5 LMT87

The LMT87 is a precision CMOS integrated-circuit temperature sensor with an analog output voltage that is linearly and inversely proportional to temperature. It can operate down to a 2.7-V supply with 5.4-µA power consumption. Package options including through-hole TO-92 package allows the LMT87 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations. LMT87 has accuracy specified in the operating range of −50°C to 150°C.

6 System Design Theory

Compared to their brushed motor counterpart, permanent magnet brushless motors are gaining importance because of their high efficiency, high torque to weight ratio, low maintenance, high reliability, low rotor inertia, low noise, and so on. A brushless permanent magnet synchronous motor (PMSM) has a wound stator and a permanent magnet rotor assembly. These motors generally use internal or external devices to sense rotor position. The sensing devices provide position information for electronically switching the stator windings in the proper sequence to maintain rotation of the magnet assembly. The electronic drive is required to control the stator currents in a brushless permanent magnet motor. The electronic drive consists of:

- Power stage with a three-phase inverter having the required power capability
- MCU to implement the motor control algorithm
- Position sensor for accurate motor current commutation
- Gate driver for driving the three-phase inverter
- Power supply to power up the MCU
- For more details about trapezoidal control, see the application report *Sensorless Trapezoidal Control of BLDC Motors* (SPRABQ7).

6.1 Power Stage Design—Battery Power Input to the Board

The battery power input section is shown in Figure 2. The input bulk aluminum electrolytic capacitors C14, C15, and C16 provide the ripple current and its voltage rating is de-rated by 50% for better life. These capacitors are rated to carry high ripple current. C17 is used as bypass capacitors to GND. D1 is the transient voltage suppression (TVS) having breakdown voltage of 30 V and maximum supply voltage of 30 V.

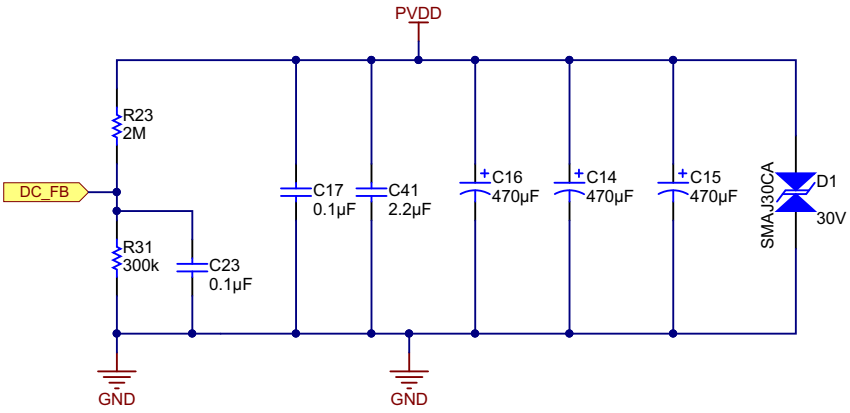

Figure 2. Schematic of Battery Power Input Section

The input supply voltage PVDD is scaled using the resistive divider network, which consists of R23, R31, and C23, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in Equation 1.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(300\ k\Omega + 2000\ k\Omega)}{300\ k\Omega} = 3.3 \times \frac{(300\ k\Omega + 2000\ k\Omega)}{300\ k\Omega} = 25.3\ V \quad (1)$$

Considering a 20% headroom for this value, the maximum recommended voltage input to the system is 25.3 × 0.8 = 20.25. So for a power stage with maximum operating voltage of 21 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 6 to 21 V.

6.2 Power Stage Design—Three-Phase Inverter

The three-phase inverter with two MOSFETs in parallel forms the power stage. Figure 3 shows one leg of the power stage, which consists of two power blocks. Each power block consists of two MOSFETs connected as a high-side and low-side FET. This device uses TI's patented stacked die technology in order to minimize parasitic inductances while offering a complete half bridge in a space saving thermally enhanced DualCool 5×6 mm package. With an exposed metal top, this power block device allows for simple heat sink applications to draw out heat through the top of the package and away from the PCB, for superior thermal performance at the higher currents demanded by many motor control applications.

The decoupling capacitors C18 and C19 are placed close across each power blocks to reduce the ringing in the supply lines because of the parasitic inductance added by the sense resistor and the power track.

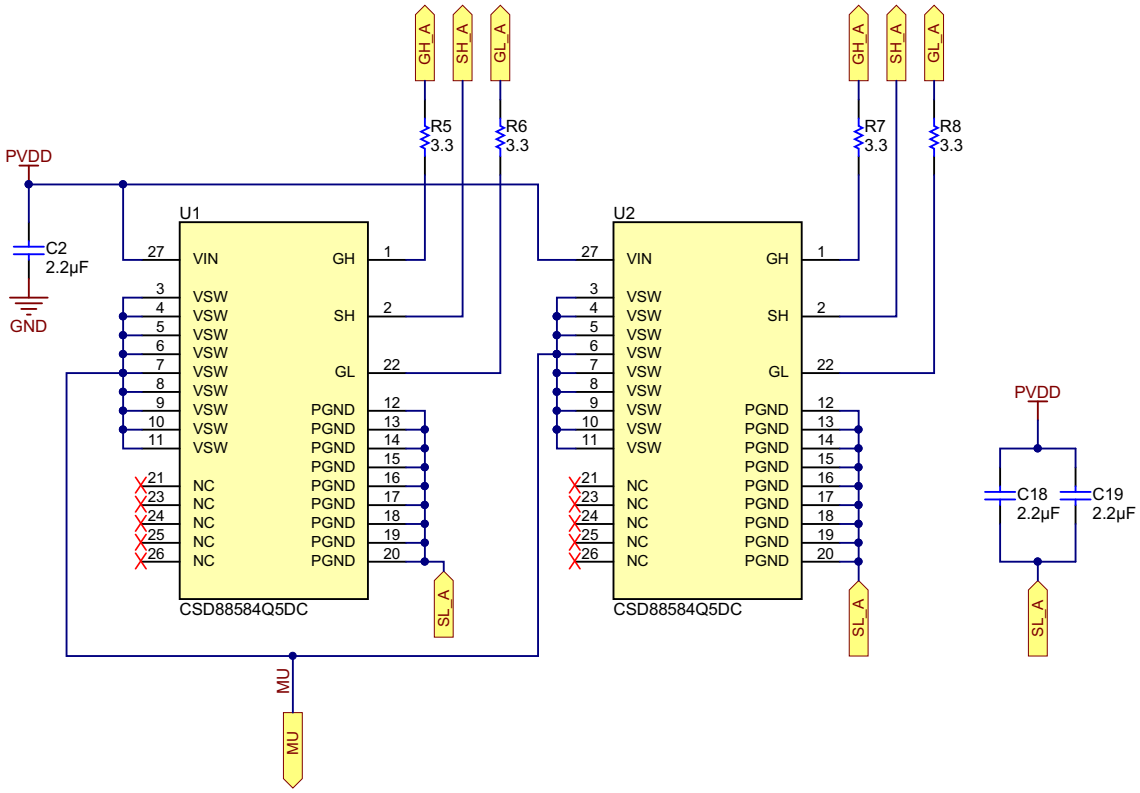

Figure 3. Schematic of Three-Phase MOSFET Inverter

NOTE: Connect the decoupling capacitors very near to the corresponding MOSFET legs for better decoupling. An improper layout or position of the decoupling capacitors can cause undesired VDS switching voltage spikes.

The DC bus current is measured using the current shunt resistors R13 and R15 mounted on the DC bus return path. The sensed currents are fed to the MCU through the current shunt amplifiers. The sense resistor is mainly used to measure the average battery current. The peak current in MOSFET is measured by monitoring the VDS.

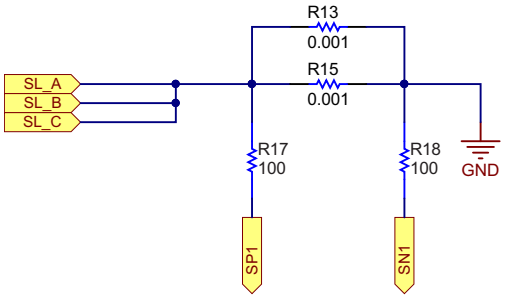

Figure 4. External Shunt for Current Sensing

6.2.1 Design Considerations in Paralleling MOSFETs

When paralleling FETs, current sharing becomes very important. All the parallel FETs are expected to carry equal current so that the losses are equally distributed. The FET operation can be split into conduction phase and switching phase. The effect of various parameters effecting current sharing in each of these phases is described in the following subsections.

6.2.1.1 Conduction Phase

In the conduction phase, the FETs are continuously conducting. The main parameter that affects current sharing during this phase is the R_{DS_ON} of the FET. If R_{DS_ON} of the FETs are not equal, then the FET with the highest on resistance carries the least current and the one with lowest on resistance carries the highest current. Because MOSFETs have a positive temperature coefficient of on resistance, the current sharing gets self-regulated. The FET carrying the highest current has the most conduction losses; this leads to temperature increase of the FET. Increased FET temperature causes an increase in the R_{DS_ON} of the FET, which in turn reduces the current through the FET. This self-regulating mechanism makes the current through each FET close to each other over time.

6.2.1.2 Switching Phase

The current sharing during the switching phase of the FET is affected by asymmetries in the gate drive circuit, differences in the circuit parasitics, and variations in device parameters such as transconductance g_{FS}, threshold voltage V_{TH}, and the input capacitances C_{GD} and C_{GS}. The effects of each parameter on current sharing are as follows:

- In order for all the FETs to be turned on at the same time, the gate drive circuit for each FET has to be very similar. The gate charge current for each parallel FET has to be equal. The gate voltage applied by the gate driver must be the same. Also there should be no skew in the gate-to-source voltages applied to the different FETs. If all these parameters are kept within a tight tolerance, the dynamic load current sharing of the paralleled FETs remains equal. One way to keep all these parameters in tight tolerance is to use a single gate driver IC to drive all the parallel FETs. This ensures minimal skew between the VGS of FETs and the V_{GS} voltage remains the same. The gate current into each FET can be maintained close to each other by choosing gate resistor values that have a tight tolerance. The gate path impedance has to be kept same in routing and this is possible by use of the miniature power blocks.
- Circuit parasitics like the source (LS) and drain (LD) inductances affect the turnon and turnoff times of the FET. If one FET has a higher LS compared to the others, a higher voltage is induced across LS when current flows through it. This reduces the effective VGS applied to the FET, which in turn slows down the turnon time of the FET effecting dynamic current sharing. One solution to this is by making the layout symmetric so that the LS and LD of each of the FETs are close to each other. Matching LS and LD also ensures that the rise and fall times of current in each FET is close.

- The threshold voltage of FETs is another important parameter affecting current sharing. The FET having the lowest V_{TH} turns on first and carries the highest current. Therefore, the FETs selected should have a tight tolerance in V_{TH}. Usually the FETs from one production batch have V_{TH} close enough that by the time the current through one FET rises significantly, the gate voltage of other FETs reach their V_{TH} reasonably quick and start conducting. Also, it is important to have individual gate resistances for each of the FET. If individual gate resistances are absent and all the gates are shorted together, then the FET—which reaches its V_{TH} first—goes into the Miller region faster and clamps the gate of the other FETs to its Miller voltage, which further slows down the gate voltages of the remaining FETs. This significantly effects the turn on behavior. V_{TH} is also dependent on temperature. The higher the temperature, the lower the V_{TH}; this ensures that the FET turns on even faster, which may lead to runaway conditions. Therefore, it is important to maintain all the FETs at equal temperature. Distributing the heat in the PCB by extending the copper planes helps here.
- Transconductance g_{FS} of the FET also affects the dynamic current sharing between the FETs. The FET with the highest g_{FS} has a faster rate of change of drain current with change in the gate-to-source voltage. So, during turnon, the FET with the highest g_{FS} conducts the most current, and during turnoff the FET with the lowest g_{FS} conducts current for a longer time.
- The input gate-to-source capacitance CGS and gate-to-drain capacitance CGD also affect dynamic current sharing. If the gate drive for all the FETs is symmetric (that is, drive voltages and currents are equal), then the FET with the lowest input capacitance CISS reaches its threshold voltage first and conducts the most current during turnon. During turnoff, the FET with the highest input capacitance reaches its threshold voltage last and conducts current for a longer time. To reduce the impact of the input capacitance on current sharing, it is important to use individual gate resistors with low values.

  Using low values ensures that all the FETs with variations in CISS reach their threshold values fairly close to each other. Selecting gate resistors is a trade-off between suppressing circulating currents and suppressing the effect of variations in CISS and V_{TH}.

6.2.2 Selecting the Sense Resistor

Power dissipation in sense resistors and the input offset error voltage of the op amps are important in selecting the sense resistance values. The sense resistors are carrying a total nominal RMS current of 60 A with a peak current of 120 A for 3 seconds. A high sense resistance value increases the power loss in the resistors. The internal current shunt amplifiers of the DRV8323 have an input offset error of 3 mV. The DRV8323 has the DC offset voltage calibration feature. In case the amplifier is used without offset calibration, it is required to select the sense resistor such that the sense voltage across the resistor is sufficiently higher than the offset error voltage to reduce the effect of the offset error. Selecting a 0.5-mΩ resistor as the sense resistor, the power loss in the resistor at 60-A_{RMS} is given by Equation 2:

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 60^2 \times 0.0005 = 1.8 \text{ W} \quad (2)$$

At a 120-A peak current, using Equation 2, the power loss in the resistor = 7.2 W (for 3 seconds)

In this reference design, two 1-mΩ, 5-W resistors are used in parallel.

NOTE: The user can consider reducing the sense resistor further down to reduce the power loss and use the current sense amplifier in maximum gain.

6.3 Power Stage Design—DRV8323 Gate Driver

Figure 5 shows the schematic of the DRV8323 gate driver. C13 is the DVDD decoupling capacitor that must be placed close to the IC. PVDD is the DC supply input; in this case, it is the battery voltage of 18 V. A 4.7-µF capacitor (C10) is used as the PVDD capacitor. C11 and C12 are charge pump capacitors. The EN_GATE of DRV8323 is connected to the MCU. This helps the MCU to enable or disable the gate drive outputs of the DRV8323. For the voltage rating and selection of these capacitors, see the DRV8323 datasheet.

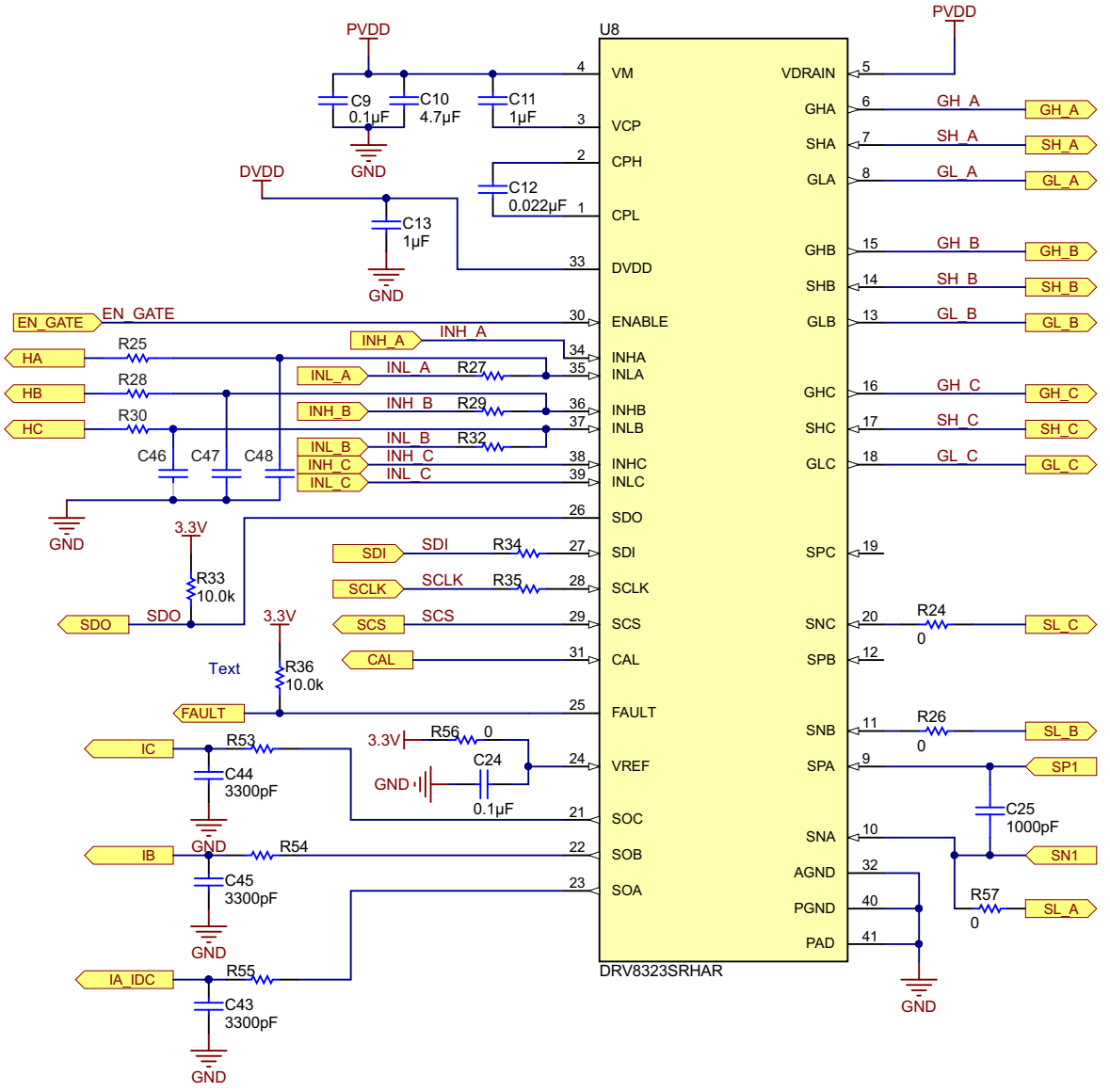

Figure 5. Schematic of DRV8323 Gate Driver

6.3.1 Gate Drive Features of DRV8323

The DRV832x integrates three half-bridge gate drivers, each capable of driving high- and low-side N-channel MOSFETs. A doubler charge pump provides the proper gate bias voltage to the high-side MOSFET across a wide operating voltage range, in addition to providing 100% duty cycle support. An internal LDO provides the gate bias voltage for the low-side MOSFETs. The DRV832x implements a smart gate drive, which allows the user to adjust the gate drive current on the fly without requiring current-limiting gate drive resistors. Current is adjustable through the SPI or on the IDRIVE pin for the hardware interface.

The DRV832x gate drivers use an adjustable, complimentary push-pull topology for both the high- and low-side drivers. This topology allows for strong pullup and pulldown of the external MOSFET gate. The gate drivers support adjustable peak current and duration settings through the IDRIVE and TDRIVE settings. This allows for adjusting the external MOSFET slew rate and provides additional system protection.

The peak source and sink current of the DRV832x gate drivers is adjustable either through the device registers or by an external pin IDRIVE. Control of the MOSFET VDS slew rates is an important parameter for optimizing emitted radiations and system efficiency. The rise and fall times also influence the energy and duration of the diode recovery spikes and dV/dt related turn on. When changing the state of the gate driver, the peak current (IDRIVE source or sink) is applied for a fixed period of time (TDRIVE) during which the gate capacitances are charged or discharged completely. After TDRIVE has expired a fixed holding current (IHOLD) is used to hold the gate at the desired state (pulled up or pulled down). During high-side turnon, the low-side gate is pulled low with a strong pulldown. This prevents the gate-to-source capacitance of the low-side MOSFET from inducing turnon.

The fixed TDRIVE time ensure that under abnormal circumstances like a short on the MOSFET gate or the inadvertent turn on of a MOSFET VGS clamp, the high peak current through the DRV832x gate drivers is limited to the energy of the peak current during the TDRIVE. Limiting this energy helps to prevent damage to the gate drive pins and external MOSFET.

The TDRIVE time must be selected to be longer than the time need to charge or discharge the MOSFET gate capacitances. IDRIVE and TDRIVE should be initially selected based on the parameters of the external MOSFET used in the system and the desired rise and fall times. TDRIVE will not increase the PWM time and will terminate if a PWM command is received while it is active. A recommended starting point is to select a TDRIVE that is approximately two times longer than the external MOSFET's switching rise and fall times. See DRV832x for more details.

6.3.2 Current Shunt Amplifier in DRV8323

The sense amplifiers on the DRV8323S can be configured to amplify the voltage across the low-side FETs. During this mode of operation, leave the SPX pins unconnected. The positive input of the amplifier is internally connected to the SHX pin. An internal clamp prevents high voltage on the SHX pin from damaging the sense amplifier inputs.

When the CSA_FET bit is set to '1', the negative reference for the low-side VDS monitor is automatically set to SNX, regardless of the state of the LS_REF bit. This is implemented in order to prevent the low-side VDS monitor from being disabled. If the system is intended to operate in FET sensing mode, take care to route the SHX an SNX pins to kelvin connections across the drain and source of the low-side FETs.

When operating in FET sensing mode, the amplifier is enabled at the end of TDRIVE. At this time, the amplifier input is connected to SHX, and the SOX output will be valid. Whenever a low-side FET receives a signal to turn off, the amplifier inputs are shorted together. When GLX is low, SPX and SNX are internally shorted.

The current shunt amplifiers have the following features:

- Can be programmed and calibrated independently
- Can support bidirectional and unidirectional current sensing
- Four programmable gain settings through SPI registers (5, 10, 20, and 40 V/V)
- Programmable output bias scaling: VREF or VREF/2
- Programmable blanking time of the amplifier outputs
- Amplifier can be used to monitor current through half-bridges and the current is approximately calculated as in Equation 3:

$$SO_X = \frac{VREF}{2} + \left(I \times CSA\_GAIN \times R_{DS\_ON}\right) \quad (3)$$

Figure 6 shows the current sense amplifier simplified block diagram.

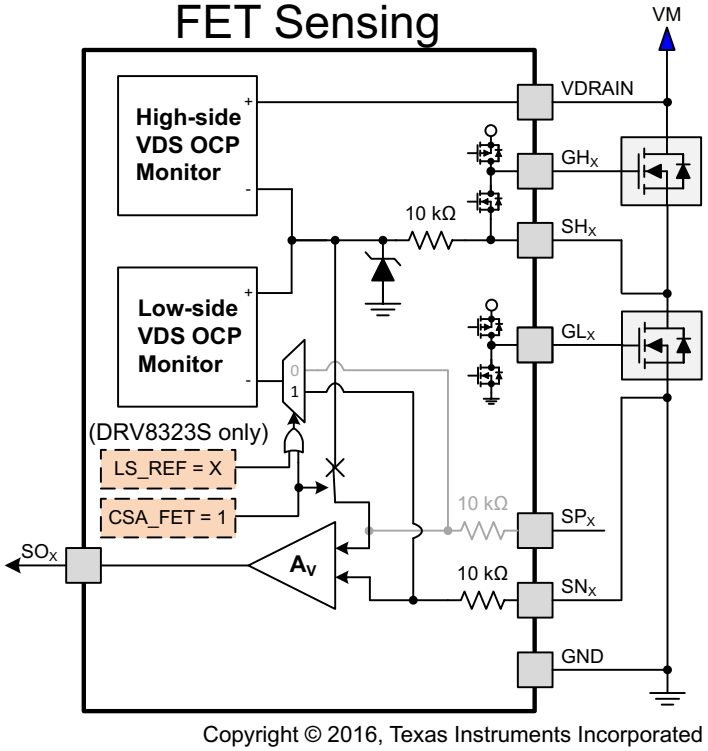

Figure 6. DRV8323 Current Shunt Amplifier Simplified Block Diagram

6.3.3 Protection Features in DRV8323

The DRV8323 integrates the following protections, which help in making a reliable power stage:

- VM undervoltage lockout
- VCP undervoltage lockout
- VDS overcurrent protection
- SENSE overcurrent protection
- Gate driver fault
- Thermal shutdown
- Thermal warning

For more details, see the DRV8323 datasheet.

6.4 Power Stage Design—18-V to 3.3-V DC-DC Converter

Figure 7 shows the schematic of the 18-V to 3.3-V DC-DC buck regulator. Table 2 shows the specification of the buck converter used for this TI Design.

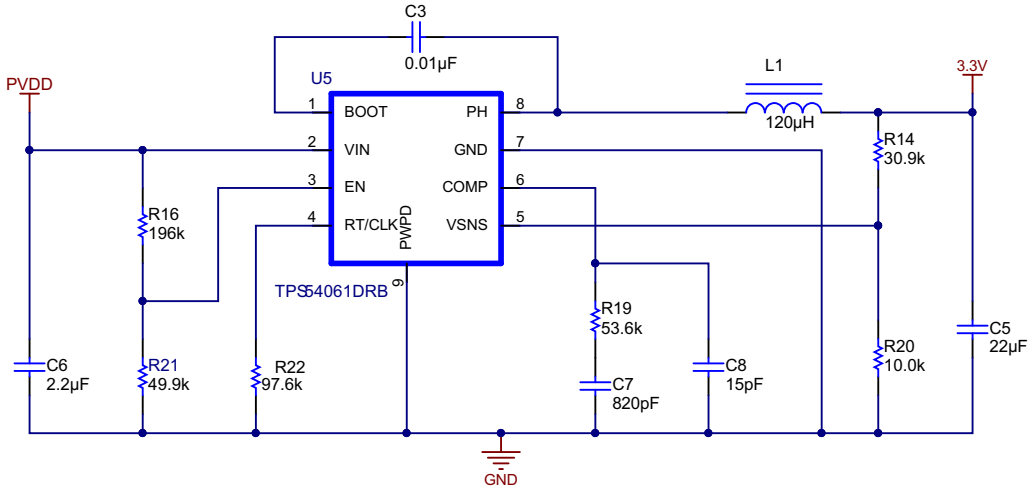

Figure 7. 18-V to 3.3-V DC Converter

Table 2. Design Requirement and Specification of 18-V to 3.3-V DC-DC Buck Regulator

PARAMETER	DESIGN REQUIREMENT
Conduction mode	Continuous conduction mode (CCM)
Output voltage	3.3 V
Transient response 50- to 150-mA load step	ΔV_{OUT} = 4%
Maximum output current	200 mA
Input voltage	18 V nom, 6 to 21 V
Output voltage ripple	0.5% of V_{OUT}
Start input voltage (rising V_{IN})	6 V
Stop input voltage (falling V_{IN})	7 V

For the detailed design of buck converter, see the TPS54061 datasheet.

6.5 Power Stage Design —Microcontroller MSP430

Figure 8 shows the schematic for configuring the MSP430F5132 MCU. The resistor R37 is used to limit the dV/dt at the supply pin of the MSP430F5132. The TIDA-00774 reference design uses 10-µF decoupling capacitors. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency.

The Timer D of the MCU is used for PWM generation. The TD0.1 instance of the timer and the corresponding pins are mapped to the high-side switch PWM. The TD0.2 instance of the timer and the corresponding pins are mapped to the low-side switch PWM. The TIDA-00774 reference design uses unipolar, trapezoidal BLDC control where the high-side switches switching at a high frequency. The low-side switches switch at the electrical frequency of the motor current, which is much lower and the same will switch at a high frequency (complimentary to high-side switch) during the freewheeling period to enable active freewheeling and hence low losses. All the feedback signal voltages including the DC bus voltage, current sense amplifier output, potentiometer voltage for speed control, and temperature sensor output are interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU. The current sense amplifier output is also connected to the comparator input.

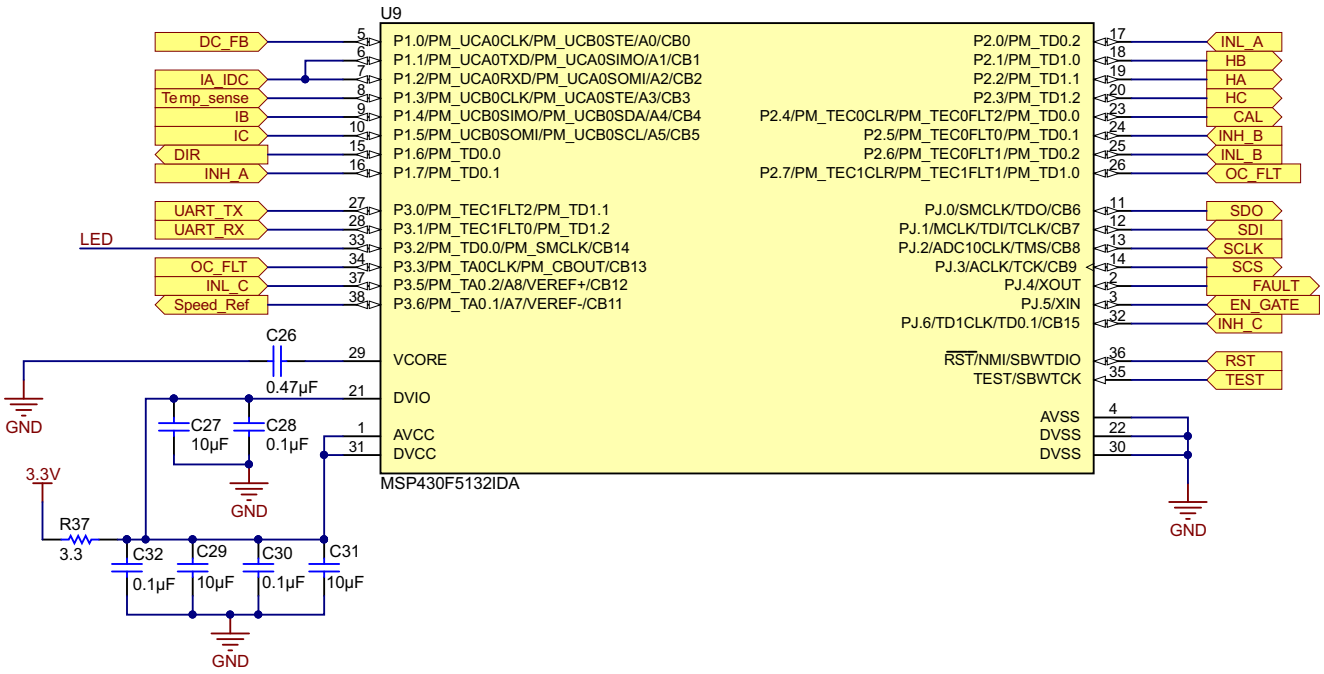

Figure 8. MSP430F5132 Schematic

6.6 Power Stage Design—Hall Sensor Interface

Figure 9 shows the Hall sensor interface from the motor to the board. The 3.3 V is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. R47, R48, and R49 are used as the pullup resistors. R50, R51, and R52 along with C38, C39, and C40 form noise filters at the Hall sensor input.

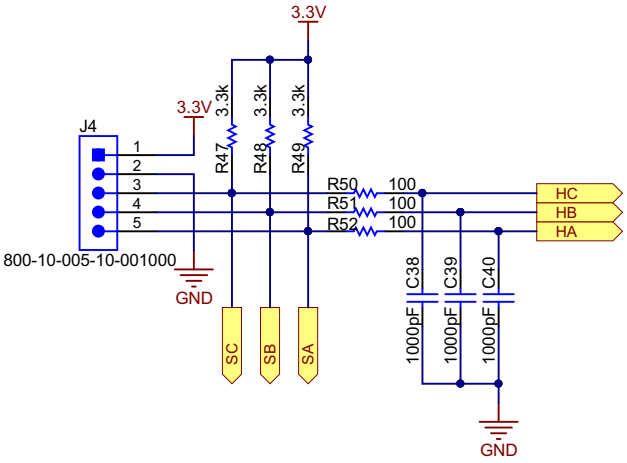

Figure 9. Hall Sensor Connector Schematic

NOTE: The Hall sensor connection must match with the winding connection for proper operation of the BLDC motor.

6.7 Temperature Sensing

Figure 10 shows the temperature sensor circuit used to measure the PCB temperature. The LMT87 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is 13.6 mV/°C.

The temperature sensor placed near the MOSFET and the output of the temperature sensor is used to calibrate the VDS sense signal. The R_{DS_ON} of the MOSFET varies with temperature and hence the VDS measured across the FET for current sensing has to be calibrated to measure the current accurately by sensing VDS.

NOTE: The temperature gradient in the board must be considered to properly calibrate the VDS of multiple FETs against R_{DS_ON} variation with temperature.

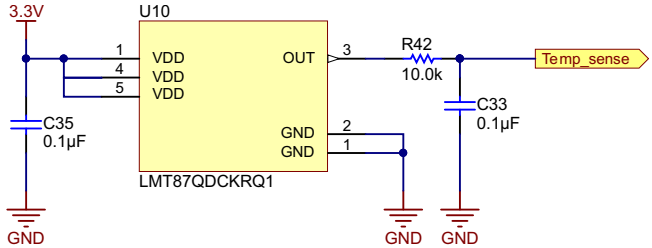

Figure 10. Temperature Sensor Schematic

6.8 Power Stage Design—External Interface Options and Indications

6.8.1 Speed Control of Motor

The speed control is done using a potentiometer (POT), and the POT voltage is fed to the ADC of the MCU. The circuit is shown in Figure 11. The POT is supplied from the 3.3 V. A 20k POT can be connected externally to the jumper J1. Connect the fixed terminals of the POT to terminal 1 and 3 of J1 and mid-point to terminal 2 of J1.

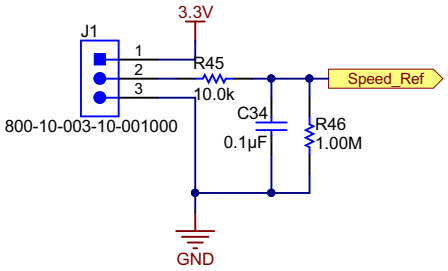

Figure 11. Potentiometer Connection for Speed Control Schematic

The resistor R46 is used to ensure that the speed control reference is zero if the POT terminal is open.

6.8.2 Direction of Rotation—Digital Input

The jumper J2 (shown in Figure 12) is used to set the direction of rotation of the motor. Close or open the jumper to change the direction of rotation.

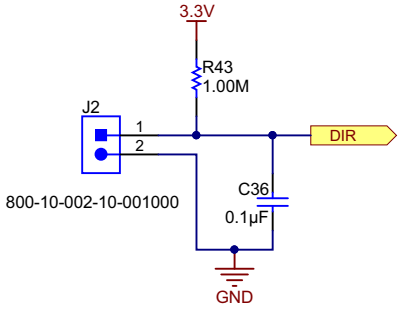

Figure 12. Digital Input to Change Direction of Rotation

6.8.3 LED Indications

Figure 13 shows the LED indications provided in the board. The LED D4 indicates the 3.3 V in the board, D2 is tied to FAULT signal from DRV8323, and D3 is driven by a digital I/O in the MCU.

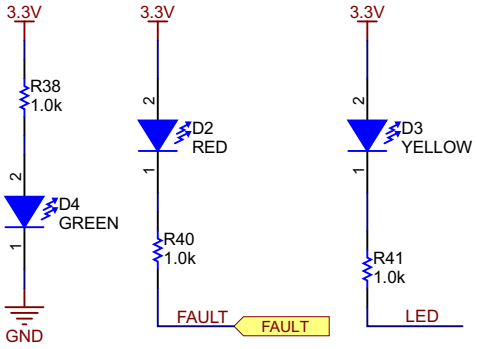

Figure 13. LED Indications Schematic

6.8.4 Signal Interface Connector for External Monitoring and Control

Figure 14 shows the signal interface connector for external monitoring and control. All the signals in the board is available at the connector J5.

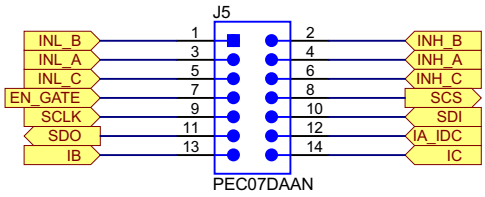

Figure 14. Signal Interface Connector for External Monitoring and Control

7 Getting Started Hardware and Software

7.1 Hardware

7.1.1 Connector Configuration of TIDA-00774

Figure 15 shows the TIDA-00774 connector configuration, which features the following:

- Two-terminal input for power supply: This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified as shown in Figure 15.
- Three-terminal output for motor winding connection: The phase output connections for connecting to the three-phase BLDC motor winding, marked as PHASE A, PHASE B, and PHASE C as shown in Figure 15.
- 3-pin connector J1: This connector can be used to interface an external potentiometer for speed reference. The two fixed terminals of the potentiometer should be connected to 3V3 pin and GND pin. The mid-point of the potentiometer should be connected to the POT pin of the connector.
- 2-pin connector J2: This connector is used for the motor direction change. Externally shorting or opening this connector will change the direction of rotation of the motor.
- 4-pin connector J3: This is the programming connector for the MSP430F5132 MCU. The two-wire Spy-Bi-Wire protocol is used to program the MSP430F5132.
- 5-pin connector J4: This is the interface for connecting the Hall position sensors from the motor
- 14-pin connector J5: All the signals in the board are available at this pin. This connector can be used for external monitoring or control.
- 2-pin connector J6: This connector is used for external UART communication interface. The RX and TX pins are available enabling the communication with external BLE or Wi-IFi.

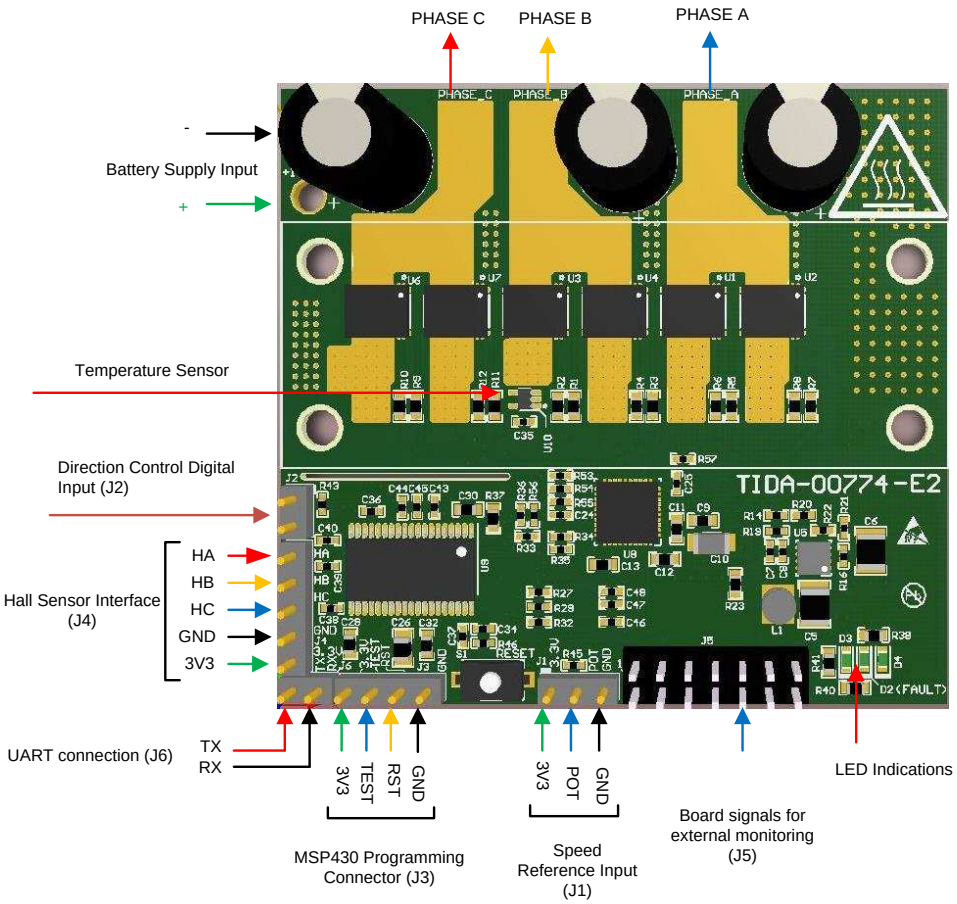

Figure 15. TIDA-00774 PCB Connectors

7.1.2 Programming of MSP430

The two-wire Spy-Bi-Wire protocol is used to program the MSP430F5132 MCU. Figure 16 shows the four-pin programming connector provided in the TIDA-00774 board.

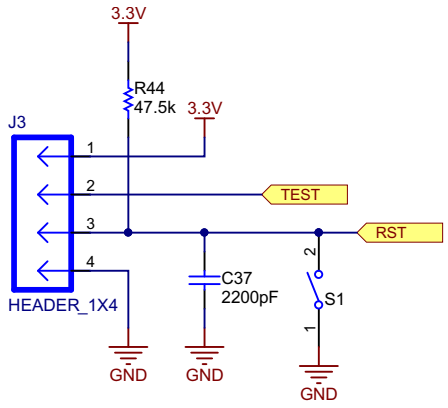

Figure 16. MSP430F5132 Programming Connector

See http://www.ti.com/product/MSP430F5132/toolssoftware#devtools for the programming options with an external JTAG interface.

The following list outlines the steps to program the MSP430F5132 MCU when the programming supply voltage is provided by the board itself:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of 6-V DC input is applied and 3.3 V is generated in the board.
2. Connect the programmer to the board.
3. Open the CCS software and then build and debug the code to program the MCU.

7.1.3 Procedure for Board Bring-up and Testing

The following list details the procedure for board bring-up and testing:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of a 6-V DC input is applied and the 3.3 V is generated in the board.
2. Program the MCU as detailed in Section 7.1.2.
3. Remove the programmer, and switch off the DC input supply.
4. Connect the inverter output to the motor winding terminals. Connect the position Hall sensor inputs to the connector J4, and make sure that the winding connection and Hall sensor connections match.
5. Connect the POT at the interface J1 and set the speed reference.
6. Use a DC power supply with current limit protection and apply 8-V DC to the board. If the Hall sensors and winding are connected properly in the matching sequence, then the motor will start running at a speed set by the POT.
7. If the motor is not rotating and takes high current or rotates and draw distorted peak winding current waveform (proper waveform shape is as shown in Figure 31), then check the winding and Hall sensor connection matching and, if wrong, correct it.
8. Adjust the POT voltage for change in speed.
9. To change direction, switch off the DC input, close the jumper J2, and switch on the DC input.

7.2 Software

7.2.1 System Features

The TIDA-00774 firmware offers the following features and user controllable parameters:

- Trapezoidal control of BLDC motor using digital position Hall sensor feedback
- Overcurrent cycle by cycle protection and latch protection using the VDS sensing feature of DRV8323S

The TIDA-00774 firmware system components are tabulated in Table 3.

Table 3. TIDA-00774 Firmware System Components

SYSTEM COMPONENT	DESCRIPTION
Development and emulation	Code Composer Studio™ v5.5
Target controller	MSP430F5132
PWM frequency	20-kHz PWM (default), programmable for higher and lower frequencies
PWM mode	Asymmetrical
Interrupts	Port 2 Interrupt for hall sensor change CPU Timer D – Implements 20-kHz ISR execution rate ADC interrupt
PWM generation—Timer configuration	High-side PWM- TIMER TD0.1, Clock-25 MHz, OUTMOD[2:0]= 2,PWM frequency set for 20 kHz Low-side PWM- TIMER TD0.2, Clock-25 MHz, OUTMOD[2:0]= 6,PWM frequency set for 20 kHz
Position feedback—Hall sensor signals	P2.2 → HA P2.1 → HB P2.3 → HC
Comparator configuration for overcurrent protection	CB2/P1.2 →CSA output (–ve input of comparator) Internal VREF (+ve input of comparator) CBOUT/P3.3 → Comparator output PM_TEC1FLT1 → PWM shut off input
ADC channel assignment	A0 → DC bus voltage sensing A1 → Low-side DC bus current sensing/PHASE A low-side MOSFET VDS sensing A3 → PCB or FET temperature feedback A4 → PHASE B low-side MOSFET VDS sensing amplifier output A5 → PHASE C low-side MOSFET VDS sensing amplifier output A7 → Speed reference from the external potentiometer
DRV8323—SPI programming pins connection	PJ.0 → SDO PJ.1 → SDI PJ.2 → SCLK PJ.3 → SCS
DRV8323—Digital inputs and outputs	PJ.5 → EN_GATE PJ.4 → FAULT P2.4 → CAL
MCU digital inputs and output	P1.6 → Direction of motor rotation P3.2 → LED3

7.2.2 Customizing the Reference Code

Select the "main.c" file. Parameters exist at the top of the file that can be optimized and are included as the configuration variables. The following section of code shows these parameters:

```
#define PWM_PERIOD 625 //PWM Frequency (Hz) = 25MHz/((2*PWM_PERIOD)-1)
#define MAX_DUTYCYCLE 625 //relative to PWM_PERIOD
#define MIN_DUTYCYCLE 50 //relative to PWM_PERIOD
#define ACCEL_RATE 320 // Ramp up time to full scale duty cycle = (Full scale duty cycle) *
ACCEL_RATE * PWM_PERIOD/PWM_Frequency
#define DEAD_TIME 1 // Dead time from MSP430 = DEAD_TIME * 0.04 uS (for 25MHz clock)
#define Block_Rotor_Duration 1250 //Blocked_rotor shut off time(s) =
Block_Rotor_Duration*30000/clock frequency
```

7.2.2.1 PWM_PERIOD

PWM_PERIOD sets the value in capture and compare register 0 of Timer_D0. The Timer_D is initialized to operate at 25 MHz; see Equation 4 to calculate the PWM frequency. The TIMER_D PWM is configured in up-down mode.

$$\text{PWM Frequency}\,(\text{Hz}) = \frac{25\ \text{MHz}}{((2 \times \text{PWM\_PERIOD}) - 1)} \tag{4}$$

For example, with PWM_PERIOD = 625:

$$\text{PWM Frequency}\,(\text{Hz}) = \frac{25\ \text{MHz}}{((2 \times 625) - 1)} \approx 20\ \text{kHz}$$

7.2.2.2 MAX_DUTYCYCLE

MAX_DUTYCYCLE sets the maximum duty cycle the user can set. Every time the duty cycle input command is compared to the MAX_DUTYCYCLE. If the duty cycle input command exceeds the MAX_DUTYCYCLE, the target duty cycle is set to the MAX_DUTYCYCLE. This number is relative to the PWM_PERIOD.

7.2.2.3 MIN_DUTYCYCLE

MIN_DUTYCYCLE sets the minimum duty cycle that can be applied to the motor. This number is relative to the PWM_PERIOD.

7.2.2.4 ACCEL_RATE

ACCEL_RATE defines how fast the motor will accelerate. For a motor with greater inertia or if it needs a longer time to accelerate, set this number to a high value such as 2000. Motors that can quickly ramp up can use a smaller ACCEL_RATE to decrease the startup time. In the application program, the start ramp-up time and the ACCEL_RATE required can be calculated using Equation 5 and Equation 6.

$$\text{Ramp up time to full scale duty cycle} = \frac{\text{Full scale duty cycle} \times \text{ACCEL\_RATE} \times \text{PWM\_PERIOD}}{\text{PWM frequency}} \tag{5}$$

$$\text{ACCEL\_RATE} = \frac{\text{Ramp up time to full scale duty cycle} \times \text{PWM Frequency}}{\text{Full scale duty cycle} \times \text{PWM\_PERIOD}} \tag{6}$$

For example: To ramp up from 0% to 100% duty cycle (Full scale duty cycle = 1) in 10 seconds, provided the PWM frequency = 20 kHz, the ACCEL_RATE can be calculated as such:

$$\text{ACCEL\_RATE} = \frac{10\ \text{s} \times 20\ \text{kHz}}{1 \times 625} = 320$$

7.2.2.5 Block_Rotor_Duration

Block_Rotor_Duration defines the time duration in which the motor blocked rotor condition is allowed before the controller turns off all the PWM. The time taken to turn off all the PWM when the motor is blocked can be calculated using Equation 7.

$$\text{Blocked rotor PWM turnoff time}(\text{s}) = \frac{\text{Block\_Rotor\_Duration} \times 30000}{25\ \text{MHz}} \quad (7)$$

where 25 MHz is the TIMER_D clock frequency.

For example, if the user wants to turns off the motor if a blocked rotor condition is observed for 1.5 seconds, then:

$$\text{Block\_Rotor\_Duration} = 1.5 \times \frac{25\ \text{MHz}}{30000} = 1250$$

7.2.3 Configuring the DRV8323 Registers (drv8323.c)

The register settings of the DRV8323 can be modified by selecting and modifying the file “drv8323.c”. See the function “DRV8x_Analog_Init()” to initialize the DRV8323 with modified values. The code snippet of the function is given as follows.

```
void DRV8x_Analog_Init(void)
{
SPI_Write(0x03, 0x03BF);
delay_1ms(1);
SPI_Write(0x03, 0x03BF);
delay_1ms(1);
SPI_Write(0x02, 0x0100);
delay_1ms(1);
SPI_Write(0x04, 0x06FF);
delay_1ms(1);
SPI_Write(0x05, 0x0160);
delay_1ms(1);
SPI_Write(0x06, 0x0683);
delay_1ms(1);
}
```

See the DRV8323 datasheet for a detailed understanding of register settings.

7.2.4 Initializing SPI Communication Between DRV8323 and MSP430 (drv8323.h)

The register initialization for the DRV8323 is done by means of SPI communication. The SPI communication pins are connected to the ports of the MSP430.

See "drv8323.h" to assign and initialize the ports of MSP430 for SPI communication. The TIDA-00774 reference design uses port connections as given in Table 4.

Table 4. SPI Communication Interface Between DRV8323 and MSP430

DRV8323 PIN	MSP430G2553 PIN
SDO	PJ.0
SDI	PJ.1
SCLK	PJ.2
SCS	PJ.3

Modify the SPI GPIO settings as per the hardware mapping. For the TIDA-00774, the mapping is shown in the following code snippet.

```
#define CPU_FREQ_MHZ (25)
/*************************************************************************
 * SPI GPIO Settings (Modify according to hardware mapping)

               *************************************************************************/
#define M1_SCLK_HIGH (PJOUT |= BIT2)
#define M1_SCLK_LOW (PJOUT &= ~BIT2)
#define M1_SDI_HIGH (PJOUT |= BIT1)
#define M1_SDI_LOW (PJOUT &= ~BIT1)
#define M1_SDO_LEVEL ((PJIN &= BIT0)?(1):(0))
#define M1_nSCS_HIGH (PJOUT |= BIT3)
#define M1_nSCS_LOW (PJOUT &= ~BIT3)
```

7.2.5 Running Project in Code Composer Studio (CCS)

To run this project in CCS:

1. Install CCS and import the project "TIDA-00774_Firmware _V1.0".
2. Read through Section 7.2.2 to customize the code.
3. Power up the board with an external supply as described in Section 7.1.2 and connect the programmer.
4. Build and debug the modified project to download the code to the MSP430F5132.

8 Testing and Results

8.1 Test Setup

Figure 17 shows the load setup used to test the motor. The load is an electrodynamometer type load by which the load torque applied to the motor can be controlled.

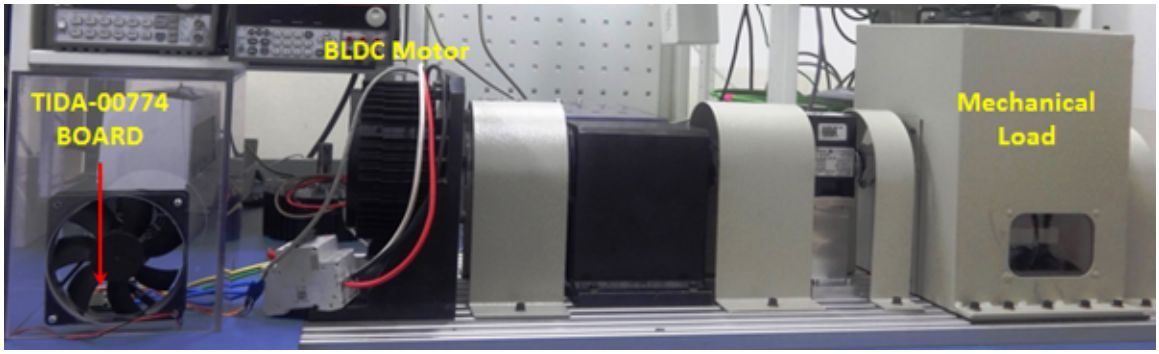

Figure 17. Board and Motor Test Setup

8.2 Test Data

8.2.1 Functional Tests

8.2.1.1 3.3-V Power Supply Generated by Step-Down Converter

Figure 18 shows the 3.3 V generated from the TPS54061 step-down converter. The ripple in the 3.3-V rail is also shown in Figure 18.

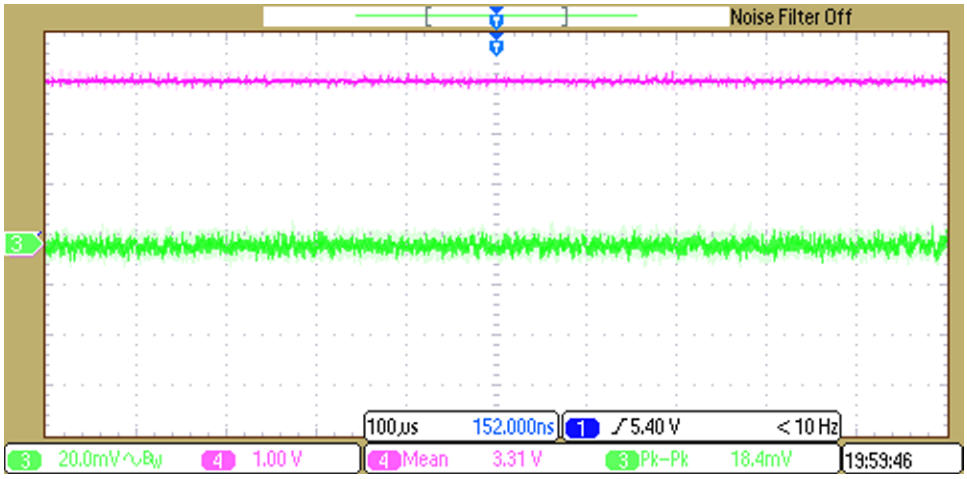

Figure 18. Output Voltage of 3.3 V From Step-Down Converter and 3.3-V Voltage Ripple

8.2.1.2 Gate Drive Voltage Generated by Gate Driver

Figure 19 shows the gate drive output voltage of DRV8323 and the corresponding MCU PWM signals at a DC bus voltage of 18-V DC. The gate drive voltage is approximately 11 V, which means effective gate driving of standard MOSFETs.

Figure 20 shows the gate drive voltage of the DRV8323 at a DC bus voltage of 8 V, which could be the minimum voltage available from a discharged Li-ion battery. The gate drive output voltage is approximately 6.5 V.

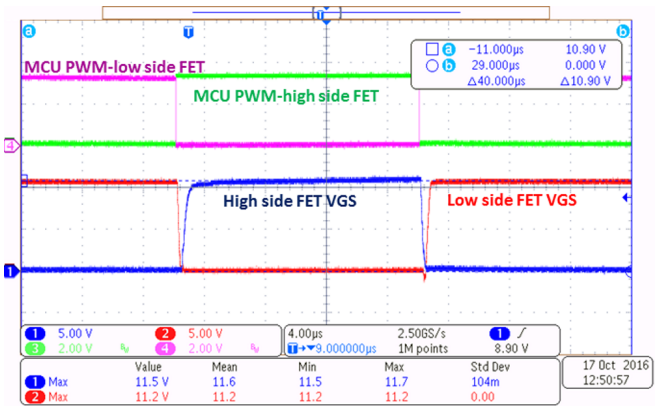

Figure 19. Low-Side and High-Side Gate Drive Voltage at 18-V DC

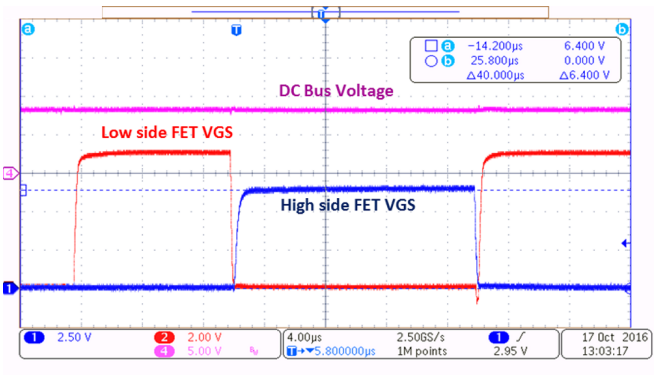

Figure 20. High-Side and Low-Side Gate Drive Voltage at 8-V DC

8.2.1.3 Dead Time From DRV8323

Figure 21 and Figure 22 shows the high-side and low-side gate source voltage from the DRV8323, which shows the dead time inserted by the DRV8323 at the both the edges of the PWM. The dead is programmed to 100 ns. DRV8323 inserts the dead time after the VGS handshake.

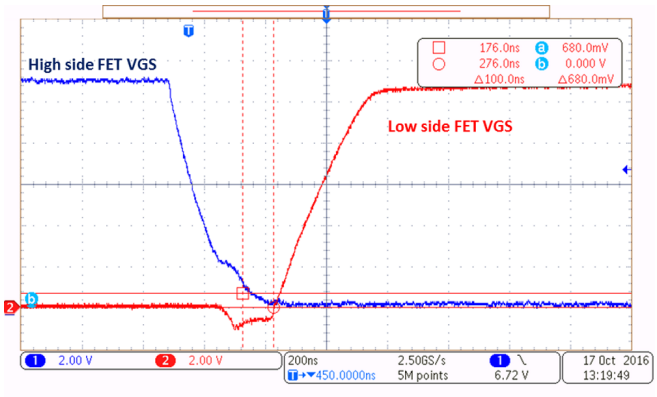

Figure 21. Dead Time at Low-Side VGS Rising Edge

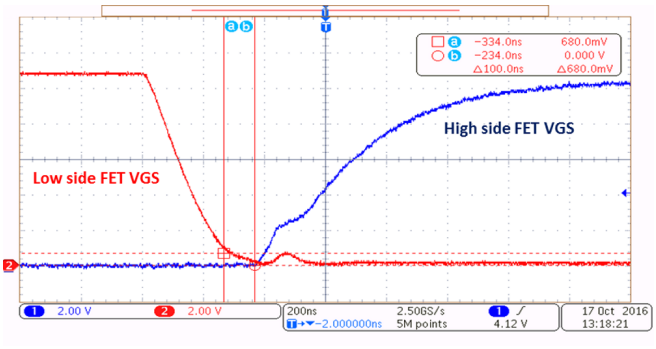

Figure 22. Dead Time at Low-Side VGS Trailing Edge

8.2.1.4 MOSFET Switching Waveforms

Figure 23 to Figure 26 shows the VDS and VGS waveforms of the low-side and high-side MOSFETs at a total gate current of the DRV8323 (IDRIVE) is set at a 680-mA source and a 2-A sink current. The design uses two FETs in parallel. Therefore, the gate drive current per FET is a 340-mA source and a 1-A sink current. The switching waveforms are captured with a 3.3-Ω gate resistor for each FET. Switching waveforms are clean without any over voltage ringing due to:

- The power block has both the high-side and low-side switches in same package, which reduces the parasitic inductance and hence reduces the phase node voltage ringing.
- The current controlled gate driver with slew rate control helps to optimize the switching.
- The IDRIVE/TDRIVE feature of the gate driver helps to shape the gate current to optimize the switching.

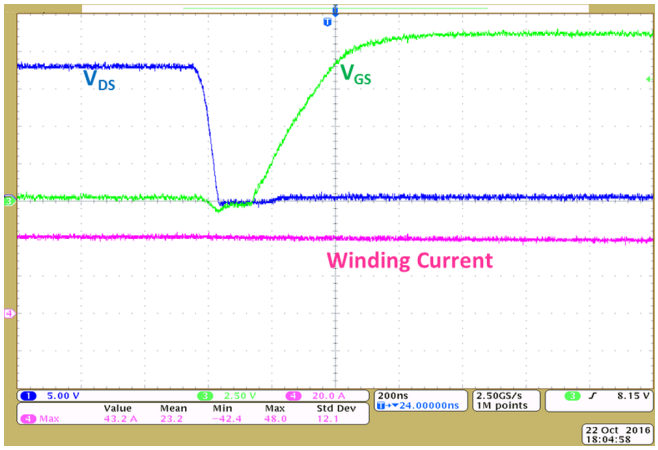

Figure 23. Turnon—Low-Side VGS and VDS at 43-A Winding Current

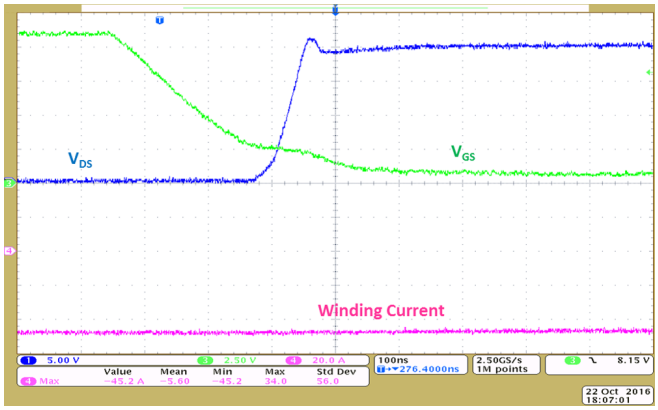

Figure 24. Turnoff—Low-Side VGS and VDS at 45-A Winding Current

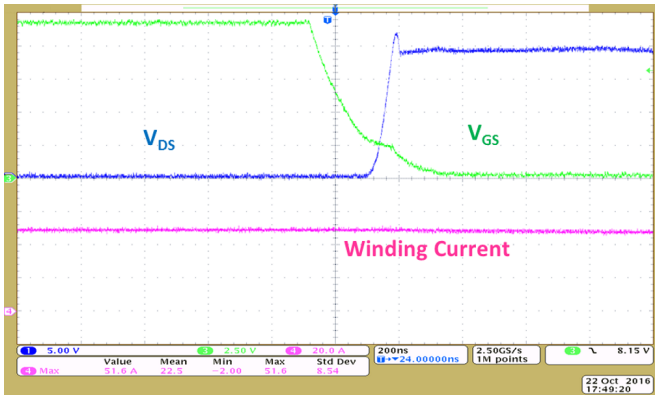

Figure 25. Turnoff—High-Side VGS and VDS at 52-A Winding Current

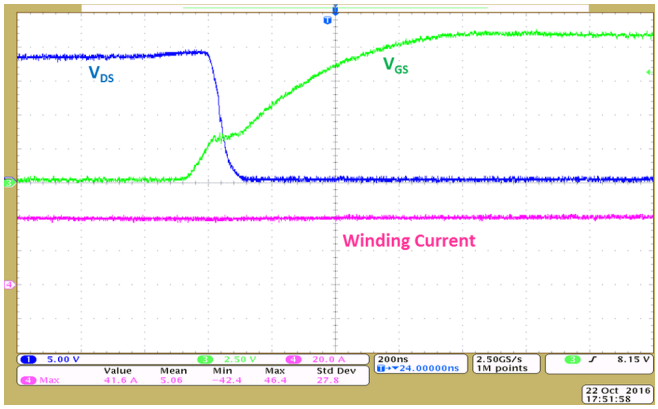

Figure 26. Turnon—High-Side VGS and VDS at 42-A Winding Current

8.2.1.5 VGS Skew of Parallel FETs During Switching

Waveforms from Figure 27 to Figure 30 show the skew in V_{GS} when comparing the parallel FETs. The gate drive current per FET is set to a 340-mA source and a 1-A sink current. The current controlled gate driver and low parasitic in the gate driver circuit path helps in dynamic characteristics during switching and ensures proper dynamic current sharing. The 3.3-Ω external gate resistor is used to limit the circulation current between the gate source of paralleled FETs. If a single MOSFET is used, the external gate resistor is not required.

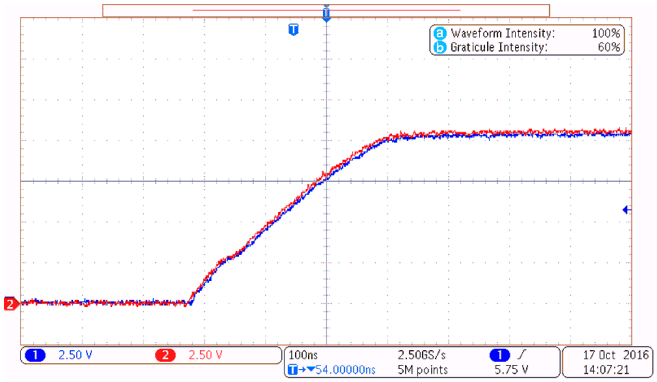

Figure 27. Low-Side FET Turnon VGS

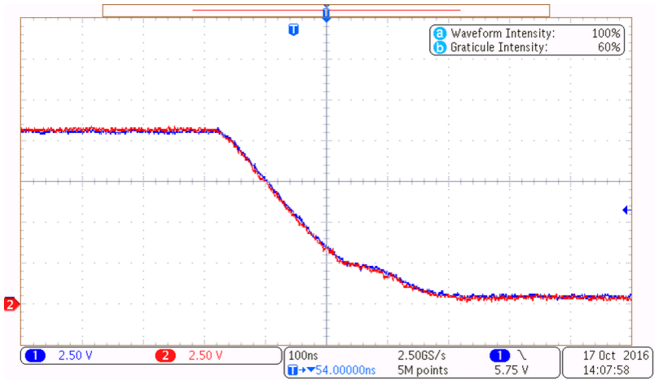

Figure 28. Low-Side FET Turnoff VGS

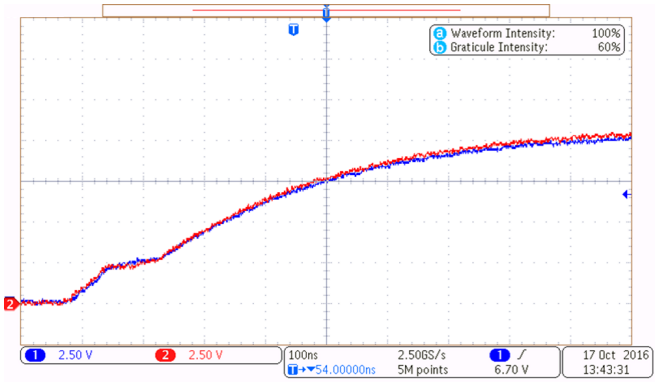

Figure 29. High-Side FET Turnon VGS

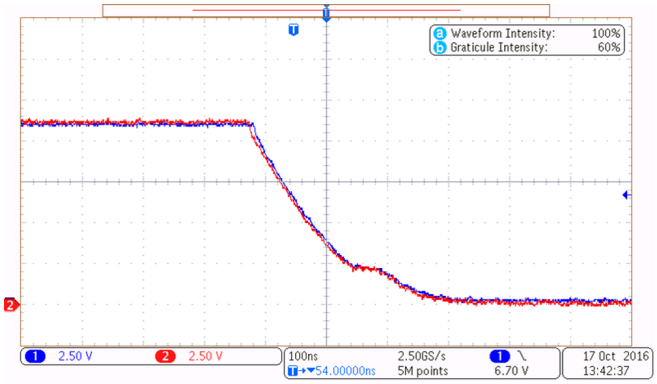

Figure 30. High-side FET Turnoff VGS

8.2.2 Load Test

The TIDA-00774 board is tested with external BLDC motor and load using the test setup in Figure 17.

8.2.2.1 Load Test Without Heat Sink

Figure 31 shows the motor winding current and winding voltage waveforms at a 18-V DC input and a 33-A_{RMS} winding current. The result is tabulated in Table 5. The testing is done at 100% duty cycle. Figure 32 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 87.9°C.

Table 5. Load Test Results at 100% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	DUTY CYCLE	INPUT POWER (W)
18	38	33	100%	680

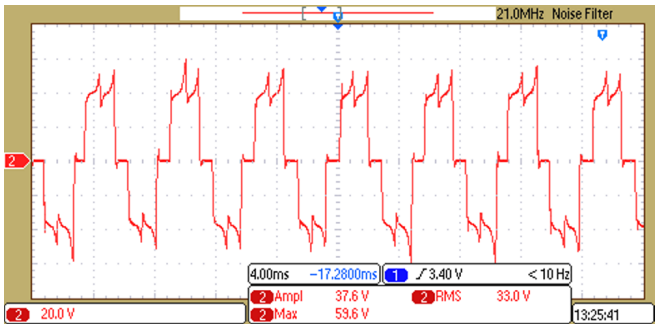

Figure 31. Load Test Results at 18-V DC Input, 33-A_{RMS} Winding Current, 100% Duty Cycle

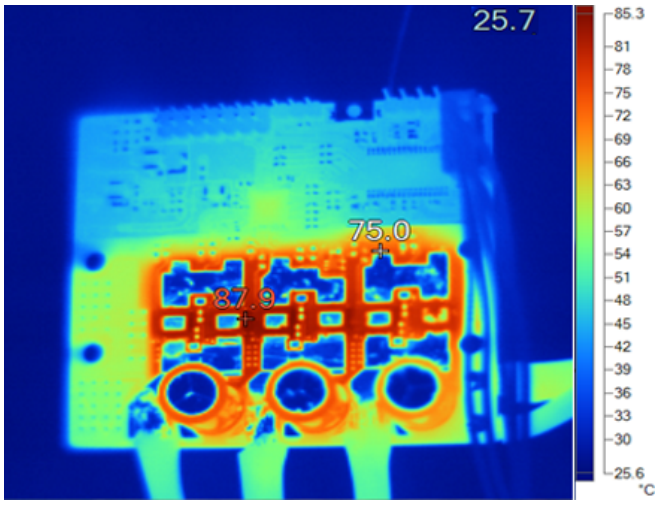

Figure 32. Thermal Image at 18-V DC Input, 33-A_{RMS} Winding Current, 100% Duty Cycle

Figure 33 shows the motor winding current and winding voltage waveforms at a 18-V DC input and a 31.8-A_{RMS} winding current. The result is tabulated in Table 6. The testing is done at 90% duty cycle. Figure 34 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 88.9°C.

Table 6. Load Test Results at 90% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	DUTY CYCLE	INPUT POWER (W)
18	33	31.8	90%	594

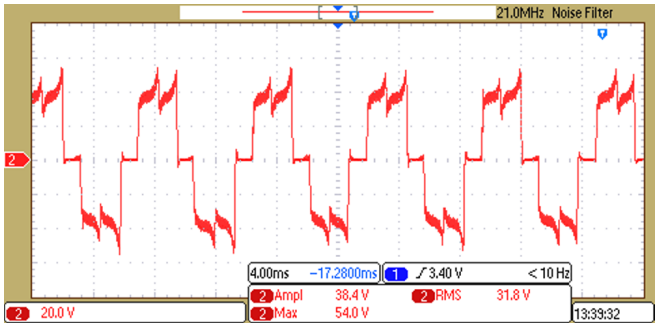

Figure 33. Load Test Results at 18-V DC Input, 31.8-A_{RMS} Winding Current, 90% Duty Cycle

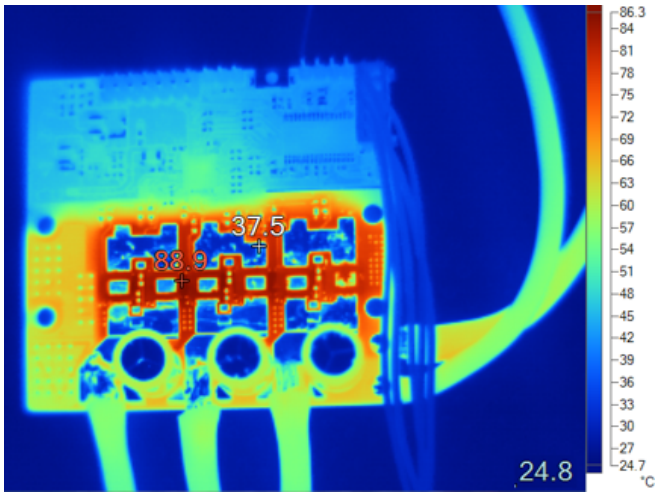

Figure 34. Thermal Image at 18-V DC Input, 31.8-A_{RMS} Winding Current, 90% Duty Cycle

8.2.2.2 Load Test With Heat Sink

Figure 35 shows the motor winding current and winding voltage waveforms at a 18-V DC input and a 42-A_{RMS} winding current with a heat sink. The result is tabulated in Table 7. The testing is done at a 100% duty cycle. Figure 36 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 85.3°C.

Table 7. Load Test Results at 100% Duty Cycle With Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	DUTY CYCLE	INPUT POWER (W)
18	48	42	100%	864

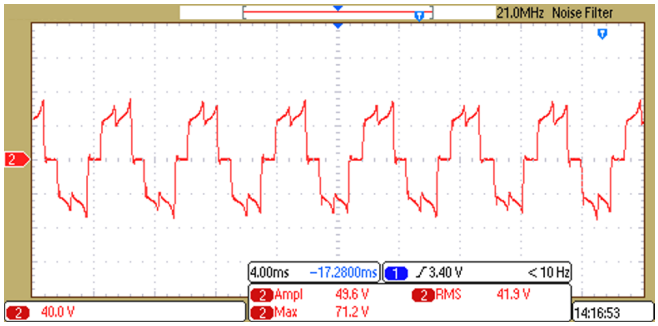

Figure 35. Load Test Results at 18-V DC Input, 42-A_{RMS} Winding Current, 100% Duty Cycle

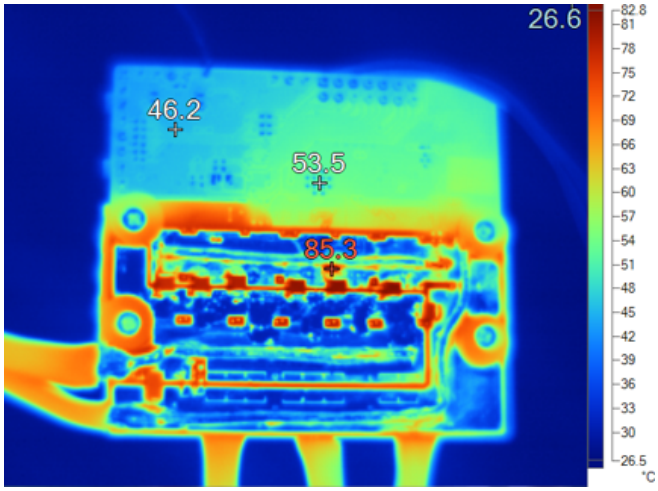

Figure 36. Thermal Image at 18-V DC Input, 42-A_{RMS} Winding Current, 100% Duty Cycle

8.2.2.3 Load Test With Heat Sink and Airflow

Figure 37 shows the motor winding current and winding voltage waveforms at a 18-V DC input and a 48.2-A_{RMS} winding current, with a heat sink and 200LFM airflow. The result is tabulated in Table 8. The testing is done at a 95% duty cycle. Figure 38 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 86.2°C.

Table 8. Load Test Results at 95% Duty Cycle With Heat Sink and Airflow

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	DUTY CYCLE	INPUT POWER (W)
18	56	48.2	95%	1008

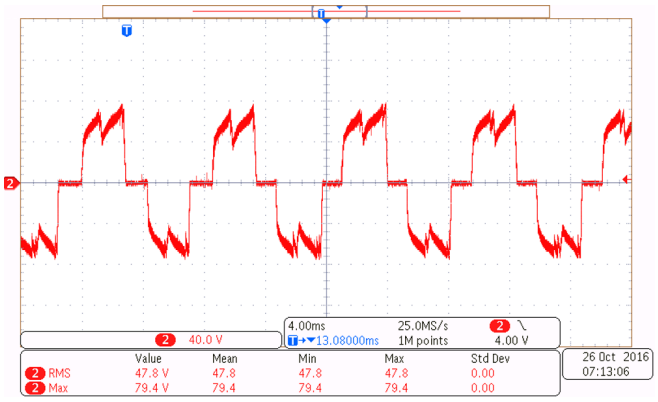

Figure 37. Load Test Results at 18-V DC Input, 48.2-A_{RMS} Winding Current, 95% Duty Cycle

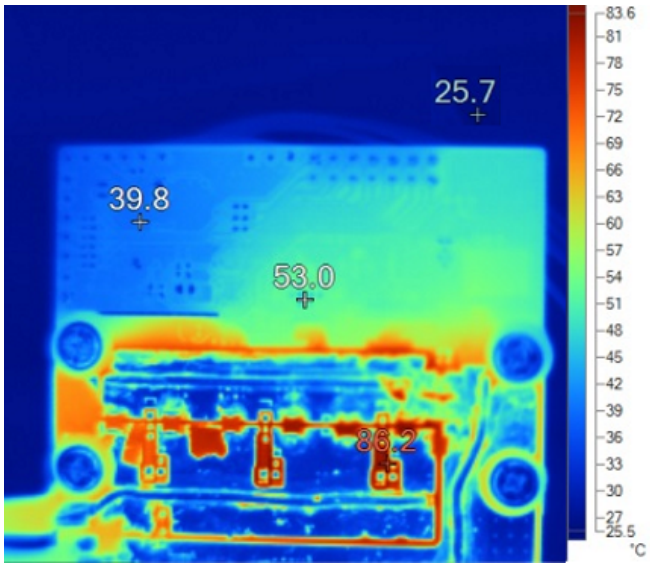

Figure 38. Thermal Image at 18-V DC Input, 48.2-A_{RMS} Winding Current, 95% Duty Cycle

8.2.3 Inverter Efficiency Test

The inverter efficiency is experimentally tested with a load setup as shown in Figure 17. The test results without a heat sink and at 100% duty cycle are tabulated in Table 9. The test results without a heat sink and at 85% duty cycle are tabulated in Table 10. The efficiency curve is shown in Figure 39.

Table 9. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
18.03	6.14	5.22	110.70	109.97	99.33
18.01	10.14	8.47	182.48	181.18	99.29
17.95	15.13	12.63	271.48	269.41	99.24
17.95	20.11	16.85	360.90	358.07	99.21
17.99	25.00	21.04	449.70	445.96	99.17
17.98	29.71	25.11	534.09	529.08	99.06
18.009	34.92	29.75	628.87	622.10	98.92
17.976	39.94	34.39	717.96	709.29	98.79

Table 10. Inverter Efficiency Test Results at 85% Duty Cycle Without Heat Sink

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
18.00	6.11	5.43	109.92	108.94	99.11
17.91	10.03	8.79	179.67	178.05	99.10
17.99	15.12	13.27	272.00	269.46	99.07
18.03	20.20	17.82	364.16	360.26	98.93
17.97	25.07	22.22	450.50	445.22	98.83
18.01	29.64	26.40	533.90	527.15	98.74
18.02	34.96	31.45	621.35	629.98	98.63
18.05	40.04	37.08	712.03	722.72	98.52

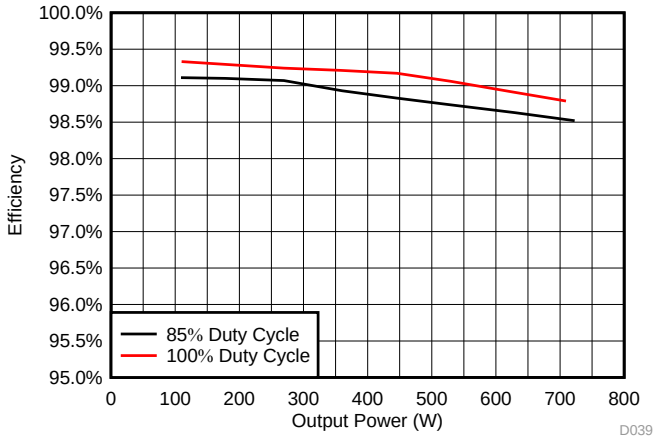

Figure 39. Inverter Efficiency versus Output Power Without Heat Sink

The test results with a heat sink and at 100% duty cycle are tabulated in Table 11. The test results with a heat sink and at 95% duty cycle are tabulated in Table 12. The efficiency curve is shown in Figure 40.

Table 11. Inverter Efficiency Test Results at 100% Duty Cycle With Heat Sink

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
18.04	6.28	5.32	113.19	112.45	99.34
18.08	10.30	8.59	186.15	184.83	99.29
18.01	15.16	12.67	273.14	271.12	99.26
18.02	20.03	16.79	360.98	358.17	99.22
17.97	24.96	21.04	448.59	444.84	99.16
17.96	29.92	25.30	537.37	532.24	99.05
18.05	34.81	29.63	628.20	622.02	99.02
18.07	39.77	33.91	718.45	710.39	98.88
18.04	44.58	38.43	804.01	794.15	98.77
18.02	47.22	40.88	851.05	839.45	98.64

Table 12. Inverter Efficiency Test Results at 95% Duty Cycle With Heat Sink

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
18.00	5.96	5.34	107.27	106.32	99.12
17.93	10.17	8.91	182.39	180.73	99.09
18.03	15.03	13.19	271.09	268.51	99.05
18.02	20.09	17.73	362.08	358.39	98.98
18.01	25.11	22.30	452.02	446.87	98.86
18.00	29.99	26.80	539.68	533.15	98.79
17.97	34.83	31.28	625.93	617.61	98.67
17.97	39.78	35.95	714.77	704.69	98.59
17.96	44.70	40.70	802.92	790.72	98.48

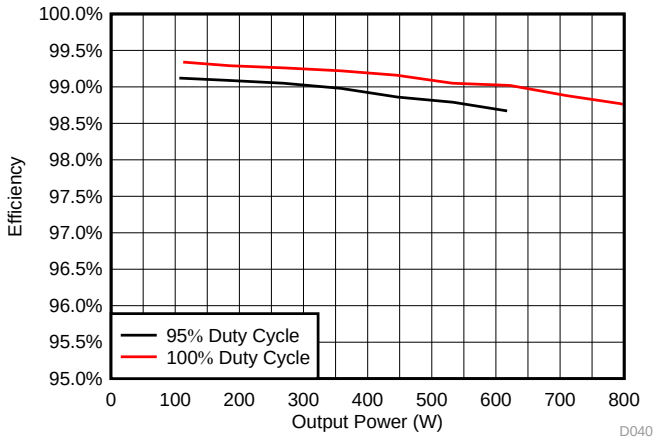

Figure 40. Inverter Efficiency versus Output Power With Heat Sink

8.2.4 Thermal Rise at Different Power Levels

Figure 41 shows the maximum steady state temperature observed on the board after running for 10 minutes at different power levels.

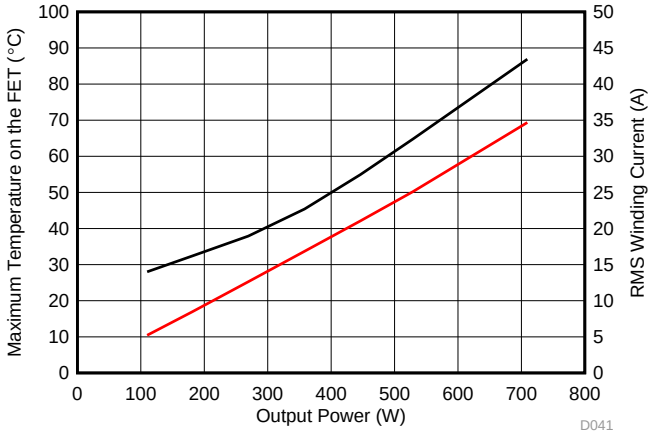

Figure 41. Maximum FET Temperature at Different Power Levels

8.2.5 Inverter Current Sensing by VDS Monitoring

The inverter leg current sensing is done by monitoring the VDS of the low side MOSFETs. Table 13 gives the theoretical and actual amplifier output at a positive and negative current. The board temperature is approximately 30°C. The percentage error is calculated without offset or temperature calibration. The equivalent R_{DS_ON} of 0.5 mΩ (two FETs in parallel) is taken for theoretical amplifier output calculation. Figure 42 to Figure 44 show the winding current and amplifier output waveform.

Table 13. Theoretical and Actual Amplifier Output at Positive and Negative Current

WINDING CURRENT (A)	AMPLIFIER OUTPUT (V)	THEORETICAL AMPLIFIER OUTPUT	% ERROR
24.4	1.86	1.894	–1.79
-22.0	1.42	1.430	–0.70

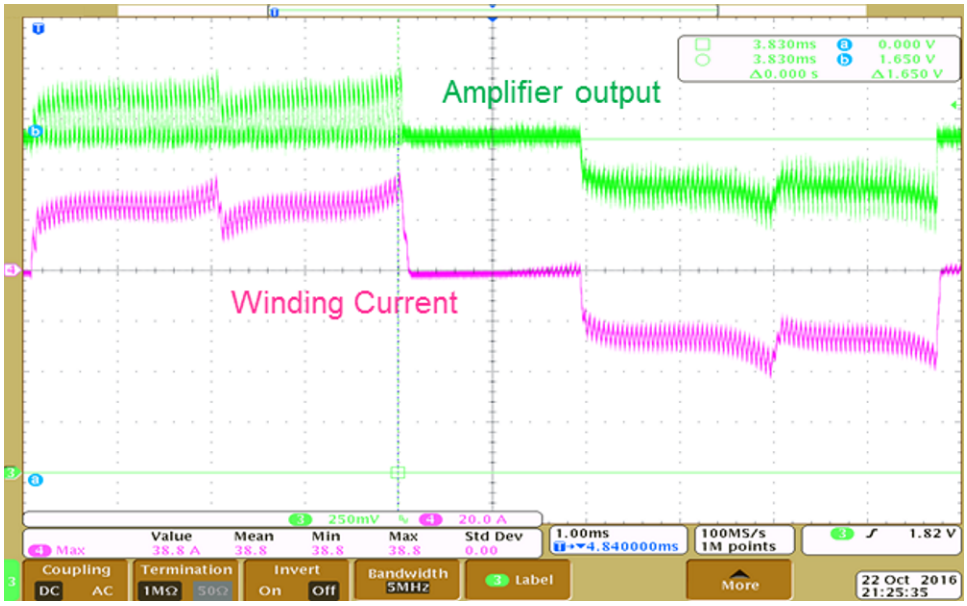

Figure 42. Current Sense Amplifier Output With Winding Current

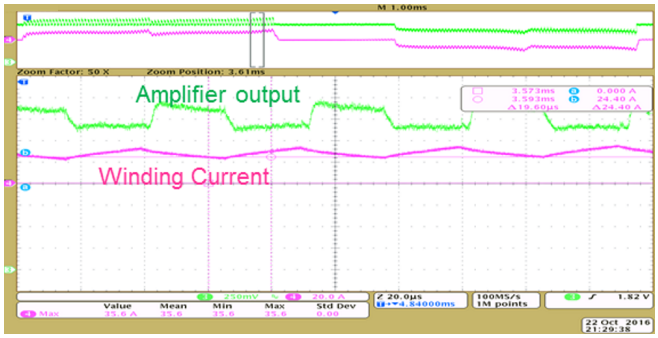

Figure 43. Current Sense Amplifier Output at Positive Winding Current

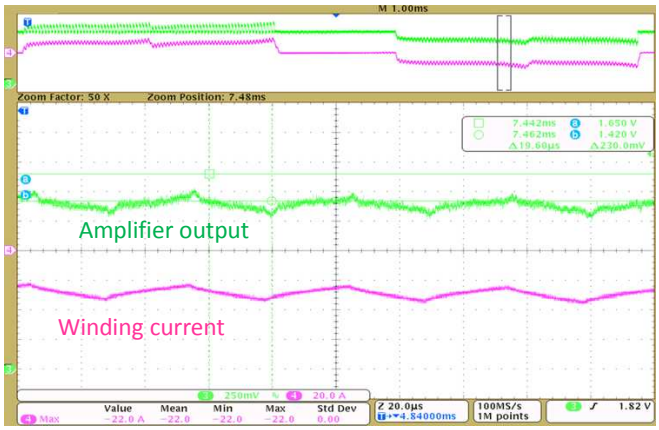

Figure 44. Current Sense Amplifier Output at Negative Winding Current

8.2.6 Overcurrent and Short-Circuit Protection Test

8.2.6.1 Cycle-by-Cycle Stall Current Protection by DRV8323 VDS Sensing

Figure 45 shows the test setup to simulate a stall current when the motor is rotating. S1 is a single-throw, double-pole switch connected between the motor terminals. This is used to create a motor winding to winding short.

Before S1 is closed, the motor was rotating at a steady speed. Figure 46 shows the waveforms obtained when the switch S1 is closed. When S1 is closed, S1 carries the short-circuit current. During this condition the motor stops, which causes the Hall state to continue at the current commutation state; therefore, the controller continues to generate the PWM corresponding to this commutation state.

The VDS reference for stall current limit is set to 0.1 V.

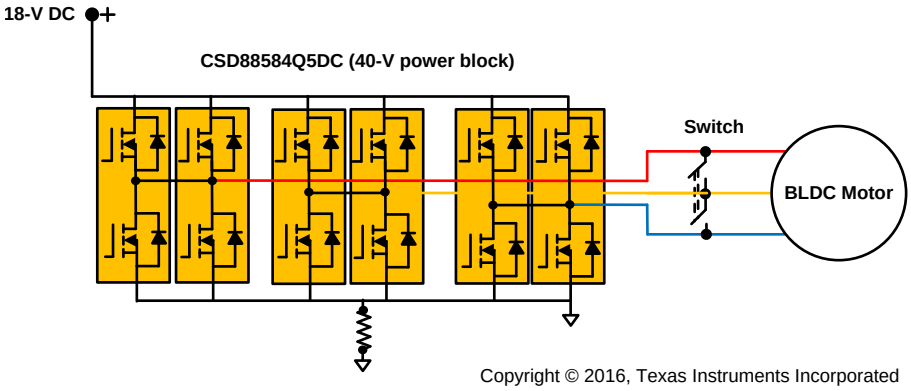

Figure 45. Test Setup to Simulate Stall Current When Motor is Running

With the VDS reference of 0.1 V and considering a 1-mΩ R_{DS_ON} / FET and with two FETs in parallel, set current limit = 0.1 / 0.0005 = 200 A

Figure 47 shows a zoomed view of Figure 46, the cycle-by-cycle overcurrent protection acted at around 178 A. Once the current hits 178 A, the PWM shuts off immediately, and the response time is less than 1 µs.

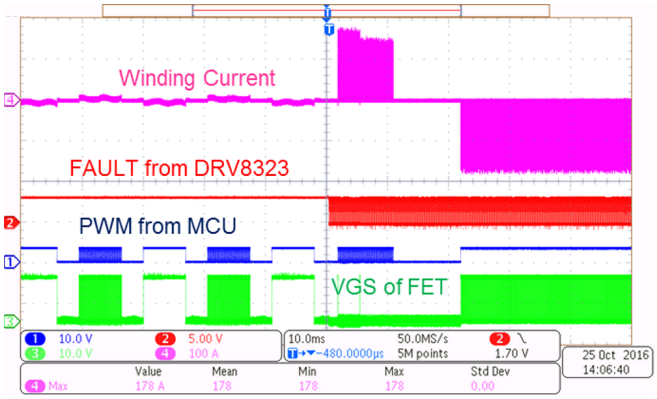

Figure 46. Cycle-by-Cycle Overcurrent Protection With Motor Stall

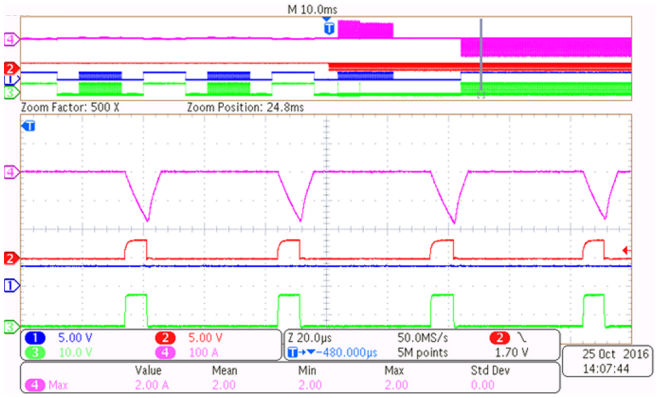

Figure 47. Zoomed View of Cycle-by-Cycle Overcurrent Protection With Motor Stall

Figure 48 shows the test setup to simulate a short circuit at the inverter output.

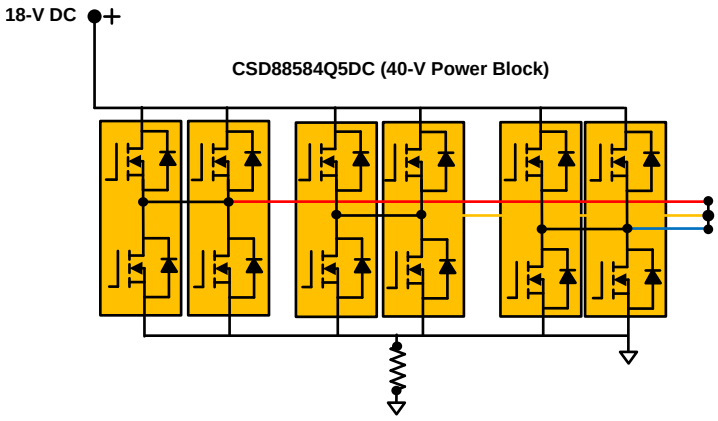

Figure 48. Test Setup to Simulate Inverter Short Circuit

The VDS reference for short circuit is set to 0.1 V. Figure 49 shows the overcurrent protection acted at around 186 A. Once the current hits 186 A, the PWM shuts off immediately and the response time is less than 1 µs.

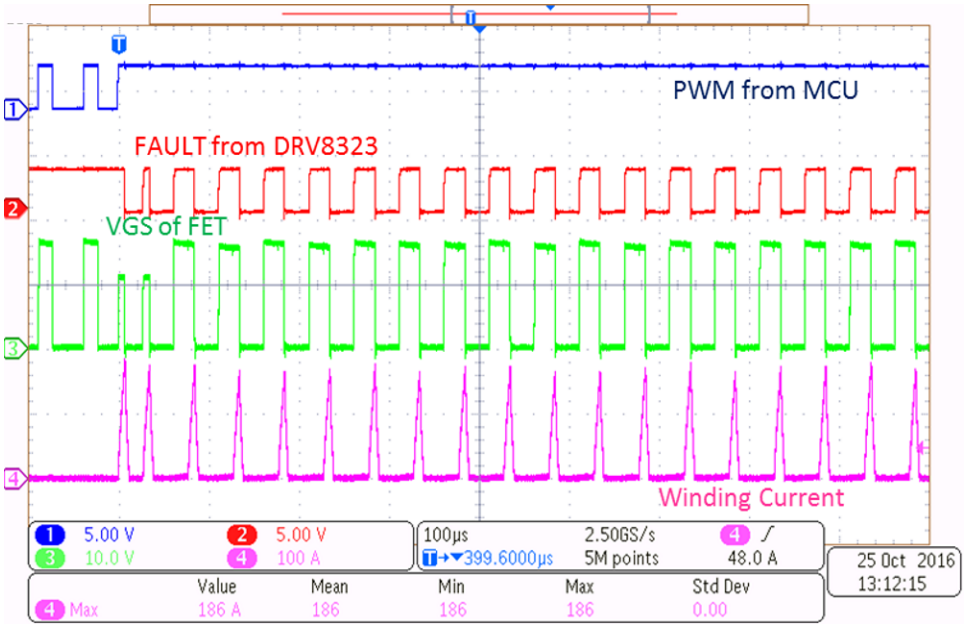

Figure 49. Cycle-by-cycle Overcurrent Protection With Inverter Output Shorted

8.2.6.2 Stall Current Latch Protection by DRV8323 VDS Sensing

The same test setup in Figure 45 is used for the stall current protection. The VDS reference used is 0.1 by writing in the register of the DRV8323. The latch protection acted at 143 A.

Figure 50 shows the test results with latch protection by VDS sensing. When a VDS overcurrent event occurs, the device will pull all gate drive outputs low to put all six external MOSFETs into high impedance mode. The fault will be reported on the nFAULT pin with the specific MOSFET in which the overcurrent event was detected is reported through the SPI status registers. Figure 51 shows the zoomed view of Figure 50.

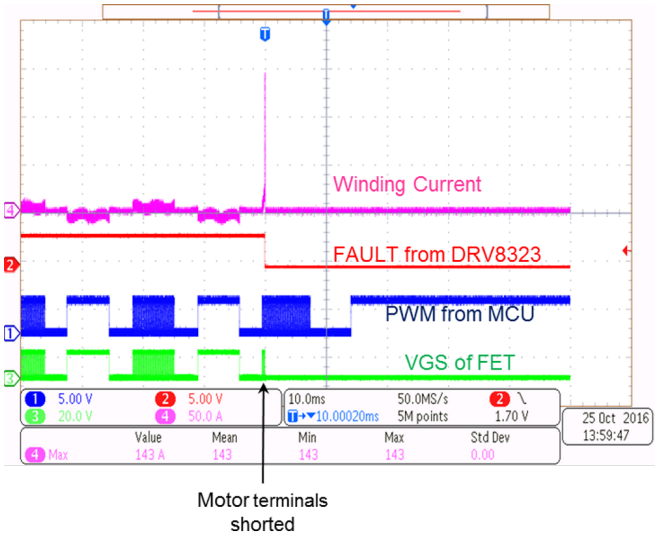

Figure 50. Overcurrent Latch Protection With Motor Stall by VDS Sensing

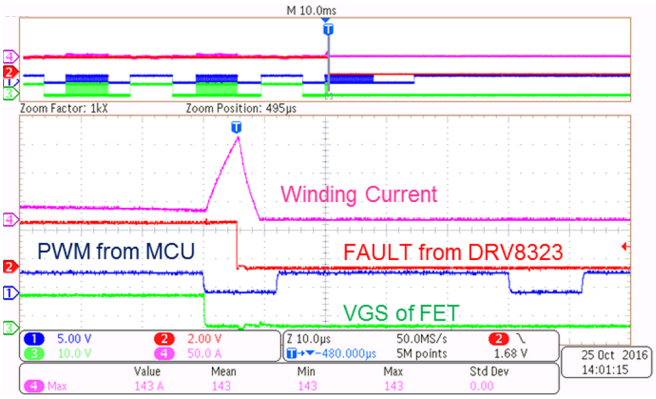

Figure 51. Zoomed View of Overcurrent Latch Protection With Motor Stall by VDS Sensing

Figure 52 shows the test results of latch protection, when the inverter output is shorted. The same test setup in Figure 48 is used for the short-circuit simulation. The VDS reference used is 0.1 V. The latch protection acted at 144 A.

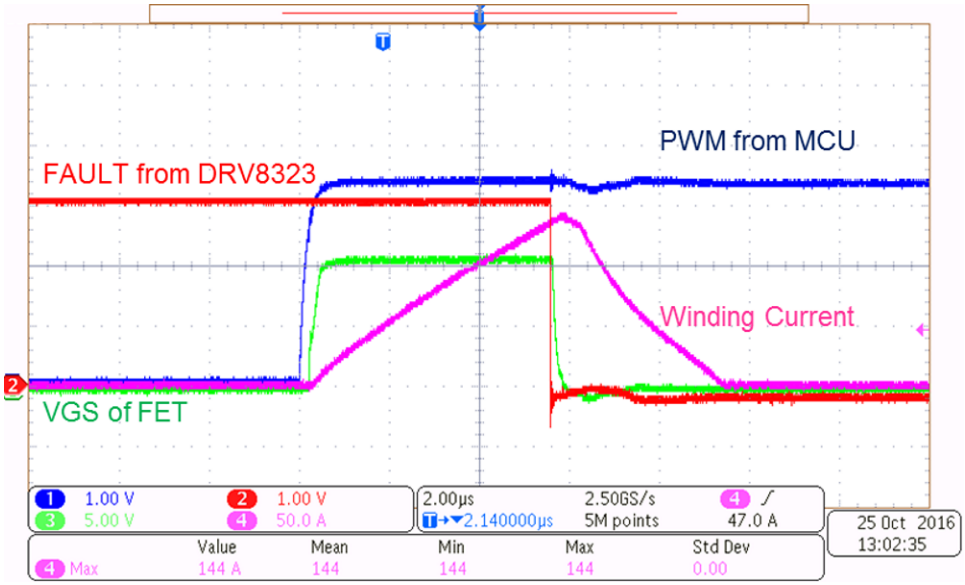

Figure 52. Overcurrent Latch Protection With Inverter Output Shorted

8.2.7 Testing for Peak Current Capability

Figure 53 shows the winding current of 120 A when the motor is stalled for 3 seconds. Figure 54 shows the thermal image of the board after 3 seconds.

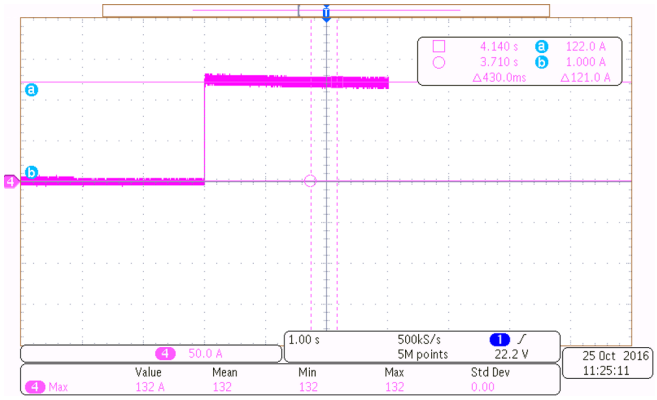

Figure 53. 120-A Peak Current in Motor Winding During Motor Stall

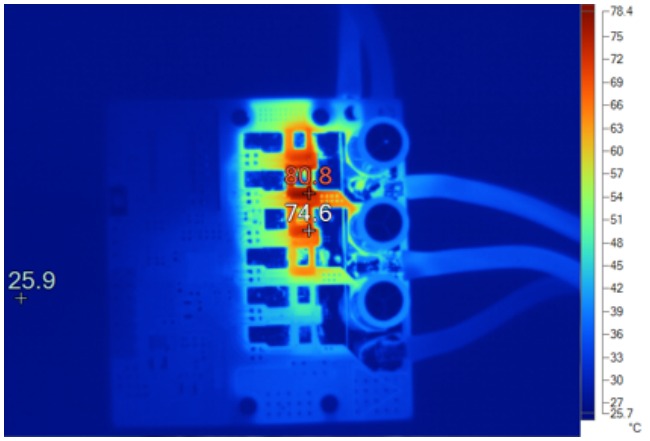

Figure 54. Thermal Image of Board After 3 Seconds With 120-A Peak Current in Motor Winding

Figure 55 shows the peak winding current of 180 A when the motor is stalled for more than 1 second. The average motor current is approximately 160 A for this duration. Figure 56 shows the thermal image of the board after 1 second.

The high peak current capability ensures that in power tool applications, the power stage aids the motor to deliver high peak torque. If the stall current continues to be high, over temperature or blocked rotor protection will act to shut off the system.

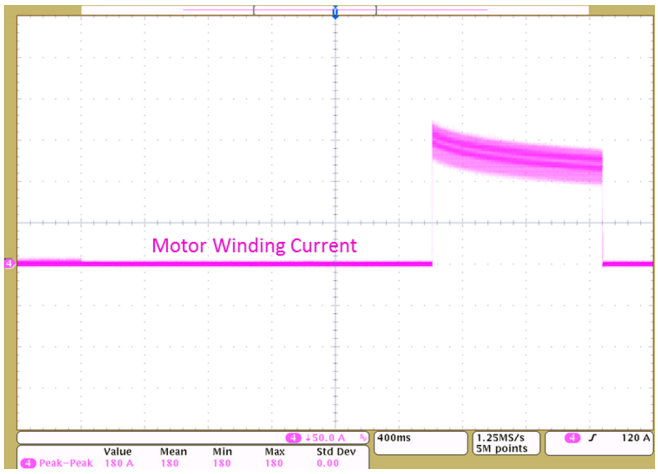

Figure 55. 160-A Peak Current in Motor Winding During Motor Stall

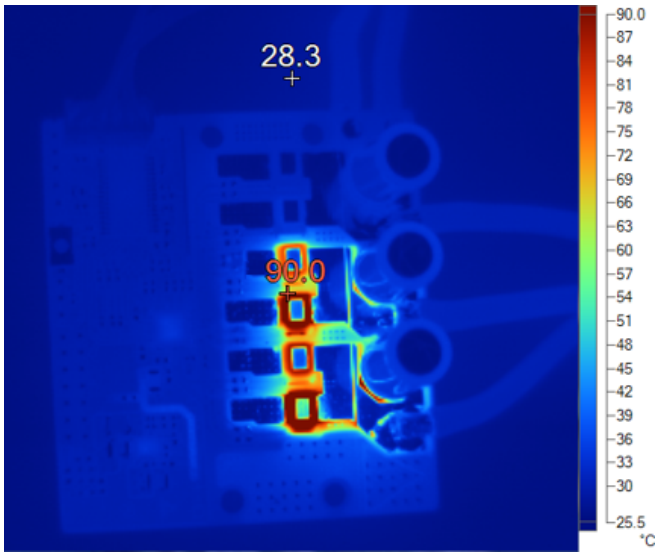

Figure 56. Thermal Image of Board After 1 Second With 160-A Peak Current in Motor Winding

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00774.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00774.

9.3 PCB Layout Recommendations

Use the following layout recommendations when designing the PCB:

- Connect the DRV8323 DVDD 1-μF bypass capacitors directly to the adjacent GND pin to minimize loop impedance for the bypass capacitor.
- Place the PVDD capacitor and charge pump capacitor directly next to the DRV8323.
- Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the DRV8323 GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8323 GL_X to the power MOSFET and returns through GND.
- Maintain equal gate path length to both the paralleled FETs.
- In the reference design, the PCB is a four-layer layout with 2-Oz (70-micron) copper thickness in every layer. The power tracks are made wide to carry a high current. The tracks are repeated in different layers and are connected by arrays of stitching vias.
- A GND star point is defined in the PCB from where the GND path for the DRV8323 and other signal circuits in the board is tapped.
- For better thermal dissipation from the MOSFET to the PCB, increase the copper area around the MOSFET pad as much as possible. Use arrays of vias under the drain pad of the MOSFET, which will spread heat better to the bottom surface copper area.

9.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00774.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00774.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00774.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00774.

10 Software Files

To download the software files, see the design files at TIDA-00774.

11 Related Documentation

1. Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers*, Application Report (SLVA714)
2. Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430*, Application Report (SLAA503)
3. Texas Instruments, *48-VDC Battery Powered Inverter Power Stage Reference Design for 5-kW Forklift AC Traction Motor*, TIDA-00364 Design Guide (TIDUCB6)

11.1 Trademarks

All trademarks are the property of their respective owners.

12 Terminology

SPI— Serial peripheral interface

PWM— Pulse width modulation

BLDC— Brushless DC motor

MCU— Microcontroller unit

FETs, MOSFETs—Metal-oxide-semiconductor field-effect transistor

ESD— Electrostatic discharge

RPM— Rotation per minute

RMS— Root mean square

13 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics and analog and mixed signal designs. He has system level product design experience in permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

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