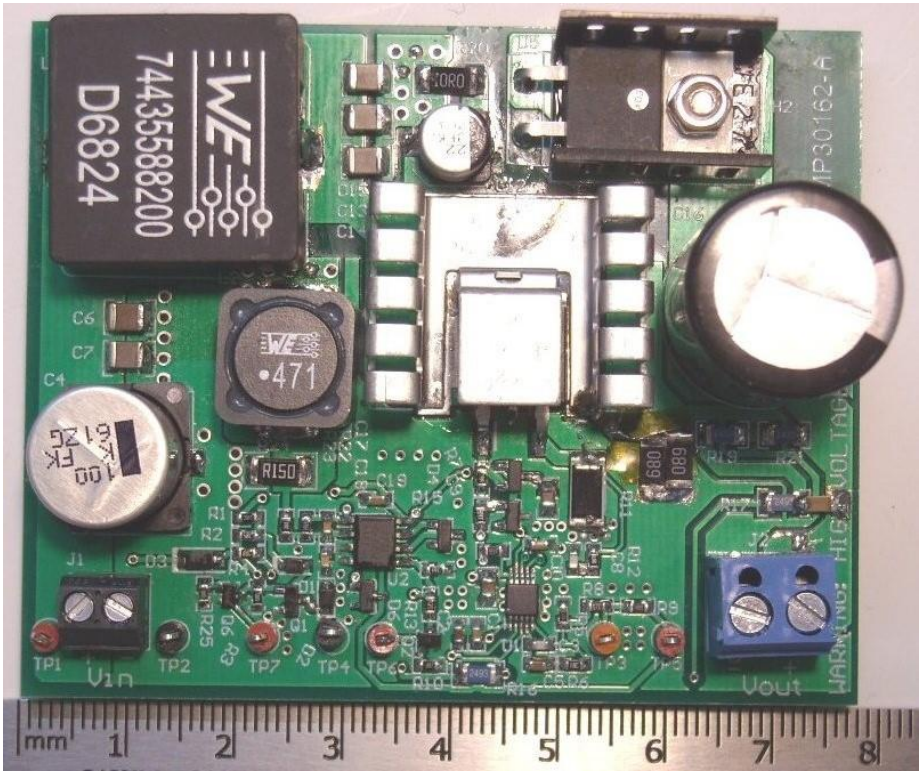
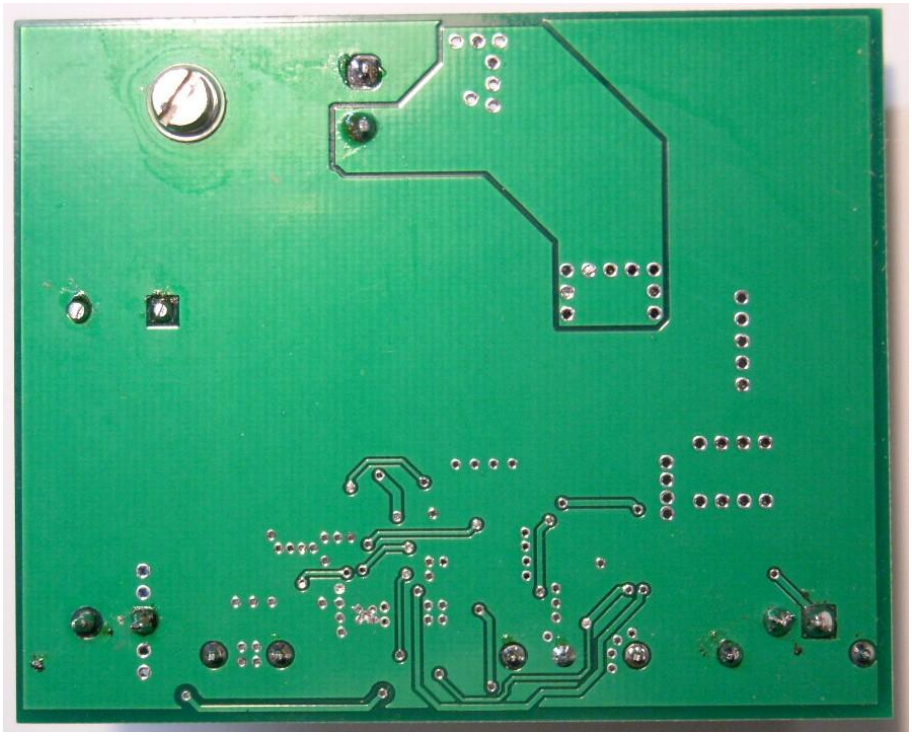
1 Photo of the prototype (62.23mm x 76.83mm).

The Reference design PMP30162 Revision B has been built on PMP30162 Revision A PCB.



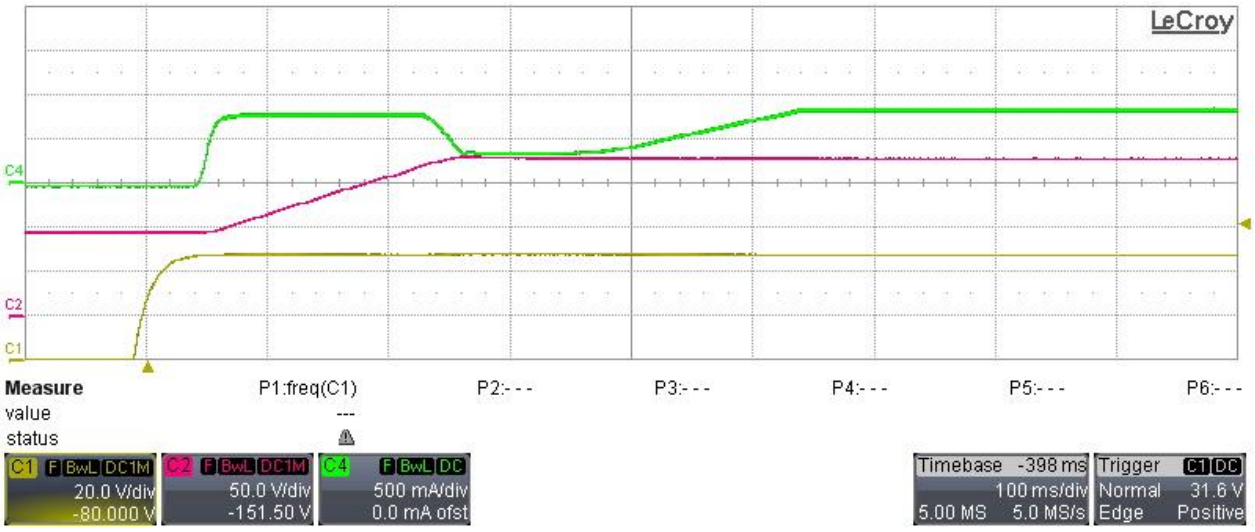


2 Startup

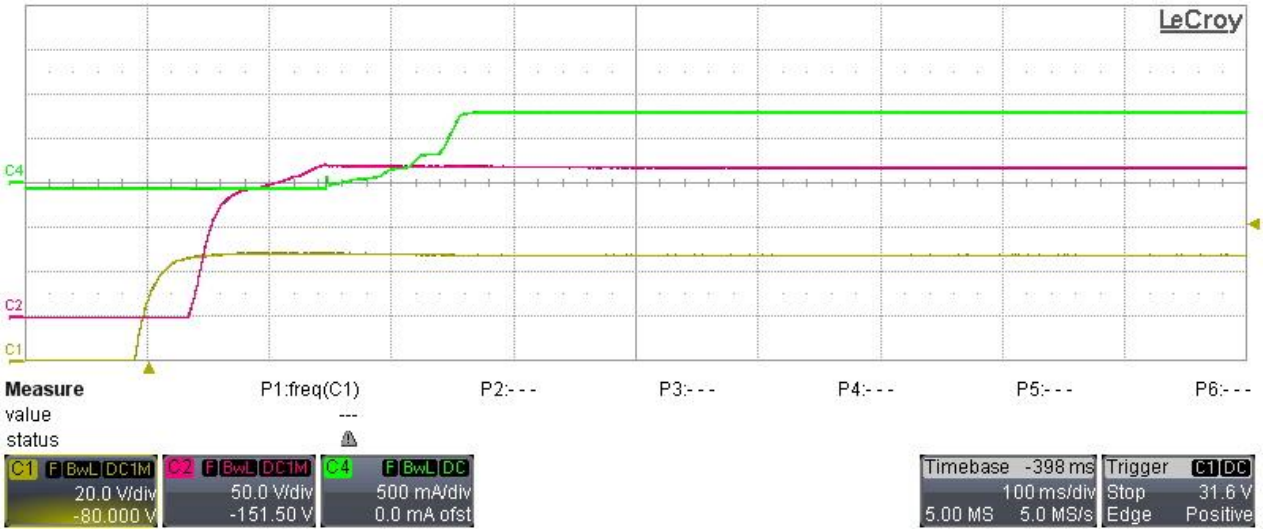
The input voltage, output current and voltage behavior in different load conditions is shown in the images below.

Ch.1: Input voltage (20V/div, 100ms/div, 20MHz BWL)
Ch.2: Output voltage (50V/div, 20MHz BWL)
Ch.4: Output current (500mA/div, 20MHz BWL)
Vout set to 180V by applying 5V to TP6.
A 2000 uF capacitor has been connected to output terminals, left open
Vin = 48V

Same condition as above but with a constant-voltage electronic load, se to 180V:

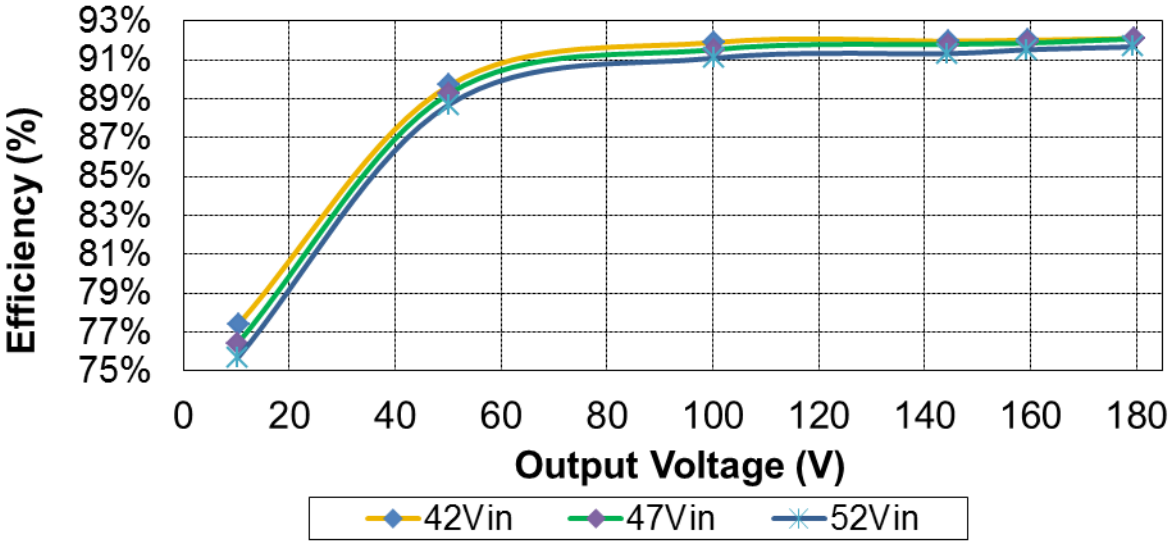


Ch.1: Input voltage (20V/div, 100ms/div, 20MHz BWL)
Ch.2: Output voltage (50V/div, 20MHz BWL)
Ch.4: Output current (500mA/div, 20MHz BWL)
Vout set to 180V by applying 5V to TP6.
No further capacitor connected to output terminals
Constant-voltage electronic load, se to 170V
Vin = 48V



3 Efficiency

The efficiency data, versus input and output voltage are shown in the tables and graph below. The load (constant-voltage electronic load) has been varied in order to get different Vout (since the converter is a constant current generator, set to deliver 420V (Q3 ON)) down to short circuit. The input voltage has been set to 47V ± 10%.



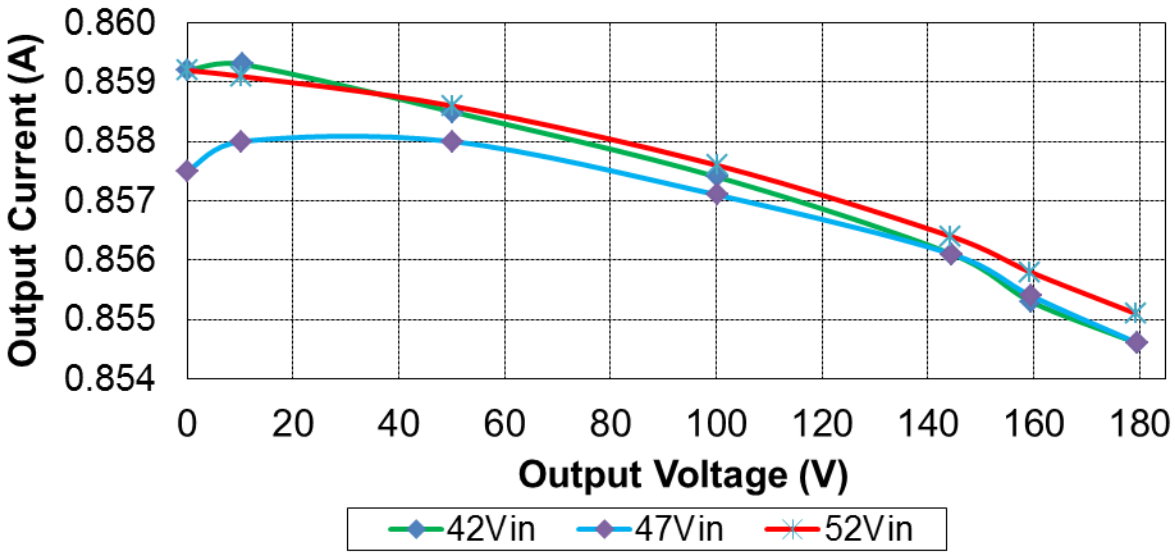
Vin (V)	Iin(A)	Pin (W)	Vout (V)	Iout(A)	Pout (W)	Efficiency (%)
42.25	0.0601	2.54	0	0.8592	0	0%
42.18	0.2751	11.60	10.453	0.8593	8.98	77.4%
42.09	1.1436	48.13	50.29	0.8585	43.17	89.7%
42.06	2.225	93.58	100.31	0.8574	86.01	91.9%
42.05	3.201	134.60	144.6	0.8561	123.79	92.0%
42.14	3.518	148.25	159.5	0.8553	136.42	92.0%
42.03	3.9650	166.649	179.6	0.8546	153.49	92.1%
42.01	0.0457	1.920	180.8	0	0	0%

Vin (V)	Iin(A)	Pin (W)	Vout (V)	Iout(A)	Pout (W)	Efficiency (%)
47.04	0.0535	2.52	0	0.8575	0	0%
47.00	0.2448	11.51	10.246	0.8580	8.79	76.4%
47.00	1.0259	48.22	50.16	0.8580	43.04	89.3%
47.02	1.995	93.80	100.18	0.8571	85.86	91.5%
47.00	2.869	134.84	144.6	0.8561	123.79	91.8%
47.04	3.157	148.51	159.5	0.8554	136.44	91.9%
47.04	3.5450	166.757	179.7	0.8546	153.57	92.1%
47.04	0.0473	2.225	180.8	0	0	0%

Vin (V)	Iin(A)	Pin (W)	Vout (V)	Iout(A)	Pout (W)	Efficiency (%)
52.06	0.0495	2.58	0	0.8592	0	0%
52.01	0.2229	11.59	10.207	0.8591	8.77	75.6%
52.05	0.9321	48.52	50.12	0.8586	43.03	88.7%
52.04	1.812	94.30	100.16	0.8576	85.90	91.1%
52.00	2.604	135.41	144.4	0.8564	123.66	91.3%
52.15	2.858	149.04	159.4	0.8558	136.41	91.5%
52.10	3.2100	167.241	179.3	0.8551	153.32	91.7%
52.00	0.0407	2.116	180.9	0	0	0%

4 Output Current Regulation

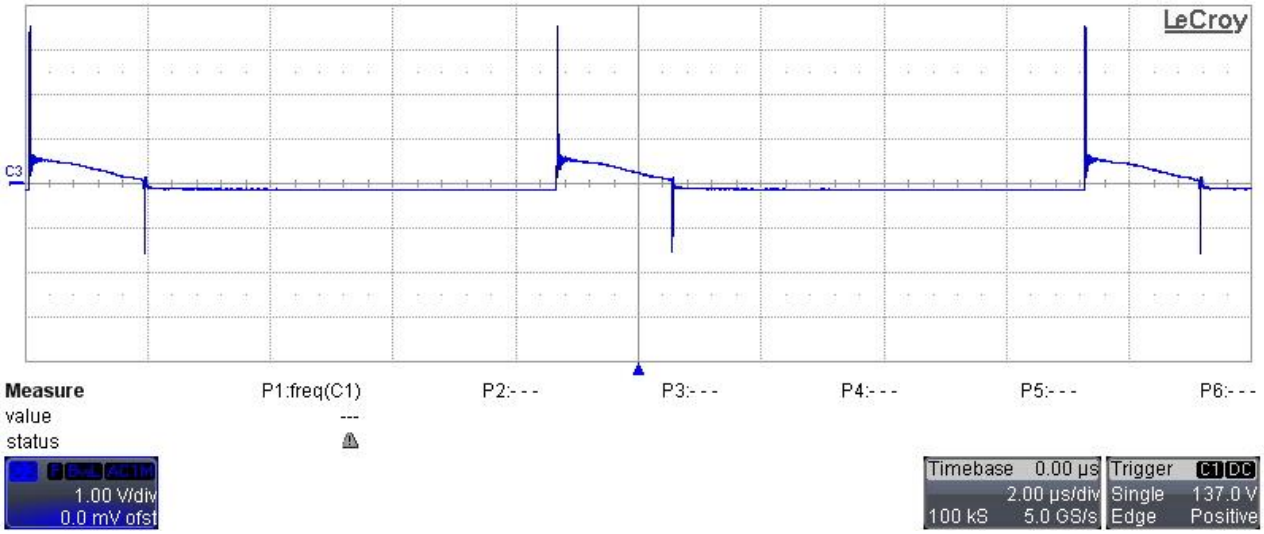
The output current variation versus output voltage, for different input voltages, is plotted below.



5 Output Ripple Voltage

The output ripple voltage has been measured by supplying the converter at 52V while running in constant current limit and set to deliver 180V.

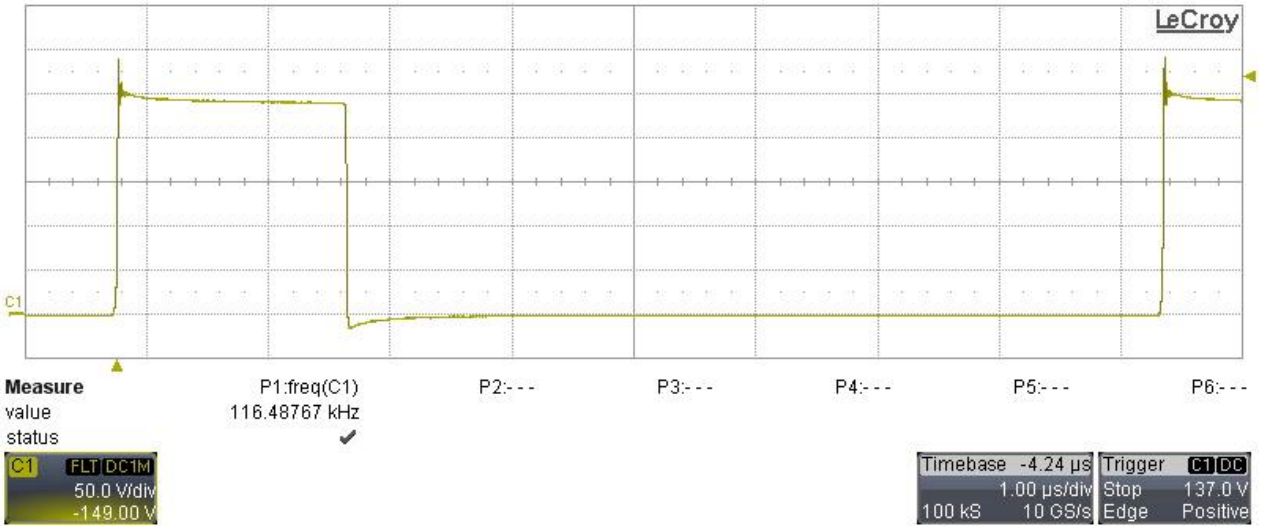
Ch.3: Output ripple voltage (1V/div, AC coupling, 2usec/div, 20MHz BWL)



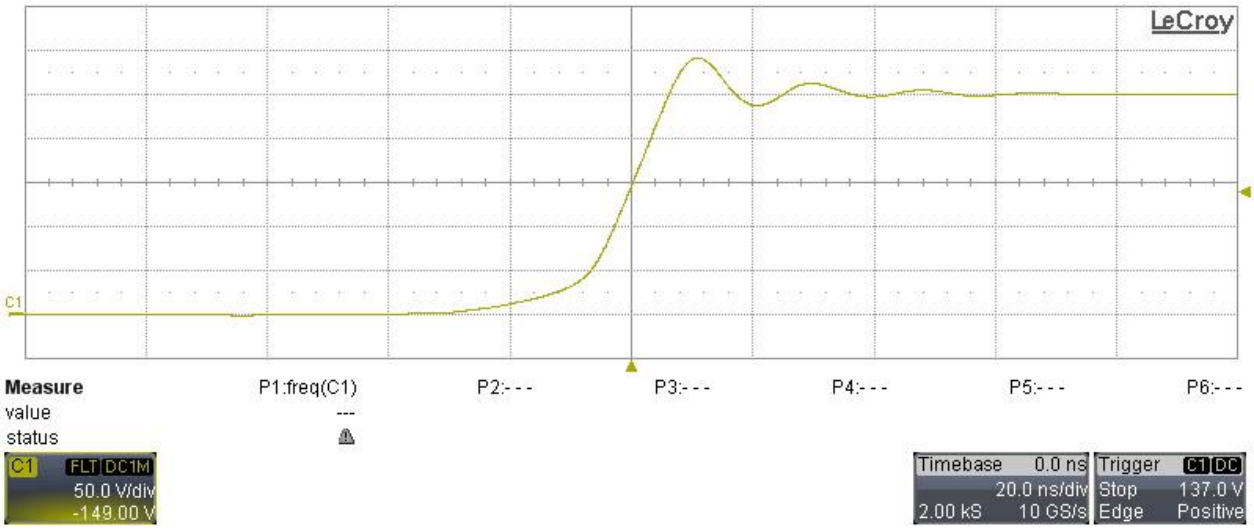
6 Switch Node

The image below shows the drain of Q5 taken at Vin = 52.7V and Vout = 180V, while delivering 855mA.

Ch.1: Q5-Drain voltage (50V/div, 1us/div, no BWL)



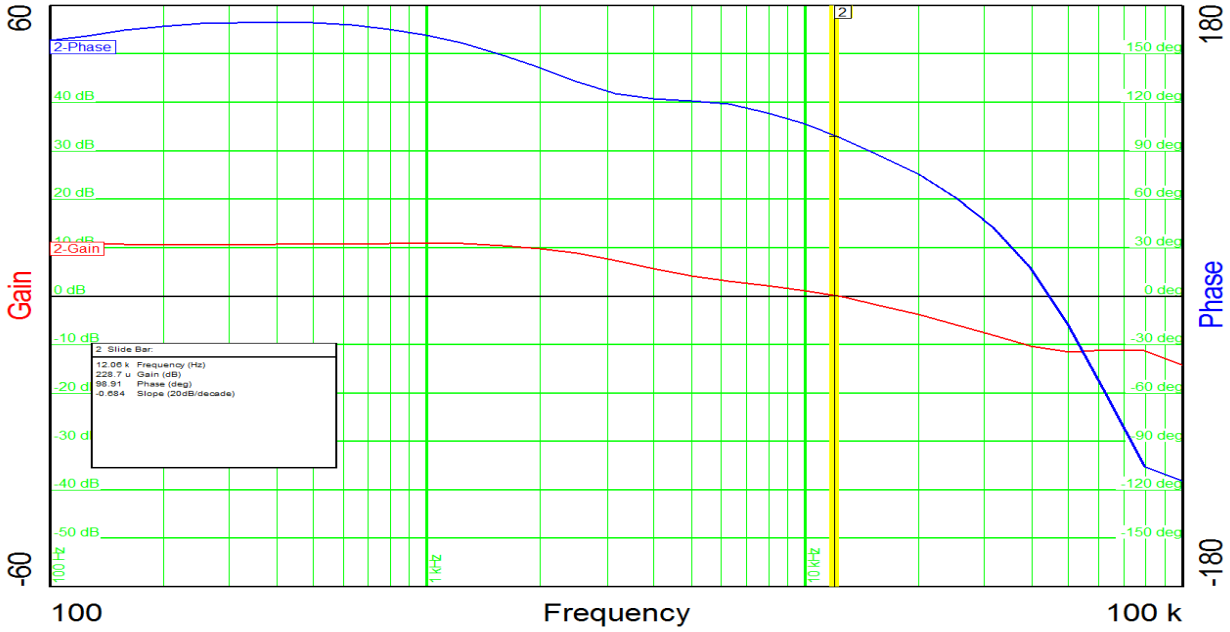
Ch.1: → same waveform as above @ 20 nsec/div (no BWL)



7 Feedback Loop Analysis

The image below shows the open loop gain and phase margin of the constant current loop. The board has been supplied at Vin = 48V and the load was a constant-voltage electronic load, set to 160V (to avoid any interference from voltage loop).

Crossover frequency: 12.06 KHz
Phase margin: 98.91 deg.
Gain margin: 10.95 dB



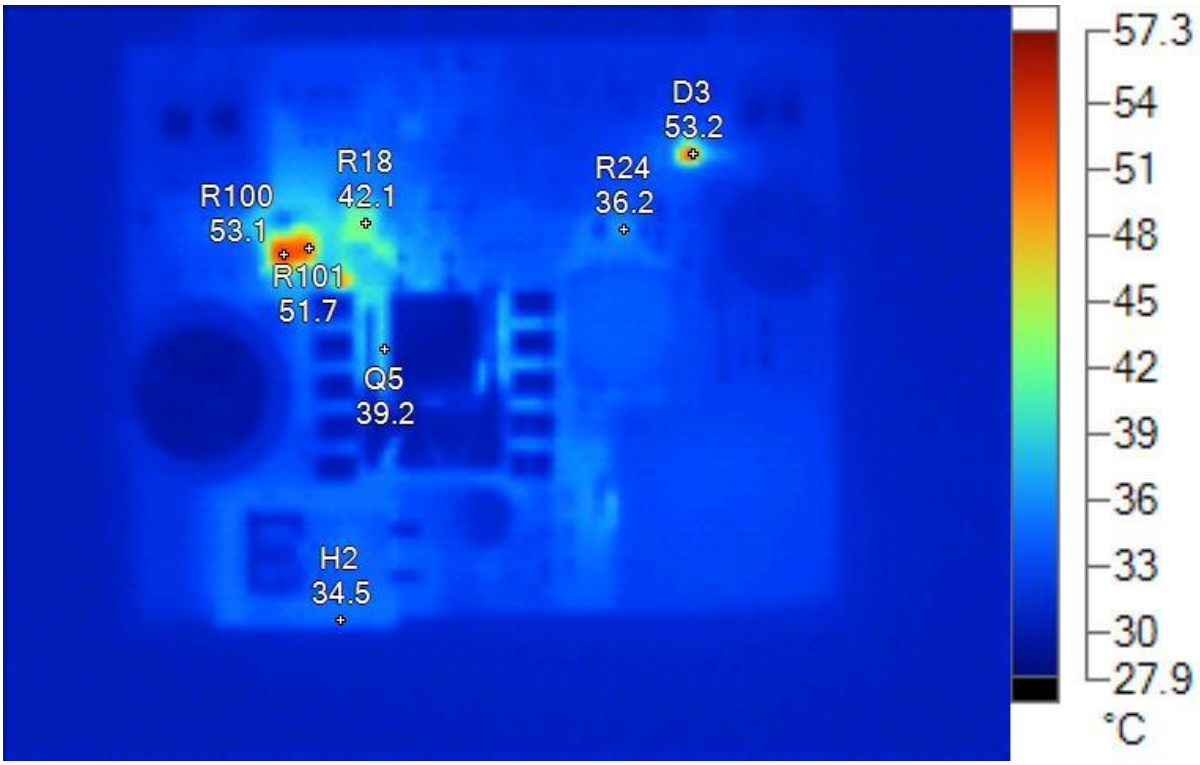
8 Thermal Analysis

During the thermal analysis, the converter has been placed horizontally on the bench in still air conditions, while supplied at 42V (worst case) and delivering 180V @ 855mA.

The thermal image has been taken after 12 seconds (minimum recharging time on the final application). Ta = 23C.

Main Image Markers

Name	Temperature	Emissivity	Background
R100	53.1°C	0.95	23.0°C
R101	51.7°C	0.95	23.0°C
D3	53.2°C	0.95	23.0°C
R24	36.2°C	0.95	23.0°C
H2	34.5°C	0.95	23.0°C
Q5	39.2°C	0.95	23.0°C
R18	42.1°C	0.95	23.0°C



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