Design Guide: TIDA-00299
EtherCAT® Slave and Multi-Protocol Industrial Ethernet Reference Design

Description

The TIDA-00299 implements a cost-optimized high EMC immunity EtherCAT® slave (dual ports) with SPI interface to the application processor. The hardware design is capable of supporting multi-protocol industrial Ethernet and field busses using the AMIC110 industrial communications processor. The design has a 5-V input. A single PMIC generates all rails required onboard. The EtherCAT slave stack can run on the AMIC110 or on the application processor using a serial peripheral interface (SPI). With a hardware switch, the AMIC110 can be configured to boot the EtherCAT slave firmware from SPI flash or to boot from application processor through SPI. The design has been tested for IEC61800-3 EMC immunity with a standard industrial PLC running the ethercat master. A JTAG interface accelerates custom firmware development.

Resources

TIDA-00299	Design Folder
AMIC110	Product Folder
DP83822H	Product Folder
TPS650250	Product Folder
TMDXICE110	Tool Folder

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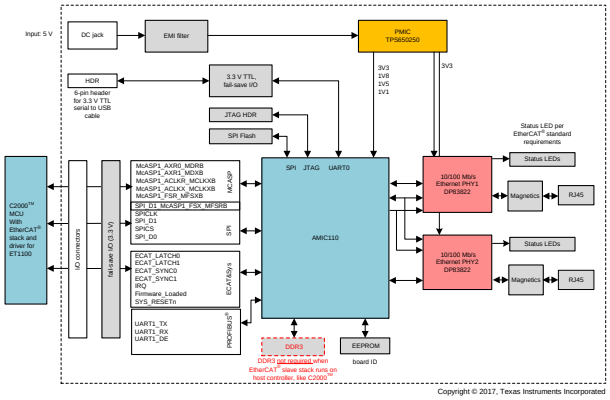
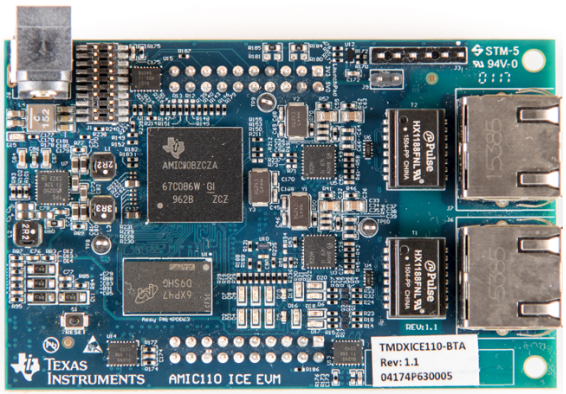
Features

- Passes EtherCAT slave conformance testing (CTT)
- Software-programmable multi-protocol industrial Ethernet and field bus support using AMIC110 communication processor
- Exceeds IEC61800-3 EMC immunity requirements running EtherCAT on both ports:
  - +/- 6-kV ESD CD per IEC 61000-4-2
  - +/- 4-kV EFT per IEC 61000-4-4 at criterion A
  - +/- 2-kV surge per IEC 61000-4-5 at criterion A
  - IEC61000-4-6 conducted RF at criterion A
  - CISPR 11 / EN55011 class A
- Low-latency, robust 10- or 100-Mbit Ethernet PHYs DP83822
- Cost-optimized, easy power management using single PMIC to supply entire board from a preregulated 5-V supply
- Operation over industrial temperature range
  - Total board power consumption less than 1.25 W in typical use case; no heatsink required for operation up to 85°C ambient

Applications

- Industrial motor drives
- Factory automation & control





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1 System Description

When building a communication module for Industrial Ethernet there are two major points to consider.

- Which or how many protocols of Industrial Ethernet is running?
- How robust is the communication of the system to EMC noise?

1.1 Industrial Ethernet Communication

Ethernet is becoming ubiquitous and cost effective, with common physical links and increased speed. As such, many industrial communication protocols are moving to Ethernet-based solutions. Ethernet communications with TCP/IP typically are nondeterministic, and reaction time is often around 100 ms. Industrial Ethernet protocols use a modified Media Access Control (MAC) layer to achieve very low latency and deterministic responses. Ethernet also enables a flexible network topology and a flexible number of nodes in the system.

The following list shows the typically used industrial Ethernet protocols:

- EtherCAT®
- PROFINET
- Sercos III
- EtherNet/IP
- POWERLINK
- Modbus /TCP
- CC-Link

To enable industrial equipment manufacturers with an economic and flexible means to implement a variety of industrial communication protocols, special cores are needed to provides a more cost-effective, flexible and future-proof solution for industrial communications supporting multi-protocols easily. For more details on this seeSection 2.3.1.

With the deterministic side of the discussion solved, a second topic to consider for this interface is to ensure it is robust against EMC noise. The trend is for more precise and robust industrial communication, adding safety features as well as predictive maintenance for lesser or complete avoidance of shutdown time of the full system. For more information on EMC immunity standards see Section 1.2.

In this design guide, the industrial protocol used is EtherCAT®. This is a software option other protocols can be supported changing software.

1.2 IEC61800-3 EMC Immunity Standard for Industrial Drives

When building an industrial drive, the customer needs to pass the compliance test of the IEC61800-3 EMC standards.

For more details on the IEC61800-3 standard see the Know your electromagnetic compatibility requirements for designing industrial drives blog or see the Why EMI/EMC and isolation standards for Motor Drives video.

The blog shows that there are several interfaces which need to be tested.

For EMC immunity, the design has been tested according to IEC61800-3 and IEC61000-6-2 for ESD, EFT, and Surge with reference to standards IEC61000-4-2, IEC61000-4-4, IEC61000-4-5, IEC61000-4-6 respectively.

Table 1. IEC618000-3 and IEC61000-6-2 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class

REQUIREMENTS				
PORT	**PHENOMENON**	**BASIC STANDARD**	**LEVEL**	**PERFORMANCE (ACCEPTANCE) CRITERION**
Enclosure ports	ESD	IEC61000-4-2	+/-4kV CD or 8kV AD, if CD not possible	B

Table 1. IEC618000-3 and IEC61000-6-2 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class (continued)

REQUIREMENTS				
PORT	**PHENOMENON**	**BASIC STANDARD**	**LEVEL**	**PERFORMANCE (ACCEPTANCE) CRITERION**
Ports for control lines and DC auxiliary supplies <60V	Fast transient Burst (EFT)	IEC61000-4-4	+/-2kV/5 kHz or 100kHz, capacitive clamp	B
	Surge 1,2/50us, 8/20us	IEC61000-4-5	+/-1kV. Since shielded cable >20m, direct coupling to shield (2Ohm/500A)	B
	Conducted RF	IEC61000-4-6	0.15-80MHz,10V/m, 80% AM (1kHz)	A

The performance (acceptance) criterion is defined as follows:

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

Depending on the country where the drive is used, different EMC standards apply. In this reference design, the designs are tested according to the IEC standard.

Table 2. IEC618000-3 and IEC61000-6-2 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class

REQUIREMENTS		
Phenomenon	Basic standard	Category 2 electric field strength component quasi-peak dB(uV/m)
EMI	EN55011/CISPR 11 class A	40 (30-230MHz) and 47 (230-1000MHz)

Depending on the country where the drive is used, different EMC standards apply. In this reference design, the designs are tested according to the IEC standard

1.3 Introduction to EtherCAT®

EtherCAT stands for Ethernet for Control Automation Technology. EtherCAT is a real-time industrial Ethernet field bus protocol originally developed by Beckhoff Automation GmbH and publicly introduced in 2003.

EtherCAT is an open technology, which is standardized by the International Electrotechnical Commission (IEC). The technology is supported and powered by the EtherCAT Technology Group (ETG), an international community of users and vendors.

The EtherCAT protocol is described in the IEC standard IEC61158. This standard is built to work with both hard and soft real-time requirements in automation technology and many other applications.

EtherCAT's key feature during development was the short cycle times (≤ 100 µs) with low jitter for accurate synchronization (≤ 1 µs). For more in depth information on EtherCAT, see *EtherCAT Technical Introduction and Overview*.

1.3.1 Typical EtherCAT® Network

EtherCAT has exactly one master node per network. The master can be implemented on a standard Ethernet media access controller (MAC) without an additional communication processor. This MAC has to provide a full-duplex 100 Mbit/s interface. A standard PC with the necessary software can act as an EtherCAT master. Figure 1 shows the scheme of a typical EtherCAT network.

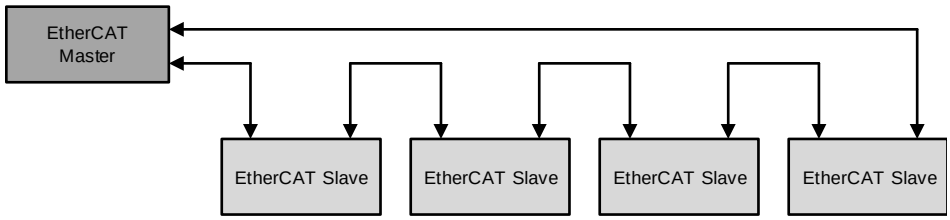

Figure 1. Typical EtherCAT® Network

The example shown in Figure 1 is a daisy-chain network topology; EtherCAT can also be implemented in a line, tree, or star configuration.

Contrary to the operation of standard Ethernet, the EtherCAT slave processes the EtherCAT frames on the fly. This means that the transmission of the new EtherCAT packet start as soon as possible before completely receiving the incoming data packet. This transmission is only possible with a hardware-based implementation and is required to ensure deterministic network performance.

This design focuses on EtherCAT slave hardware and software requirements.

1.3.2 Components of an EtherCAT® Slave

Each EtherCAT slave controller (ESC) has three main components: interface to the physical layer, EtherCAT MAC layer, and the application layer. Figure 2 shows these components.

Physical layer:

The physical layer uses 100BASE-TX copper, 100BASE-FX optical fiber, or E-bus (Ethernet-Klemmenbus) based on LVDS signaling as a transmit medium. The signals are interfaced from the medium to the appliance through the physical layer circuit, which is known as PHY. In the Ethernet standard, the PHY uses the so called media-independent interface (MII) or its derivatives to connect to the MAC.

EtherCAT MAC layer:

In the IEEE 802 reference model of computer networking, the MAC layer is an interface between the logical link control (LLC) sublayer and the network's PHY. The MAC layer is implemented according to the EtherCAT standard specification IEC61158. This layer is typically also known as the EtherCAT slave controller. The implementation has to support the standard TCP-IP and UDP-IP protocols besides handling the EtherCAT data frames. Received data is passed to the application layer, and also sent to the second port to transmit toward the next node to achieve lowest latency.

EtherCAT application layer:

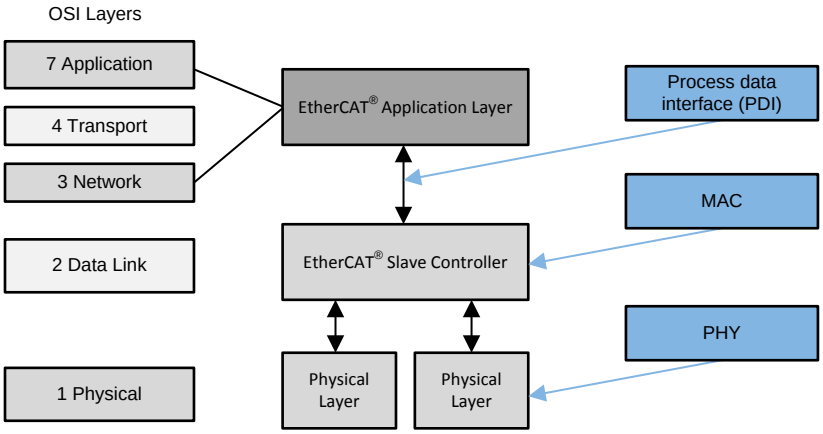

Figure 2. EtherCAT® Slave Configuration

For the application layer connection, different process data interfaces (PDI) are available, depending on the chosen ESC. Typical interface options vary from 32-bit to 8- or 16-bit parallel IO interfaces or serial interfaces like SPI. In the application layer the EtherCAT slave processes data or executes various functions, which are defined in specific profiles.

For more information on these profiles see the EtherCAT web page.

1.4 Key System Specifications

This design implements a cost-optimized EtherCAT slave (dual ports) with SPI connection to the application processor. The hardware design is capable of supporting multi-protocol industrial Ethernet and field busses using the AMIC110 industrial communications processor. The design has a 5-V input. A single PMIC generates all rails required onboard. The EtherCAT slave stack can run on the AMIC110 or on the application processor using a SPI. With a hardware switch, the AMIC110 can be configured to boot the EtherCAT slave firmware from SPI flash or from the application processor through SPI. The design is in a BoosterPack Plug-in Module form factor with a connector compatible to the TI LaunchPad Development Kit for easy evaluation with a C2000 MCU. A JTAG interface accelerates custom firmware development.

The major building blocks of this TI Design are the single 5-V PMIC, the two Ethernet PHYs, and the AMIC110 Sitara™ processor as the ESC with an SPI (slave) connection to a host controller.

For the firmware build to test the TIDA-00299 against the EtherCAT CTT, the EtherCAT stack runs on the onboard AMIC110 Sitara.

Table 3. TIDA-00299 Specifications

PARAMETER	VALUE	COMMENT
DC input voltage	5 V ±5%	2.1-mm ID and 5.5-mm ODM barrel DC jack 5-V input to supply the board using a single PMIC to generate all necessary supplies.
DC input current	250 mA (typical)	When EtherCAT slave is running connected to a EtherCAT master
Power consumption	1.25 W (typical)	Total board consumption with EtherCAT slave example code, measured on the 5-V supply
Industrial Ethernet standard	EtherCAT slave	Passes CTT of EtherCAT
	Sercos III, EtherNet/IP, PROFINET, POWERLINK	Hardware capable, firmware change required (not provided). The AMIC110 communication processor has software-programmable multiprotocol industrial Ethernet, and field bus support.
Industrial Ethernet stack	EtherCAT stack	Possibility to run EtherCAT stack onboard (AMIC110, as tested in this design) or on external application processor. When stack runs on external application processor, there is no requirement for the DDR3 memory.
Indicator LEDs	Supporting the available industrial Ethernet standards	Each industrial Ethernet standard defines their own indicator LEDs, which are used to show the status of the Ethernet interface. To be compatible with multiple industrial Ethernet protocols, the hardware supports the requirements of all standards.
IO interface signaling voltage	3.3 V	3.3-V fail safe IO. Compatible with TI LaunchPad.
Host processor SPI date rate	16 MHz (slave) or 48 MHz (master)	This interface can be used to communicate to an external processor.
Temperature range	-40°C to 85°C	Industrial temperature range -40°C to 85°C. No heat sink required.
Electromagnetic compatibility (EMC)	According to IEC61800-3	Meets IEC61800-3 EMC levels and pass criterion for ESD, EFT and Surge according to test method described in: • IEC61000-4-2 • IEC61000-4-4 • IEC61000-4-5 • IEC61000-4-6
EMI	CISPR11, EN55011	Meets EN55011, class A
EtherCAT firmware storage	SPI flash	This Flash interface is used for the ROM bootloader and standalone operation.
Board identification	EEPROM	Using an EEPROM to store Board identification values during run time
Debugging interface	JTAG header	JTAG header for custom firmware development
Cable Reach	> 100 m	Typically the systems need to support cable lengths up to at least 100 m

2 System Overview

2.1 Block Diagram

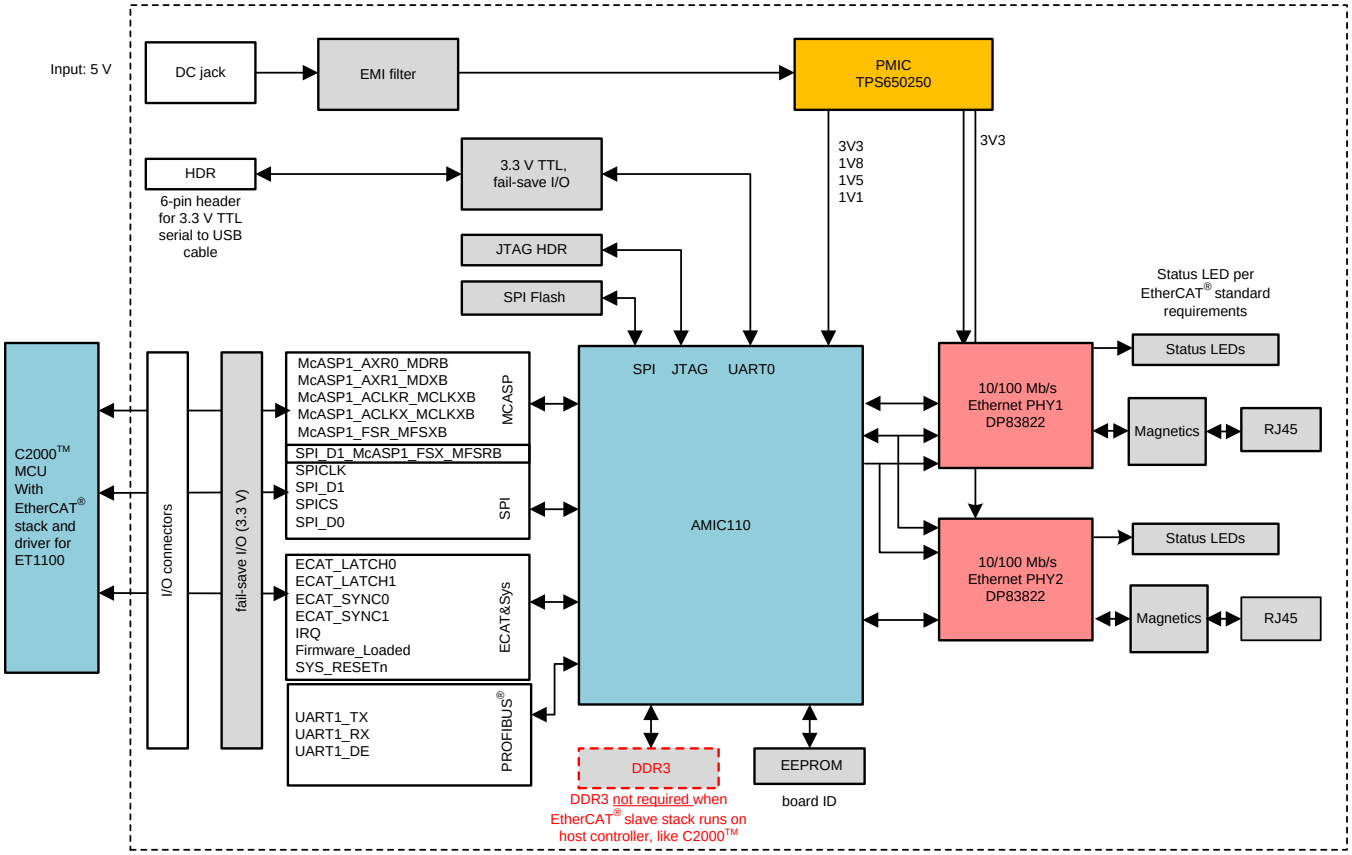

Figure 3. System Block Diagram of TIDA-00299

2.2 Design Considerations

2.2.1 Hardware Design

In this chapter different subsections of the TI Design are described, which explain component selection considerations and circuit design process. The subsections described are:

- Power management
- 10/100 Mbit Ethernet PHY
- EtherCAT controller
- Logic IC
- Host processor interface

2.2.1.1 Power Management

The main challenge in power management is the operating temperature range that the design must withstand. Because multiple rails have to be supplied, a highly-integrated solution is preferred to save onboard space and component count. At first, the power requirements for each active component must be considered.

2.2.1.1.1 DP83822 Current Consumption

To power the DP83822 there are several options to choose from, which depend on the power budget. Table 4 shows the maximum power consumption with all different rail options, which is taken from the datasheet of the DP83822.

Table 4. Power Consumption of the DP83822

VOLTAGE OPTION	PARAMETER	VOLTAGE	MAXIMUM POWER CONSUMPTION	COMMENT
One	IO supply	3.3 V	261 mW	Choose voltage depending on power budget on different rails
	Analog supply	3.3 V		
Two	IO supply	1.8 V	126 mW	Choose voltage depending on power budget on different rails
	Analog supply	1.8 V		

2.2.1.1.2 Sitara™ AMIC110 Current Consumption

Refer to *AMIC110 Sitara SoC*[7] for custom designs.

The *AM335x Power Consumption Summary* Wiki page gives reference power consumption values for the AM335x chip. The AMIC110 was derived from the AM335x. Thus, these AM335x reference values can give us an estimate of the worst-case power requirements of this AMIC110 TI Design.

In Table 5 the power requirement of the example *3D Chameleon Man* is used because this is the example with the highest consumption. This example includes 3D graphics processing, which is not present on the AMIC110; therefore the power consumption of the AMIC110 is expected to be lower.

Table 5. Current Consumption of AM335x, Including DDR3

RAIL	SITARA	DDR3
1.1 V	~420 mA	—
1.5 V(1)	~120 mA	~140 mA
1.8 V	~33 mA	—
3.3 V	~34 mA	—

(1) is DDR3 interface using 1.5 V

2.2.1.1.3 Current Consumption of Additional Components

The complete system has several additional components on the 3.3-V rail, including:

- Glue logic between AMIC110 and DP83822
- Status LEDs for EtherCAT
- SPI RAM for booting the AMIC110
- Switching losses on IO lines

The glue logic is required for the AMIC110 boot sequence and to ensure that no two outputs are driving against each other during startup. For this purpose, the SN74LV244A MUX and SN74LVC2G66 dual switch were used. The devices' current consumption is based on the *SN74LV244A Octal Buffers and Drivers With 3-State Outputs*[9] datasheet and *SN74LVC2G66 Dual Bilateral Analog Switch*[10] datasheet and is approximated to be 10 mA.

The status LEDs of the real-time Ethernet protocols integrates 14 LEDs in total: eight LEDs at 3.3 V at 2 mA and six LEDs at 5 V at 2 mA..

The flash chip is the W25Q64 from Winbond™. The worst case current consumption is 25 mA according to the W25Q64FV datasheet. For IO driving current, the following worst-case calculation was done:

$$P_{IO,out} = \left(C_{out} \times (V_{IO})^2 \times f\right) = 20\ pF\ (3.3\ V)^2 \times 25\ MHz = 5.4\ mW \quad (1)$$

The IO capacitance is approximated with the typical load capacitance of the AMIC110's PRU pins, which based on the *AMIC110 Sitaro SoC*[7] datasheet values. The MII signals have 25-MHz clock frequency.

This means about 1.67-mA drive current per 3.3-V IO pin. In this design approximately 50 pins are used.

Table 6. Current Requirement for External Circuits and Driving IOs

RAIL	FLASH	GLUE LOGIC	LEDS	DRIVING IO
3.3 V	~25 mA	~10 mA	~16 mA	~83 mA

2.2.1.1.4 System Current Consumption

The total power requirement for the four rails of the power supply is summarized in Table 7.

Table 7. System Current Requirements

RAIL	AMIC110	DDR3	SINGLE SUPPLY DP83822	EXTERNAL CIRCUIT
1.1 V	~420 mA	—	—	—
1.5 V(1)	~120 mA	~140 mA	—	—
1.8 V	~33 mA	—	—	—
3.3 V	~34 mA	—	~159 mA	~138 mA

(1) The designer can decide to supply the DP83822 either by one or by two power rails. For this design, only one power rail option was considered. The choice was to use 3.3 V.

Table 8. System Current Requirements, Option OneTable 4

RAIL	SINGLE SUPPLY
1.1 V	~420 mA
1.5 V(1)	~260 mA
1.8 V	~33 mA
3.3 V	~327 mA

(1) Using a margin of 50% is reasonable to account for transient events.

2.2.1.1.5 TPS650250-Based Single-Chip Power Supply Solution

The TPS650250 PMIC is designed to power up the Sitara family of processors, such as the AM335x and AMIC110. For detailed explanation and examples, see the *Powering the AM335x With the TPS650250*[8] user's guide. The user's guide shows how to match the requirements of the AMIC110 family of devices. Our system runs from a preregulated 5-V supply.

For the power loss calculations in Table 9, Equation 2 was used for the switch mode power supply (SMPS) and Equation 3 for the LDO. For these calculations the SMPS efficiency was assumed to be 80%.

$$P_{SMPS} = V_{OUT} \times I_{OUT} \times \left(\frac{1}{\eta} - 1 \right) \quad (2)$$

$$P_{LDO} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

Table 9. System Power Dissipation

RAIL	TPS650250 MAXIMUM CURRENT	TOPOLOGY	SINGLE SUPPLY	POWER DISSIPATION
1.1 V	1600 mA	SMPS	~420 mA	0.12 W
1.5 V	800 mA	SMPS	~260 mA	0.1 W
1.8 V	400 mA	LDO	~33 mA	0.1 W
3.3 V	800 mA	SMPS	~331 mA	0.28 W

The total power dissipation in the TPS650250 in the single supply configuration is 0.6 W.

The power dissipation rating of the TPS650250 can be found in the Section 7.5 of the *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*[12] datasheet. The reference junction-to-ambient thermal resistance $R_{\theta JA}$ for the package is 35 K/W. Based on this, 1.14 W can be dissipated without external cooling at 85°C temperature.

For the supply line connections between the TPS650250 and the AMIC110 device, see Table 10.

Table 10. AMIC110 Supply Line Connections to TPS650250 Power Rails

RAIL	TPS650250	AMIC110
1.1 V	DCDC1	VDD_CORE, VDD_MPU, VDD_RTC
1.5 V	DCDC2	VDDS_DDR
1.8 V	VLDO1	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC, VDDSHVx, VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD,VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1
1.8 V	VLDO2	VDDS,VDDS_RTC, VDDSHVx
3.3 V	DCDC3	VDDA3P3V_USB0, VDDA3P3V_USB1, VDDSHVx

The TPS650250 integrates a supply undervoltage comparator. In this design instead of monitoring the upstream 5-V supply, the PWRFAIL_SNS signal is used to monitor the voltage on the 1.1-V (processor core) rail and to use its open-drain output to assert the nRESET line of AMIC110 while the core voltage is below 1.0 V. The enable inputs of the various supply rails are cascaded to provide power-on sequencing, as shown on Figure 4. An undervoltage protection on the 5-V input supply is not implemented; the user must ensure that the input voltage on the DC jack is between 4.5 V and 5.5 V for proper operation.

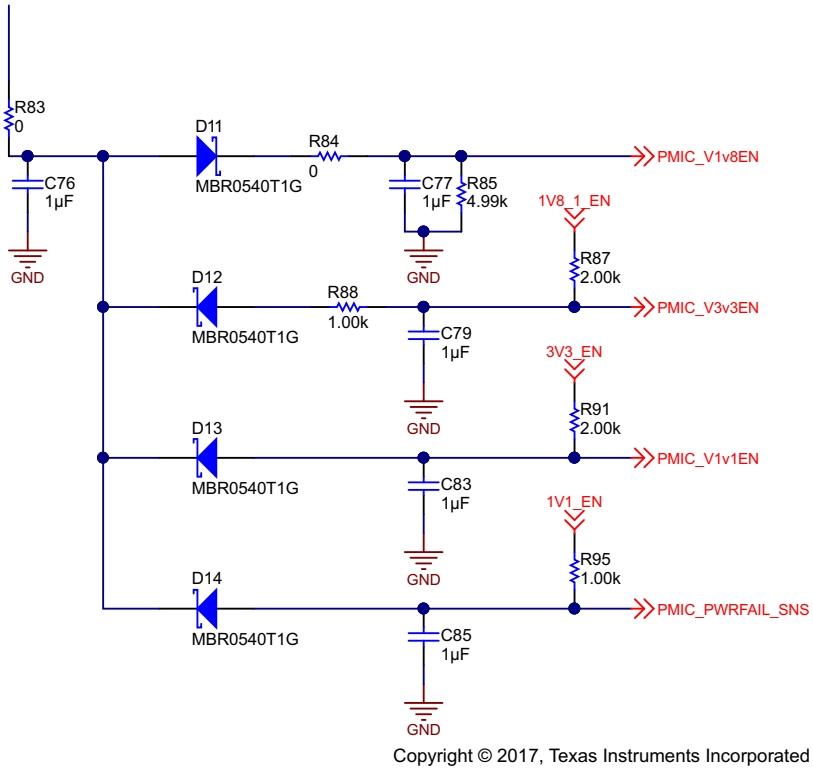

Figure 4. Power-up Sequencing Network

2.2.1.2 DP83822: 10/100 Mbit Ethernet PHY

Because of the harsh industrial environments where EtherCAT is typically used, the DP83822 PHY was chosen due to its excellent EMI performance. The device is easy to use with shielded Ethernet cables. The PHY chip uses a few pins for hardware configuration; these are called bootstrap pins or *straps*. Strap pins have internal pull-up or pull-down resistors, which provide a default configuration. By using external resistors, these defaults can be changed. The values of these pins are sampled at power-up or hardware reset. Because bootstrap pins may have alternate functions after reset is de-asserted, the pins should not be connected directly to VCC or GND.

In this design, in order to reduce the number of necessary components, most of the PHY's functionality is configured through the MDIO interface from the initialization routines, and the straps are used only to configure the MDIO PHY address.

Another feature of the DP83822 is the low receive and transmission latency which makes this PHY perfectly suited for the real time Ethernet systems.

For the MII interface 100BASE-TX, this information is documented in the data sheet. Transmission latency is 48 ns and receive latency is 194 ns.

2.2.1.2.1 Dual PHY Considerations

The MDIO interface is a serial bus defined for the Ethernet family of IEEE 802.3 standards for the MII. The MDIO bus only supports a single MAC as the master and can have up to 32 PHY slaves. The MDIO interface uses two signals. The MDC clock is driven by the MAC device to the PHY, and MDIO data is bidirectional; the PHY drives the MDC clock to provide register data at the end of a read operation.

In dual-PHY configuration, the MDIO interface addresses of the two PHYs have to be different. This is achieved by using strap options on the DP83822. The addresses 01 and 13 were chosen for PHY1 and PHY2 respectively. The strap configuration description can be seen in the *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*[12] Section 8.5.1. The strap configuration when using an indicator LED pin used on the PHY is described in Section 8.5.2.

During startup the PHYs are held in reset mode by keeping their nRESET pin low to ensure that the PHYs are not active before the Sitara processor is properly booted. The reset circuitry is shown in Figure 5.

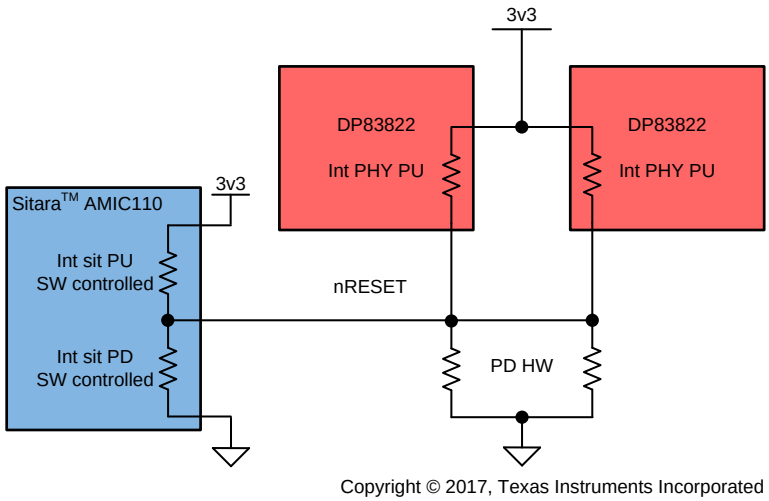

Figure 5. Reset Circuitry on TIDA-00299 of DP83822

Each PHY's nRESET pin has an internal fixed 9-kΩ pull-up. Aside from the push-pull GPIO, the AMIC110 Sitara has a 15-kΩ pull-up and a 35-kΩ pull-down, which are selectable by software (but not on all pins). While uninitialized, the pin is a high-impedance input. The PHYs interpret nRESET as low when the signal's voltage is at or below 0.8 V. In order to achieve this, a 1.1-kΩ pull-down resistor is necessary. For the possibility of independent reset signaling, two 2.2-kΩ pull-down resistors are used, one for each PHY. These resistors result in a voltage on nRESET of approximately 0.77 V.

2.2.1.2.2 MII Between DP83822 and the AMIC110

The connection between the PHY (DP83822) and the MAC (AMIC110) follows the MII standard. The interface uses single-ended, 3.3-V signaling. The DP83822 PHY is available with 1.8-V, 2.5-V, and 3.3-V IO voltage options. The required signal lines are listed in Table 11.

Table 11. Data Lines of the MII per Port

DESCRIPTION	NET NAME	PINS
Transmit clock	PHYx_TXCLK	1
Transmit data	PHYx_TXDn	4
Transmit enable	PHYx_TXEN	1
Receive clock	PHYx_RXCLK	1
Receive data	PHYx_RXDn	4
Receive error	PHYx_RXER	1
Receive data valid	PHYx_RXDV	1
Collision detect	PHYx_COL	1
Carrier sense	PHYx_CRS	1
Total	—	15

As EtherCAT is full duplex communication, the COL (Collision detect) and CRC (Carrier Sense) signals are not needed.

2.2.1.2.3 MDI

To enhance EMC an RJ-45 Ethernet jack without indicator LEDs was chosen. A second consideration was to separate transformer and RJ45 connector. This separation gives a slightly larger PCB, but improves the overall EMC and EMI performance. The third important factor is the easy PCB routing from PHY trough the Ethernet transformer to RJ-45 jack; here the pins of the jack and the transformer have to match the pins on the PHY.

The signals from the RJ-45 connector to the transformer and from transformer to the PHY are differential pairs, which have to be routed accordingly. For high signal quality, the length mismatch between the differential pairs should be below 10 mil (0.254 mm).

Figure 6 shows the schematic of the PHY-to-JACK connection. U4 is an ESD protector.

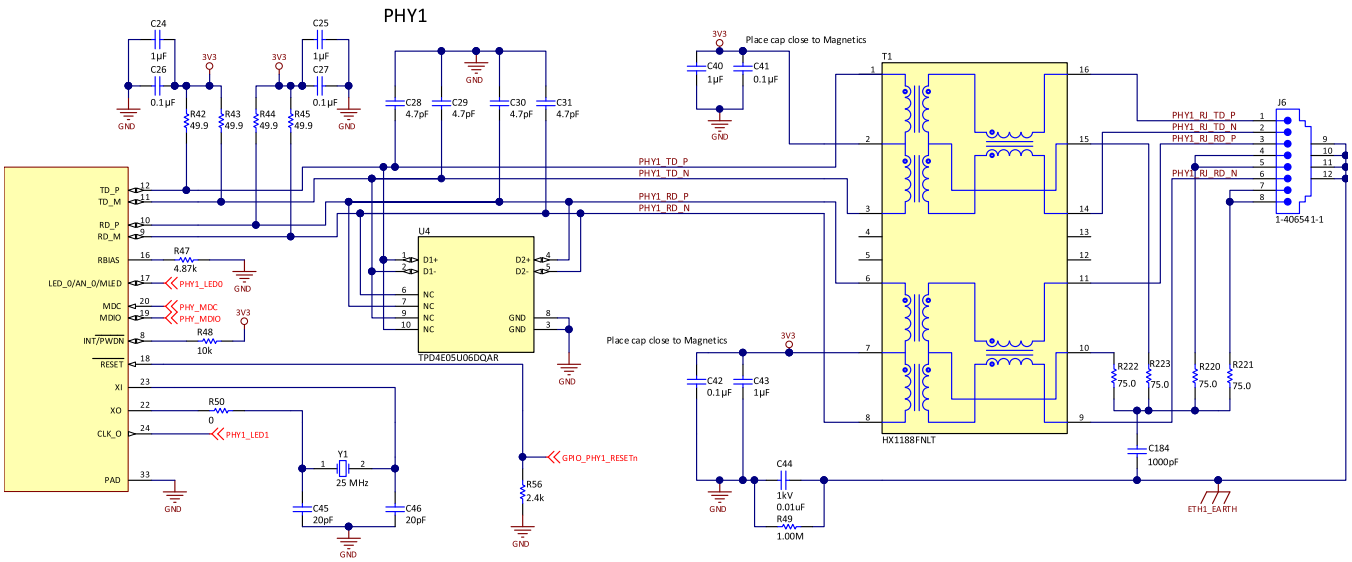

Figure 6. PHY to RJ-45 Connection on the TIDA-00299

The Ethernet transformer provides DC isolation between the local circuitry and the network cable. The center tap of the isolated winding has a Bob Smith termination through 75-Ω resistors (R220-R223) and a 1000-pF capacitor (C184) to chassis ground (earth). The termination capacitor should have a breakdown voltage rating of at least 2 kV. Bob Smith termination is used to reduce common mode noise.

2.2.1.2.3.1 Earth-to-GND Connection

Special consideration needs to be made when designing this connection as this can have a huge impact on the EMC performance of the system.

It has an influence of the Earth potential compared to the GND potential of the board if GND potential drifts too far apart due to the EMC event. This can lead to communication errors of the PHY due to the potential difference being outside of the specification of the PHY.

To prevent this, an RC-connection is proposed for this design using C44 and R49. This can also be an RCD connection depending on the overall system connection to the connecting PHY.

In this design, several tests were made with different R and RC options. This can be seen in Section 3.2.2.3.3.2.

2.2.1.3 AMIC110 Sitara™ - EtherCAT® Controller

For more details on the EtherCAT standard, see the *AM335x/AM437x SOC pins used for EtherCAT functionality* section of the *PRU ICSS EtherCAT firmware API guide* Wiki page. This section describes which pins are used for enable the EtherCAT functionality of the Sitara processor.

2.2.1.3.1 Memory Interface

DDR3

Because only one DDR3 memory chip is necessary, the termination of the DDR3 data lines can be neglected if the layout is done correctly. The characteristic impedance of each trace must match the one of the DDR3 IC. This was already implemented and tested on the BeagleBone Black and its DDR3 interface has been reused in this design.

SPI flash

This flash chip was chosen to have a cost-optimized boot option. The boot configuration pins of the AMIC110 are set so that it will boot from the SPI flash. The detailed description of the boot configuration can be found in the Table 26-7 of the *AM335x and AMIC110 Sitara Processors Technical Reference Manual*[13]. The boot configuration used in this design is shown in Table 12 where PD means a pull-down resistor, PU is a pull-up, and X means that it has no effect.

Table 12. Boot Configuration Pins

GROUP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Sysboot pin	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Resistor	PU	PD	PD	PD	X	X	X	X	X	X	PD	PU	PU	PD	PD	PD

I2C EEPROM

An EEPROM memory has been added to the board for identification purposes. The Ethernet MAC addresses can also be stored there if the firmware supports this function. The EEPROM chip is accessible on the I2C address 0x50.

2.2.1.3.2 Ethernet Protocol-Specific Indicator LEDs

The board was built with the main focus on EtherCAT, but the necessary indicator LEDs of other protocols were added for extensibility. A definition of the required indicator LEDs and their meaning is shown in Table 13 and summarized in Table 14. With firmware update, the hardware has the potential to support the following industrial Ethernet protocols:

- EtherCAT (example firmware provided)
- PROFINET
- SERCOS III
- Ethernet/IP
- Ethernet POWERLINK

Table 13. Industrial Ethernet Indicator LED Definitions

—	—	POWERLINK	EtherCAT	Ethernet/IP	SERCOS III	PROFINET
Link and activity LED	Color	Green (per port)	Green (per port)	Green (per port)	Green (per port)	Green (per port)
—	Behavior	Solid on link, blink on activity	Solid on link, blink on activity	Solid on link, blink on activity (optional)	Solid on link	Solid on link, Blink on command from PLC (not on activity)
Activity LED	Color	—	—	Orange (per port)	Orange (per port)	—
—	Behavior	—	—	Blink on activity	Blink on activity	—
Status and error LED	Color	Bi-color green and red	—	—	—	—
—	Behavior	—	—	—	—	—
RUN LED	Color	—	Green	—	—	—
ERROR LED	Color	—	Red	—	—	—
Module status	Color	—	—	Bi-color (green, red)	—	—
Network status	Color	—	—	Bi-color (green, red)	—	—
S LED	Color	—	—	—	Tri-color (orange, green, red)	—
SD1 LED	Color	—	—	—	Tri-color (orange, green, red)	—
ON	Color	—	—	—	—	Green
—	Behavior	—	—	—	—	Device is on
BF	Color	—	—	—	—	Red
SF	Color	—	—	—	—	Red
MT	Color	—	—	—	—	Yellow
SF	Color	—	—	—	—	Red
MT	Color	—	—	—	—	Yellow

Based on these definitions, the LEDs listed in Table 14 are necessary to support all of these five protocols.

Table 14. Industrial Ethernet Indicator LED Summary

GROUP	1	2	3	4	5
LED type	Green	Yellow	Orange	Red	Multicolor LED
Number of LEDs	Three	Two	Two	One	Two tricolor (red, green, yellow)

Meaning a total of six LEDs and two multicolor LEDs were added to implement every protocol shown in Table 14.

In Figure 7 the indicator LED circuitry is shown. Because of unexpected RoHS and REACH compliance issues, the multicolor LEDs had to be separated to three single LEDs. This separation shows the functionality of the LED but must be combined with a lens or changed to a multicolor LED to comply to the standards such as SERCOS III, Ethernet/IP, and POWERLINK.

The additional parallel resistors R188, R189, R235, and R236 are required for the boot-time configuration of the PHYs.

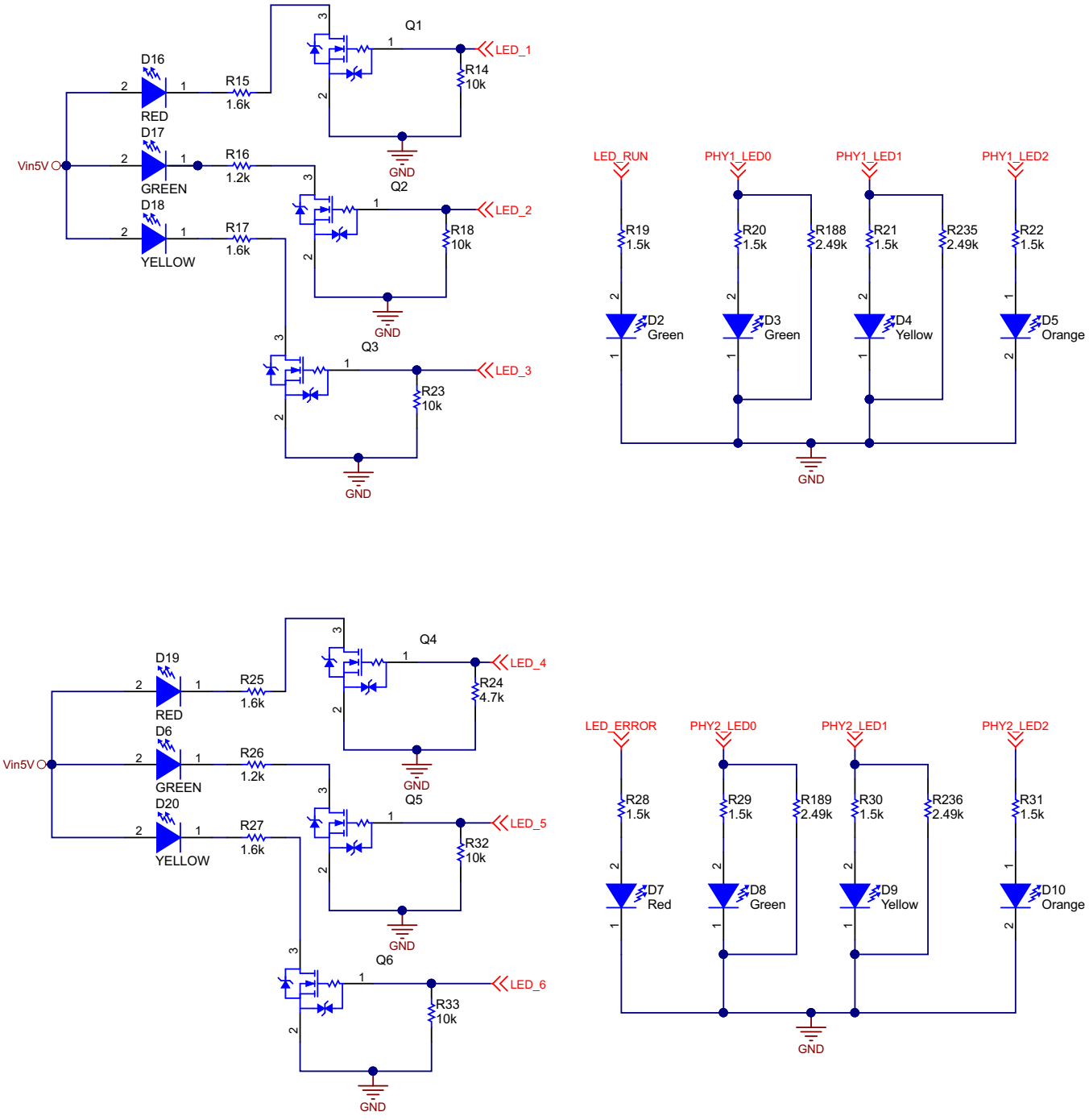

Figure 7. Indicator LEDs of TIDA-00299

2.2.1.3.3 Boot-time GPIO Considerations for the AMIC110

During the multi-stage boot process of the AMIC110, some pins have a high-Z state during boot up. Some of these pins should not be left floating and require a definite external pull-up or pull-down resistor.

The pins in question are summarized in Table 15 and Table 16 and can be found in *AMIC110 Sitara SoC*[7] datasheet Table 4-4.

The pins are described in the table by pull-down resistor (PD), pull-up resistor (PU) or high-Z state (Z), which means that during the boot process these pins are either always high-Z and that pull-up or pull-down resistor can be chosen, or that the pin during boot state has an internal PU or PD connected and must be either pulled up or down.

Table 15. High-Z Pins, Which Require External Pull-Down or Pull-up

GROUP	1	2	3	4	5	6	7	8	9	10	11	12	13
ZCZ BALL NUMBER	B6	C7	B7	A7	C8	B8	A8	C9	C18	B18	C17	C16	R6
PD OR PU OR Z	Z	Z	Z	Z	Z	Z	Z	Z	PD	PU	PU	PU	PD
ZCZ BALL NUMBER	R1	R2	R3	R4	T1	T2	T3	T4	U1	U2	U3	U4	V2
PD OR PU OR Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
ZCZ BALL NUMBER	V3	V4	T5	R5	V5	U5	B15	B4	B5	D14	A17	A16	C15
PD OR PU OR Z	Z	Z	Z	PD	PD	PD	Z	Z	Z	PD	PU	PU	PU
ZCZ BALL NUMBER	B17	B16	E16	E18	E15	E17	D15	D16	D17	D18	A9	B9	A15
PD OR PU OR Z	PU	PU	PU	PU	PU	PU	PU	PU	PU	PU	Z	Z	PD

Table 16. High-Z Pins, Which May Be Left Floating

GROUP	1	2	3	4	5	6	7	8	9	10	11	12
ZCZ BALL NUMBER	P16	N17	P18	P17	T18	R17	R18	M15	P15	N18	V10	A4
PD OR PU OR Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

For this boot-time configuration, two pieces of SN74LVC541 tri-state octal buffers were used in order to disconnect all the boot-time required pull-up (10 kΩ) or pull-down (100 kΩ) resistors after the boot sequence is complete.

2.2.1.3.4 Unused Peripherals and Interfaces

To reduce power consumption, unused peripherals and interfaces can be disabled. This also saves on external components, therefore PCB space, BOM count, and cost. The following parts were disabled:

- RTC circuit
- USB interface

To disable the RTC circuit, see the *RTC* section of the *AM335x Schematic Checklist* Wiki page.

The configuration from Table 17 must be used.

Table 17. Disabling AMIC110's Real-time Clock Subsystem

PIN	CONNECT TO
VDDS_RTC	1.8V
CAP_VDD_RTC	1.1V(VDD_CORE)
RTC_KALDO_ENn	1.8V(VDDS_RTC)
RTC_PWRONRSTn	GND(VSS)
PMIC_POWER_EN	NC
EXT_WAKEUP	GND(VSS)
RTC_XTAL	NC
VSS_RTC	GND(VSS)

To disable the USB interface, see the *USB* section of the *AM335x Schematic Checklist* Wiki page..

Table 18. Disabling AMIC110's USB Interface

PIN	CONNECT TO
VDDA1P8V_USB	1.8V
VDDA3P3V_USB	3.3V or GND
VSSA_USB	GND
USBx_DP	NC or GND
USBx_DM	NC or GND
USBx_CE	NC
USBx_ID	NC or GND
USBx_DRVVBUS	NC
USBx_VBUS	NC or GND

2.2.1.3.5 Sitara™ Peripheral Interfaces and Their Signals on Connectors

Inter-processor interface signals are available through the connectors J4 and J5.

Table 19. TIDA-00299 Inter-Processor Peripheral Connections

FUNCTION	SIGNALS	IO [3.3 V]	COMMENT
AMIC110 to host processor SPI connection	SPIx_D1 (I)	Digital input	Data input for serial communication
	SPIx_CS0n (I)	Digital input	Chip-select signal; active low
	SPIx_SCLK (I)	Digital input, up to 16 MHz	Clock for serial communication
	SPIx_D0 (O)	Digital output	Data output for serial communication
AMIC110 UART1 interface	UART1_TX	Digital output	—
	UART1_EN	Digital output	—
	UART1_RX	Digital input	—

GPIO signals are available on the connectors J4 and J5.

Table 20. TIDA-00299 GPIO Signal Connections

FUNCTION	SIGNALS	IO [3.3 V]	COMMENT
AMIC110 GPIO signals	GPIO1_1	Digital input/output	GPIO free for further use
	GPIO2_27	Digital input/output	GPIO free for further use
AMIC110 reset signal	SYS_RESETn	Digital input	Input to reset the BoosterPack

Available EtherCAT-specific signals through the connectors J4 and J5.

Table 21. TIDA-00299 EtherCAT®-Specific Signals Connections

FUNCTION	SIGNALS	IO [3.3 V]	COMMENT
AMIC110 EtherCAT specific signals	ECAT_LATCH0	Digital input	EtherCAT Distributed Clock Latch 0 (external event input)
	ECAT_LATCH1	Digital input	EtherCAT Distributed Clock Latch 1 (external event input)
	ECAT_SYNC0	Digital output	EtherCAT Distributed Clock Sync0 output, single shot and cyclic mode supported
	ECAT_SYNC1	Digital output	EtherCAT Distributed Clock Sync1; multiple of SYNC0 cycle time
	IRQ	Digital input	EtherCAT interrupt signal
	FIRMWARE_LOADED	Digital output	EtherCAT operation ready signal

Serial port for USB to 3.3-V UART serial cable interface on the connector J3.

Table 22. TIDA-00299 Serial Port Connection

FUNCTION	SIGNALS	IO [3.3 V]	COMMENT
AMIC110 UART0 interface	UART0_TX	Digital output	Serial port connection for virtual COM port
	UART0_RX	Digital input	Serial port connection for virtual COM port

2.2.1.3.6 Glue Logic

Because the boot pins of the AMIC110 are also used for the Ethernet MII, the boot resistors have to be decoupled from the MII traces. This is done using two octal buffers with tri-state outputs. When the MII is in use, the buffer disconnects the pull-up and pull-down resistors, which makes the interface independent from the boot circuit.

During startup of the AMIC110 device, two boot pins of the AMIC110 are going to output-by-default pins of the DP83822s. To disconnect these two pins during the boot sequence, a dual FET logic is necessary to achieve low latency and a bandwidth that does not influence the MII signals. Due to these requirements, the SN74LVC2G66 dual analog switch was chosen. It has 150 MHz of bandwidth and a propagation delay of only 0.8 ns because the switch will always be on during operation of the MII.

As the frequency of the MII signals is 25-MHz maximum, the 0.8-ns propagation delay translates to 2% of the shortest period time.

The AMIC110's IOs are not fail-safe on their own; therefore, SN74CB3Q3245 bus switches were added before the LaunchPad connectors. The SN74CB3Q3245 was selected as it has a bandwidth of 500 MHz without inserting any significant propagation delay.

The SN74CB3Q3245 is also 3.3-V tolerant, even when powered down, avoiding any power supply sequencing issues regardless of the attached LaunchPad or other BoosterPacks. The SN74CB3Q3245 protects the AMIC110 device until power has been applied to the BoosterPack and software has enabled the bus switches.

2.2.1.4 Host Processor Interface

Two 2×10-pin, 2.54-mm headers are provided to connect to a host processor board. This interface fits the LaunchPad LAUNCHXL-F28377S and LAUNCHXL-F28379D.

The interface is compliant to 3.3-V IO systems. For details on the connector pin assignment, refer to Section 2.2.1.3.5 and Section 3.1.1.2.

2.2.1.5 Design Optimizations for Functional Updates and Further Cost Reduction

- Remove 0-Ω resistors, which are used for testing and debug purposes.
- Remove termination resistors on the RGMII signals, which are not required from the design.
- Replace LaunchPad Connectors with customer interboard connection.
- Remove JTAG connector and circuitry.
- Remove the crystal oscillator from PHY2, and let PHY1 drive PHY2's clock. In this case, an independent reset circuit for the PHYs must be implemented (the TIDA-00299 can be modified to test this).
- Change the PHYs nRESET circuit to reduce static power consumption.
- DDR3 is not required if the EtherCAT stack runs on the host processors and not on the AMIC110.
- EEPROM might not be necessary.
- Bus switches can be neglected.
- PMIC reset signal changed to avoid 0.6 V on Sitara pin during turn off.
- Change the LEDs to fit the standard desired if multi-color LEDs are required from Table 13.

2.2.2 Software Design

The software used in this design guide is taken from the Processor SDK software package, which can be found at Processor SDK.

For more information on the AMIC110 software options, see the *AMIC110SW* Wiki page.

This package includes all additional software packages required to compile and run the code. Additionally, it may be necessary to install Code Composer Studio™ (CCS). Download CCS from *Code Composer Studio (CCS) Integrated Development Environment (IDE)*.

The Processor SDK ships only a simplified EtherCAT stack and only as a library with headers. For full functionality, the EtherCAT Slave Stack (ET9300) must be downloaded from EtherCAT Technology Group. In order to do this, you have to obtain a license from ETG. To use the full-featured EtherCAT stack, search for EtherCAT in the *TI Processors Wiki*. This search will result a list of various trainings and walkthroughs to show how this update can be completed.

Table 23 shows a list of the required files and their functions.

Table 23. AMIC110 Initialization Files Required

REQUIRED FILES	FUNCTION OF FILE
GEL file	A memory map of the TIDA-00299 processor required for the JTAG connection
Bootloader (MLO)	A bootloader file, which setups the TIDA-00299 board and loads the app file
Application file (app)	The application file, which includes the EtherCAT functionality
Flash writer	An application to program the onboard flash of the TIDA-00299 board

For further support, visit the Sitara Processors Forum of TI E2E Community.

2.2.2.1 Prebuilt Files

The Processor SDK for AMIC110 comes with the bootloader (MLO). When installed with the default settings on Windows platform, the MLO can be found under C:\ti\pdk_DEVICE_Version\packages\ti\starterware\binary\bootloader\bin\EVM_TYPE\gcc.

To program the onboard SPI memory, the SDK comes with a flash tool, which can also be found in this package.

The bootloader has to be configured to boot from SPI flash. This configuration can be completed by picking the correct build option. For details on the configuration, see the user guide of the software package.

A user guide, the EtherCAT libraries, prebuilt binaries, and example source code can be found at *PRU-ICSS-ETHERCAT-SLAVE 01_00_02_01*.

2.2.2.2 Booting Through McSPI Flash

The AMIC110 Sitara processor is configured to boot through McSPI0 from the onboard flash memory. The bootloader copies the TIDA-00299 example firmware from the SPI flash into the DDR3 RAM and launches the application. Figure 8 shows the flow chart of the boot process.

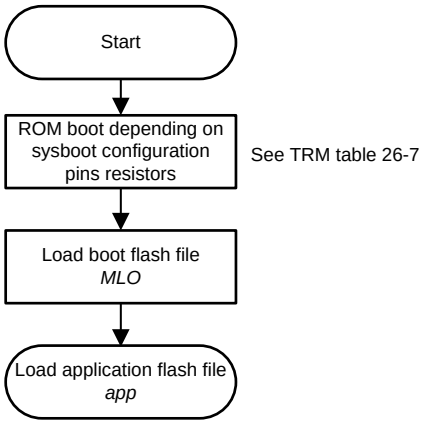

Figure 8. AMIC110 Boot Process From Power-up to Application Running

2.2.2.2.1 Flashing Bootloader and Application to SPI Flash

To write the flash memory, use the *Flash Writer* application. This application enables the AMIC110 to write the binary bootloader (MLO) and the application binary *app* to the onboard flash. The process is as follows:

1. Select the target configuration. This configuration includes JTAG port and target processor.
2. Load the GEL file.
3. Connect the target.
4. Load the *Flash Writer* out file.
5. It is recommended to erase the flash beforehand.
6. Halt execution, and repeat steps two through four. Continue from step six.
7. Select *Flash an Image* option, which will prompt for the binary file name.
8. Choose the Bootloader file called *MLO.bin*, which will prompt again for load address in flash.
9. Provide the address 0x00000 when loading the bootloader.
10. Halt execution, and repeat steps two through four. Continue from step ten.
11. Select *Flash an Image* option, which will prompt for the binary file name
12. Load the created app.bin, which will prompt again for load address in flash.
13. Provide the address 0x20000 when loading the application binary.
14. Once SPI flash writing completes, disconnect from CCS.
15. Reset the board, and the application file will be loaded from the SPI flash into memory.

2.3 Highlighted Products

2.3.1 AMIC110

The AMIC110 device is a multi-protocol programmable industrial communications processor providing ready-to-use solutions for most industrial Ethernet and field bus communications slaves as well as some masters. The device is based on the ARM® Cortex®-A8 processor, peripherals, and industrial interface options. The device supports high-level operating systems (HLOS). Linux® and TI-RTOS are available free of charge from TI. Other RTOS are also offered by TI ecosystem partners. The AMIC110 microprocessor is an ideal companion communications chip to the C2000 family of MCUs for connected drives.

The microprocessor unit (MPU) subsystem is based on the ARM Cortex-A8 processor. The PRU-ICSS is separate from the ARM core, which allows independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET IRT, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos III, and others. Additionally, the programmable nature of the PRU-ICSS, along with its access to pins, events, and all system-on-chip (SoC) resources, provides flexibility in implementing fast, real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of SoC.

2.3.2 DP83822

The DP83822 is a low-power single-port 10/100 Mbps Ethernet PHY.

The device supports multiple industrial buses with its fast link-down timing as well as Auto-MDIX in forced modes.

The DP83822 comes in a 32-pin, 5.00-mm × 5.00-mm QFN package.

Features:

- ±16-kV HBM ESD protection
- ±8-kV IEC 61000-4-2 ESD protection
- Operating temperature: –40°C to 125°C
- IO voltages: 3.3 V, 2.5 V, and 1.8 V
- Cable diagnostics
- Built-in Self-Test (BIST)
- MDC and Management Data Input-Output (MDIO) Interface

2.4 TPS650250

The TPS650250 device is an integrated power management IC that generates multiple power rails. The TPS650250 incorporates three highly-efficient, step-down converters targeted at providing the core voltage, peripheral, IO, and memory rails in a processor-based system.

The TPS650250 comes in a small, 5-mm × 5-mm, 32-pin QFN package.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 PCB Overview

Figure 9 and Figure 10 show photos of the top and bottom side of the TIDA-00299 PCB. The headers and default jumper settings are explained in Section 3.1.1.2.

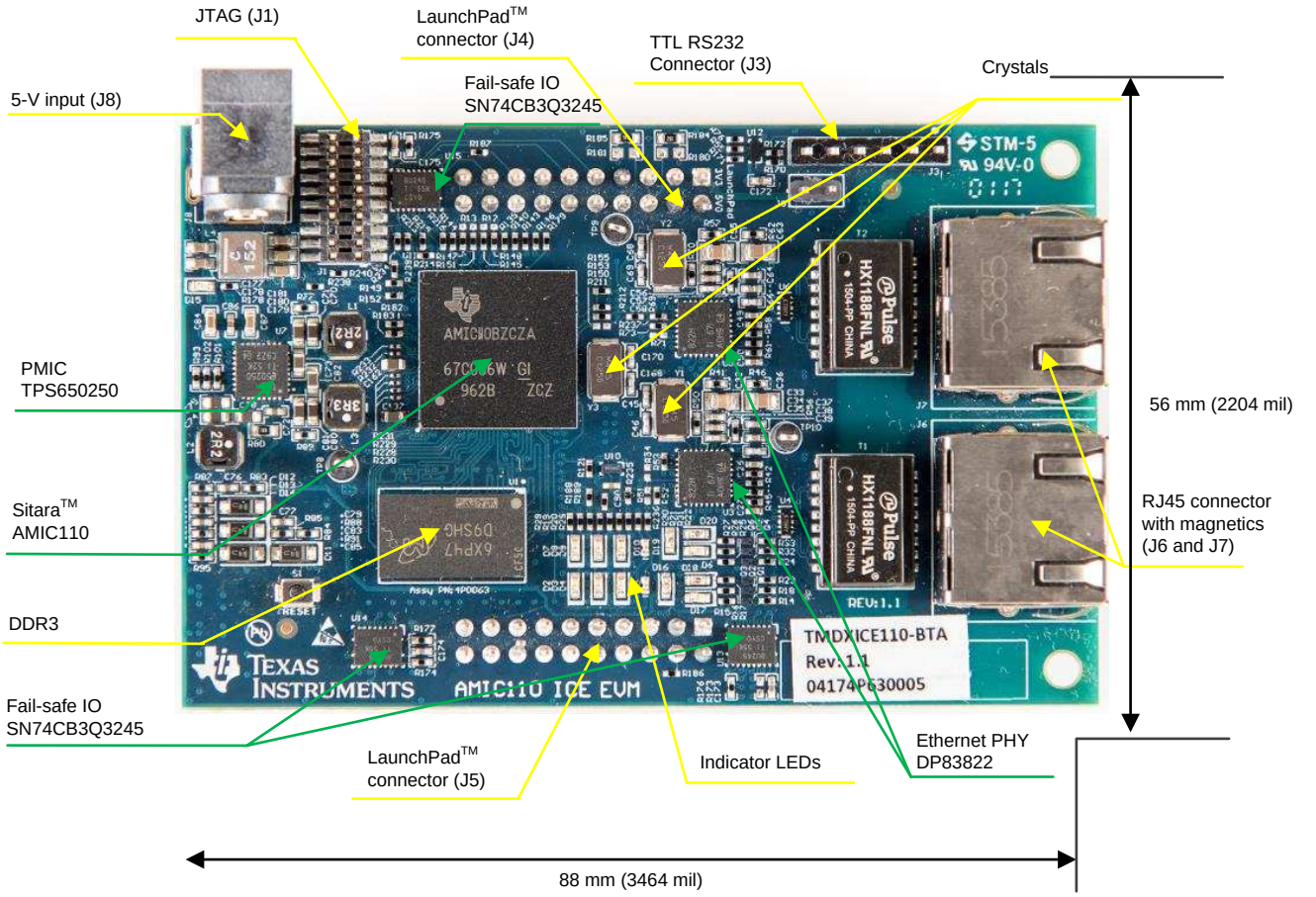

Figure 9. Board Picture (Top View)

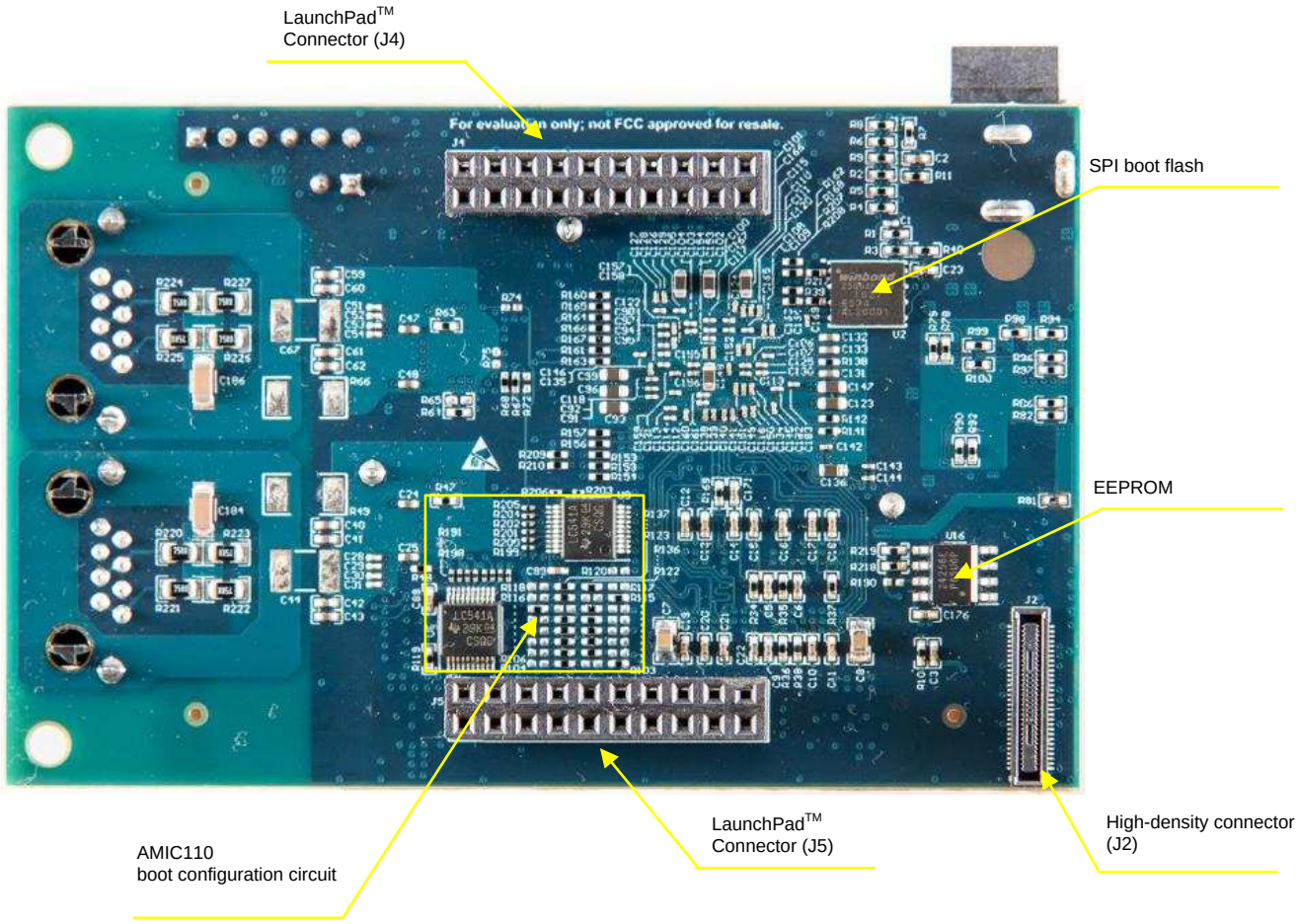

Figure 10. Board Picture (Bottom View)

3.1.1.2 Connector and Jumper Settings

3.1.1.2.1 Power Connectors

The 5-V nominal input voltage can be supplied through the connector J8; the chosen connector is a RAPC722X from Switchcraft.

This connector expects a 2.1-mm ID and 5.5-mm OD mating barrel connector.

3.1.1.2.2 Default Jumper Configuration

Prior to working with the TIDA-00299 board, make sure the correct jumper settings are applied. Figure 9 and Figure 10 show the default jumper configuration.

Table 24. Default Jumpers Settings

HEADER	JUMPER SETTING
J9	Insert a jumper between J2 pins 1 and 2 to enable the 3.3-V intermediate rail connect to power the LaunchPad.

Caution:

CAUTION

When using this jumper the user must ensure that the LaunchPad is not powered from its USB connection.

3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Design Evaluation

Table 25 lists the hardware equipment and software required for the evaluation of the TIDA-00299 TI Design.

Table 25. Prerequisites

EQUIPMENT	COMMENT
5-V DC power supply	5-V output power brick with at least 2-A output current capability. 2.1mm ID/5.5mm OD mating barrel connector
TIDA-00299 hardware	With the default jumper settings per Section 3.1.1.2
One jumper for board settings	Two pins, 2.54 mm (100 mil)
TIDA-00299 firmware	Download from TIDA-00299 design folder
InstaSPIN-Motion F28377S LaunchPad	Available through TI eStore
JTAG interface (XDS100v2 or XDS100v3)	Buy from XDS100 link
EtherCAT Conformance Test Tool (CTT)	Buy the software from https://www.ethercat.org
CCS 6	Download from https://www.ti.com

3.2.1.2 Hardware Setup

Table 26 shows the signals the EtherCAT BoosterPack uses to communicate with the C2000 LaunchPad.

Table 26. Pinout of J4 and J5 Host Processor Interface

TIDA-00299 revE2			
J4 (LEFT)	J4 (RIGHT)	J5 (LEFT)	J5 (RIGHT)
3V3	-	McASP1_AXR1	GND
-	GND	McASP1_AXR0	SPI_CS (SPI_D1/McASP1_FSX)
ECAT_SYNC0	AIN0	McASP1_ACLKR	GPMC_AD1 (V7)
ECAT_SYNC1	AIN1	McASP1_FSR	-
UART_RX (PROFIBUS)	-	ECAT_LATCH0	-
MMC0_DAT2 (F18)	-	ECAT_LATCH1	SPI_D0
SPI_CLK (McASP1_ACLKX)	-	FIRMWARE_LD	SPI_D1/McASP1_FSX
SPI_CS (SPI_D1/McASP1_FSX)	-	-	-
UART_DE (PROFIBUS)	-	-	SYS_RESETn
UART_TX (PROFIBUS)	-	-	IRQ

3.2.1.3 Software Setup

At the beginning, the TIDA-00299 board has the onboard flash programmed with:

- A bootloader, which boots the Sitara to load the application file from SPI flash
- EtherCAT slave application file running from SPI flash

For more details on the software, see Section 2.2.2.

3.2.1.4 User Interface

To test the TIDA-00299 EtherCAT slave board, an EtherCAT master is necessary. It is possible to use a PC to provide an EtherCAT master with a program called TwinCAT® 3.

The TwinCAT 3 tool uses the standard Ethernet adapter on the PC or laptop and adds the EtherCAT protocol to this adapter. On most hardware TwinCAT 3 will work easily, but in some cases the TwinCAT driver does not support the Ethernet adapter. For more information, see *TwinCAT driver for Ethernet cards*.

If the Ethernet adapter can be used by the TwinCAT driver, an installation guide and a brief introduction to TwinCAT 3 can be found at the *EtherCAT* section of the *SYSBIOS Industrial SDK 02.01.00.01 User Guide* Wiki page.

With the default software on the TIDA-00299 board, blinking a LED can be shown when changing the payload of the EtherCAT package in the TwinCAT 3 tool.

3.2.2 Test Results

Tests were conducted to characterize each individual functional block as well as the entire board. In particular, the following tests were conducted:

- Power management
- Ethernet signal
- System performance
  - EtherCAT compliance

Tests were conducted at room temperature around 22°C. Table 27 describes the equipment used for the TIDA-00299 testing session.

Table 27. Equipment for TIDA-00299 Performance Tests

TEST EQUIPMENT	PART NUMBER
Low-speed oscilloscope (suitable for power supply tests)	Tektronix™ TDS2024B
High-speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Differential probes	Tektronix P6630
Single-ended probes	Tektronix P6139A
Power supply (5 V)	Agilent™ E3648A with 2.1mm ID and 5.5mm OD mating barrel connector cable
True RMS multimeter	Fluke 179
General purpose PC	Capable of running TwinCAT 3 on Ethernet port
General purpose PC (optional, can be the same PC as above)	Running CCS
Ethernet cables	Twisted-pair shielded Cat 7 cable

Figure 11 shows the test setup.

Figure 11. TIDA-00299 Test Setup

3.2.2.1 Power Management

For the power management subsystem of the TIDA-00299 board, the following tests were done:

- Testing the power-up sequence of the power rails
- Testing the power loss scenario
- Testing the current consumption on each power rail

Tests were performed with the test setup shown in Figure 12.

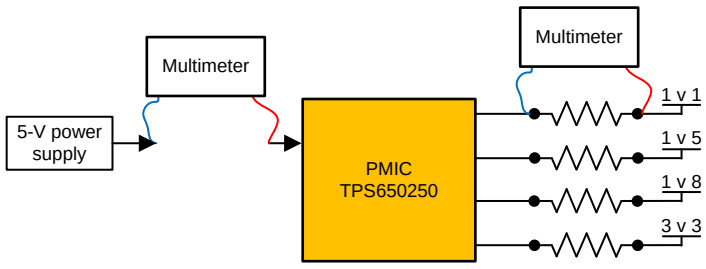

Figure 12. Diagram of Test Setup for TIDA-00299

3.2.2.1.1 Power-up Behavior of the Onboard Supply Rails

Testing the power up sequence was completed by first showing the rails 1v1, 1v5, 3v3, and reset, as shown in Figure 13.

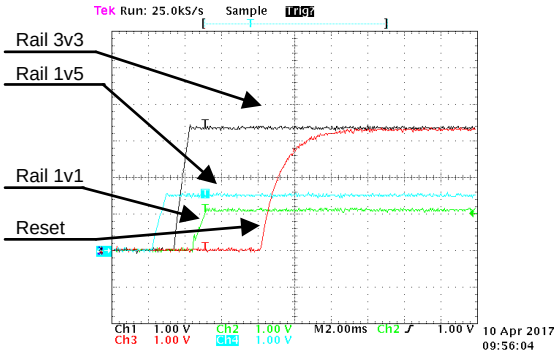

Figure 13. Power-up Sequence, Showing Rails 1v1, 1v5, 3v3, and Reset

The second test shows the power up sequence showing 1v5, 1v8, 3v3, and reset signal, as shown in Figure 14.

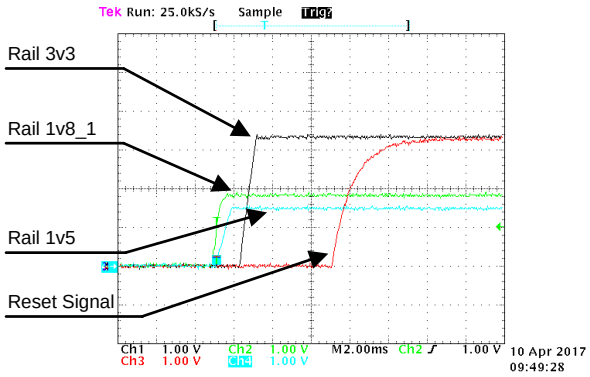

Figure 14. Power-up Sequence, Showing Rails 1v5, 1v8_1, 3v3, and Reset

For these measurements the rail 1v8 is always chosen to be 1v8_1. During the test 1v8_1 and 1v8_2 was compared and always show the same startup and shut down behavior.

3.2.2.1.2 Power-Down Behavior of the Onboard Supply

Figure 15 shows the power-down behavior of the rails 1v1, 1v8_1, and 3v3.

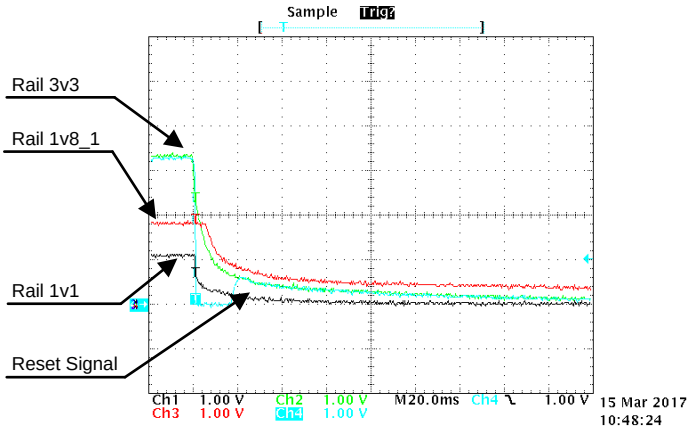

Figure 15. Power-Down Behavior, Showing Rails 1v1, 1v8_1, 3v3, and Reset

During power off, the TPS650250 PMIC can no longer hold the reset signal low after its supply voltage falls below the recommended input voltage range of the PMIC. After that point, the reset signal floats up to the 3v3 rail. This voltage is slightly above the maximum allowed low-level signal (0.5 V) as defined in the *AMIC110 Sitara SoC*[7] datasheet. The bump does not signal a high level, which must be at least 1.35 V. During power off all IO pins must be IO supply rail 0.3 V as the reset pin and the 3.3 V are powered from the same rail, which is always the case (see the *AMIC110 Sitara SoC*[7] datasheet Section 5.1).

On Figure 16, the power-down test shows the rails 1v5, 1v8_1, 3v3 and reset.

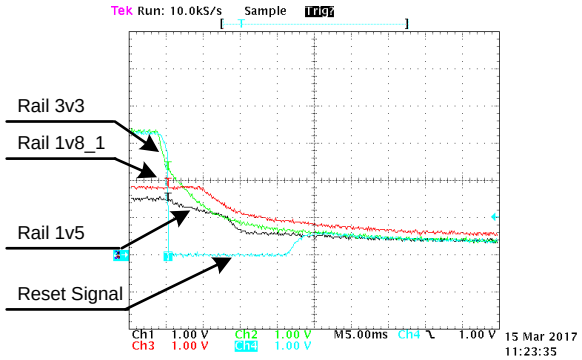

Figure 16. Power-Down Behavior, Showing Rails 1v5, 1v8_1, 3v3, and Reset

3.2.2.1.3 Power Consumption of the System

This test was performed while running the EtherCAT slave firmware on the TIDA-00299 design, which was connected to a TwinCAT 3 terminal on the PC. The system performance is shown in Table 28.

Table 28. Measured System Power Consumption

RAIL	TPS650250 MAXIMUM OUTPUT CURRENT	TECHNOLOGY	CURRENT CONSUMPTION	POWER CONSUMPTION
1.1 V	1600 mA	SMPS	349 mA	0.384 W
1.5 V	800 mA	SMPS	35.8 mA	0.054 W
1.8 V	400 mA	LDO	26.23 mA	0.047 W
3.3 V	800 mA	SMPS	128 mA	0.422 W

The current consumption measurement was completed using a multimeter and by removing the series 0-Ω resistors from each power rail. At the 5-V input, a multimeter was connected to measure the current.

When using the multimeter in this way, the voltage drop on its internal shunt must be taken into account. The rail's voltage after the current meter must be measured as well.

The total power consumption of the board is 0.91 W. The total supply current from the 5-V system power supply measured 248 mA, giving an input power of 1.24 W on the 5-V rail. This measurement means that the overall efficiency of the TPS650250 is around 78% for the complete system with 0.33 W of power dissipation in the package.

Using the given package thermal to junction performance from the *TPS650250 Power Management IC for Li-Ion Powered Systems*[11] datasheet, this means that temperature increase of the part compared to surrounding temperature is expected to be:

$$T_{TPS650250} = R_{\theta JA} \times P_{Dissipation} = \frac{35°C}{W \times 0.333W} \approx 11.7°C \quad (4)$$

At 85°C ambient, the estimated junction temperature is 97°C.

With the maximal operating junction temperature of 125°C in mind and running the TPS650250 at 85°C ambient temperature, the device can dissipate 1.14 W without forced cooling.

3.2.2.1.4 Thermal Test

While running the EtherCAT slave, a thermal image was taken of the board. This image is used see if there are thermal hot spots on the design.

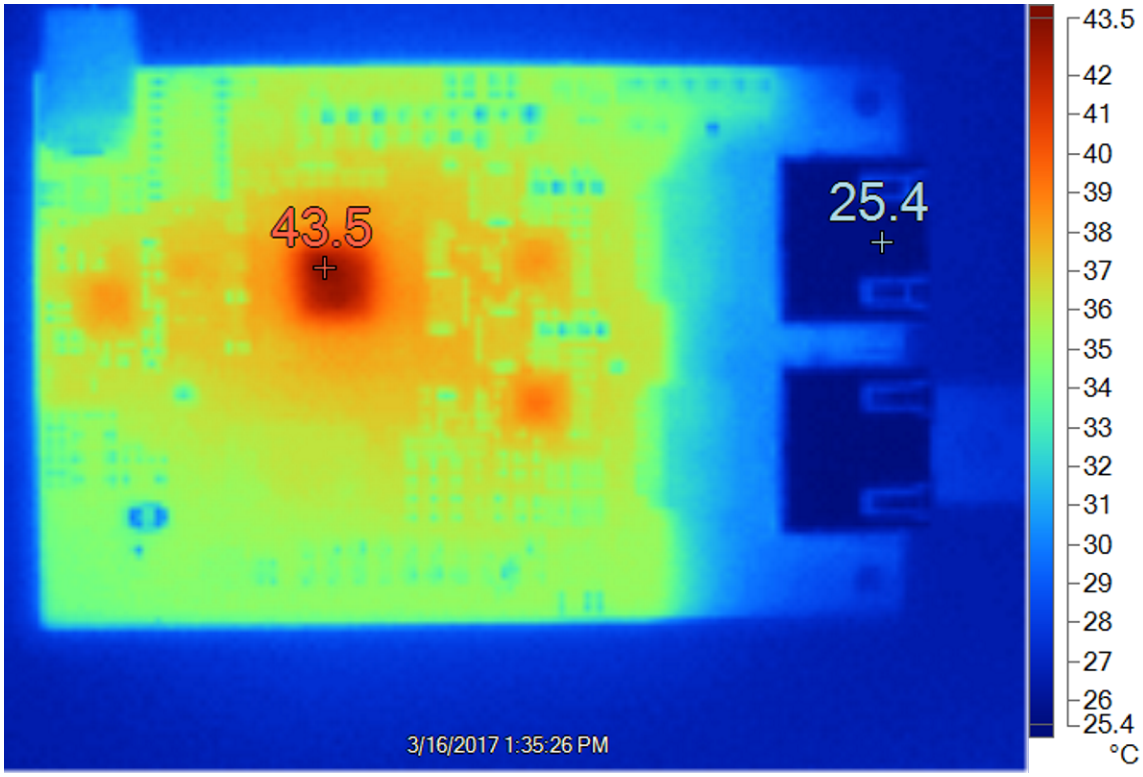

Figure 17. Thermal Image of TIDA-00299 Board

Figure 17 shows that the power supply is heating up to around 37°C with an ambient temperature of 25.4°C.

Using the value from the *TPS650250 Power Management IC for Li-Ion Powered Systems*[11] datasheet, the theoretical heating of the part using the evaluation board can be calculated.

$$T_{TPS650250} = R_{\theta JC(top)} \times P_{Dissipation} = \frac{21.8°C}{W \times 0.333\ W} \approx 7.3°C \quad (5)$$

In that value the additional heating of other ICs of the board and the PCB thermal performance is not taken into account, which is why the measured value is higher than the calculated value.

The hottest spot on the board is the AMIC110 device, which has a temperature rise of 18.1°C.

3.2.2.2 Ethernet Signal Tests

3.2.2.2.1 MII Signals

The MII signals between the MAC and the PHY are tested with a 100-Mbit connection on both PHY1 and PHY2 RX and TX. Figure 18 through Figure 21 show the clock signal and corresponding RX_D1 and TX_D1 data signals. The other data signals D0, D2, and D3 were measured as well and exhibited similar waveforms. This result was expected because the design was optimized for impedance and matched length of the clock and data lines.

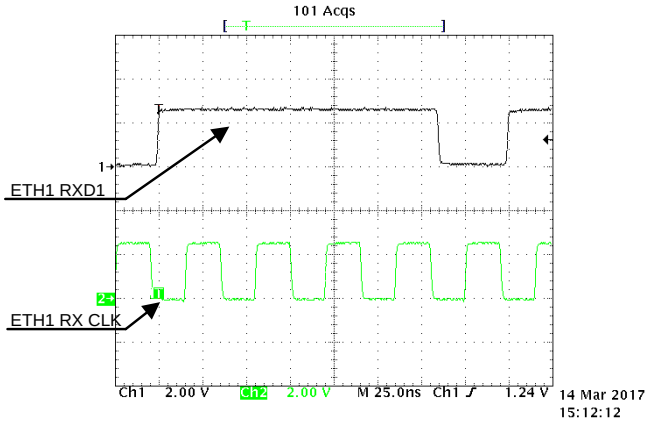

Figure 18. ETH1 MII RX Clock and Data Signals During Ethernet Communication

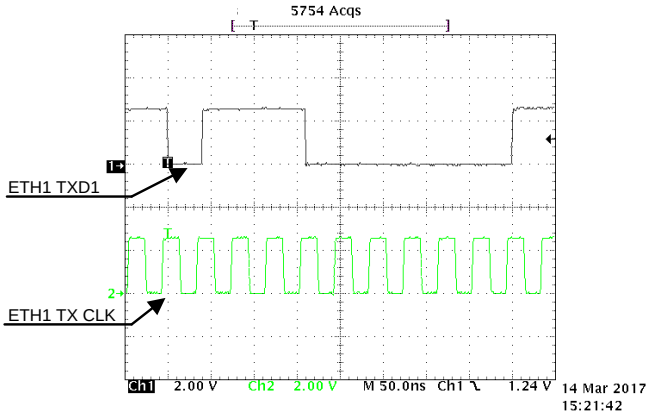

Figure 19. ETH1 MII TX Clock and Data Signals During Ethernet Communication

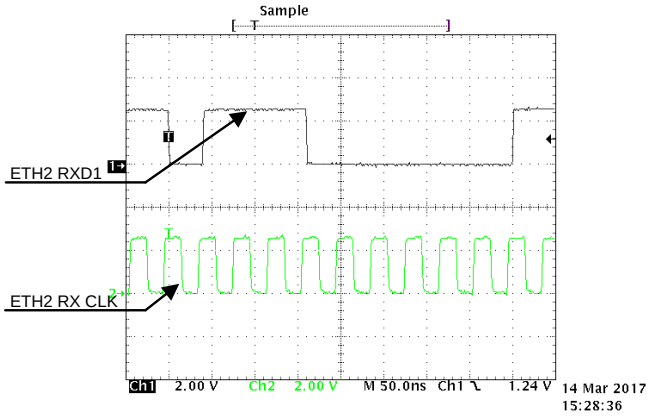

Figure 20. ETH2 MII RX Clock and Data Signals During Ethernet Communication

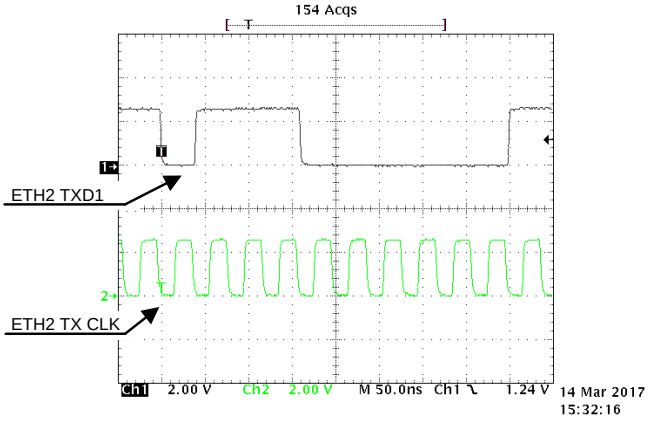

Figure 21. ETH2 MII TX Clock and Data Signals During Ethernet Communication

3.2.2.2.2 Serial Management Interface (SMI)

The maximum clock frequency of the SMI of the AMIC110 is 2.5 MHz. For this test, it is not necessary to have an active Ethernet connection. Figure 22 shows the MDC (clock) and MDIO (bidirectional data) signals between the AMIC110 Sitara and the two DP83822Hs PHY1 and PHY2. The Sitara is the MDIO master, and both PHYs are slaves, which share the same clock and data lines.

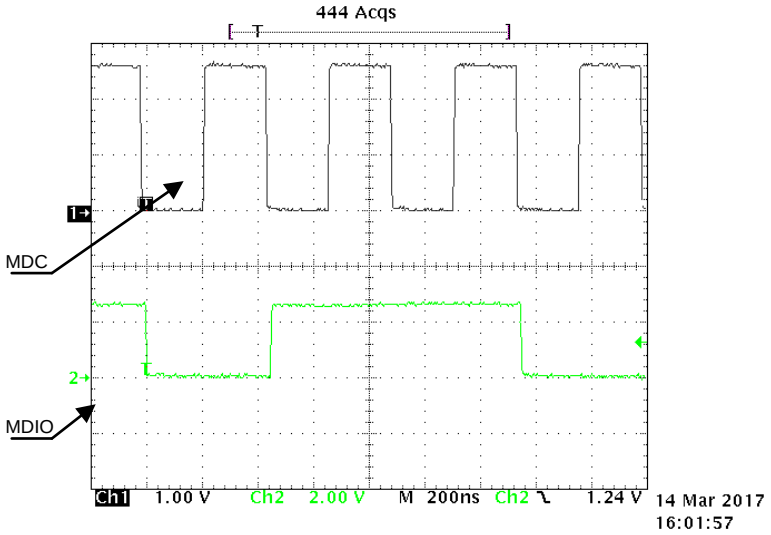

Figure 22. SMI Clock and Data Signals at 2.2 MHz

3.2.2.3 System Performance

To test EtherCAT slave functionality, the EtherCAT CTT can be used. This tool is meant to do in-house tests before the design is sent to an EtherCAT Test Center (ETC). After an independent conformance test at an ETC, the equipment may get the official conformance certificate.

To find an ETC, see the EtherCAT Test Center web page.

For more information on EtherCAT conformance, see the EtherCAT Conformance web page.

Another tool used for this design is TwinCAT® 3, a development environment for an EtherCAT Master implementation.

For more information on TwinCAT 3 see the Beckhoff® web page at https://www.beckhoff.com/twincat3/.

3.2.2.3.1 EtherCAT Conformance Test Tool

The EtherCAT CTT uses an XML file, which is configured to work with the default firmware running on the TIDA-00299 board. Figure 23 and Figure 24 show screenshots of the CTT.

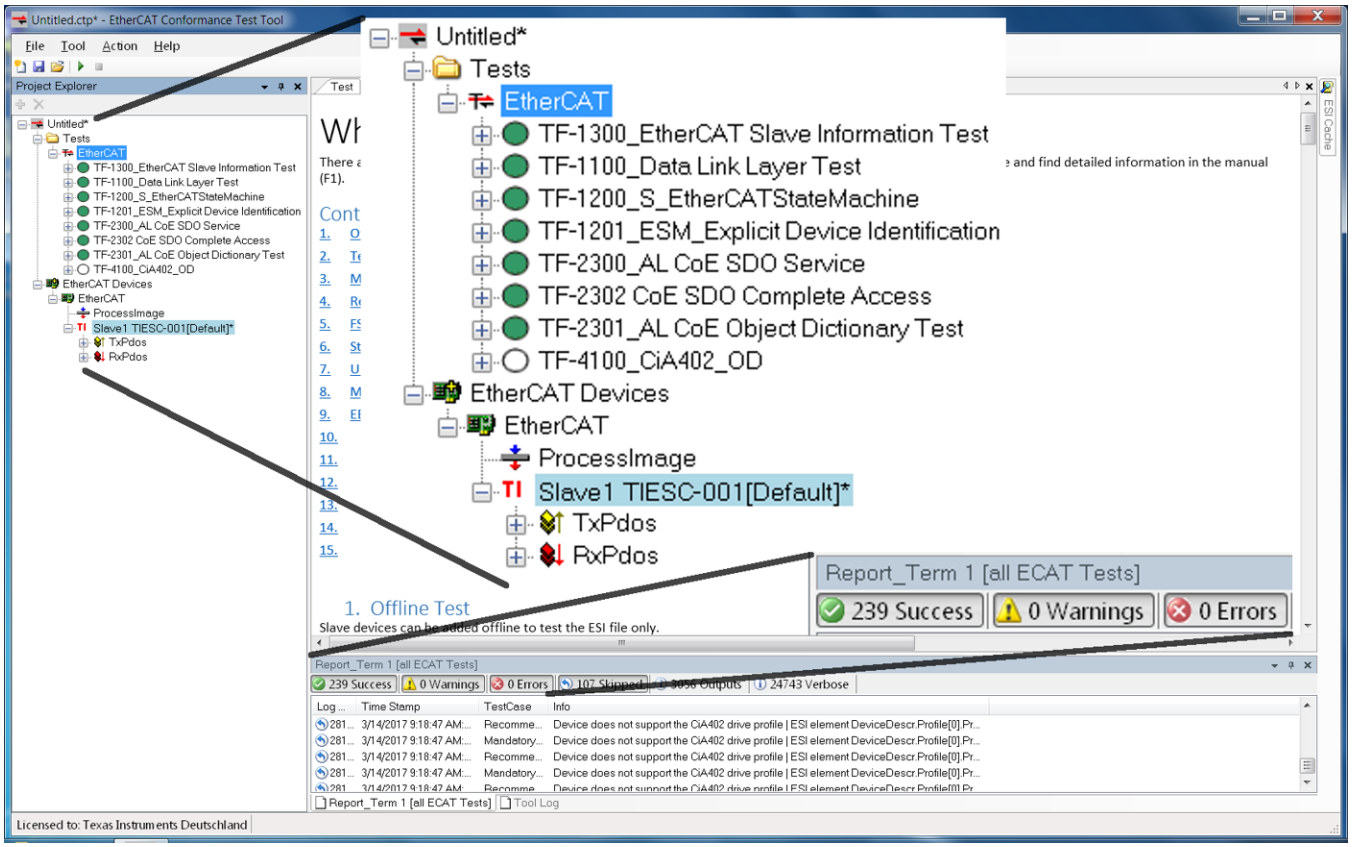

Figure 23. Screenshot of CTT Result for PHY1

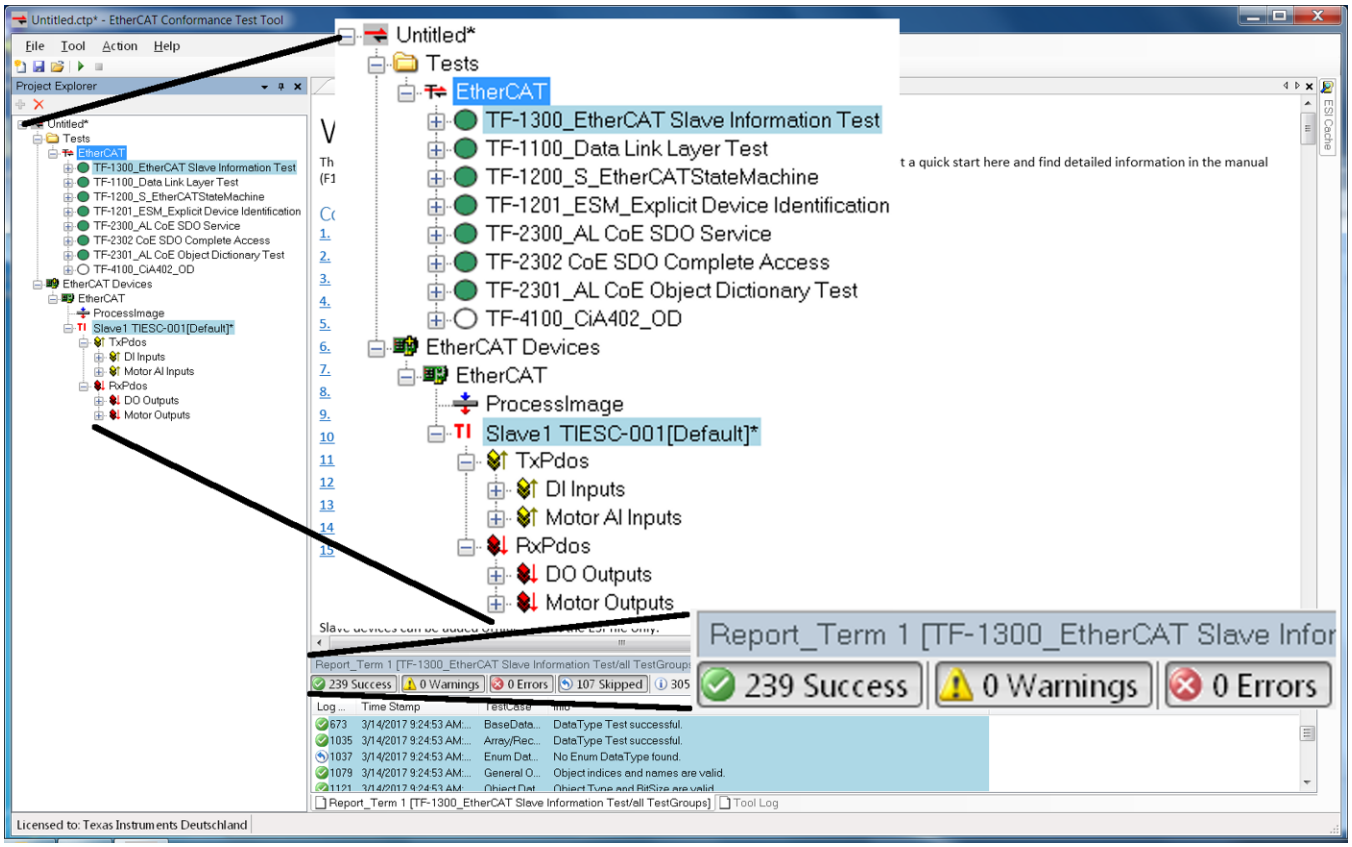

Figure 24. Screenshot of CTT Result for PHY2

From the screenshots in Figure 23 and Figure 24, the TIDA-00299 board passes the CTT test.

3.2.2.3.2 EtherCAT Cable Length Test

Using TwinCAT® 3 to emulate an EtherCAT master on a Dell™ PC, different cable lengths were tested. The test was done with the EtherCAT master sending packets at a 20-kHz frequency to one slave. The test was conducted for 2 minutes, and the EtherCAT packet size was 108 Bytes.

The test was conducted with different types of cables and lengths.

- Cat 7 cable was Draka® UC900 Super Screen 27
- Cat 6 cable was GigaSPEED XL® 3071 ETL

The results can be seen in Table 29.

Table 29. Table Length Test Results

CABLE	LENGTH	CRC ERROR (2 minutes)	TOTAL PACKETS SENT (2 minutes)
Cat 7	3	0	2.400.000
Cat 7	30	0	2.400.000
Cat 7	50	0	2.400.000
Cat 6	150	0	2.400.000

3.2.2.3.3 EMC/EMI Test Results

The TIDA-00299 design has been tested for EMI according to CISPR 11 / EN55011 class A radiated emissions. For EMC immunity, the design has been tested according to IEC61800-3 and IEC61000-6-2 for ESD, EFT, Surge, and Conducted RF with reference to standards IEC61000-4-2, IEC61000-4-4, IEC61000-4-5, respectively.

The design is compliant to these standards and exceeds the voltage requirements according to IEC61800-3 EMC immunity requirements for second environment. A summary is shown in the following tables and more details in the following sections.

Table 30. EMC Immunity Test Results Summary

REQUIREMENTS					TIDA-00299 MEASUREMENTS		
Port	**Phenomenon**	**Basic Standard**	**Level**	**Performance (Acceptance) Criterion**	**Level**	**Performance (Achieved) Criterion**	**Test**
Enclosure ports	ESD	IEC61000-4-2	+/- 4 kV CD or 8 kV AD, if CD not possible	B	+/- 8 kV CD	B	PASS (EXCEED)
Ports for control lines and DC auxiliary supplies <60 V	Fast transient Burst (EFT)	IEC61000-4-4	+/- 2 kV / 5 kHz or 100 kHz, capacitive clamp	B	+/- 4 kV	A	PASS (EXCEED)
	Surge 1,2/50 us, 8/20 us	IEC61000-4-5	+/-1 kV. Since shielded cable >20 m, direct coupling to shield (2 Ohm/500 A)	B	+/- 2 kV	A	PASS (EXCEED)
	Conducted RF	IEC61000-4-6	0.15-80 MHz,10V/m, 80% AM (1 kHz)	A	10 V/M	A	PASS

The performance (acceptance) criterion is defined as follows:

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

Table 31. Radiated Emissions (EMI) Test Results Summary

REQUIREMENTS			TIDA-00299 MEASUREMENTS	
Phenomenon	**Basic Standard**	**Category 2 Electric Field Strength Component Quasi-Peak dB(uV/m)**	**Measured Minimum Margin To Limit**	**Test**
EMI	EN55011/CISPR 11 class A	40 (30-230 MHz) 47 (230-1000 MHz)	Horizontal: 6.9 dB (55.22 MHz) Vertical: 5.1 dB (99.743 MHz)	Pass

3.2.2.3.3.1 Test Setup

The TIDA-00299 design has been tested at the testing laboratory of CSA Group Bayern in Strasskirchen, Germany.

The TIDA-00299 with the test equipment is shown in Figure 25.

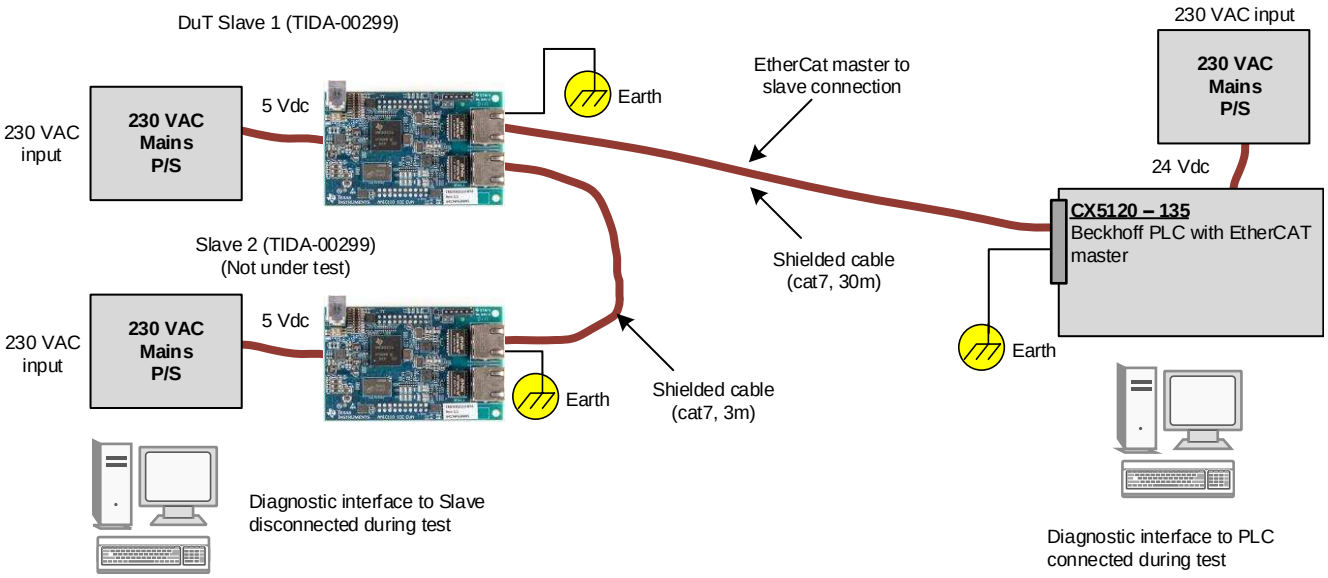

Figure 25. TIDA-00299 Test Equipment Overview for EMI/EMC Tests

Images of the specific test setups for EMI, ESD, EFT and Surge are shown in the following sections.

During the time of the test, the Beckhoff PLC was programmed as shown in Table 32.

Table 32. Beckhoff PLC Settings During Test

PARAMETER	VALUE
Ethernet Protocol	EtherCAT
EtherCAT transmit rate	20 kHz
EtherCAT packet size	108 Bytes

The EtherCAT system manager is used to read out error data, Lost Frames of the master, TX/RX error, crc errors on each active slave port.

Counter reading if a lost link has happened based on the EtherCAT state machine (ESM).

- When slave leaves Operational (OP) mode a counter is set high
- Counting the packets which could have been transmitted during a lost link

This can be seen in Figure 26.

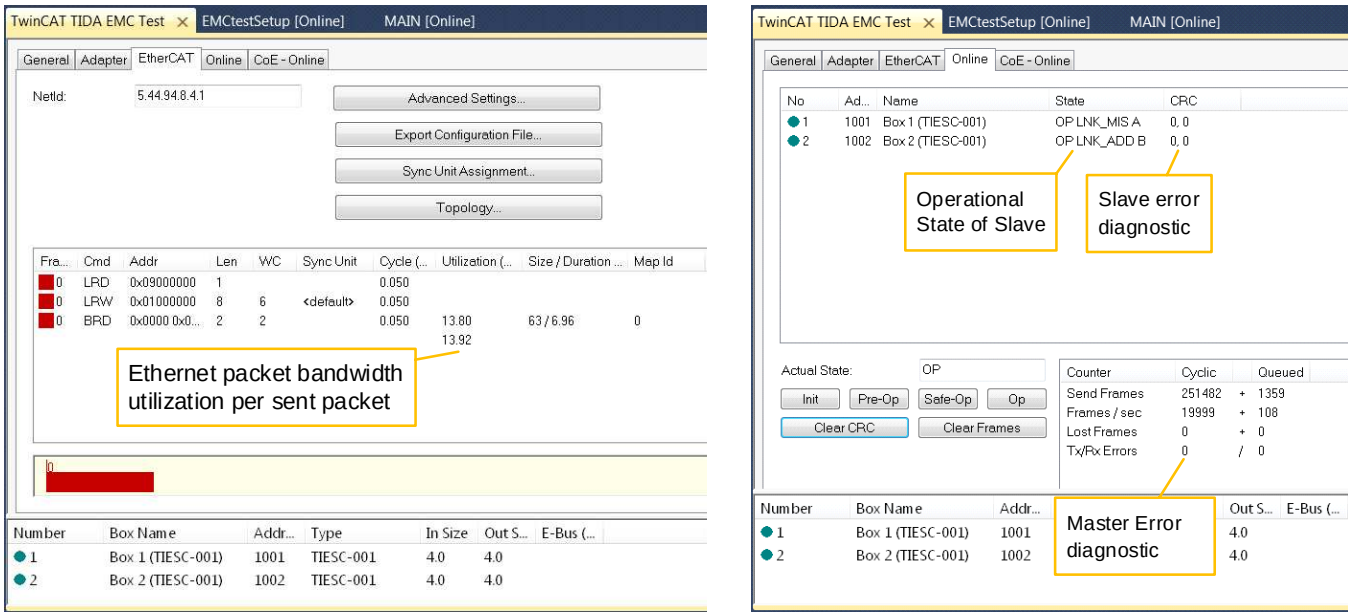

Figure 26. PLC System Manager Diagnostic Options Used During Tests

The Beckhoff PLC payload was a counter which the slaves can do error diagnostics on. This error diagnostic compares the payload and defines on the counter how many consecutive errors was had during the test and how many single errors was had, here the limit was set to up to 8 consecutive errors and then 9 or more errors.

The TIDA-00299 hardware was tested without connection between GND and Earth expect for the EFT to test for optimized performance during the EFT test. It is planned at a later time to do the remaining test with the optimized EFT EARTH and GND connection and both options of FAST link Down, R49 = R66 =1 M Ohm and C44 = C67 = 10 nF. See Figure 6 for details on the Earth-to-GND connection of Ethernet port 1 using R49 and C44 for Ethernet port 2 R66. C67 was used in the same configuration.

3.2.2.3.3.2 IEC-61000-4-4 EFT Test Results

Figure 27 shows the EFT test setup for the TIDA-00299. The capacitive clamp can be seen in the front of the image.

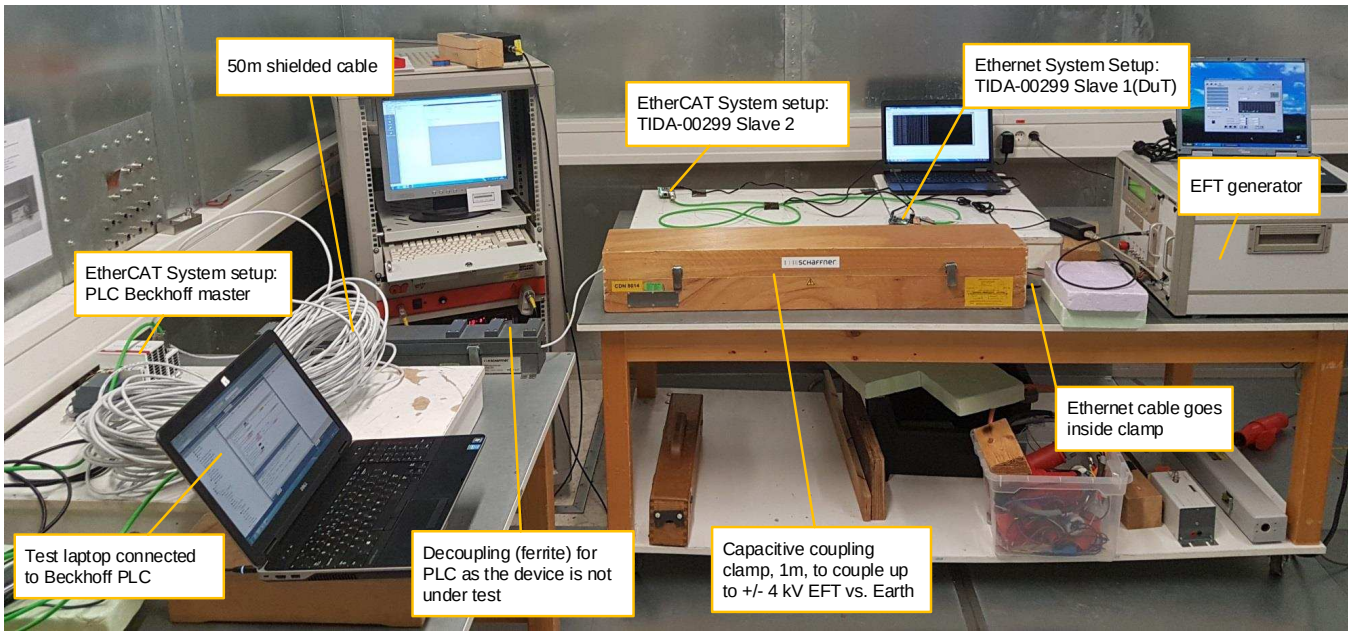

Figure 27. IEC61000-4-4 EFT Test Setup for TIDA-00299

During the EFT test, the system setup was as described in Section 3.2.2.3.3.1.

The EFT test was done with populated Earth-to-GND connection to R_{49} = R_{66} = 1 M Ohm and C_{44} = C_{67} = 10 nF. With an update to the TIDA-00299 design, the following results could be observed.

The final test results are shown in Table 33.

Table 33. IEC-61000-4-4 EFT Test Results for TIDA-00299 With Populated RC GND to Earth Connection

PHENOMENON	BASIC STANDARD	LEVEL	ACHIEVED PERFORMANCE CRITERION	COMMENT
EFT	IEC61000-4-4	+/- 1 kV / 5 kHz, cap clamp	A	
EFT	IEC61000-4-4	+/- 2 kV / 5 kHz, cap clamp	A	
EFT	IEC61000-4-4	+/- 4 kV / 5 kHz, cap clamp	A	Not required per IEC61800-3
EFT	IEC61000-4-4	+/- 1 kV / 100 kHz, cap clamp	A	
EFT	IEC61000-4-4	+/- 2 kV / 100 kHz, cap clamp	A	
EFT	IEC61000-4-4	+/- 4 kV / 100 kHz, cap clamp	A	Not required per IEC61800-3

Here it can be seen that the TIDA-00299 passes the tests as per IEC61800-3. The readout diagnostic result of the Beckhoff PLC is shown in Table 34.

Table 34. IEC-61000-4-4 EFT Diagnostic Results for TIDA-00299

			Beckhoff PLC DIAGNOSTIC RESULTS		
PHENOMENON	**BASIC STANDARD**	**LEVEL**	**LINK LOST**	**FRAME LOST**	**Tx / Rx ERROR**
EFT	IEC61000-4-4	+/- 1 kV / 5 kHz, cap clamp	0	0	0/0
EFT	IEC61000-4-4	+/- 2 kV / 5 kHz, cap clamp	0	0	0/0
EFT	IEC61000-4-4	+/- 4 kV / 5 kHz, cap clamp	0	0	0/0
EFT	IEC61000-4-4	+/- 1 kV / 100 kHz, cap clamp	0	0	0/0
EFT	IEC61000-4-4	+/- 2 kV / 100 kHz, cap clamp	0	0	0/0
EFT	IEC61000-4-4	+/- 4 kV / 100 kHz, cap clamp	0	0	0/0

This test was also conducted with unpopulated Earth-to-GND connection where only criterion B was achieved.

This shows the importance of the earth connection of the system while testing the TIDA-00299 design and surrounding building blocks. When testing EMC performance, there are significant improvements of system performance when optimizing the external circuit of the PHY. The chosen connection must be optimized per subsystem.

This system aspect needs to be optimized to achieve best performance and it is important to consider every earth connection which is present in the system.

The other tests were done previously and were conducted with unpopulated Earth-to-GND connection.

3.2.2.3.3.3 IEC-61000-4-2 ESD Test Results

The ESD test setup is shown in Figure 28. The ESD strike was applied to the RJ45 case / shield of port 1 and port 2. Both RJ45 cases were electrically connected with a conductive copper foil. During the ESD test, the system setup was as described in Section 3.2.2.3.3.1.

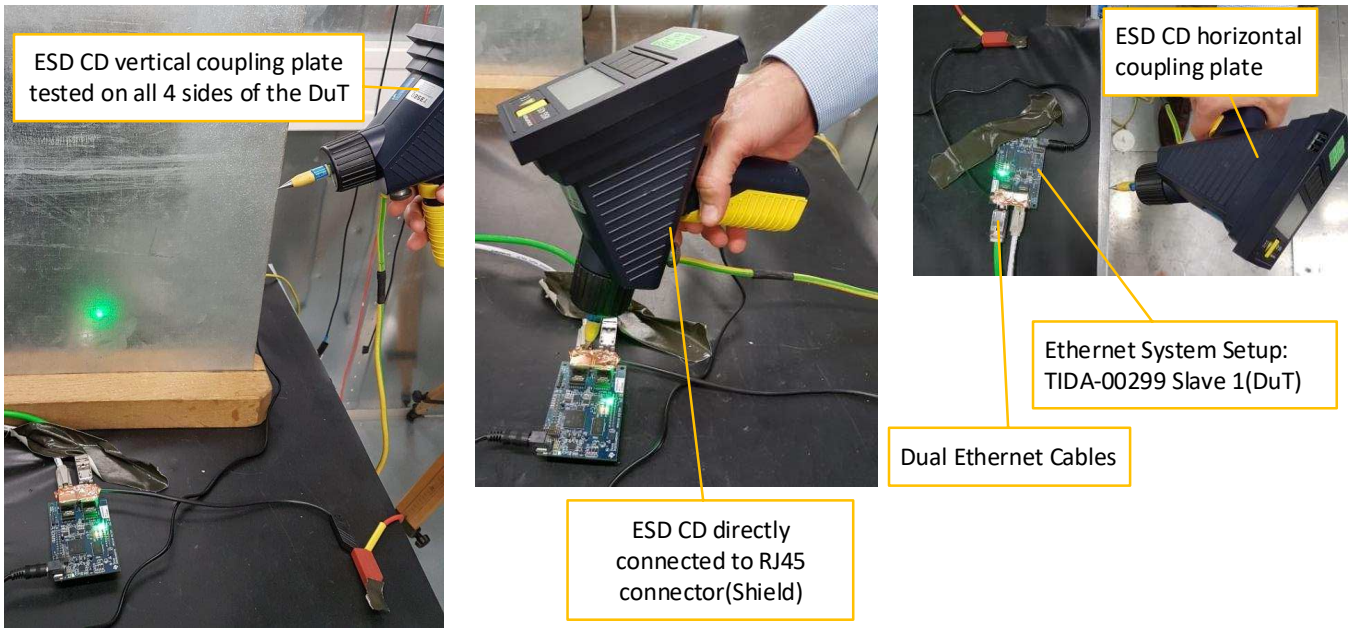

Figure 28. IEC61000-4-2 Test Setup for TIDA-00299 Showing CD

Table 35 shows the complete ESD test results for contact and air discharge at voltage levels which also exceed the requirements per IEC618000-3. This is marked accordingly.

These tests have been conducted with unpopulated Earth-to-GND connection.

Table 35. IEC-61000-4-2 ESD Test Results for TIDA-00299

PHENOMENON	BASIC STANDARD	LEVEL	ACHIEVED PERFORMANCE CRITERION	COMMENT
ESD	IEC61000-4-2	+/- 4 kV Contact discharge	B	
ESD	IEC61000-4-2	+/- 6 kV Contact discharge	B	Not required per IEC61800-3
ESD	IEC61000-4-2	+/- 8 kV Contact discharge	B	Not required per IEC61800-3
ESD	IEC61000-4-2	+/- 8 kV Contact discharge, vertical and horizontal	B	Not required per IEC61800-3

Class B was claimed when there was a network utilization reduction and a link loss. This link was automatically reconnected without a power reset of the system.

Table 36. IEC-61000-4-2 ESD Diagnostic Results for TIDA-00299

			Beckhoff PLC DIAGNOSTIC RESULTS		
PHENOMENON	BASIC STANDARD	LEVEL	LINK LOST	FRAME LOST	Tx / Rx ERROR
ESD	IEC61000-4-2	+/- 2 kV Contact discharge	0	3	0/1
ESD	IEC61000-4-2	+/- 4 kV Contact discharge	1	14	0/3
ESD	IEC61000-4-2	+/- 6 kV Contact discharge	1	23	0/6
ESD	IEC61000-4-2	+/- 8 kV Contact discharge	1	67	0/2
ESD	IEC61000-4-2	+/- 8 kV Contact discharge, vertical and horizontal	1	27	0/5

Table 36 shows the readout diagnostic result of the Beckhoff PLC.

3.2.2.3.3.4 IEC-61000-4-5 Surge Test Results

The surge test setup for the TIDA-00299 is shown in Figure 29.

These tests have been conducted with unpopulated Earth-to-GND connection.

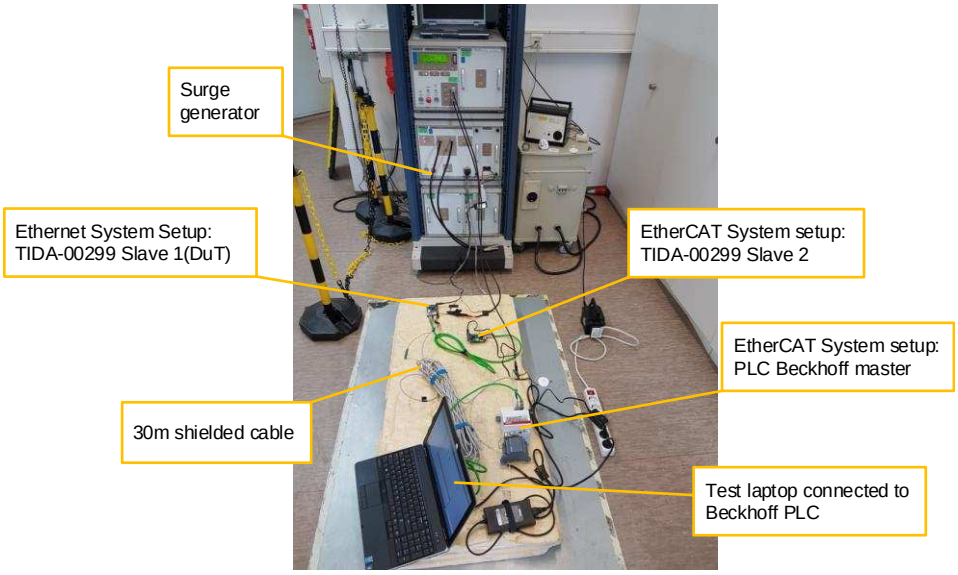

Figure 29. IEC61000-4-5 Surge Test Setup for TIDA-00299

During the EFT test, the system setup was as described in Section 3.2.2.3.3.1. The test results are shown in Table 37.

Table 37. IEC-61000-4-5 Surge Test Results for TIDA-00299

PHENOMENON	BASIC STANDARD	LEVEL	ACHIEVED PERFORMANCE CRITERION	COMMENT
Surge	IEC61000-4-5	+/- 0.5 kV, 2-ohm / 500 A (20 m shielded cat7 Ethernet cable)	A	Exceeds IEC61800-3, since only class B required
Surge	IEC61000-4-5	+/- 1 kV, 2-ohm / 500 A (20 m shielded cat7 Ethernet cable)	A	Exceeds IEC61800-3, since only class B required
Surge	IEC61000-4-5	+/- 2 kV, 2-ohm / 500 A (20 m shielded cat7 Ethernet cable)	A	Exceeds IEC61800-3, since only class B required

3.2.2.3.3.5 IEC-61000-4-6 Conducted RF Test Results

The conducted RF test setup and coupler for TIDA-00299 is shown in Figure 30.

These tests have been conducted with unpopulated Earth-to-GND connection.

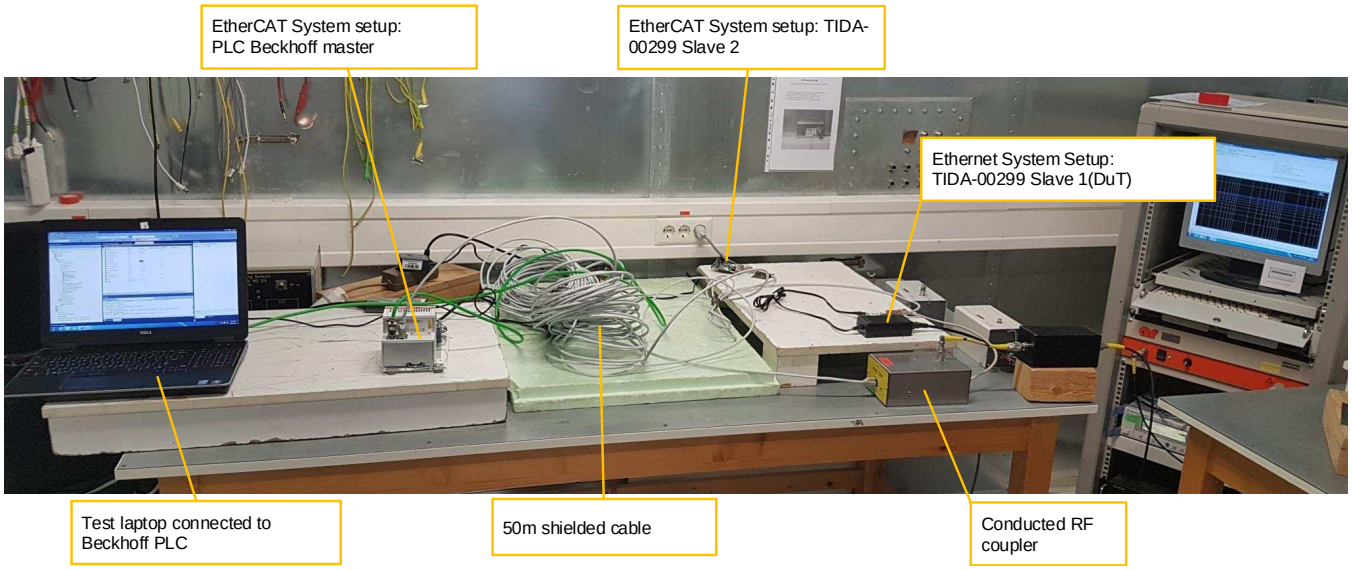

Figure 30. IEC61000-4-6 Conducted RF Test Setup for TIDA-00299

During the EFT test, the system setup was as described in Section 3.2.2.3.3.1. The test results are shown in Table 38.

Table 38. IEC-61000-4-6 Conducted RF Test Results for TIDA-00299

PHENOMENON	BASIC STANDARD	LEVEL	ACHIEVED PERFORMANCE CRITERION	COMMENT
Conducted RF	IEC61000-4-6	0.15-80 MHz, 10 V/m, 80% AM (1kHz)	A	

3.2.2.3.3.6 EN55011 CISPR 11 Radiated Emission Test Results

The TIDA-00299 meets EN55011/CSPR 11 class A requirements for category 2 with at least **5.1 dB** of margin (far-field measurements at 125 Mhz, vertical polarization). The minimum margin in horizontal polarization was **6.9 dB** at 125 MHz, also.

An automatic pre-test with near-field measurement (3-m antenna distance to device under test) was used to identify the frequencies of maximum EMI in each horizontal and vertical polarization as preparation for the final test with 10-m antenna distance.

Figure 31 shows the test setup of the final measurement with 10-m antenna distance to device under test.

These tests have been conducted with unpopulated Earth-to-GND connection.

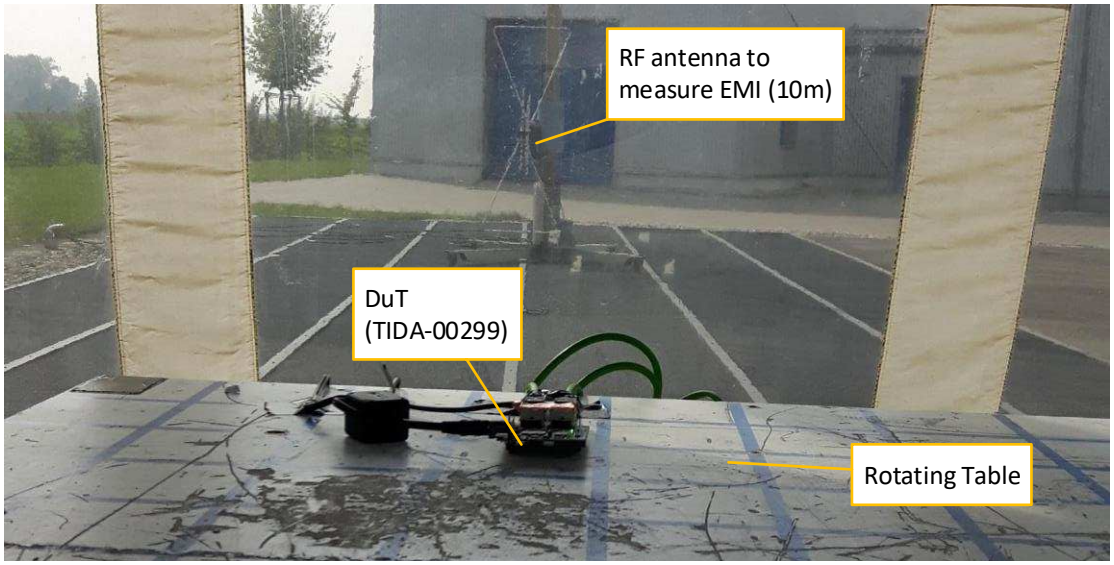

Figure 31. EN55011 / CISPR 11 Test Setup for Far-Field With 10-m Antenna Distance to TIDA-00299 DuT

The following two tables show the measured spectral density with the final measurement with 10-m antenna at the critical frequencies identified during the pre-test. As mentioned previously, the minimum margin was 6.9 dB in vertical and 5.1 dB in horizontal polarization, each at 125 MHz.

Table 39. Measured EMI Spectrum (Quasi-Peak) According to EN55011, 10-m far-field, Horizontal Polarization

FREQUENCY	READING (dBuV)	CORRECTION	VALUES (dBuV / m)	LIMIT (dBuV / m)	MARGIN (dB)
MHz	QP (Quasi-Peak)	dB	QP	QP	QP
87.6	17.0	13.6	30.6	40	9.4
99.80	14.8	15.0	29.8	40	10.2
125.01	17.4	17.5	34.9	40	5.1
250.01	9.7	17.6	27.3	47	19.4
445.50	0.3	22.6	22.9	47	24.1

Table 40. Measured EMI Spectrum (Quasi-Peak) According to EN55011, 10-m Far-Field, Vertical Polarization

FREQUENCY	READING (dBuV)	CORRECTION	VALUES (dBuV / m)	LIMIT (dBuV / m)	MARGIN (dB)
MHz	QP (Quasi-Peak)	dB	QP	QP	QP
60.0	3.5	18.9	22.4	40	17.6
125.01	15.6	17.5	33.1	40	6.9
156.05	4.4	19.5	23.9	40	16.1
250.01	8.9	17.6	26.5	47	20.5
275.00	3.0	18.3	21.3	47	25.7

3.2.2.3.3.7 Pre-Test Results With 3-m Antenna Distance

Figure 32 shows the test setup of the pre-test measurement with 3-m antenna distance to device under test.

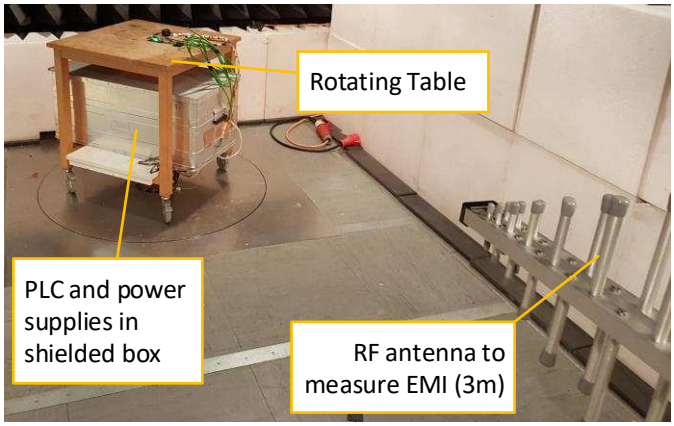

Figure 32. Automatic Pre-Test Setup for EMI With 3-m Antenna Distance to DuT (TIDA-00299)

A pre-test was done to identify the critical frequencies on each polarization. This test has been done in a chamber with a 3-m distance to the antenna.

Table 41. Pre-Test Equipment Setup

TYPE	NAME
Antenna	A5_VULB9168_24-14-007
Cable	A5_Cable_50-13-018
Cable	A5_Cable_50-13-019
Preamplifier	Ohm1_MTS TVV-695_50-01-059
Receiver	Ohm1_FSP7_11-05-002
Turntable	CO1000

The measured spectrum of the pre-test is shown on the following two figures for horizontal and vertical polarization.

Due to the shorter distance of 3 m instead of 10 m, the threshold for EN55011 for radiated EMI is higher by 10 dB too and set as shown in the following pictures.

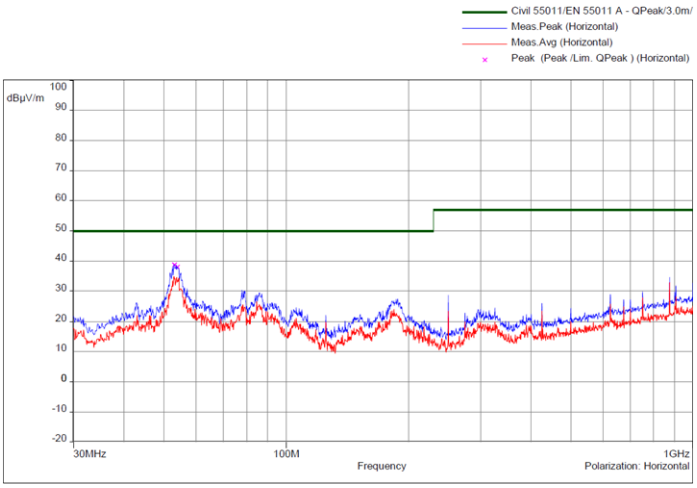

Figure 33. Measured EMI Spectrum According to EN55011, 3-m Near-Field, Horizontal Polarization (Pre-Test)

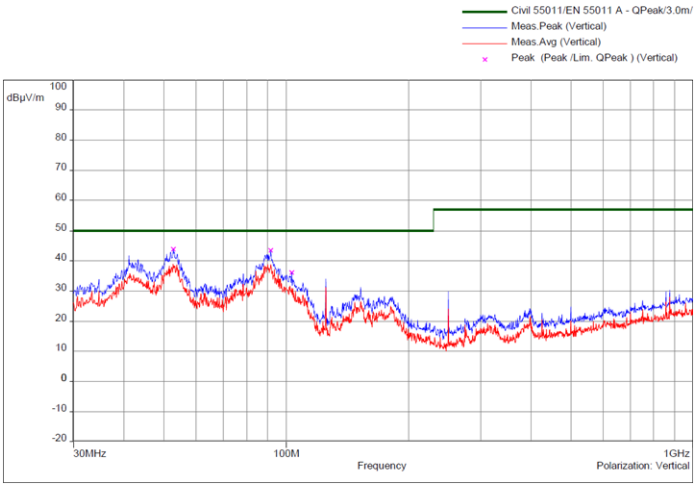

Figure 34. Measured EMI Spectrum According to EN55011, 3-m Near-Field, Vertical Polarization (Pre-Test)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00299.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00299.

4.3 PCB Layout

The design uses an eight-layer PCB. Figure 35 shows the layer stack.

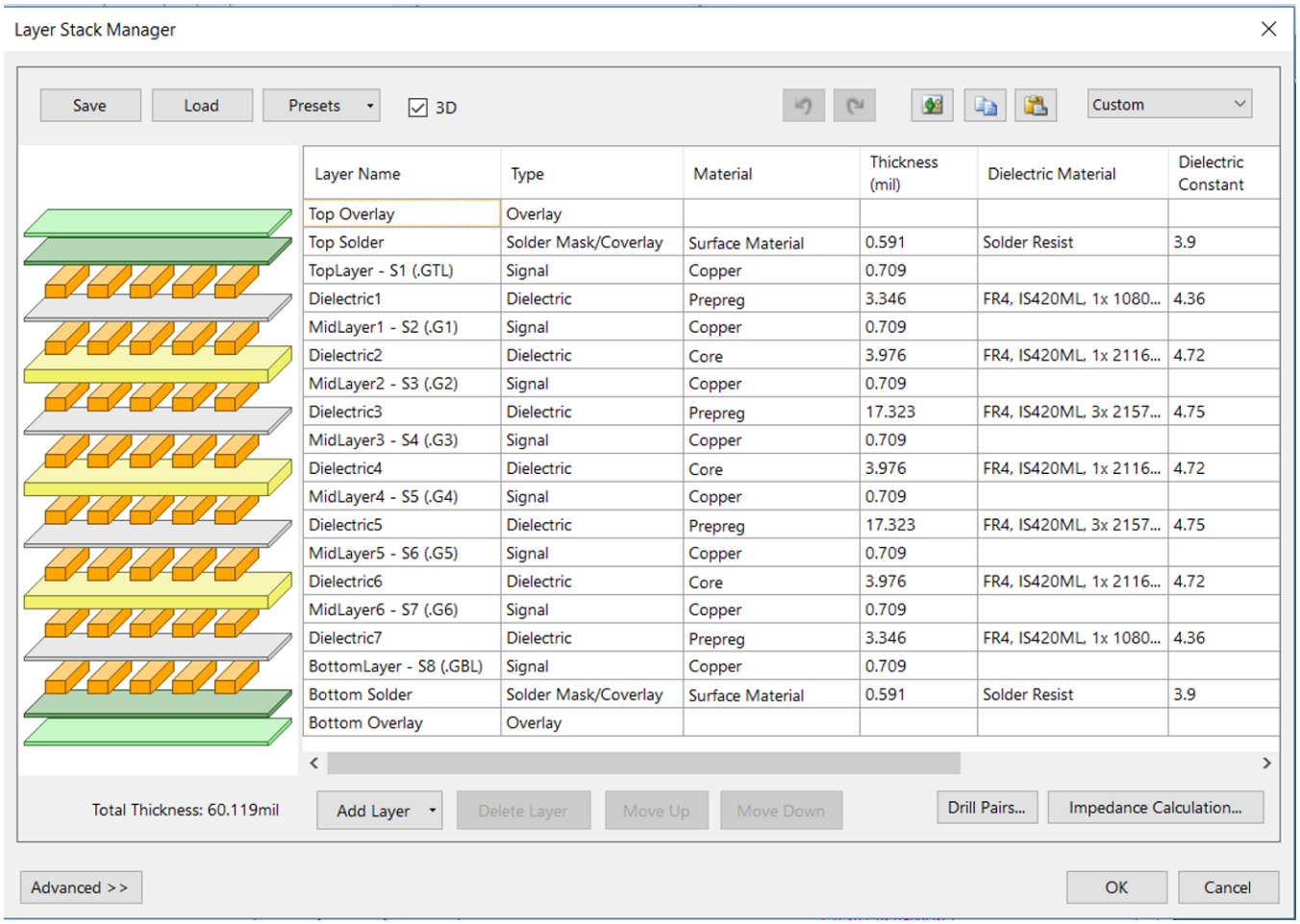

Figure 35. Layer Stack

Layers S2, S4, and S7 are used as ground planes, S5 is used as a power plane, and S1, S3, S6, and S8 are used as signal layers. This setup provides ground current return paths for the signal planes, which are as short as possible.

The applied layout guidelines can be found in the datasheets of the TI parts used in this TI Design.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00299.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00299.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00299.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00299.

5 Software Files

To download the software files, see the Processor SDK software package at Processor SDK.

For details, see Section 2.2.2

6 Terminology

ACRONYM	DESCRIPTION
ESC	EtherCAT slave controller
PDI	Process data interface
ETG	EtherCAT technology group
IEC	International electrotechnical commission
CTT	Compliance test tool
PHY	Physical layer
MAC	Media access control
MII	Media-independent interface
PMIC	Power management integrated circuit

7 Related Documentation

1. Texas Instruments, *Sitara*, Wiki Page
2. Texas Instruments, *AMIC110*, Wiki Page
3. *EtherCAT Technology Group*
4. Beagle Board, *BeagleBone Black*
5. Texas Instruments, *C2000 Delfino MCUs F28379D LaunchPad Development Kit*, LAUNCHXL-F28379D Tools Folder
6. IEC 61800-3:2017, *Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods*
7. Texas Instruments, *AMIC110 Sitara SoC*, AMIC110 Datasheet (SPRS971)
8. Texas Instruments, *Powering the AM335x With the TPS650250*, User's Guide (SLVU731)
9. Texas Instruments, *SN74LV244A Octal Buffers and Drivers With 3-State Outputs*, SN74LV244A Datasheet (SCLS383)
10. Texas Instruments, *SN74LVC2G66 Dual Bilateral Analog Switch*, SN74LVC2G66 Datasheet (SCES325)
11. Texas Instruments, *TPS650250 Power Management IC for Li-Ion Powered Systems*, TPS650250 Datasheet (SLVS843)
12. Texas Instruments, *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*, DP83822HF, DP83822IF, DP83822H, DP83822I Datasheet (SNLS505)
13. Texas Instruments, *AM335x and AMIC110 Sitara Processors Technical Reference Manual*, User's Guide (SPRUH73)

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8 About the Author

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to A Revision **Page**

- Changed information in *Description* 1
- Added TMDXICE110 to design resources 1
- Changed information in *Features* 1
- Added information to *System Description* 2
- Added *EC61800-3 EMC Immunity Standard* section 2
- Deleted information regarding other industrial protocols 3
- Changed information in *TIDA-00299 Specifications* table 6
- Added information to *DP83822: 10/100 Mbit Ethernet PHY* 11
- Added information to *MII Between DP83822 and the AMIC110* 13
- Changed *PHY to RJ-45 Connection on the TIDA-00299* image 13
- Added *Earth-to-GND Connection* section 14
- Changed information in *Equipment for TIDA-00299 Performance Tests* table 28
- Added information regarding TwinCat 3 to *System Performance* section 36
- Changed section 3.2.2.3.1 title from *System Performance* to *EtherCAT Conformance Test Tool* 36
- Added *EtherCAT Cable Length Test* section 37
- Added *EMC/EMI Test Results* section 38

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