TI Designs: TIDA-01367
High-Power Voltage Regulator Reference Design for Cavium ThunderX2® Arm® Processors

Description

This reference design uses the TPS53679 multiphase controller and CSD95490Q5MC Smart Power Stages to implement a high-performance design suitable for powering networking application-specific integrated circuits (ASICs). The dual outputs of the controller target a 240-A, 0.8-V core rail with a six-phase design and a 20-A, 0.85-V auxiliary rail. The smart power stages and integrated PMBus™ allow for easy output voltage setting and telemetry of key design parameters. The design enables configuration, smart VID adjustment, and compensation adjustment of the power supply, while providing monitoring of input and output voltage, current, power, and temperature. TI's Fusion Digital Power™ Designer is used for programming, monitoring, validation, and characterization of the system.

Resources

TIDA-01367	Design Folder
TPS53679	Product Folder
CSD95490Q5MC	Product Folder
Fusion Digital Power™ Designer	Product Folder

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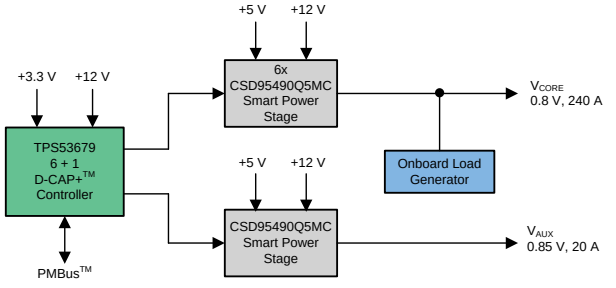
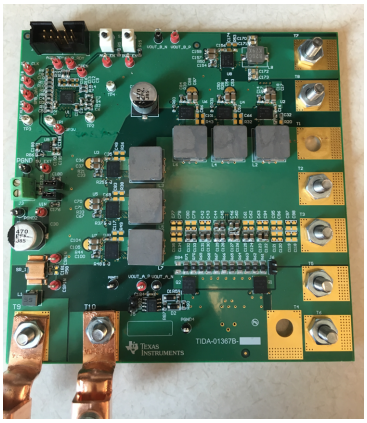
Features

- Dual Rail 6+1 Design – High-Powered Core Rail and Single-Phase Auxiliary Rail
- Peak Efficiencies of 90% and 91% for Core and Aux Rails
- D-CAP+™ Modulator for Superior Current-Sharing Capabilities and Transient Response
- PMBus Compatibility for Output Voltage Setting and Telemetry for V_{IN}, V_{OUT}, I_{OUT}, and Temperature
- Full Compensation Tuning Through PMBus
- Minimal Output Capacitance Required for ±5% V_{OUT} Target With 150-A Step

Applications

- Enterprise Switches
- Enterprise Server Motherboards
- Networking ASICs
- Microservers
- Netowork Attached Storage





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1 System Description

The *High-Power Voltage Regulator Reference Design for Cavium ThunderX2® Arm® Processors* is a power-dense, high-performance design targeted at powering complex networking ASICs that can be found anywhere from enterprise switches to server motherboards. The dual-output multiphase controller and TI's proprietary Smart Power Stages allow for an integrated design, which, when compared to more traditional discrete designs, eliminates a number of passive components and reduces the printed-circuit board (PCB) layout area. High-performance networking ASICs require excellent thermal performance, efficiency, and a fast transient response from their voltage regulators while also requiring on-the-fly optimization through PMBus. This design meets all the criteria with a minimal number of output capacitors and a simple thermal solution. Most importantly, a 240-A maximum current on the core rail can be handled with only a six-phase solution while competing vendors may require eight or more phases for the same specifications.

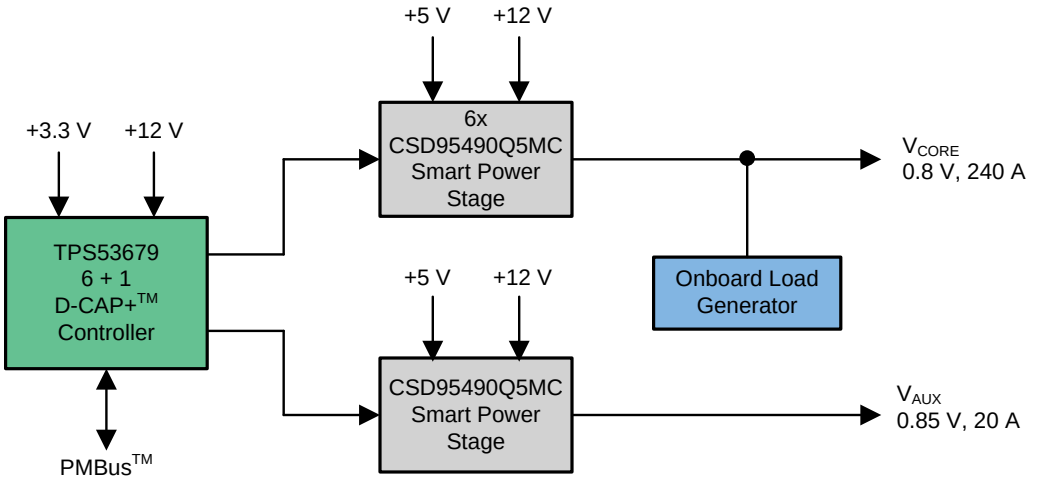
1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input supply	12 V, ±5%
DC tolerance	± 2%
AC tolerance	± 5%
Switching frequency	600 kHz
Nominal output voltage – core rail	0.8 V
Max output current – core rail	240 A
TDC current – core rail	200 A
DC load line – core rail	0.5 mΩ
Max load step – core rail	150 A at 500 A/µs
Number of phases – core rail	6
Nominal output voltage – aux rail	0.85 V
Max output current – aux rail	20 A
TDC current – aux rail	16 A
DC load line – aux rail	—
Max load step – aux rail	10 A at 20 A/µs
Number of phases – aux rail	1

2 System Overview

2.1 Block Diagram



2.2 Highlighted Products

2.2.1 TPS53679 – Dual-Channel D-CAP+™ Step-Down Multiphase Controller With NVM and PMBus™ for VR13 Server V_{CORE} Applications

- Configurable for 6+1 or 5+2 scenarios
- Programmable loop compensation through PMBus
- Configurable with non-volatile memory (NVM) for low external component counts
- Dynamic phase shedding with programmable current threshold for optimizing efficiency at light and heavy loads
- PMBus™ system interface for telemetry of voltage, current, power, temperature, and fault conditions
- 5 mm × 5 mm, 40-pin, QFN PowerPad™ integrated circuit package

2.2.2 CSD95490Q5MC – 75-A Synchronous Buck NexFET™ Power Stage With DualCool™ Packaging

- 75-A continuous current capability
- 95% system efficiency at 25 A
- Up to 1.25-MHz switching frequencies supported
- Temperature-compensated bidirectional current sense signal
- Analog temperature output and fault monitoring
- High-density, low-inductance, SON 5x6-mm package

2.3 System Design Theory

The D-CAP+ modulator of the TPS53679 controller is integral to the high-performance of this reference design. This modulator allows the control loops of both rails to remain stable over a wide range of operating conditions because the transfer function is insensitive to variations in input voltage, load current, and phase number. Phase margins of 71.1° and 52.7° were measured for the core and auxiliary rails, respectively, with crossover frequencies of 64 kHz and 79 kHz. Placing the unity gain frequencies higher than 1/10 the switching frequencies allows for a faster transient response that can keep V_{OUT} within its regulation limits during large load steps, such as the 150-A step on the core rail. Stability is maintained even as the load current duty cycle and frequency are varied. Compensation can easily be adjusted through the PMBus using TI's Fusion graphical user interface (GUI), which allows the user to easily tune the design for a wide range of output filters, including using all ceramic output capacitors, should the design requirements change. At high load currents, the D-CAP+ modulator can keep all phase currents evenly balanced to avoid thermally stressing or damaging either the field-effect transistors (FETs), inductors, or load while maintaining tight output voltage regulation.

The CSD95490Q5MC Smart Power Stage features an optimized driver-FET solution in a thermally-efficient package that provides high efficiency up to 75 A of DC load current. Higher efficiency means lower power loss and thus excellent thermal performance, which allows for the high current requirements on the core rail to be met with only six phases as opposed to eight or more on competing solutions. Integrated fault monitoring and temperature reports back to the TPS53679 device and complements the PMBus functionality, which allows for operational telemetry, painless debug, validation, and configuration of the design. On-chip bidirectional current sensing offers increased accuracy compared to discrete circuitry and eliminates the requirement to implement and tune a direct current resistance (DCR) or resistor sense passive network.

3 Getting Started Hardware and Software

3.1 Hardware

The hardware for this design is as follows:

- 12-V, 20-A power supply
- 5-V, 1-A power supply
- 500-MHz oscilloscope with differential and passive probes
- Function generator capable of pulse with < 1-µs rise times (hook to J5 on load transient circuit)
- Digital multimeter
- USB interface adapter EVM

3.2 Software

This design uses TI's Digital Fusion Power Designer software.

3.3 Test Setup

Figure 1 shows the test setup of this reference design.

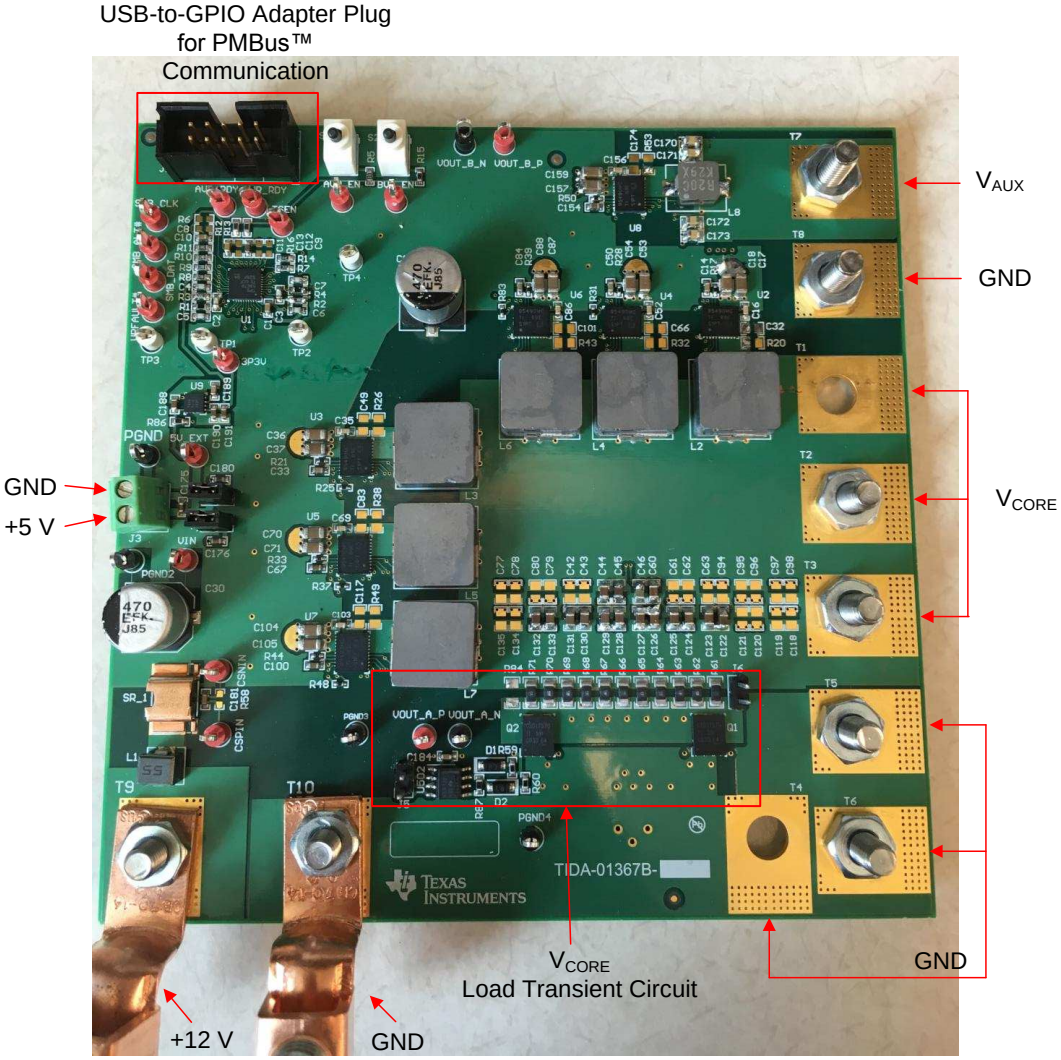


Figure 1. TIDA-01367 Test Setup

4 Test Results

4.1 Efficiency and Power Loss

For the core rail, a peak efficiency of 89.6% was measured at the target output voltage of 0.8 V at 45 A of load current (see Figure 2, Figure 3). An 85.1% efficiency was measured at the 200-A thermal design current (TDC). At an output voltage of 1 V, the peak efficiency of 91.1% came at 50 A while the TDC efficiency was 86.7%. Both curves include the inductor losses and VDD rail losses of the CSD95490Q5MC power stages. The full 240-A efficiency curve cannot be taken due to the max current capability of the electronic load rolling off for loads of 190 A to 200 A at output voltages less than 1 V. During testing, the DC loadline of this rail was disabled to get the high possible current range from the load.

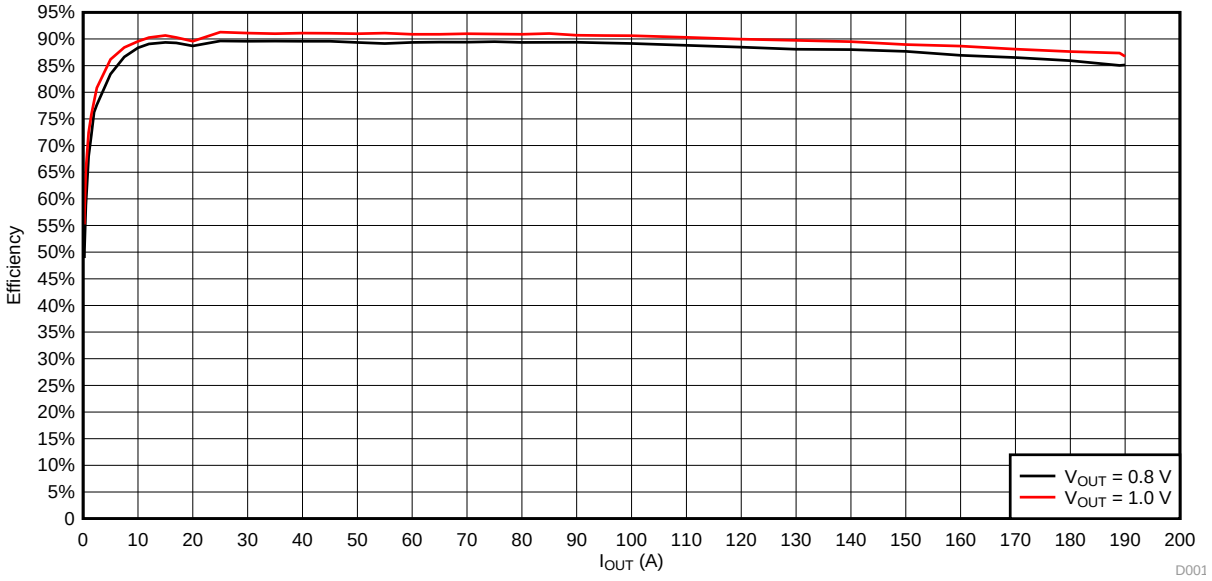


Figure 2. Core Rail Efficiency

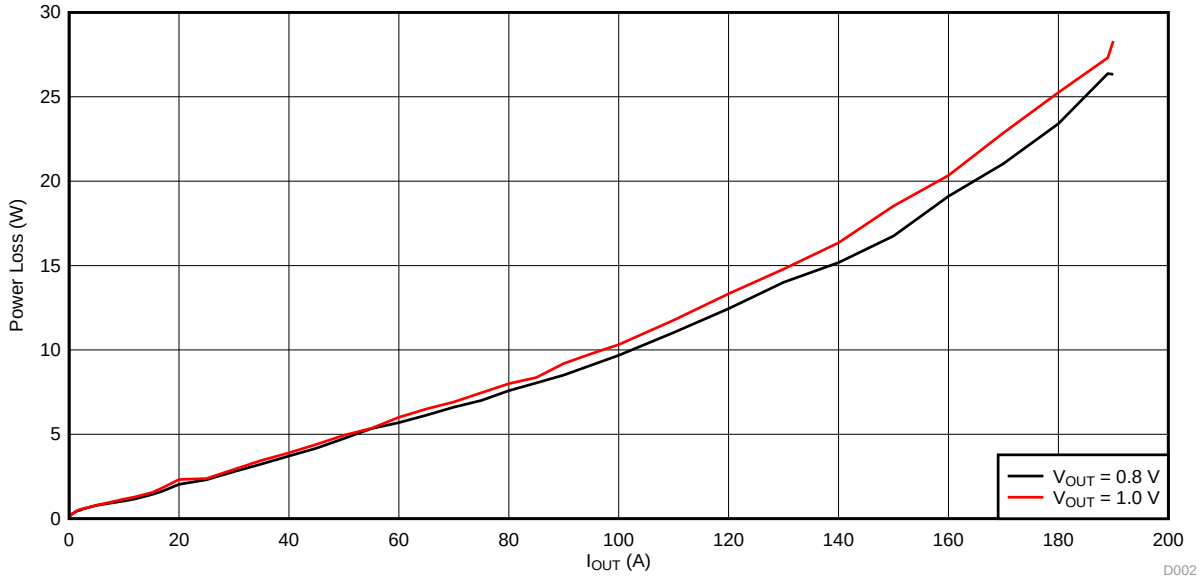


Figure 3. Core Rail Power Loss

Efficiency measurements on the single-phase auxiliary rail were more straightforward and a full 20-A curve was taken (see Figure 4, Figure 5). The inductor and VDD power stage loss are included in the results. A peak efficiency of 91% was measured at a load of 9 A and the 16-A TDC efficiency was 89.9% for an output voltage of 0.85 V.

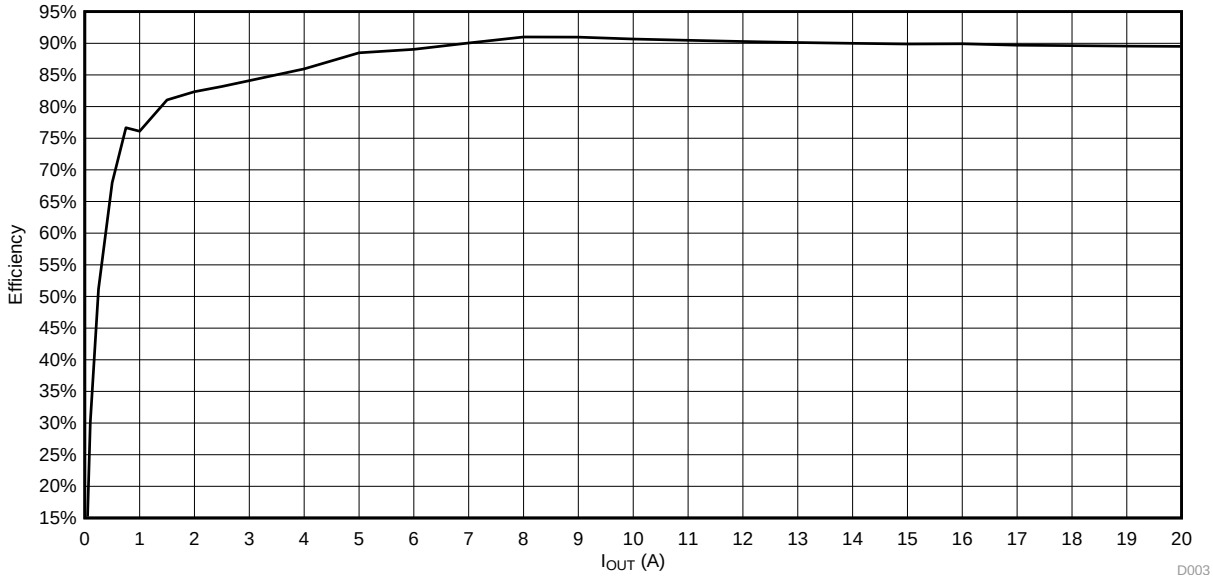


Figure 4. Auxiliary Rail Efficiency

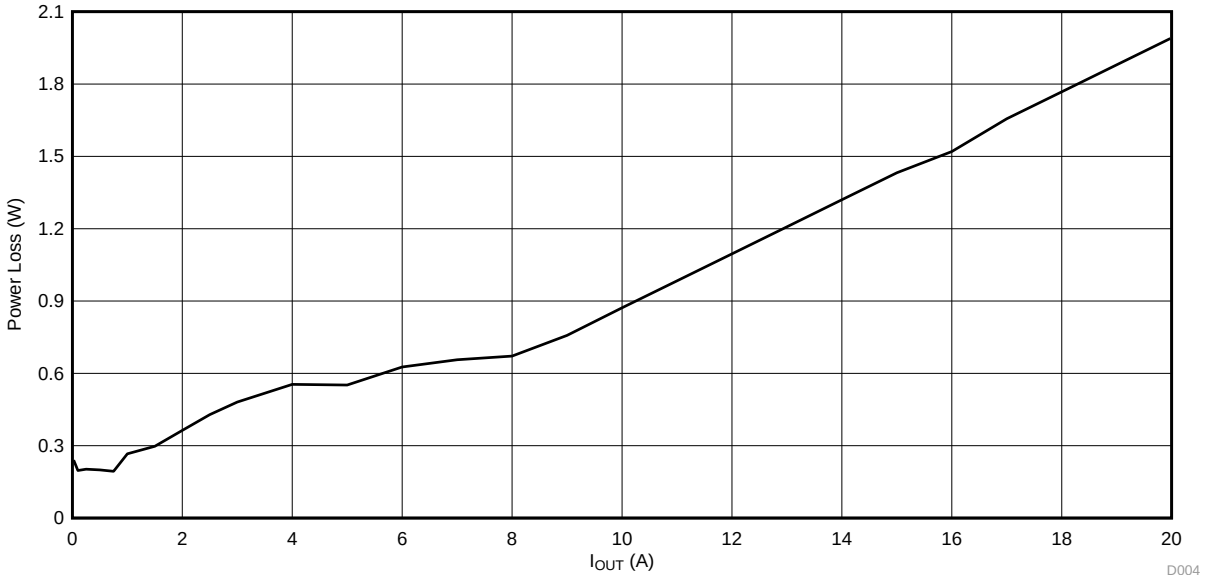


Figure 5. Auxiliary Rail Power Loss

4.2 Steady-State Regulation and Phase Ringing

Both rails of this design were tested for steady-state stability across their entire load ranges without recording any failures or anomalies. DC ripple remained within the design targets and the measured switching frequency was within the data sheet limits. Care was taken to ensure that the noise floor of the output voltage differential probe did not impact the results to cause false failures in output ripple or stability. TI recommends probing a phase node during testing to check against any possible questions regarding stability that may be attributed to a noisy differential probe. The design is likely stable if the switching frequency is consistent between phase pulses and varies within the TPS53679 data sheet limits. If an adequate differential probe is not available, a passive probe with tight ground connection should be used instead to verify the design.

Figure 6 and Figure 7 show the results from the core rail at 100 A and 200 A. Figure 8 and Figure 9 show the auxiliary rail results at 16 A and 20 A.

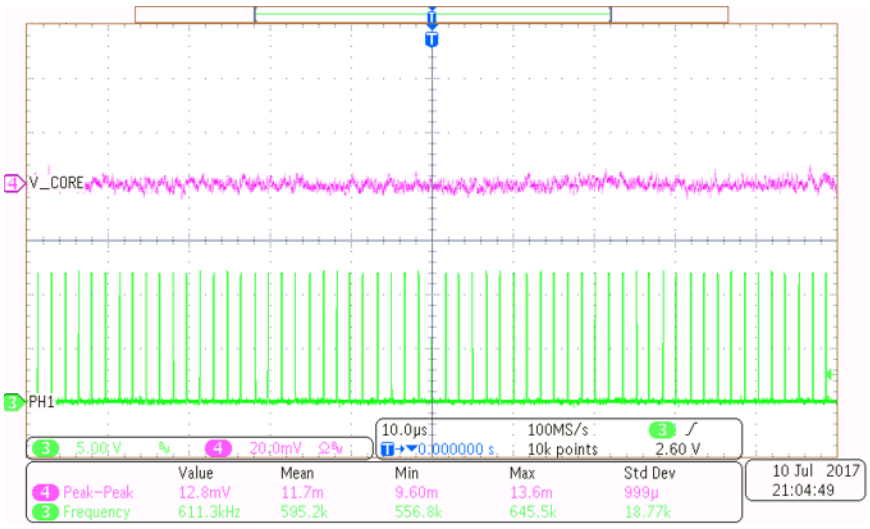


Figure 6. Core Rail — Steady State, 100 A

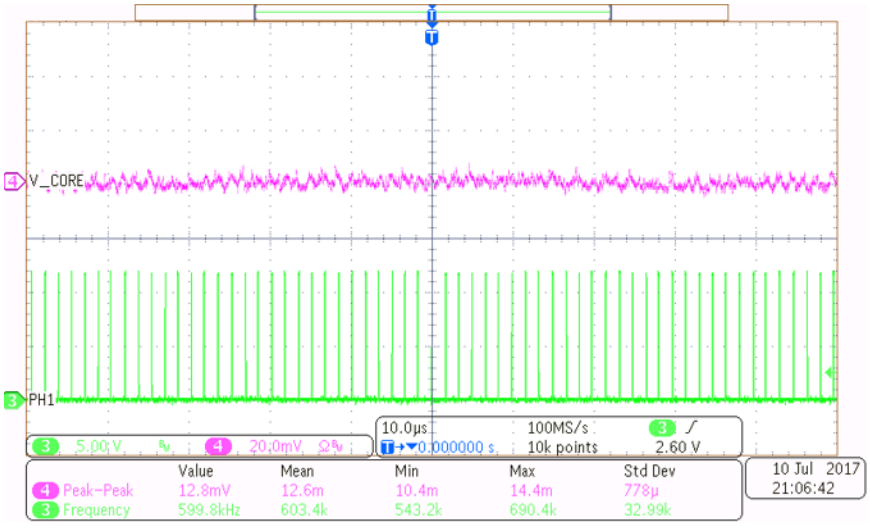


Figure 7. Core Rail — Steady State, 200 A

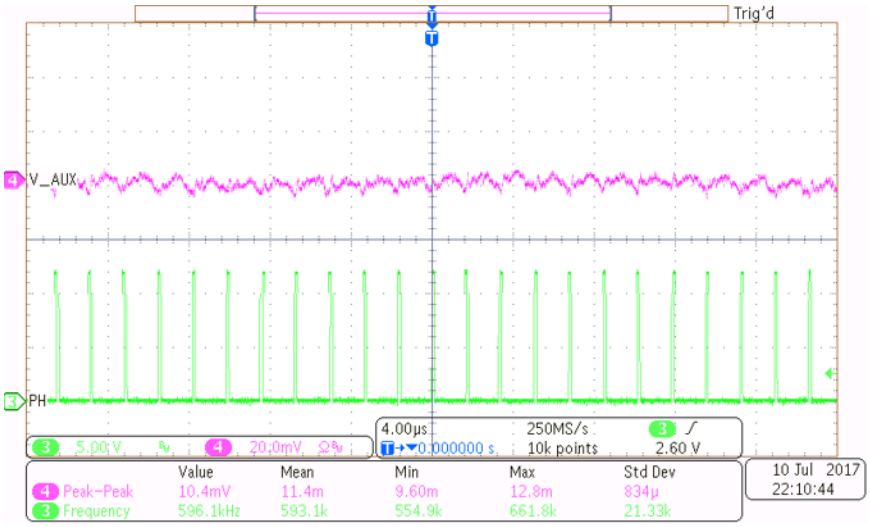


Figure 8. Auxiliary Rail — Steady State, 16 A

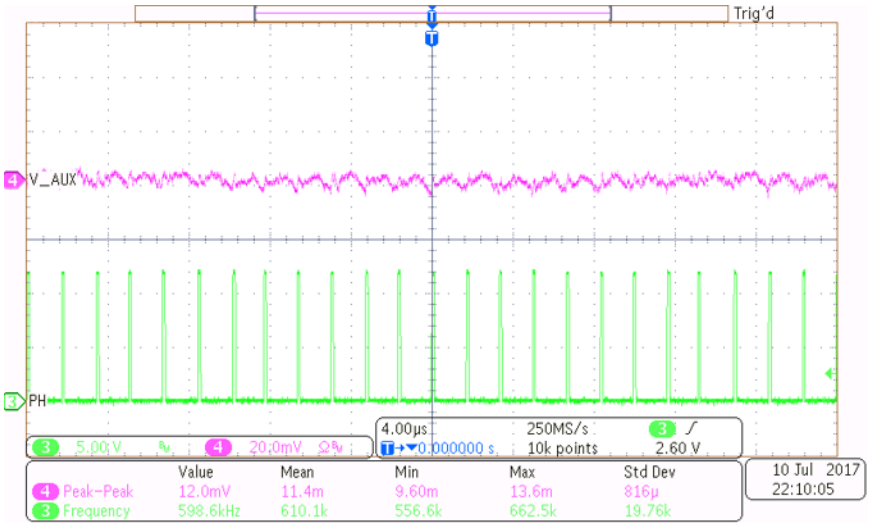


Figure 9. Auxiliary Rail — Steady State, 20 A

To ensure no possible damage to the power MOSFETs, the phase node was measured on the core rail to determine if shoot-through was occurring and if any ringing was within the CSD95490Q5MC data sheet specifications. Without any boot resistor or phase snubber in place, the phase nodes of the rail did not exhibit any issues across the entire load range (see Figure 10). However, the impact of several boot resistors and snubbers on efficiency were studied (see Figure 11) and the results are summarized in Table 2. If electromagnetic interference (EMI) concerns are present on the end application board, then an appropriate boot resistor or snubber should be used that minimizes the hit on efficiency.

The auxiliary rail showed identical results when tested in the same manner as the core rail.

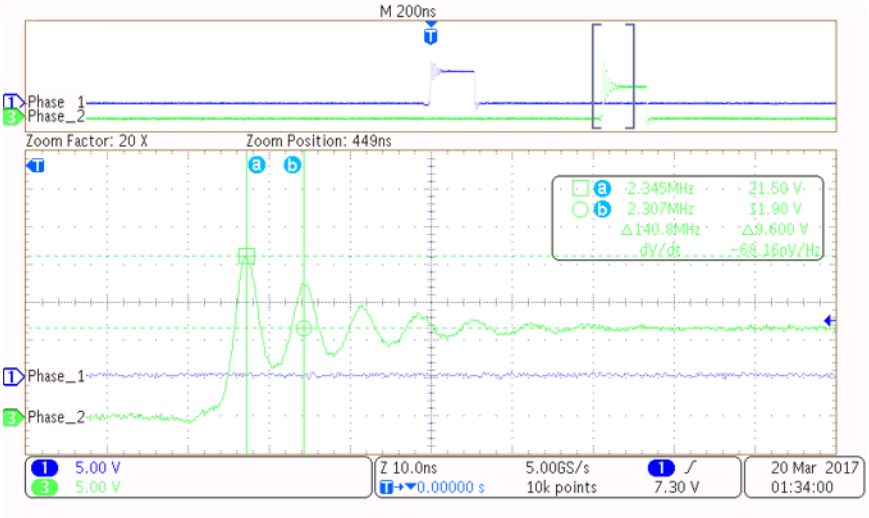


Figure 10. Phase Ringing — 200 A, No Snubber or Boot Resistor

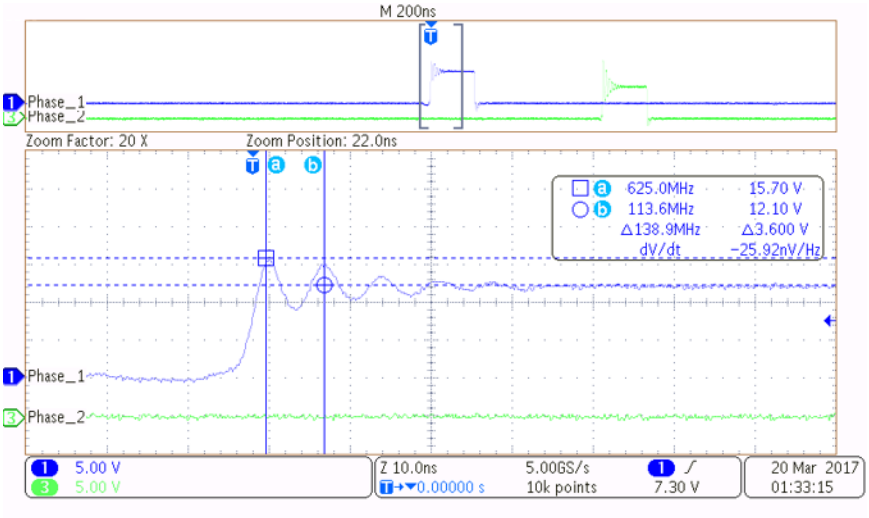


Figure 11. Phase Ringing — 200-A, 2-Ω Boot Resistor

Table 2. Phase Ringing Methods Effects on Efficiency

ADDITIONAL COMPONENTS	EFFICIENCY CHANGE	RINGING OUTSIDE DATA SHEET LIMITS (23 V FOR 10-ns MAX)
None	—	No
2-Ω boot resistor	–1.0%	No
1-Ω boot resistor	–0.5%	No
1-Ω + 1500-pF snubber	–0.75%	No

4.3 Transient Response

A load transient circuit was placed on the board close to the output of the core rail to generate the 150-A step at the fast slew rate of 500 A/µs. The single-step response (see Figure 12 and Figure 13) showed little to no undershoot and the expected 75 mV of droop from the DC loadline while the overshoot was less than the allowable 115 mV. The output voltage remained stable as the load duty cycle was swept from 10% to 80%, as Figure 14 shows. Minimal undershoot was once again measured and the overshoot was less than 115 mV. The transient circuit was able to hit the quick slew rate, but it could not handle load frequencies above 200 kHz and so a beat frequency check at 600 kHz could not be performed. However, Figure 15 shows that, as the frequency of the load step was swept up to 200 kHz, no instabilities were observed. A few faint traces show the overshoot occasionally exceeds 115 mV at high frequency but this can be mitigated on the end application board by placing small 0402 or 0201 ceramic capacitors between the ASIC power pins. On a demo board such as this, there is not much benefit to placing these capacitors because the distance from their footprints to the load would be too great, which negates their effect.

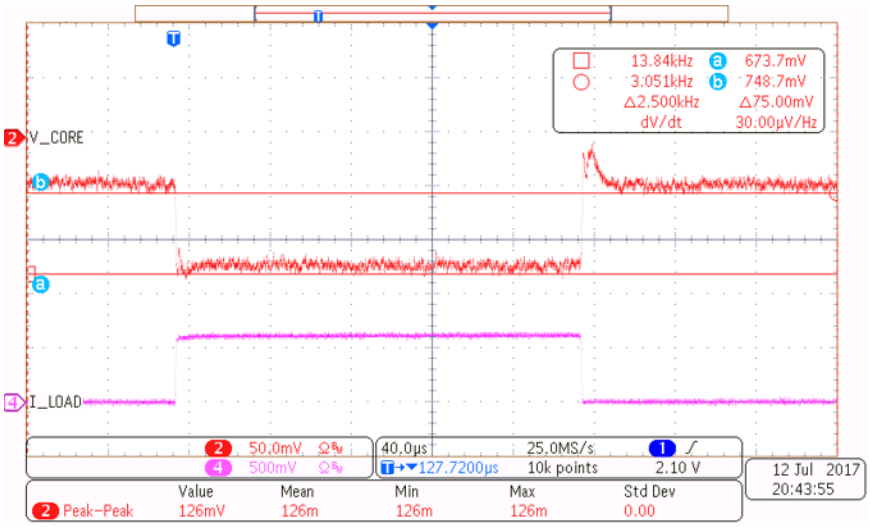


Figure 12. Core Rail — 90-A to 240-A Transient Undershoot, 20% Duty Cycle

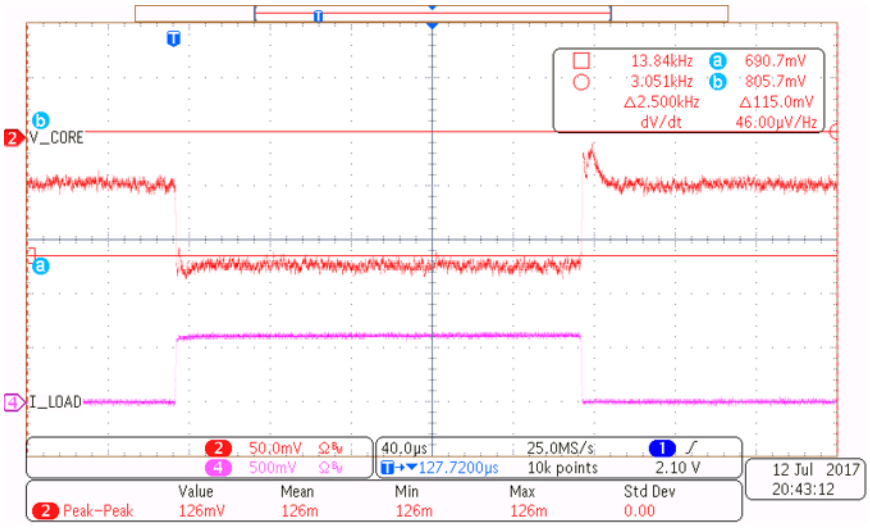


Figure 13. Core Rail — 90-A to 240-A Transient Overshoot, 20% Duty Cycle

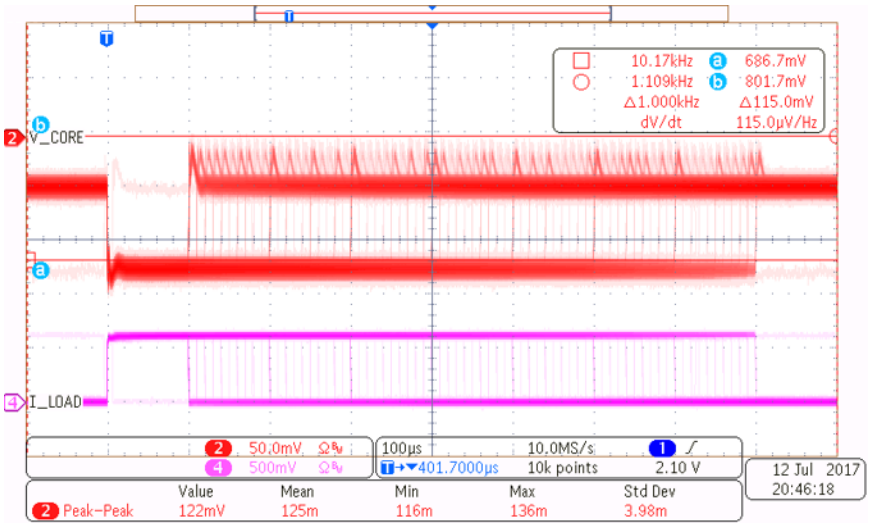


Figure 14. Core Rail — 90-A to 240-A Transient, 10% to 80% Duty Cycle Sweep

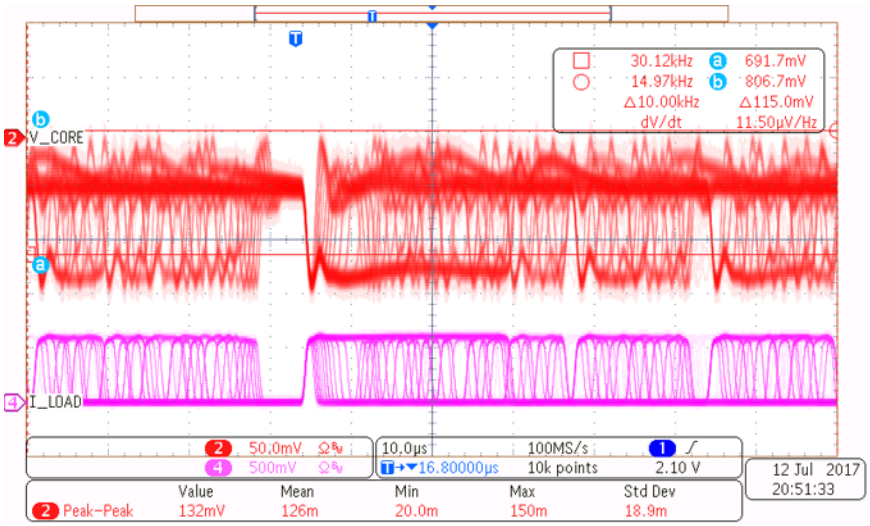


Figure 15. Core Rail — 90-A to 240-A Transient, 10-kHz to 200-kHz Load Frequency Sweep

A 10-A current step was applied to the auxiliary rail using an external load transient circuit, as the required slew rate was only 20 A/µs (see Figure 16). The transient response of the rail was also tested as the load duty cycle (see Figure 17) and frequency (see Figure 18) were swept across a wide range of values. No instabilities were observed during this sweep and the output voltage remained in its ±5% window around 0.85 V with the exception of some very-high frequency spikes. The spikes are easy to deal with on an end application board using the same method as the core rail with local decoupling using small 0201 or 0402 capacitors. Unlike with the core rail, the load frequency on the auxiliary rail can be swept up to the switching frequency of 600 kHz (see Figure 19) to check for beat frequencies. No beat frequencies were recorded and regulation on the output was maintained.

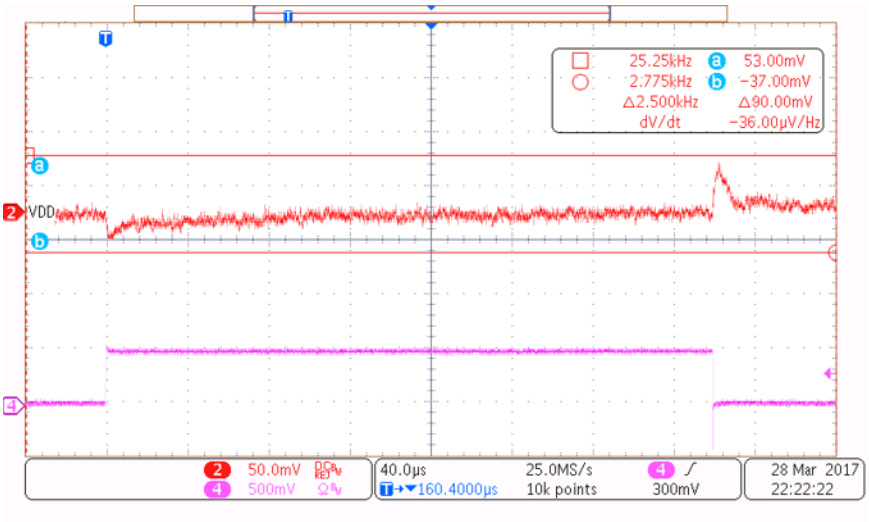


Figure 16. Auxiliary Rail — 10-A to 20-A Transient, 30% Duty Cycle

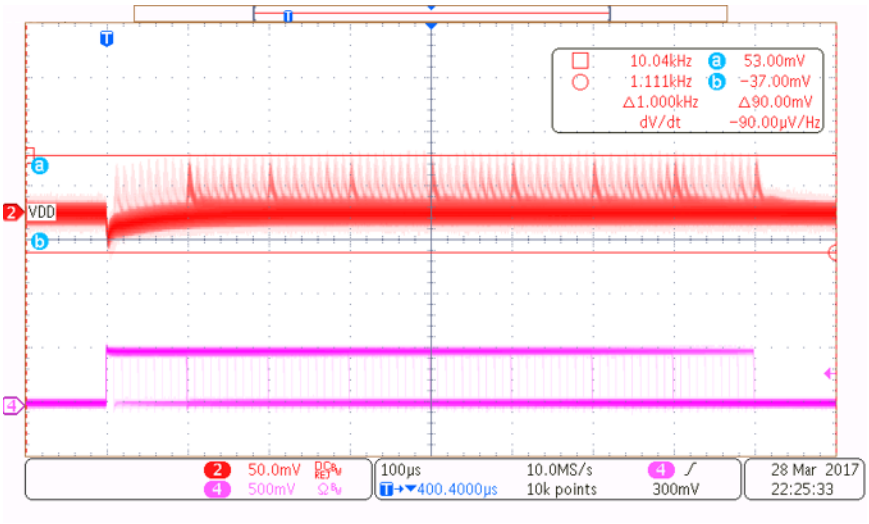


Figure 17. Auxiliary Rail — 10-A to 20-A Transient, 10% to 80% Duty Cycle Sweep

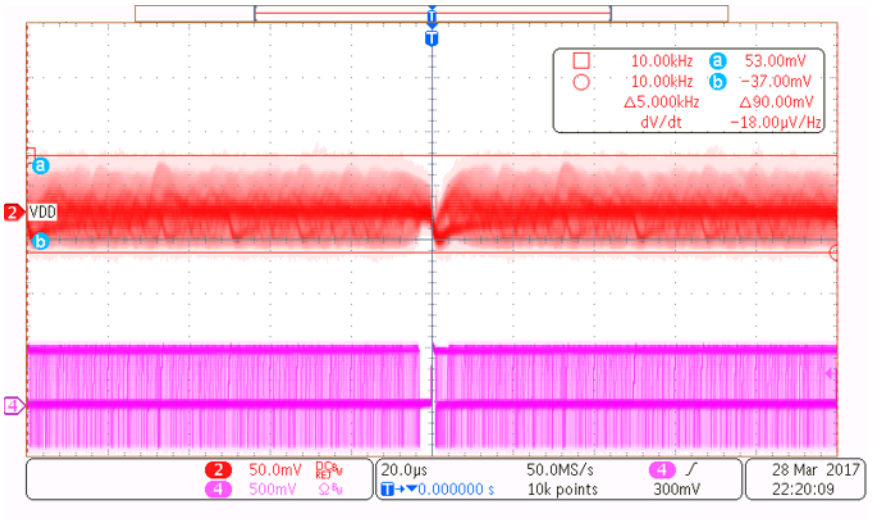


Figure 18. Auxiliary Rail — 10-A to 20-A Transient, 10-kHz to 200-kHz Load Frequency Sweep

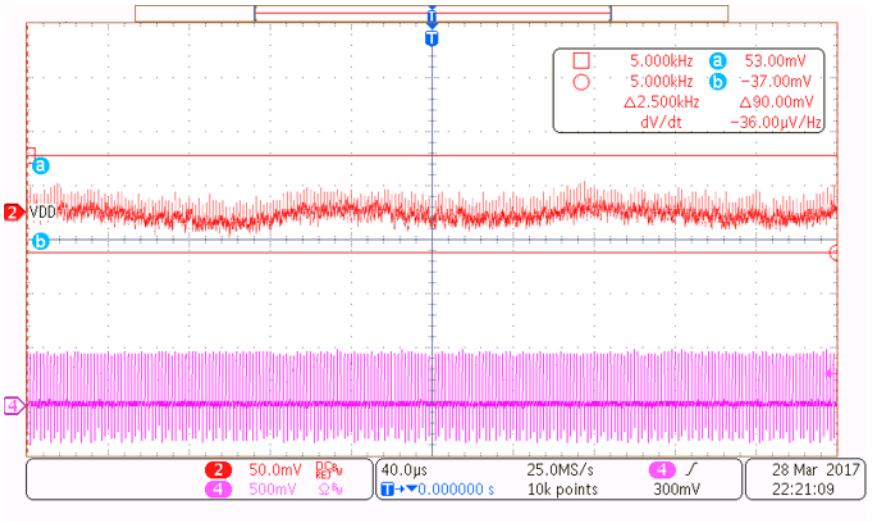


Figure 19. Auxiliary Rail — 10-A to 20-A Transient, 600-kHz Load Frequency

4.4 Bode Plots

Bode plots for each rail were taken using a network analyzer to determine the transfer function and to check the stability of the control loop for each rail. The core rail has a unity gain frequency of 64 kHz with a phase margin of 71.1°, which indicates stability. Marker 2 of Figure 20 is placed above the crossover point on a concerning peak in the plot which occurs above the crossover frequency. However, this peak remains well below 0 dB and has no impact on the stability of the core rail.

The auxiliary rail is also stable with a phase margin of 52.7° at a crossover of 79 kHz (see Figure 21).

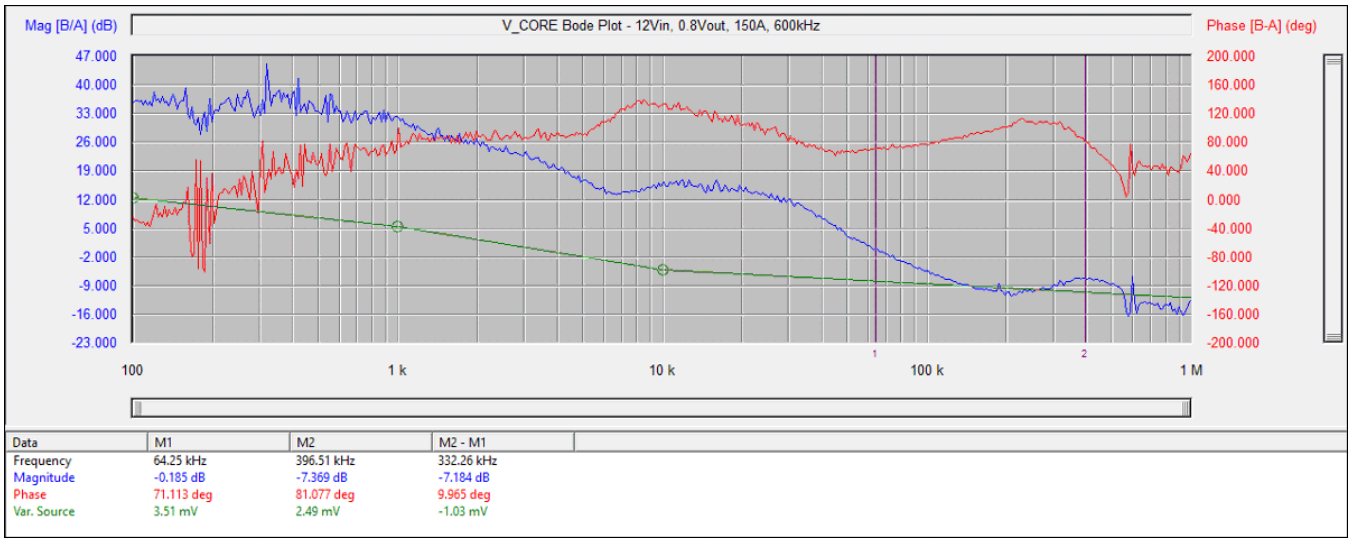


Figure 20. Core Rail Bode Plot

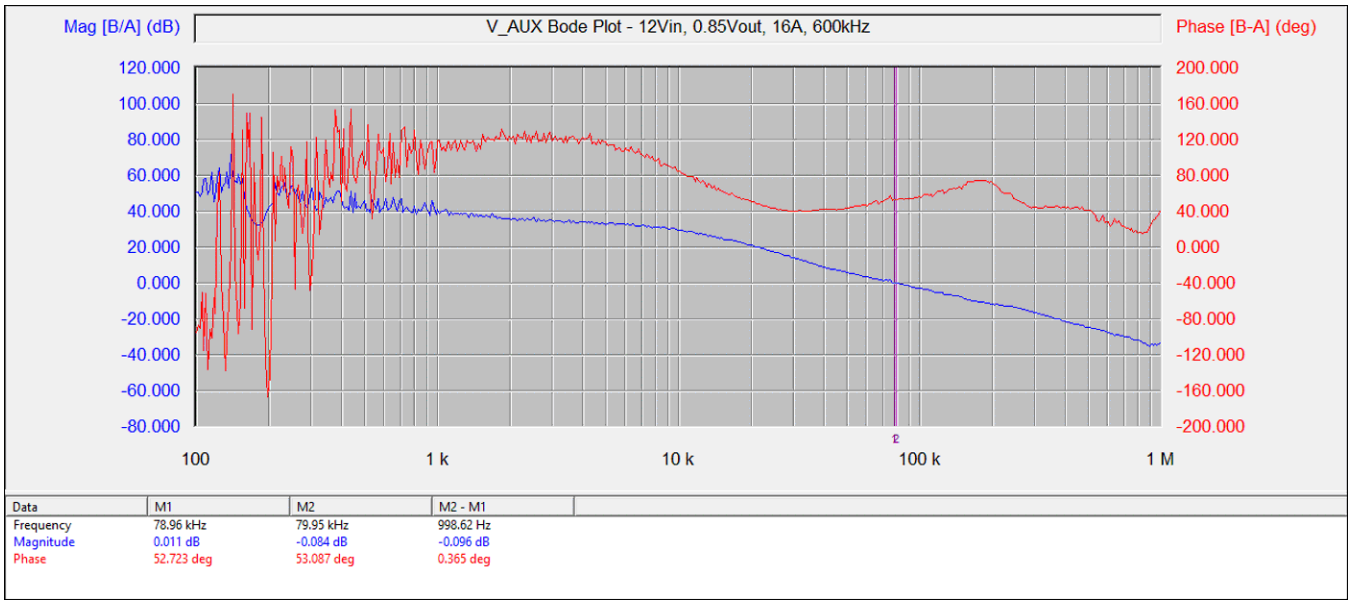


Figure 21. Auxiliary Rail Bode Plot

4.5 Thermal Performance

The thermal performance of the core rail was tested for 100-A and 200-A loads both with and without airflow. In a real application, a combination of heat sinks and airflow are likely to be used and thus testing without any airflow represents a worst-case scenario. The ambient temperature was 23°C for each test case and the design was allowed to soak for 5 minutes under load to reach thermal equilibrium. A speed of 500 ft/min was used when testing with airflow. As with the steady-state testing, the performance of the electronic load affected the testing and the DC loadline was disabled to obtain the largest possible output load from the equipment.

Performance was significantly increased with airflow. Case temperatures dropped by 10.8°C at 100 A and 20.2°C for 200-A loads.

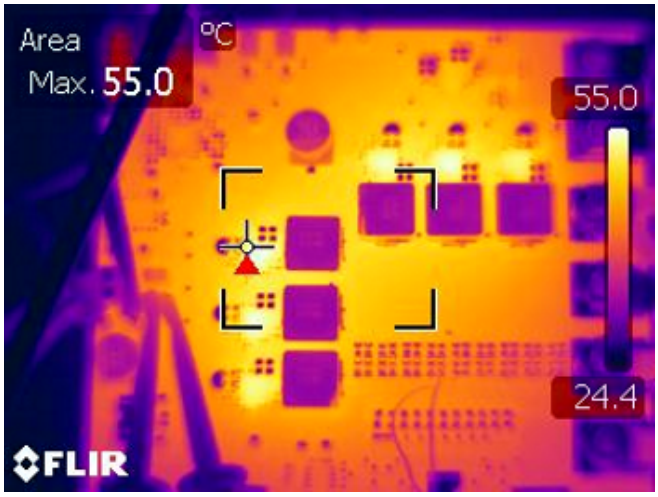


Figure 22. CSD95490Q5MC Temperature 100-A Load, No Airflow

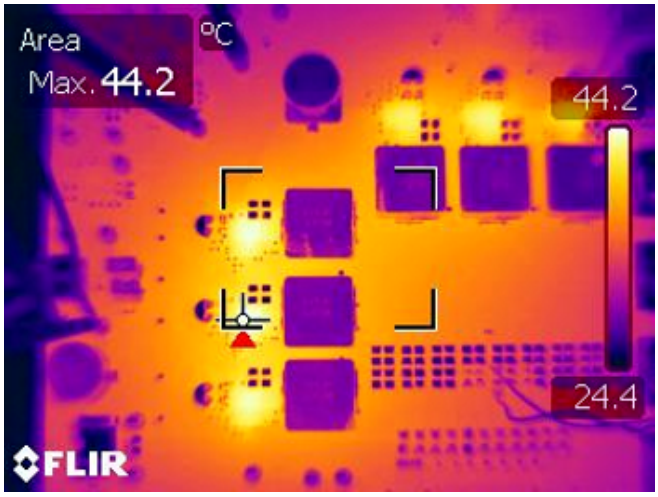


Figure 23. CSD95490Q5MC Temperature 100-A Load, 500-ft/min Airflow

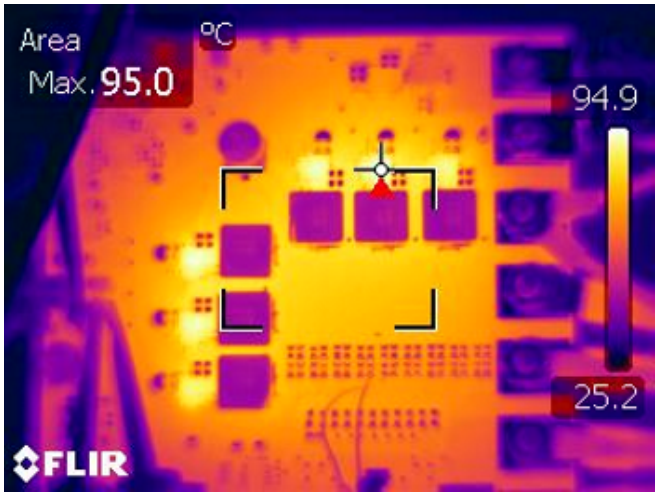


Figure 24. CSD95490Q5MC Temperature 200-A Load, No Airflow

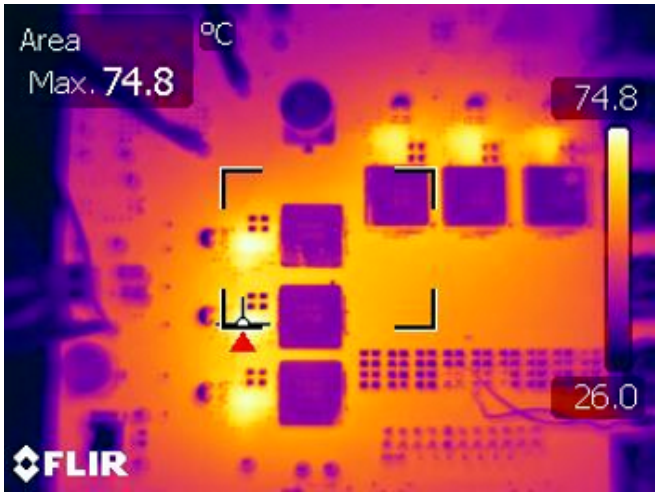


Figure 25. CSD95490Q5MC Temperature 200-A Load, 500-ft/min Airflow

During the thermal soak a snapshot of the PMBus telemetry was taken using Fusion GUI to check the phase current balancing. In all scenarios, the six-phase currents were within the ±2.5% specifications listed in the power stage data sheet (see Figure 26).

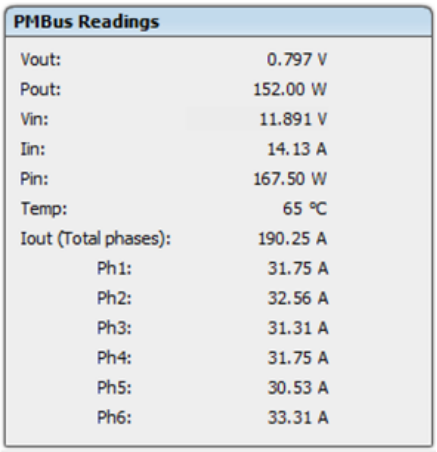


Figure 26. Temperature Monitoring and Phase Current Balancing Seen in Fusion GUI

4.6 Protection Circuitry

The overcurrent and overtemperature protections were tested on both outputs and showed identical performance on each one. Through the PMBus, each rail was configured to shut down for both conditions until the enable pin was toggled. A restart option after 20 ms is also available. When a fault occurs, the controller tri-states the phase node (or multiple phase nodes) and allows the output to decay according to the load current (see Figure 27 and Figure 29). At the same time, the PGOOD signal is also pulled low to indicate the loss of regulation. During the overcurrent shutdown in Figure 27, the output voltage can be observed swinging below ground due to the electronic load trying to maintain the load current. In a real application this action would not occur and V_{CORE} would simply decay to 0 V.

During testing, the status of the system was monitored through Fusion GUI (see Figure 28 and Figure 30) to check for both the warning and fault flags that are triggered as either the current or temperature exceeds the preset limits. No issues were observed and the part responded per expectations for both overcurrent and temperature shutdown. Note that the trip limits of the rail (as seen in the GUI under test) were lowered to speed up testing, as this was only a basic functionality check.

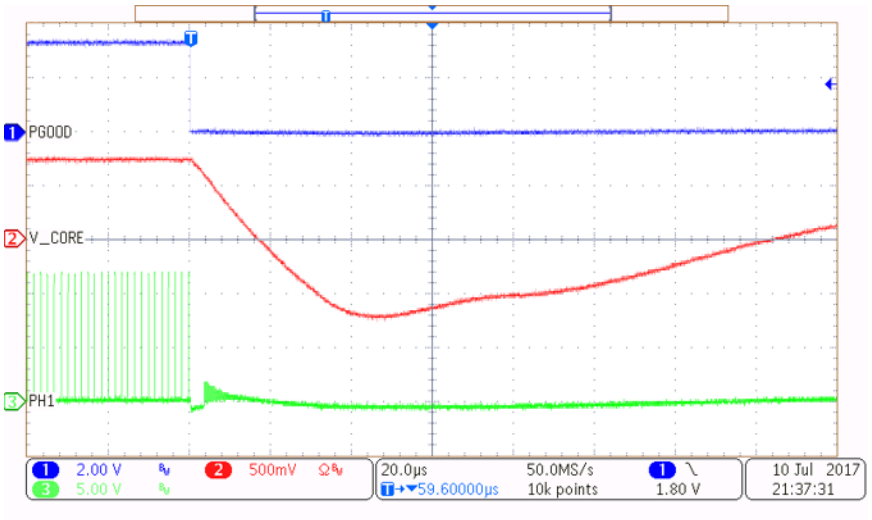


Figure 27. Overcurrent Shutdown

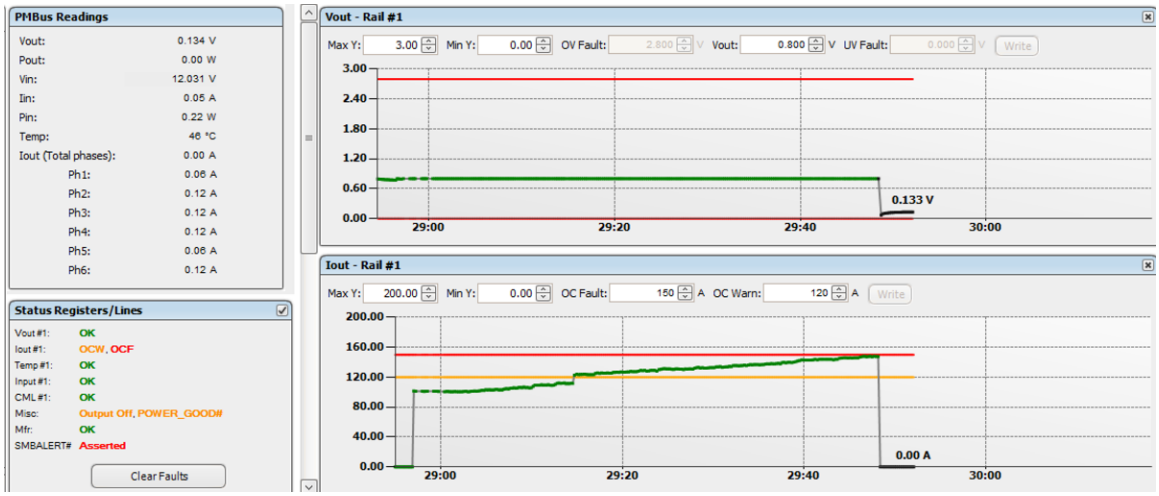


Figure 28. Overcurrent Shutdown as Seen in Fusion GUI

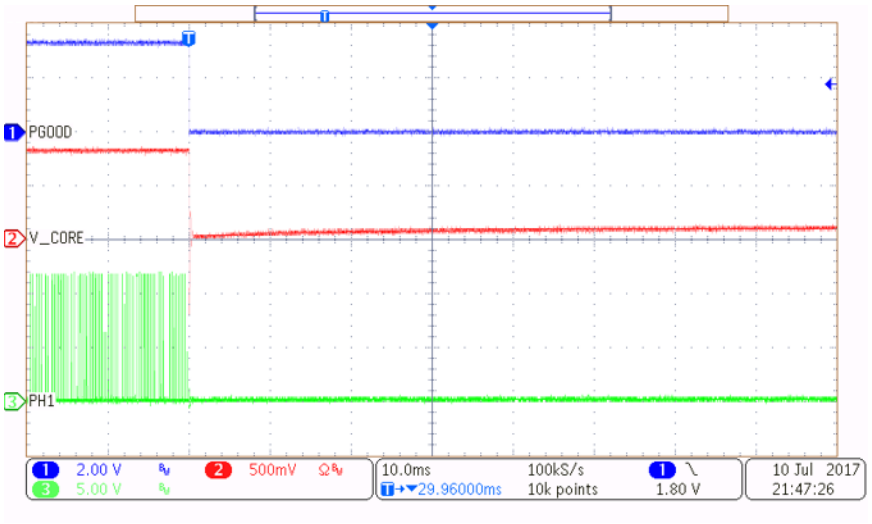


Figure 29. Overtemperature Shutdown

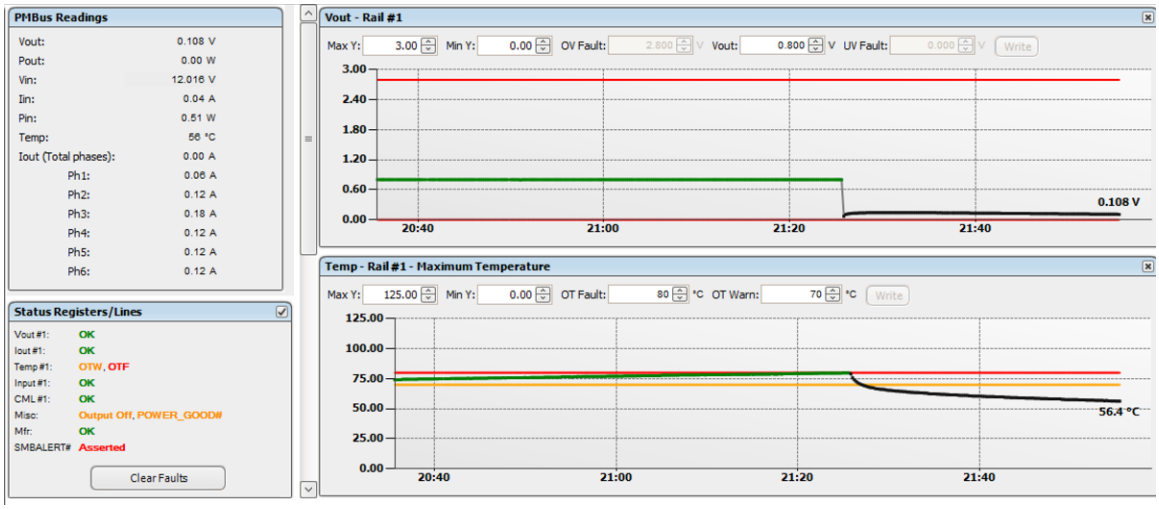


Figure 30. Overtemperature Shutdown as Seen in Fusion GUI

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01367.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01367.

5.3 PCB Layout Recommendations

Follow all the layout instructions as specified in the respective data sheet for each part when laying out a design using the TPS53679 controller and CSD95490 Smart Power Stage. Some other guidelines to consider include:

- Keep the layout for all six phases on the core rail identical to ensure optimal current balancing and thermal performance between phases.
- Route noisy traces such as pulse width modulation (PWM) and the PMBus lines on a separate layer than the sensitive analog sense lines such as VSP, VSN, COMP, IMON, and so forth.
- Use quality capacitors for both the input and output decoupling to obtain the maximum performance possible with respect to DC ripple and transient response. Ceramic capacitors must be rated to at least 16 V on V_{IN} and 2.5 V on V_{OUT} with a dielectric rating of X5R or better.
- Ensure that the V_{OUT} and GND nodes are routed on multiple layers of copper and connected with enough vias to handle the current requirements for the best thermal performance. Following this guideline allows for a maximum amount of heat to flow out of the power stages and inductors into the board.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01367.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01367.

6 Software Files

To download the Fusion Digital Power Designer software, see the following tool folder.

7 Related Documentation

1. Texas Instruments, *TPS53679 Dual-Channel (6-Phase +1-Phase) or (5-Phase + 2-Phase) D-CAP+™ Step-Down Multiphase Controller with NVM and PMBus™ for VR13 Server VCORE*, TPS53679 Data Sheet (SLUSC47)
2. Texas Instruments, *CSD95490Q5MC Synchronous Buck NexFET™ Smart Power Stage*, CSD95490Q5MC Data Sheet (SLPS653)

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8 About the Author

CARMEN PARISI is a Senior Applications Engineer working in the Multiphase and Control Solutions (MCS) group at TI developing reference designs and application notes. He has six years of experience in power electronics working on mobile, desktop, and server V_{CORE} applications; battery chargers; and system PMICs. Carmen earned a combined BS/MS degree in electrical engineering from the Rochester Institute of Technology.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2017) to A Revision	Page
• Changed design title from *High-Power 6+1 Voltage Regulator Reference Design for Networking ASICs Using TPS53679* to *High-Power Voltage Regulator Reference Design for Cavium ThunderX2® Arm® Processors*	1

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