TI Designs: TIDA-01055

ADC Voltage Reference Buffer Optimization Reference Design for High-Performance DAQ Systems

Description

This reference design for high-performance DAQ systems optimizes the ADC reference buffer to improve SNR performance and reduce power consumption with the TI OPA837 high-speed op amp. This device is used in a composite buffer configuration and provides a 22% power improvement over traditional op amps. Voltage reference sources with an integrated buffer often lack the drive strength required to achieve optimal performance in a high-channel count systems. This reference design is capable of driving several ADCs and achieves a system ENOB of 15.77 bits using an 18-bit, 2-MSPS SAR ADC.

Features

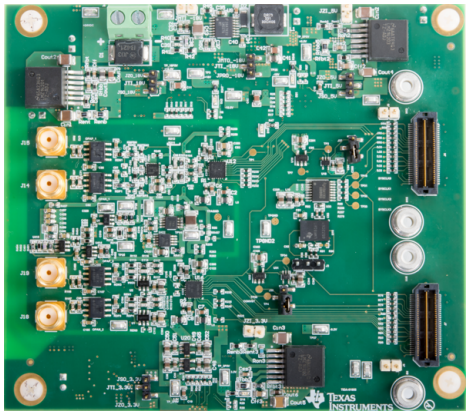
- Two-Stage Buffer Design for Reducing Noise Generated From Voltage Reference
- Implements New Low-Power Reference Driver With Slew Rate Capability to Drive a 2-MSPS SAR ADC

Applications

- Data Acquisition (DAQ)
- Semiconductor Test Equipment
- LCD Test Equipment
- Lab Instrumentation
- Battery Test

Resources

TIDA-01055	Design Folder
LM53635-Q1	Product Folder
LM5574, LM46001, TPS7A3001	Product Folder
TPS7A47, LM7705	Product Folder
SN74AHC1G04, SN74AUP1G80	Product Folder
LMK61E2, LMK00804B	Product Folder
OPA827, OPA625, THS4551, OPA837, OPA378	Product Folder
REF6041, REF5040	Product Folder



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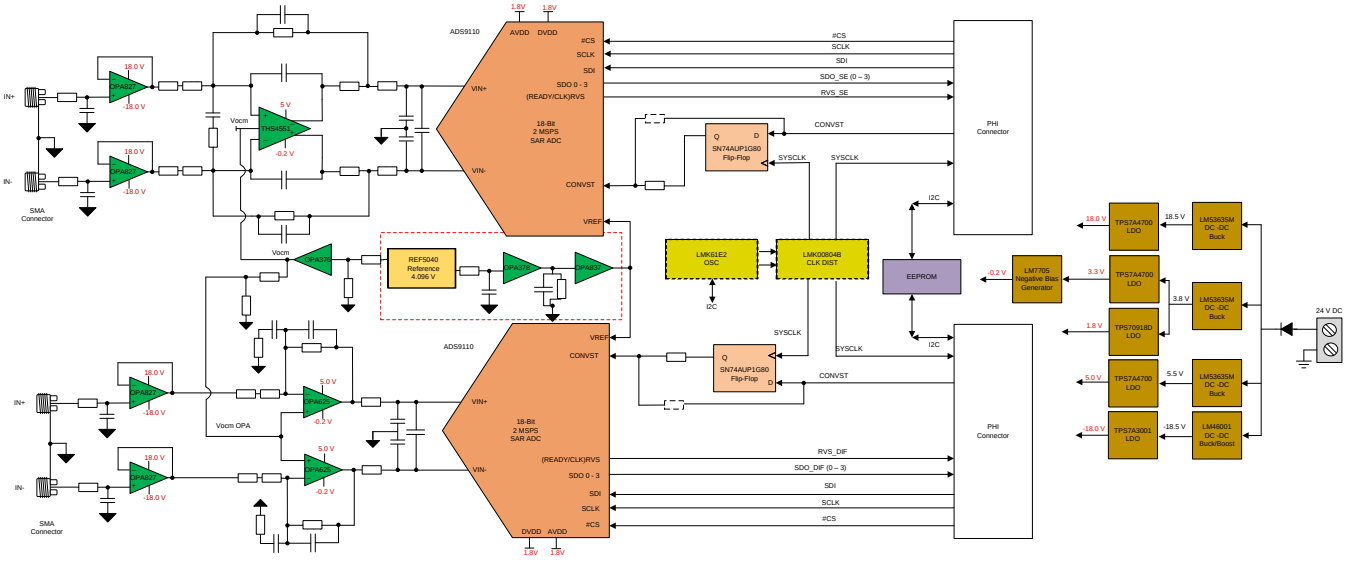

1 System Description

Multi-input systems requiring the simultaneous or parallel sampling of many data channels present many design challenges to engineers developing data acquisition (DAQ) modules and automatic testers for applications such as semiconductor tests, memory tests, LCD tests, and battery tests. In these systems, sometimes hundreds or even thousands of data channels are required and thus maximizing SNR performance while minimizing power, component count, and cost are all key design criteria. One of the critical parts of these systems is the reference voltage circuit for the analog-to-digital converter (ADC). The reference pin of the ADC needs to be adequately driven to a precise voltage as to not add more noise to the system. Advanced buffering circuits are created to do this, but more components consume more power.

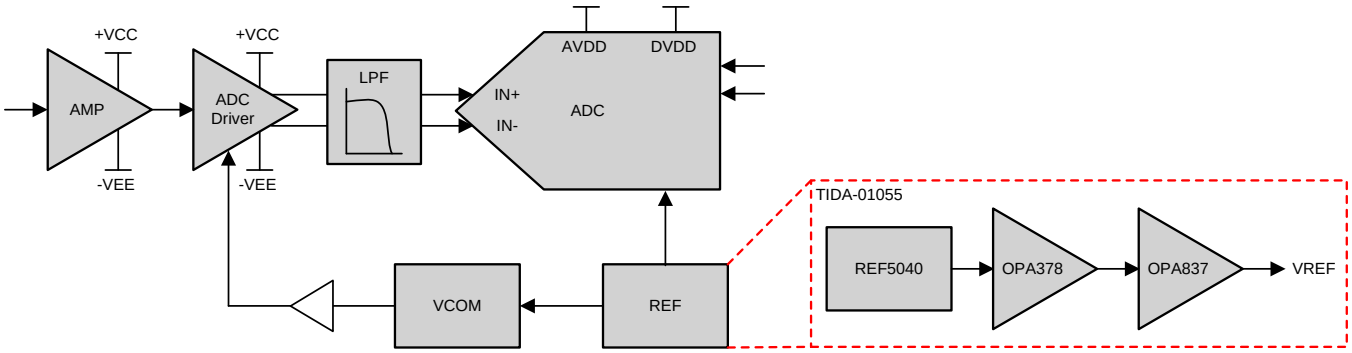

Figure 1. Generic Analog Front End

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASURED
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	8-V_{PP} fully differential	8-V_{PP} fully differential
Resolution	18 bits	18 bits
SNR	> 96 dB	96.70 dB
THD	< –118 dB	–119.76 dB
ENOB	> 15 bit	15.77 bits
System power	< 2.5 W	1.94 W
Form factor (L × W)	120 × 100 mm	112.98 × 99.82 mm

2 System Overview

2.1 Block Diagram

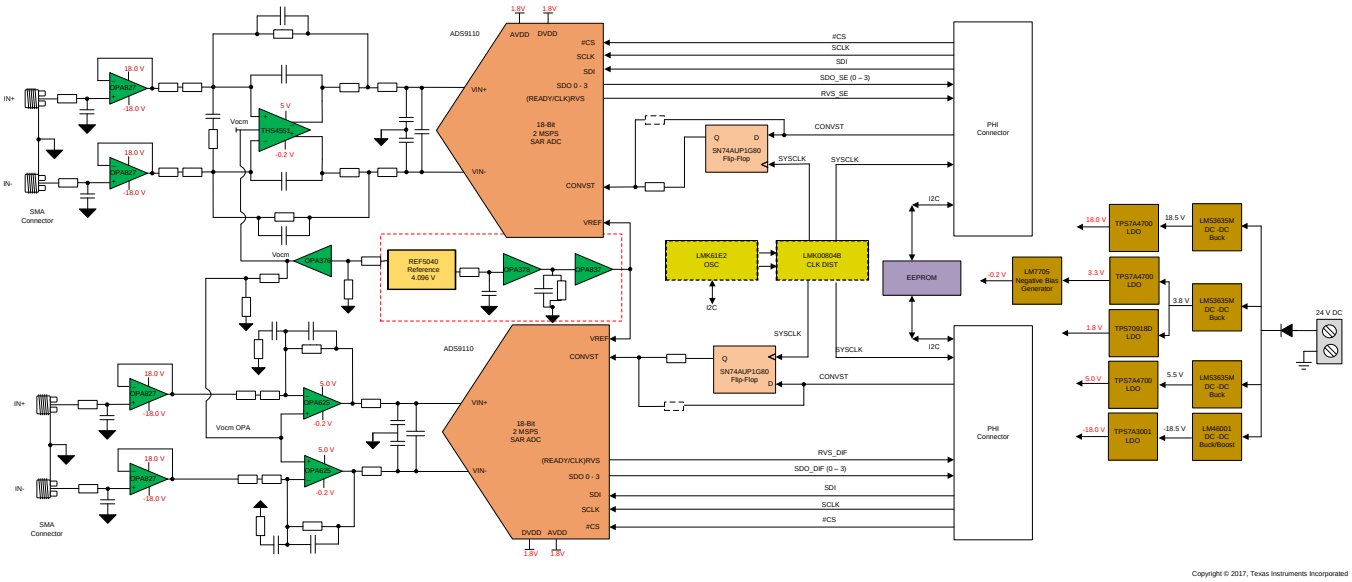

Figure 2. System Block Diagram

This reference design focuses on the voltage reference for the ADS9110 ADC. This design has two reference options: the REF6041 and REF5040. The REF5040 requires an external reference buffer whereas the REF6041 has one integrated in the device. With the external buffer, there are two op-amp options: the OPA625 and OPA837. The OPA625 is currently a popular op amp for this application, but the new OPA837 can match the same great performance at a much lower power.

The ideal setup for this reference design uses the REF5040 with the dual-stage composite reference buffer containing the OPA837. This composite buffer also includes the OPA378, which is a high-precision op amp that accounts for offset and drift error, which combined with the high-speed OPA837 provides a low-offset, low-drift, wide bandwidth and low-output impedance solution to drive the reference. For more information on the benefits of the composite buffer design, see Section 3.2.2 of the TIPD113 reference guide and Section 3.5 of the TIPD115 reference guide.

2.2 System Design Theory

2.2.1 Stability Analysis

Both the OPA837 and the OPA625 are used in the reference buffer. To make sure that the devices function properly, a loop gain analysis is setup in TINA-TI™ to verify stability. Figure 3 and Figure 4 show the circuits set up in TINA-TI for both devices.

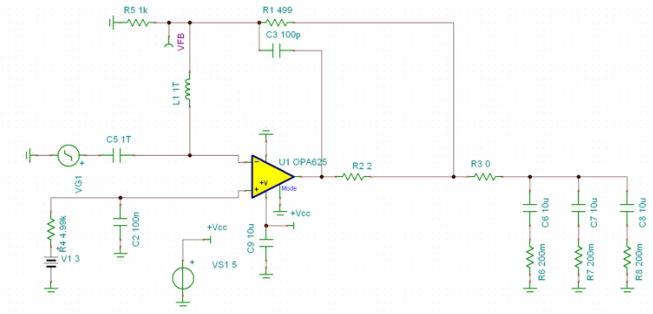

Figure 3. OPA625 Stability Circuit

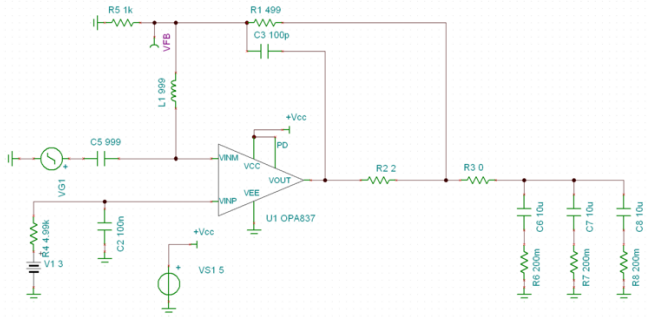

Figure 4. OPA837 Stability Circuit

Figure 3 shows the OPA625 circuit created to test stability. Figure 4 shows the same setup with the OPA837 to test stability. Both devices are pin-to-pin compatible with the exception of the Mode and PD pin. This compatibility makes it easy to swap out each op amp during testing by using a 0-Ω resistor. An AC analysis is performed to verify stability with the results illustrated in Figure 5.

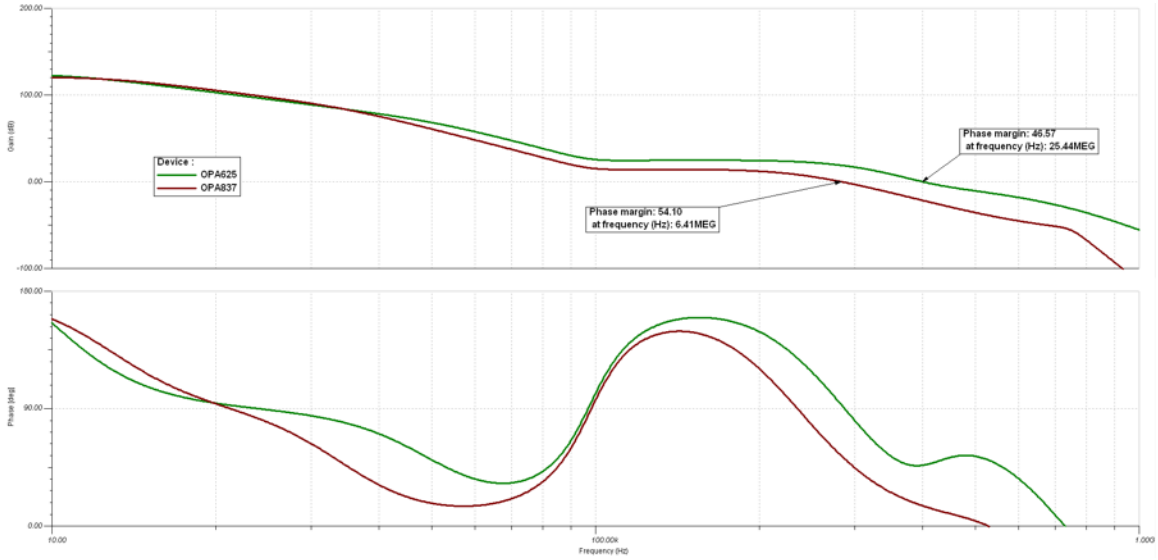

Figure 5. AC Analysis Results for Both Op Amps

The rule of thumb for op-amp stability is to have a phase margin of at least 45 degrees or above. The OPA625 has a phase margin of 46.57 degrees, and the OPA837 has a phase margin of 54.10 degrees. Both op amps are stable in the same configuration, which is important as to not create additional variables for performance comparison.

With the stability for each op amp individually verified, the full dual-stage buffer system is created in TINA-TI to test the stability of the overall system. These circuits can be seen in Figure 6 and Figure 7.

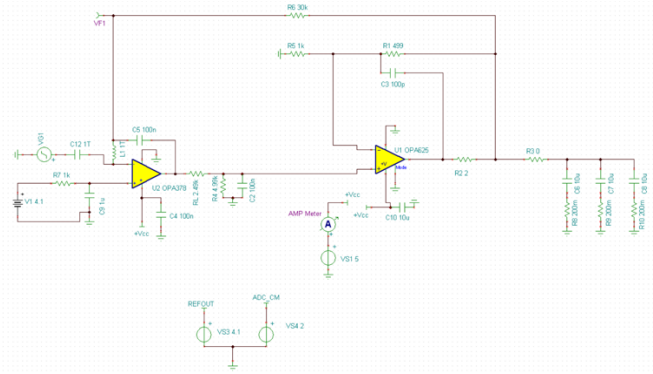

Figure 6. OPA625 Full-Loop Stability Circuit

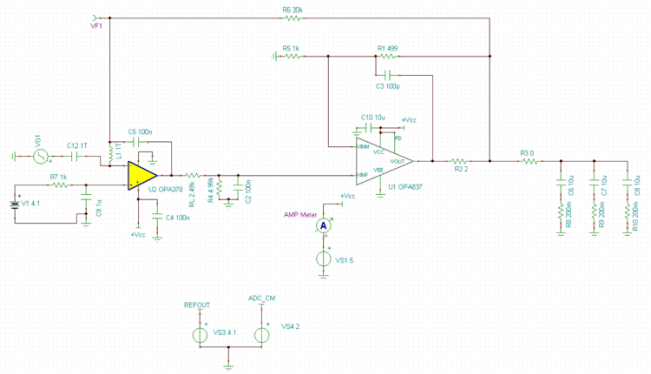

Figure 7. OPA837 Full-Loop Stability Circuit

Both circuits are now simulated with the OPA378 added to the front end. The overall circuit is simulated with a 4.1-V input that emulates the output of the REF5040. Again, an AC analysis is performed for these two circuits to verify the stability. The results are illustrated in Figure 8.

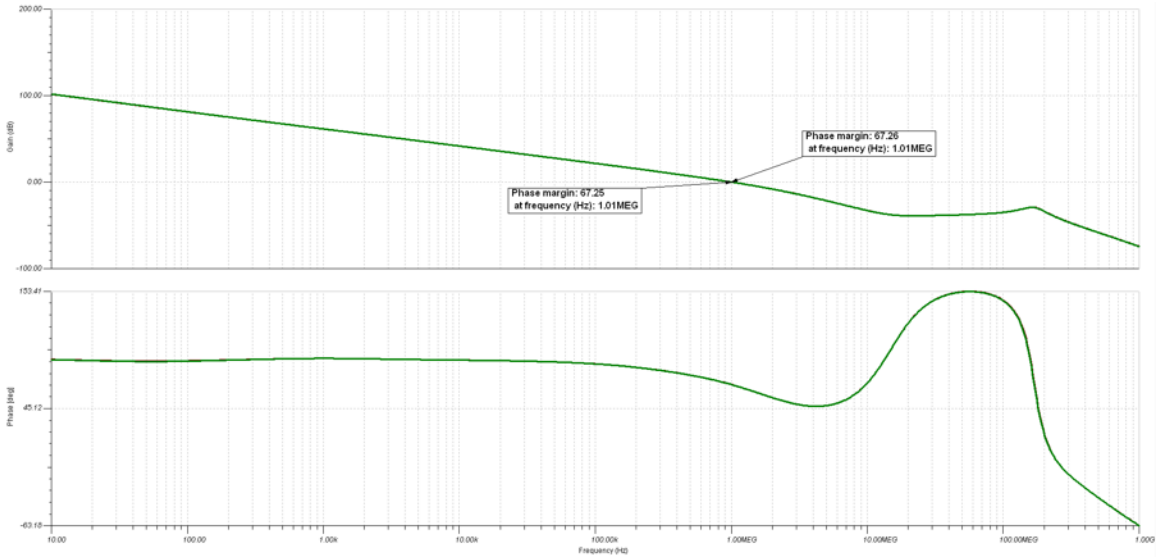

Figure 8. Full-Loop AC Analysis Results for Both Op Amps

Both circuits have identical phase margin of 67.26 degrees, making both op amps stable in the whole buffer system. With circuit stability verified, more simulations are made to observe the noise and power performance of the buffer system.

2.2.2 Power and Noise Analysis

The main benefit of the OPA837 comes from its lower power consumption compared to the OPA625. A simulation is created in TINA-TI to verify that the overall power consumption of the buffer system implementing the OPA837 is indeed lower than that of the system implementing the OPA625. Two circuits are made in TINA-TI: one containing the OPA625 (see Figure 9) and the other containing the OPA837 (see Figure 10).

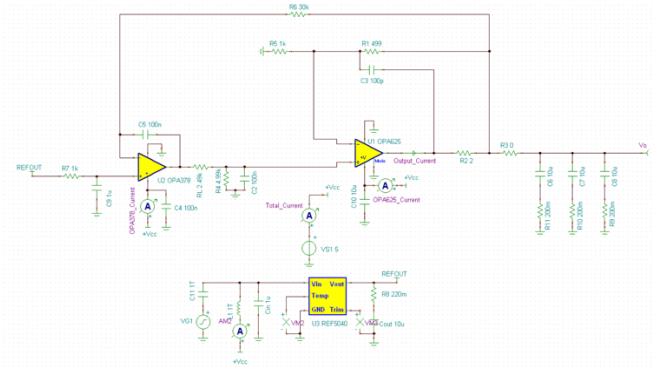

Figure 9. OPA625 Power and Noise Optimization Circuit

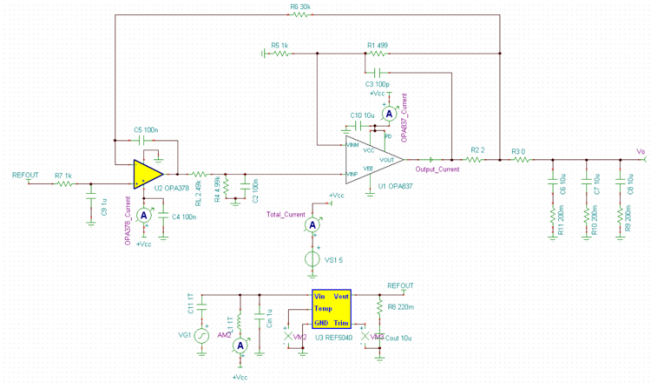

Figure 10. OPA837 Power and Noise Optimization Circuit

Both circuits contain current probes to observe the amount of current being drawn from the power source. A DC analysis is performed on both circuits in Figure 9 (containing the OPA625) and Figure 10 (containing the OPA837). The results are displayed in Figure 11 and Figure 12, respectively.

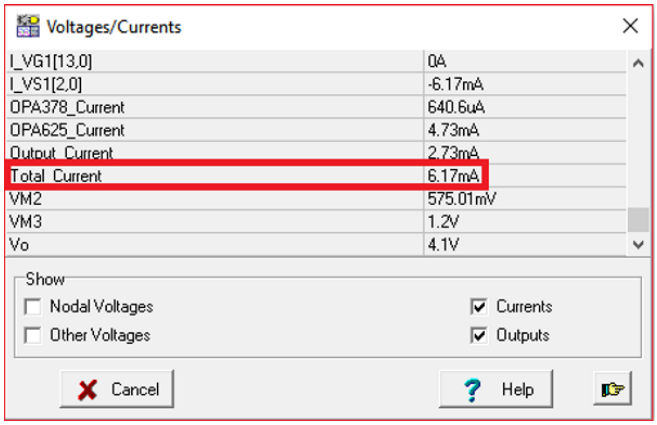

Figure 11. OPA625 DC Analysis Results

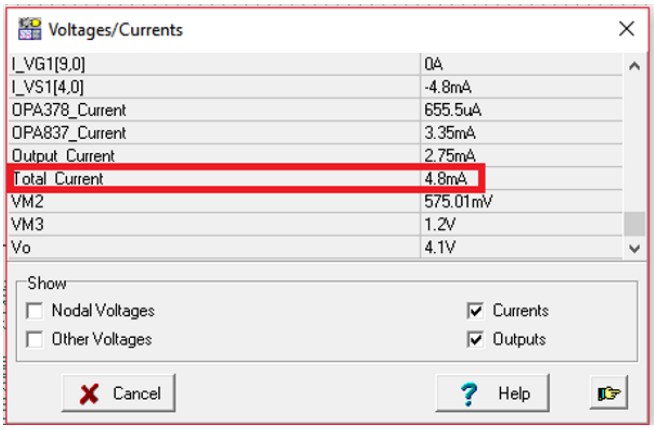

Figure 12. OPA837 DC Analysis Results

The current drawn for the OPA837 circuit is 1.37 mA less than that of the OPA625. This equates to a 6.85 mW power improvement. This result is expected by comparing the quiescent current values from the device datasheets.

The OPA837 is the better device when it comes to power efficiency, but it is also important to verify that the total noise on the output is comparable to the OPA625. To do this, the same two circuits are used from the power simulations to perform a noise analysis. The results of that analysis are illustrated in Figure 13.

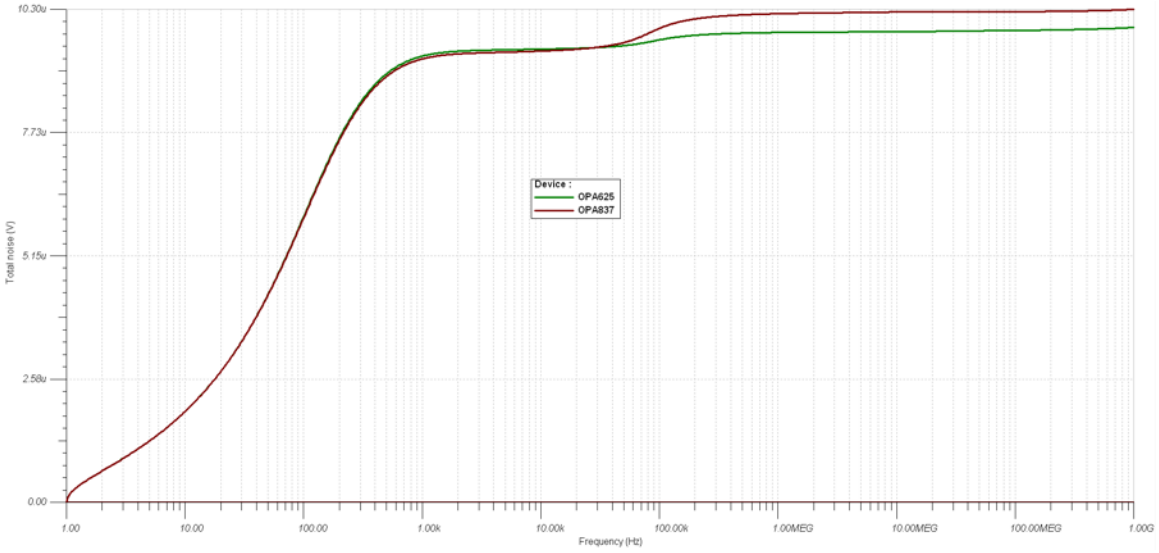

Figure 13. Noise Analysis Results for Both Op Amps

The total noise performance is similar with both op amps. The OPA625 has 300 nV less noise than the OPA837. To verify if the noise affects the performance of the ADC, it needs to be compared to the LSB value of the ADC. The value of 1 LSB for an 18-bit ADC with a 4.096-V reference voltage is 15.625 µV. The results show that the noise reaches 10.3 µV, which is not ideal because it exceeds half an LSB; however, this is done to achieve lowest power.

2.2.3 Transient Analysis

The ADS9110 is a high-performance successive approximation register (SAR) ADC with a sampling rate of 2 MSPS. With that, it takes a fast slew rate to charge the sampling capacitors before each sample occurs. To verify that the slew rates of both op amps are fast enough to recover after each sample of the ADC, a transient simulation is set up in TINA-TI. Both circuits for the OPA625 and OPA837 created in TINA-TI are shown in Figure 14 and Figure 15, respectively.

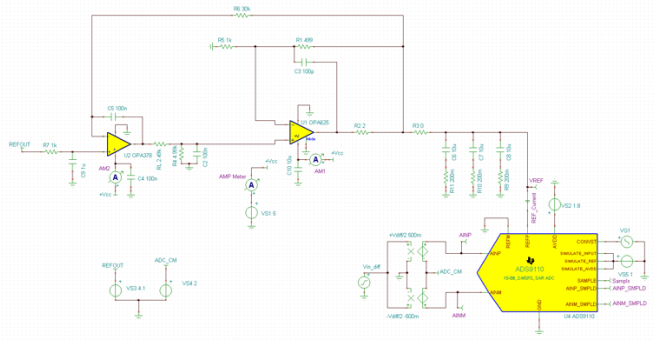

Figure 14. OPA625 Transient Circuit

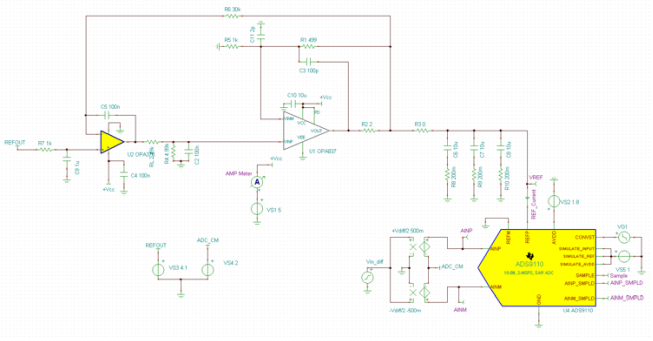

Figure 15. OPA837 Transient Circuit

The ADS9110 is simulated to mirror the physical test setup. A 10-µs transient analysis is performed on both circuits, and the results are displayed in Figure 16 and Figure 17.

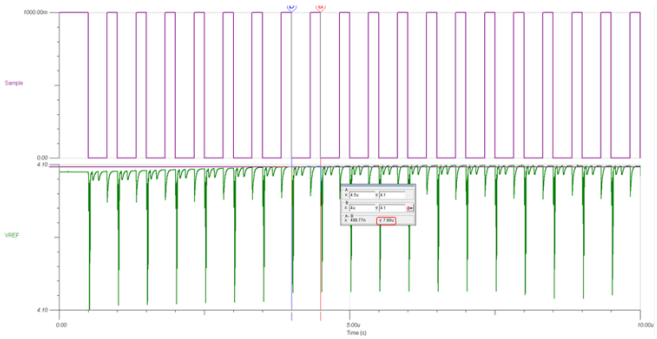

Figure 16. OPA625 Transient Analysis Results

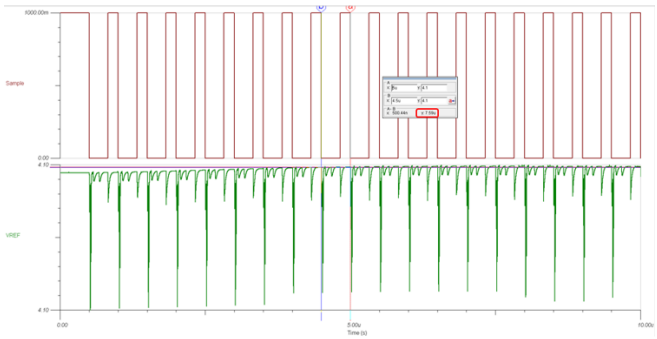

Figure 17. OPA837 Transient Analysis Results

The top waveform named "Sample" is the simulated 2 MSPS for the ADS9110. Each sample occurs on the falling edge of the square wave. The waveform named "VREF" is the input of the REF pin of the ADS9110. Markers are placed at the beginning of two samples on the VREF waveform to measure the difference in voltage between them. The OPA625 has a voltage difference between samples of about 7.68 µV, which is slightly above the 7.59 µV of the OPA837. The transient performance for each op amp is very comparable.

2.3 Highlighted Products

2.3.1 OPA837

The OPA837 unity-gain stable, voltage feedback op amp provides among the highest MHz/mW of bandwidth versus power. Using only 600 µA on a single 5-V supply, this 3.0-mW device delivers 105 MHz of bandwidth at a gain of 1 V/V. The very low-trimmed offset voltage of ±120 µV maximum comes with a typical drift of ±0.4 µV/°C. The OPA837 provides one of the lowest input noise levels at 4.7 nV for its 3-mW quiescent power. The very high 50-MHz gain bandwidth product provides the low output impedance to high frequencies required to supply the fast charging currents in SAR driver application. This low dynamic output impedance also makes this a great reference buffer as it is used in this reference design.

2.3.2 REF5040

The REF5040 is a low-noise, low-drift, very high-precision voltage reference. This reference is capable of both sinking and sourcing current and has excellent line and load regulation. Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. Combined with very low noise, these features make the REF5040 reference ideal for use in high-precision DAQ systems.

2.3.3 ADS9110

The ADS9110 is an 18-bit, 2-MSPS, SAR ADC with enhanced performance features. The high throughput enables developers to oversample the input signal to improve dynamic range and accuracy of the measurement. The ADS9120 is a pin-compatible, 16-bit, 2.5-MSPS variant of the ADS9110. The ADS9110 boosts analog performance while maintaining high-resolution data transfer by using TI's enhanced SPI feature. Enhanced SPI enables the ADS9110 to achieve high throughput at lower clock speeds, thereby simplifying board layout and lowering system cost.

2.3.4 OPA378

The OPA378 is a unity-gain stable, precision operational amplifier that is free from phase reversal. The use of proprietary Zero-Drift circuitry gives the benefit of low input offset voltage over time and temperature as well as lowering the 1/f noise component. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies, excellent CMRR, and a rail-to-rail output that swings within 10 mV of the supplies. This design results in superior performance for driving ADCs without degradation of differential linearity.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

The ensuing section outlines the information for getting the board up and running as fast as possible. To learn about the PHI board or the onboard clocking and jitter cleaner, see the TIDA-01052 reference design. Take care when moving jumper pins to avoid possible damage to the components.

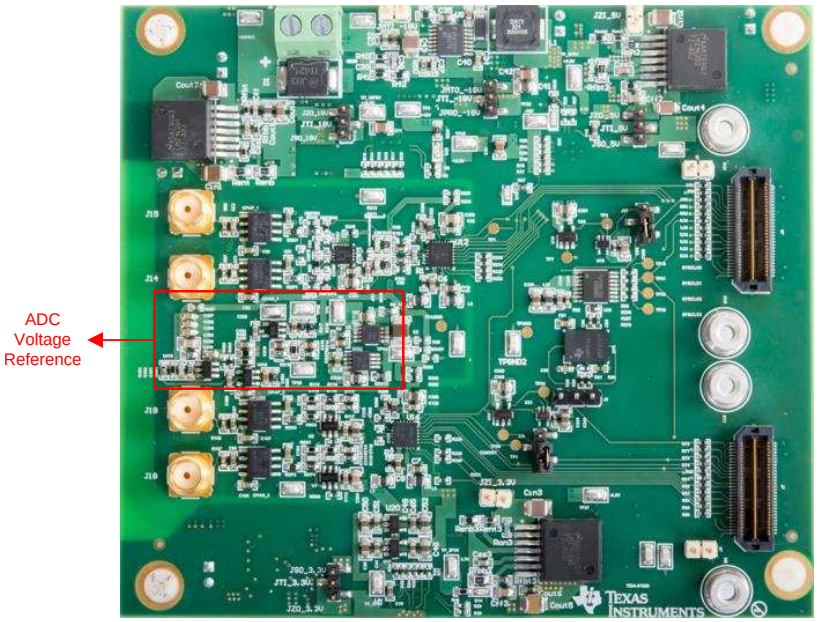

Figure 18. TIDA-01055 Hardware

3.1.1 Jumper Configuration

This system has several configurable power options. These options are selectable through the use of three-pin jumpers and two-pin jumpers. Table 2 highlights the purpose of each jumper and will assist in changing the configuration to fit the user's needs.

Table 2. Jumper Configuration

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
JSI_18V	Power to LM53635 18-V rail	—	Short
JTI_18V	Connects LM53635 to TPS7A700 for 18-V rail	Connects LMZ14201 to TPS7A700 for 18-V rail	Short pins 1 and 2
JSI_5V	Power to LM53635 5-V rail	—	Short
JTI_5V	Connects LM53635 to TPS7A700 for 5-V rail	Connects LMZ14203 to TPS7A700 for 5-V rail	Short pins 1 and 2
JSI_3.3V	Power to LM53635 3.3-V rail	—	Short
JTI_3.3V	Connects LM53635 to TPS7A700 for 3.3-V rail	Connects LMZ14202 to TPS7A700 for 3.3-V rail	Short pins 1 and 2
JPRI_-18V	Power to LM46001 –18-V rail	—	Short
JTI_18V	Connects LM46001 to TPS7A3001 for –18-V rail	Connects LM5574 to TPS7A3001 for –18-V rail	Short pins 1 and 2
JMTI_-18V	Power to LM5574 –18-V rail	—	Open
JZI_18V	Power to LMZ14201 18-V rail	—	Open
JZI_3.3V	Power to LMZ14202 3.3-V rail	—	Open
JZI_5V	Power to LMZ14203 5-V rail	—	Open
J39	Connects –0.2-V rail to OPA625 and THS4551	Shorts –0.2-V rail to ground	Short pins 1 and 2

3.2 Testing and Results

An Audio Precision 2700 series signal generator is used as the signal source to test the AFE and ADC performance. The noise and THD of the AP2700 have adequate performance and do not limit measurements or the systems performance. A generic DC power supply generates the 24-V DC input voltage.

A PHI controller board is used to connect the TIDA-01055 board to the host PC running the ADS9110 EVM GUI. This software allows for measuring SNR, THD, SFDR, SINAD, and ENOB for the ADC by running a spectral analysis. The AP2700 is set to output a 2-kHz 8-Vpk-pk sinusoid. 2 kHz is chosen because it is the standard frequency when measuring noise and THD, and 8-Vpk-pk grants the full range on the THS4551 or OPA625, thus granting the full range of 0 to VREF for the ADC.

3.2.1 OPA625 versus OPA837 Results

Both the OPA625 and OPA837 are used in the dual-stage composite buffer to drive the REF pin of the ADS9110. Both op amps are exceptional devices when used as buffers, but the newer OPA837 provides the same great performance with lower power consumption. This test is performed to compare system performance when using the OPA625 and then replacing it with the OPA837.

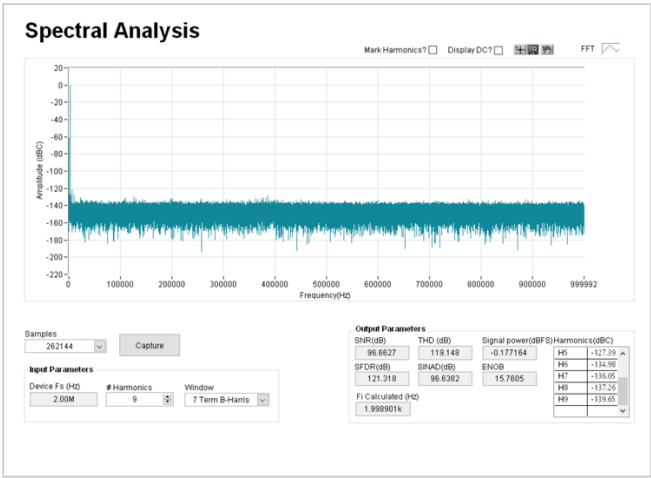

Figure 19. OPA625 With Buffer Spectral Analysis

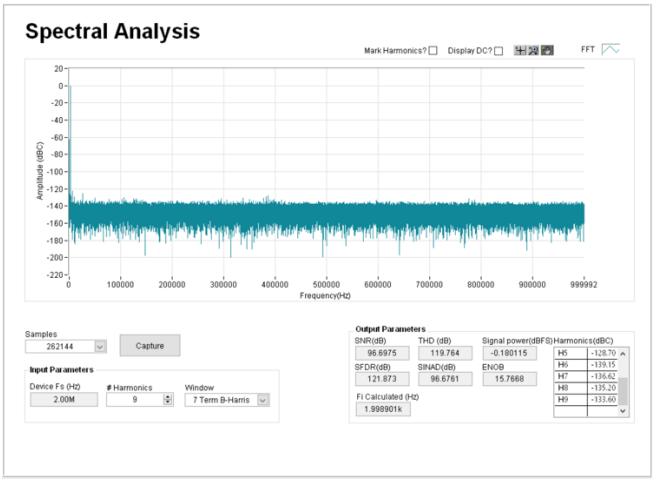

Figure 20. OPA837 With Buffer Spectral Analysis

Figure 19 shows the performance of the system when using the OPA625. It is very similar to Figure 20, which is the system performance when the OPA625 is replaced with the OPA837. The system performance of each op amp is comparable, which is expected due to the simulations. The OPA837 provides the same great performance as the commonly used OPA625, and coupled with its improved power efficiency makes this device a better option.

Some applications require the DAQ to capture data in bursts. The ADC needs to have sufficient precision for the first few samples when burst sampling. This requirement makes the settling time and voltage droop of the reference critical because it limits the accuracy of the first few samples. These specifications are measured for both of the op amps and the waveforms are combined for comparison.

Figure 21 shows the reference settling analysis for both op amps. From the comparison, the OPA837 outperforms the OPA625 with its smaller voltage droop and quicker settling time. This helps solidify the OPA837 as the better option for the composite buffer.

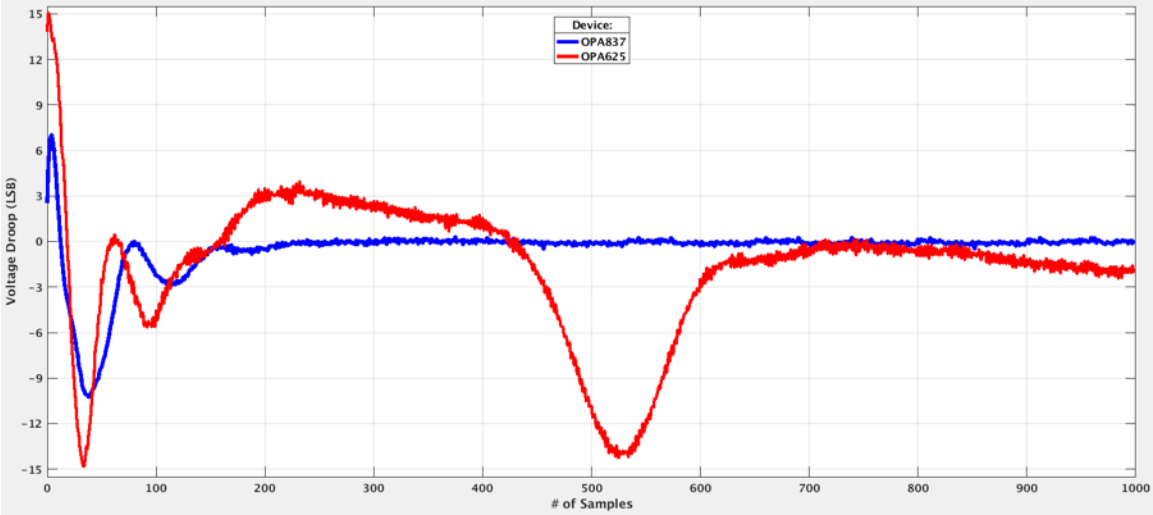

Figure 21. Reference Settling Analysis

3.2.2 Thick Trace versus Thin Trace Results

This design has two different trace options that connect the reference voltage to the REF pin of the ADS9110. This is to illustrate how a non-ideal layout can impact the system performance of a high-performance ADC. One of the traces is thick with a short length, and the other trace is thin with a long length. The long thin trace is not ideal because it has more resistance than the thick trace. Figure 22 and Figure 23 compare the performances of the thick trace and thin trace using the OPA837 in the buffer system.

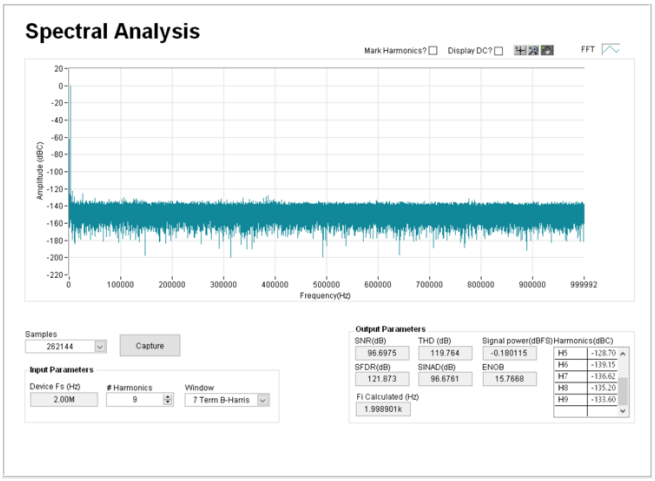

Figure 22. Spectral Analysis Using Thick Trace

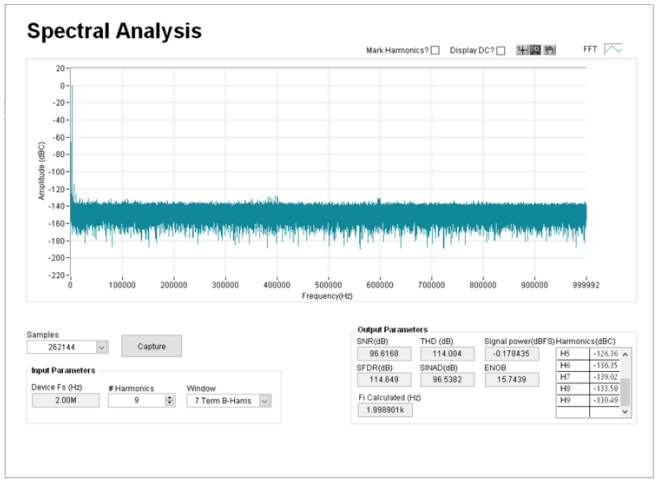

Figure 23. Spectral Analysis Using Thin Trace

From the comparison, the thin trace causes a large amount of performance degradation compared to the thick trace. Most of that degradation is attributed to the trace length, causing it to function as an antenna and coupling with the EMI from the power supplies. The higher resistance of the thin trace causes variations in the sampling capacitor charging time, which causes distortion adding to the THD. To see how the traces are laid out, see Section 4.3.

3.2.3 REF6041 Results

The REF6041 is another option for the ADC reference voltage that is included in this reference design. This device is put through the same simulations as the REF5040 and the dual stage composite buffer. In these simulations, the REF6041 performed similar to both op amps used in the buffer.

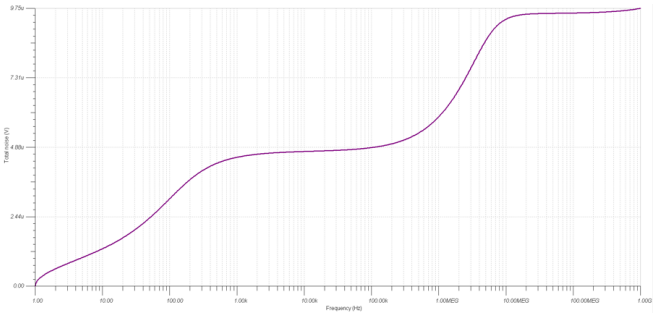

Figure 24. REF6041 Noise Analysis Results

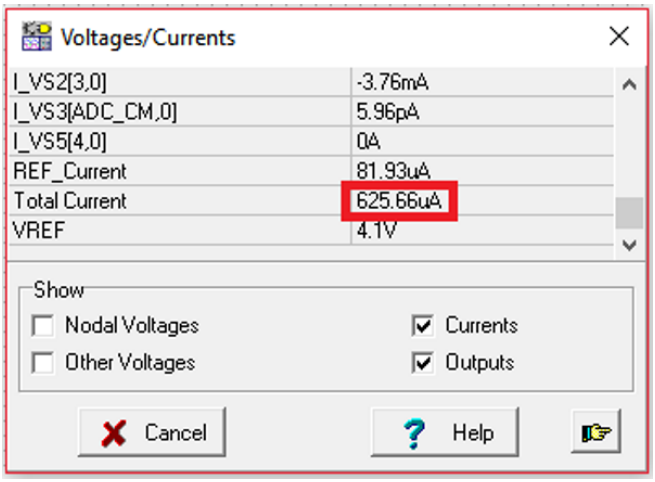

Figure 25. REF6041 DC Analysis

The noise performance of the REF6041 is comparable with both op-amps, but the power consumption is quite a bit lower. However, this device falls short in its current driving capability of only 4 mA. This is an important specifications to consider when using multiple ADCs in the system. The REF6041 is tested with the two ADCs in this design, and it is not able to successfully drive both. A TINA-TI simulation is made to verify results obtained from testing.

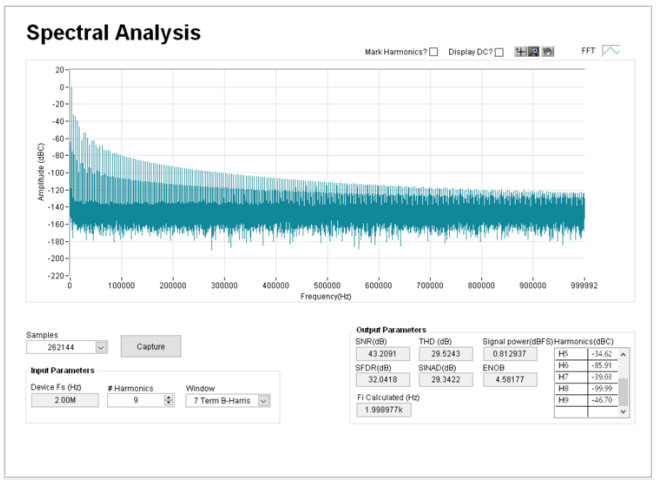

Figure 26. REF6041 Spectral Analysis

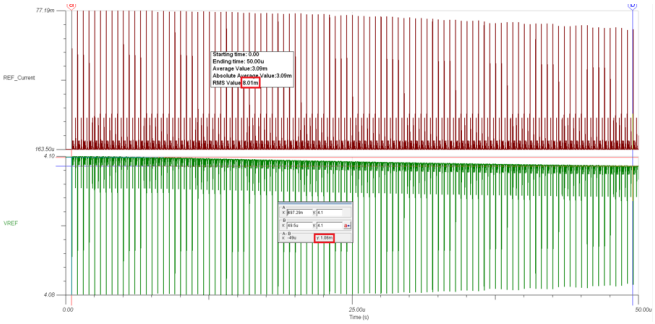

Figure 27. REF6041 Transient Analysis Results

Figure 26 shows the spectral analysis performed on the ADC output. The system performance is horrible when the REF6041 is used to drive two ADS9110 ADCs at 2 MSPS. The TINA-TI simulation results in Figure 27 show the voltage and current output of the REF6041. Notice how the voltage "VREF" slowly drops as more and more samples are being taken. Markers are set to measure the voltage drop of 1.06 mV from the first sample to the last in the 50-µs window. The RMS value of the current "Iout" was taken to average out the current spikes from each sample. This RMS current value is 8 mA, which exceeds the drive capability of the REF6041. A good representation of how this affects the output of the ADC is displayed in Figure 28.

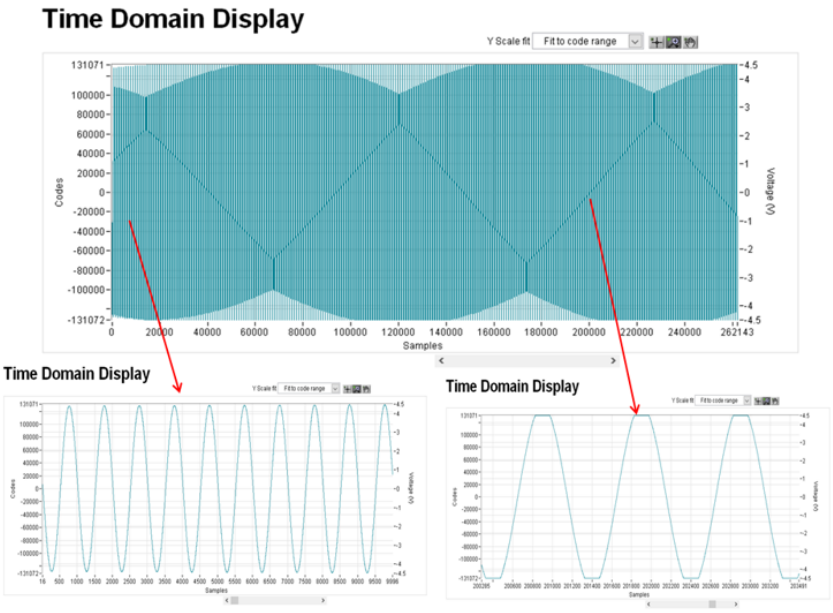

Figure 28. REF6041 Time Domain Waveform

Figure 28 displays the results from Figure 26 in the time domain. The waveforms magnitude begins to gradually increase as more samples are taken and then the waveform starts to clip after around 20,000 samples. The input signal amplitude is not actually increasing, but the REF6041 output voltage is not able to recover back to the 4.096 V as seen in the TINA-TI simulation. Therefore, the ADC samples with a lower reference voltage and the full-scale range is decreasing to a point below the input signal amplitude causing the clipping.

The results of all these tests help highlight the benefit of using the dual-stage composite buffer with the OPA837. The system performance is identical to the OPA625 and it accomplishes this at lower power consumption. The REF6041 is a great device for providing a reference voltage for a single 18-bit ADC sampling at 2 MSPS. However, this reference design is meant for end-equipment with a high number of channels containing ADCs. The REF5040 with the composite buffer is able to drive multiple ADCs with great performance. This coupled with the power consumption improvement of the OPA837, makes it the better option over using a REF6041 with each ADC in the system. Lastly, consider the layout of this reference driver as the system performance is greatly impacted by a non-ideal layout. The trace must be thick enough not to add additional resistance and short enough not to act as an antenna for any radiated signals to couple to. Table 3 highlights all of the results taken from each test to help observe the performance differences, including test results for the REF6041 driving only one ADC.

Table 3. Summary of Measured Results

LAYOUT OPTION	BUFFER ARCHITECTURE	REFERENCE DEVICE	SNR (dB)	SINAD (dB)	THD (dB)	SFDR (dB)	ENOB (Bits)
Thick trace	OPA625	REF5040	96.66	96.64	–119.15	121.32	15.76
Thick trace	OPA837	REF5040	96.70	96.68	–119.76	121.87	15.77
Thin trace	OPA625	REF5040	96.50	96.39	–112.40	112.82	15.72
Thin trace	OPA837	REF5040	96.62	96.67	–114.00	114.65	15.74
Thick trace	—	REF6041	96.70	96.67	–117.87	118.99	15.77

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01055.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01055.

4.3 PCB Layout Recommendations

This reference design contains two layout options for the ADC reference voltage circuit. One is an ideal layout where the trace connected to the ADC REF pin is thick and has a short length. The non-ideal layout option has a long, thin trace connected to the ADC REF pin. Figure 29 and Figure 30 show these two different traces.

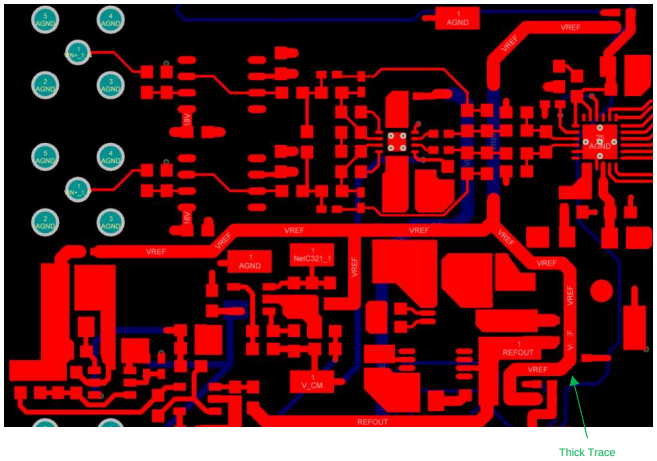

Figure 29. Thick Trace Layout

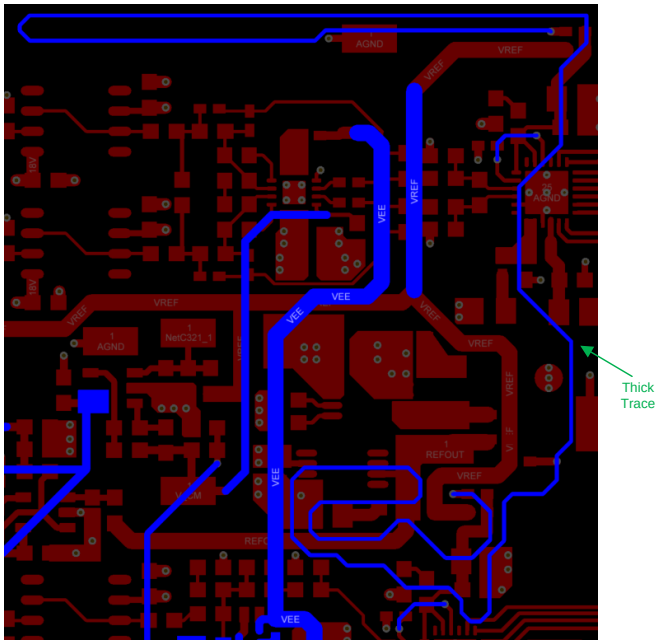

Figure 30. Thin Trace Layout

The thick trace is labeled VREF and the thin trace is labeled VREF1 though it cannot be seen due to the magnification. The thick trace is routed in a direct manner to the REF pin from the source, and the thin trace is routed to emulate the length of trace in a system with several of these channels. The thin trace is long and is routed by various power supplies making it susceptible to EMI coupling. For more layout recommendations regarding the AFE or the power design, see the TIDA-01050 and TIDA-01054 reference designs.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01055.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01055.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01055.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01055.

5 Software Files

To download the software files, see the design files at TIDA-01055.

6 Related Documentation

1. Texas Instruments, *TIDA-01052 ADC Driver Reference Design Improving Full-Scale THD Using Negative Supply Design Guide*
2. Texas Instruments, *TIDA-01054 Multi-Rail Power Reference Design for Eliminating EMI Effects in High-Performance DAQ Systems Design Guide*
3. Texas Instruments, *TIPD113 18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power Design Guide*
4. Texas Instruments, *TIPD115 18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise Design Guide*

6.1 Trademarks

7 About the Authors

DYLAN HUBBARD is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the test and measurement industry. Dylan obtained his bachelor's degree from Texas A&M University in Electronic Systems Engineering Technology (ESET).

TARAS DUDAR is a systems design engineer and architect at Texas Instruments, where he is responsible for developing reference design solutions for the test and measurement industry. Previously, Taras designed high-speed analog SOC integrated circuits for Gbps data communications. Taras has earned his master of science in electrical engineering (MSEE) degree from the Oregon State University in Corvallis, OR.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2017) to A Revision	Page
• Added OPA378 to *Resources*	1
• Added Section 2.3.4: *OPA378*	9

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