Design Guide: TIDA-010004

12-V, 15-W Power Limit, Single Driver-Based Stepper, Brushed DC and Actuator Drive Reference Design

Description

This reference design demonstrates a multi-load drive using one driver chip in multiple configurations enabling reduced inventory. The multiple loads include one bipolar stepper motor, one brushed DC motor, and three actuator or solenoid loads driven from a 12-V DC supply. The design shows accurate input current limit, that helps to achieve a precise power limit for helping easy qualification as a low-power circuit, defined by IEC 60335-1. This reference design incorporates enhanced protections like open load detect, noise tolerant short circuit, overcurrent, overvoltage, undervoltage, overtemperature, surge and ESD protection all which helps to achieve a reliable and robust system design.

Resources

TIDA-010004	Design Folder
TIDA-01447	Design Folder
DRV8847	Product Folder
TPS2596	Product Folder
TVS1400	Product Folder
TPD1E10B06	Product Folder
MSP430FR5739	Product Folder

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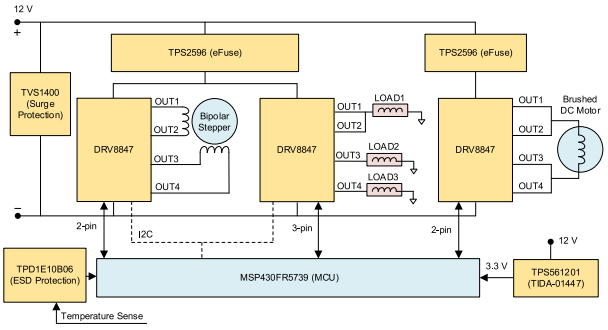
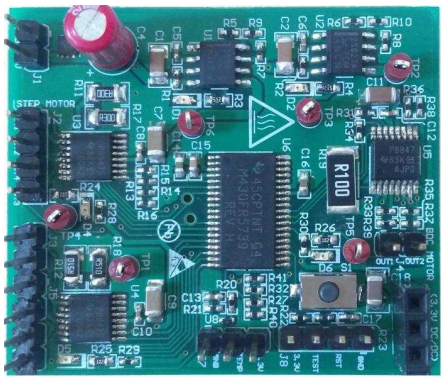
Features

- Operates at voltage ranging from 2.7 V to 16 V
- Supports multiple drives
  - Bipolar stepper drive - 0.5 A_{RMS} in full or half step with 2 or 4 pin control from MCU
  - Brushed DC drive - 1.2 A_{RMS} with two half bridges in parallel mode
  - Solenoid and actuator drives - 0.2 A_{RMS} each
- Bipolar stepper drive DRV8847 efficiency > 95 %
- Single MCU control with multi-slave operation of DRV8847S devices via I2C, and detailed fault diagnosis
- Motor control using only I2C lines (optional)
- Open load detect, overcurrent, short circuit, overvoltage, undervoltage and overtemperature protections
- Protected for surge (1 kV) and ESD (±8 kV) events
- Input current limit with < ±8% error to help easy low-power circuit qualification with IEC 60335-1
- Operating ambient: –10 to +70°C

Applications

- Refrigerator & freezer
- Washer & dryer
- Coffee machine
- Air conditioner indoor unit





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1 System Description

Many of the home appliances like refrigerators, washers and dryers, dishwashers, and coffee machines use multiple stepper motors, brushed DC motors, and many solenoid valves and actuators for their operation. For example, a commonly-used medium-end refrigerator uses a damper unit for controlling the cold air flow between the freezer and rest of the compartment. The damper valve opening or closing is usually controlled by a bipolar stepper motor. Similarly, the ice maker unit in the refrigerator has an ice dispenser motor and ice crusher motor, usually with brushed DC motor. The refrigerator has a heater unit and a couple of other valves controlled by solenoids.

For driving these different subsystems in a single end equipment, designers normally uses different electronic drive chips. For example, the bipolar stepper motor in the damper needs a power stage with two full bridges. For driving the brushed DC motor in both the directions (bidirectional control) designers use a single full bridge power stage. For driving a brushed DC motor in one direction (unidirectional control) and for driving a solenoid, heater, actuators, LEDs and for realizing a DC/DC power supply, designers may use a single high- or low-side switch or one half bridge power stage. This leads to the use of different types of driver chips for driving the subsystems. This increases the inventory during production and adds the inventory management cost. Similar subsystems are found in other appliances as well.

This reference design demonstrates a multi-load drive using one driver chip in multiple configurations enabling reduced inventory. The multiple loads include one bipolar stepper motor, one brushed DC motor, and three actuator or solenoid loads driven from a 12-V DC supply. This single chip based driver configuration for multiple loads is achieved by using the DRV8847, dual H-bridge motor driver. The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges to drive motor windings or four independent half bridges (in independent bridge interface). This device can be used for driving two DC motors, one bipolar stepper motor, or other loads such as relays or solenoids. The DRV8847 device supports a wide input-supply range from 2.7 to 18 V, and also provides fixed off time peak current control.

Many of the household appliances has to be designed to meet specific UL (Underwriters Laboratories) or IEC (International Electrotechnical Commission) safety standards. For example, IEC 60335-1 and IEC 60730 are typically followed for household appliances. The standards define low-power circuit (LPC) in home appliances subsystems. A low-power point can be identified as the node where the maximum power delivered is less than 15 W. The part of the circuit farther from the supply source than a low-power point is considered as a low-power circuit. A proven LPC may help to skip the glow wire test, needle flame test, and certain abnormal fault conditions as per the definition and requirements from the respective standards, leading to reduced qualification and design time, and money.

Such LPCs are found in household appliances like refrigerators. For example, the damper module in refrigerator, ice maker units, heater units, hand multiple valves typically consuming less than 15 W power each. The use of an eFuse at the input of those sub-systems helps to achieve a precise power limit even during abnormal fault conditions. The design with the TPS259631 eFuse at the 12-V input may helps the designer to qualify the circuit as a low-power circuit. The reference design shows less than ±8% accuracy error in input current limit which leads to a precise power limit per the set threshold for helping easy qualification as a low-power circuit, defined by IEC 60335-1.

This reference design incorporates enhanced protections like open load detect, noise tolerant short circuit, overcurrent, overvoltage, undervoltage and overtemperature protection. The reliability and robustness of the system is further increased by surge protection provided by the TVS1400. The TPD1E10B06 provides ESD protection on the MCU pin connected to external temperature sensing.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS		
Input voltage	12-V DC (4.5-V minimum to 16-V maximum)		
Overvoltage cutoff threshold	13.5 V		
Undervoltage cutoff threshold	6.8 V		
Protections	Short circuit, overcurrent, open load detect, undervoltage, overvoltage, overtemperature,		
Operating ambient	–10°C to +70°C temperature, 85% humidity		
PCB specifications	Two layer, 1-oz copper		
SUBSYSTEM	**BIPOLAR STEPPER**	**BRUSHED DC MOTOR**	**SOLENOID AND ACTUATOR**
RMS current	0.5 A	1.2 A	0.2 A each (three outputs)
Control method	Bipolar- full step (2 pin), optional half step (4 pin)	Unidirectional and bidirectional	Current controlled
Switching frequency	20 µs fixed off time	20 kHz	Based on peak current control
Efficiency	> 95 % at 0.3-A RMS Current	-	-
Cooling method	No thermal pad	Thermal PAD to PCB	No thermal pad
Fault diagnosis through I2C	Yes	No	Yes

2 System Overview

2.1 Block Diagram

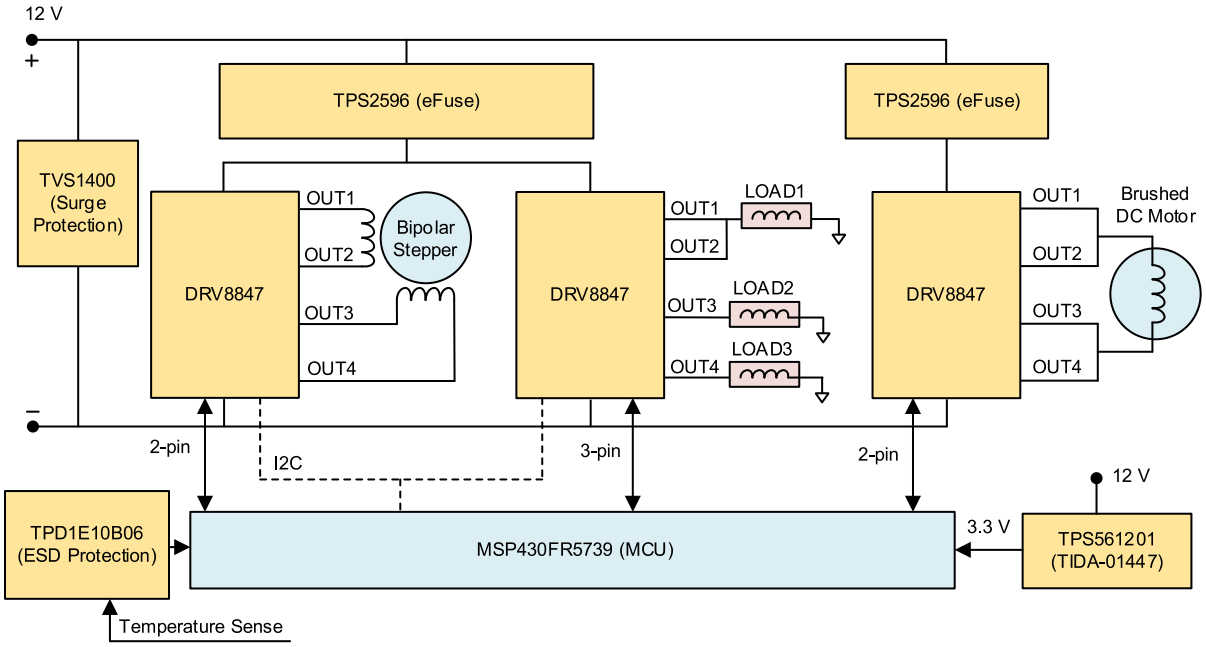

Figure 1. TIDA-010004 Block Diagram

2.2 Highlighted Products

2.2.1 DRV8847

The key requirements in selecting the motor drive are:

- Highly-integrated device to drive a bipolar stepper motor with built-in current control modes enabling reduced design time.
- Configurable for different operating modes like independent control of half bridges, parallel operation of half-bridges, built-in stepper motor control modes to enable usability in driving multiple load and hence reduced inventory.
- Optimized $R_{DS(on)}$ for best efficiency and good thermal dissipation with multiple package options.
- Enhanced multi-level protection for a reliable and robust design.
- Easy interface with MCU and diagnosis features

This reference design uses the dual H-bridge motor driver DRV8847 to drive the bipolar stepper motor, bidirectional brushed DC motor, and multiple other loads such as solenoids, actuators, heaters and so forth. The DRV8847 device satisfies all the key requirements to be used as a multi-load drive in the design. The output stage of the DRV8847 driver consists of N-channel power MOSFETs configured as two full H-bridges to drive motor windings or four independent half bridges (in independent bridge interface), making it suitable to drive multiple loads with the same chip and hence reducing the inventory in production. The device comes with low $R_{DS(on)}$ of 1000 mΩ per half bridge (HS+LS) at 25°C. The device support 1-A RMS driver current at T_A = 25°C and 2-A RMS driver current in parallel mode at T_A = 25°C. The different interface options like, 4-pin interface, 2-pin interface, parallel bridge interface, independent bridge interface, and so forth, optimizes the use of MCU pins while driving multiple loads.

The device integrates multiple protection. The 20-µs fixed off time current regulation with mixed decay and slow decay modes enable overcurrent protection in drives and also helps to achieve the best current regulation.

The DRV8847 device brings multiple levels of built-in protection including undervoltage-lockout, overcurrent protection on each FET with deglitch time, short-circuit protection, open-load detection, and overtemperature protection increases the robustness and reliability of the system. Fault conditions are indicated on the nFAULT pin. The I^2C device variant (DRV8847S) has detailed diagnostics, and can communicate the same to the MCU.

2.2.2 TPS2596

From the design specifications mentioned in Table 1, two circuits having a total power consumption less than 15 W can be identified. The description of these circuits follows:

- The circuits consisting of two DRV8847S drivers, which drive the bipolar stepper and multiple solenoid and actuator loads
- The circuit consisting of the DRV8847PWP driver, which drives the brushed DC motor in half-bridge parallel mode.

The 12-V supply line nodes, for powering these two circuits can be identified as nodes where load power is typically less than 15 W, under nominal operation. In design, if the power consumption on these nodes is ensured to be within 15 W, even under any abnormal condition, those nodes may qualify as low-power nodes (nodes with power consumption less than 15 W), and the downstream circuit at nodes away from the power source may qualify as low-power circuits (LPCs) as per the definition in IEC 60335-1. A low-power circuit may save on design costs and also may enable faster safety qualification of the subsystems with LPCs.

NOTE: The end-equipment manufacturer and the designer must refer to the standard IEC 60335-1 to understand the definition of low-power circuits and any further requirements to qualify the same. The end-equipment manufacturer and the designer should refer to the standard to understand the benefits of LPCs.

The TPS2596xx family of eFuses (integrated FET hot-swap devices) is a highly integrated circuit protection and power management solution providing multiple protections against overloads, short circuits, voltage surges, and excessive inrush current. The device is available in two variants. For the TPS25962x variants, in case of an input overvoltage condition, internal clamping circuits limit the output to a safe fixed maximum voltage (pin selectable), with no external components. The TPS25963x variants provides an option to set a user defined overvoltage cutoff threshold.

In this reference design, two TPS259631 eFuse chips are connected on the 12-V line, each on the LPC nodes. eFuses are a simple and cost effective way to limit the power delivered to the downstream load and protect the system under any abnormal conditions. The TPS259631 offers adjustable overvoltage lock out (OVLO) with auto-retry response during thermal shutdown. The precise current limit with less than ±5% error, at 25˚C, provides excellent accuracy, making the TPS259631 device well-suited for many system power limit and protection applications. For the given load condition, higher input voltage will produce more power at the load and that may be more than 15 W if the load current is not reduced.

Load, source, and device protection are provided with multiple programmable features including overcurrent, short circuit, excessive inrush current, overvoltage, and undervoltage. A threshold accuracy less than ±6% for UV and OV ensures tight supervision of bus voltages, eliminating the need for supervisor circuitry. If the 12-V power supply line is very poorly regulated, the TPS259631 device helps to optimize the working voltage range of the downstream converters by the UV-OV protection. This reduces the design margin of downstream converters and reduces production costs. The TPS259631 device is rated to operate from 2.7 V to 20 V absolute voltage, and helps to design a rugged system even with a poor regulated 12-V line.

Fault flag output (FLT) is provided for system status monitoring and downstream load control.

For hot-plug-in boards, the TPS259631 device provides in-rush current control and programmable output ramp-rate. Output ramp rate is programmable using a capacitor at the dVdt pin, for maximum design flexibility.

2.2.3 TVS1400

Why is surge protection needed on the 12-V line? A poor AC input EMI filter may cause the surge voltage to get propagated to the DC rails such as the 12-V bus lines. The TVS1400 device ensures that any propagated or direct surge voltage into the 12-V line is clamped properly and the downstream circuits are well protected.

The reference design uses the TVS1400 device to provide surge protection. The TVS1400 device enables a precision clamp with a low, flat-clamping voltage during transient overvoltage events like surge and protects the system with zero voltage overshoot. The TVS1400 device is a precision clamp that handles 43 A of IEC 61000-4-5 8/20 µs surge pulse. The flat-clamping feature helps keep the clamping voltage very low to prevent the downstream circuits from being stressed. The flat-clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower-voltage tolerant downstream ICs. The TVS1400 device has minimal leakage under the standoff voltage of 14 V, making it an ideal candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events.

2.2.4 MSP430FR5739

The TI MSP430FR573x family of ultra-low-power microcontrollers consists of multiple devices that feature embedded FRAM nonvolatile memory, ultra-low-power 16-bit MSP430™ CPU, and different peripherals targeted for various applications. The architecture, FRAM, and peripherals, combined with seven low-power modes, are optimized to achieve extended battery life in portable and wireless sensing applications. FRAM is a new nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption. Peripherals include a 10-bit ADC, a 16-channel comparator with voltage reference generation and hysteresis capabilities, three enhanced serial channels capable of I^2C, SPI, or UART protocols, an internal DMA, a hardware multiplier, an RTC, five 16-bit timers, and digital I/Os.

2.2.5 TPD1E10B06

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications. Typical applications of this ESD protection product are circuit protection for audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports, and general-purpose I/O ports.

2.2.6 TIDA-01447 (3.3 V DC-DC UsingTPS561201)

The TIDA-010004 reference design, requires a 3.3-V supply for the functioning of the MCU and is generated using another TI reference design, the TIDA-01447.

The TIDA-01447 demonstrates a small solution size, high-efficiency, and low-EMI DC/DC module for LDO replacement. Replacing LDOs with DC/DC modules drastically improves system efficiency, saving on solution size, and BOM cost while also eliminating the need for heat sinks. The module takes up the same amount of space as a TO-247 package and is pin-to-pin compatible with the TO-220 LDO, such as the UA7805 device, enabling quick evaluation and reduced time-to-market. The TPS561201 power converter used in the TIDA-01447 enables a higher output current and lower power consumption at full-load, low-load, and standby operation. The TIDA-01447 has 1.1-µA standby current and 423-µA no load current.

The TPS561201 device used in the TIDA-01447 is a 1-A synchronous step-down converter in a SOT-23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current. The TPS561201 device operates in pulse skip mode, which maintains high efficiency during light load operation.

2.3 System Design Theory

2.3.1 Surge Protection at the Input

The reference design uses the TVS1400 device at the input to provide surge protection. The TVS1400 enables a precision clamp with a low, flat-clamping voltage during transient overvoltage events like surge and protects the system with zero voltage overshoot. The TVS1400 device is a precision clamp that handles 43 A of IEC 61000-4-5 8/20 µs surge pulse.

Figure 2 shows the DC input section of the schematic with the TVS1400 device. A 12-V supply is given at J1. The TVS1400 device is connected after J1 and very close to J1. The capacitor C4 is the bulk electrolytic capacitor connected at the 12-V line to provide the ripple current as demanded by the downstream circuits.

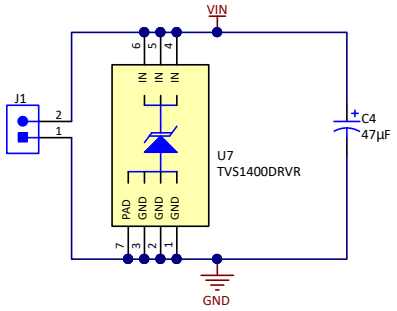

Figure 2. Power Supply Input Schematic With Surge Protection

2.3.2 Low-Power Circuit With eFuse

The eFuse circuit is incorporated and designed to limit the downstream circuit power less than 15 W, and hence helps easy qualification as a low-power circuit. The eFuse also provides the undervoltage and overvoltage protections to increase the reliability of subsystem. Table 2 shows the design parameters for the eFuse circuit. Figure 3 shows the schematic of the TPS259631 eFuse circuit.

Table 2. Design Parameters for eFuse

DESIGN PARAMETER	DESIGN VALUE
Input voltage range	2.7–17.5 V (12 V nominal) (17.5 V is considered as the clamp voltage of TVS1400)
Undervoltage lockout set point, V_{UV}	6.8 V
Overvoltage lockout set point, V_{OV}	13.5 V
Current limit	1.11 A
Load capacitance	44 µF

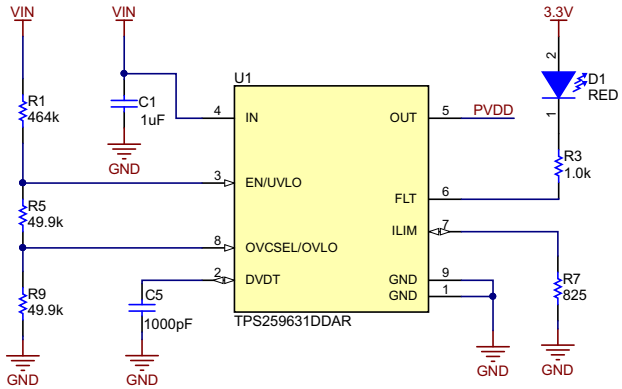

Figure 3. Schematic of eFuse Circuit

The R_{ILIM} resistor at the ILIM pin sets the overcurrent limit, set this using Equation 1.

$$R_{LIM}(\Omega) = \frac{905}{I_{LIM} - 0.015} \quad (1)$$

For I_{LIMIT} = 1.11 A, using Equation 1, R_{ILIM} = 826.48 Ω. Selecting the nearest standard resistor value, R_{ILIM} = 825 Ω, I_{LIMIT} = 1.1119 A

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using the external voltage divider network of R1, R5, and R9 as connected between the IN, EN, OVLO, and GND pins of the device. The values required for setting the undervoltage and overvoltage during input voltage rising are calculated by solving Equation 2 and Equation 3:

$$V_{OV} = V_{OVLO} \times \frac{R1 + R5 + R9}{R9} \quad (2)$$

$$V_{UV} = V_{UVLO} \times \frac{R1 + R5 + R9}{R5 + R9} \quad (3)$$

From the device electrical specifications, V_{UVLO} = 1.2 V and V_{OVLO} = 1.2 V, during input voltage rising.

The resistance values are selected to minimize the current consumption in the resistor network. For design requirements, V_{OV} is 13.5 V and V_{UV} is 6.8 V. Selecting R9 = 49.9 kΩ, and by solving Equation 2 and Equation 3, R5 = 49.9 kΩ, R1 = 464 kΩ.

NOTE: For designing the circuit to limit the input power to less than 15 W (to ease the LPC qualification), the over voltage protection threshold tolerance of the TPS259631, current limit tolerance of the TPS259631, and the tolerance of external threshold setting resistors must be considered. For example, considering the maximum $V_{OLVO(R)}$ threshold (1.27 V) of the TPS259631, the maximum over voltage trip point is 14.35 V (using Equation 2). For a 15-W power limit, the current limit can be calculated as 1.0453 A at 14.35 V. Allowing 8% tolerance (maximum tolerance of the TPS259631), the current limit has to be set at 0.9617 A. This analysis did not consider the tolerance of the external resistors for setting the thresholds for the TPS259631. The designer has to consider all the design tolerances for the power limit calculation.

The power failure threshold is detected on the falling edge of the supply. This threshold voltage is 1.1 V typical.

Using Equation 3 and V_{UVLO} = 1.1 V, V_{PFAIL} = 6.2 V, the power fail threshold is 6.2 V.

Calculate the total ramp time (t_{SS}) of V_{OUT} for 0 to V_{IN} using Equation 4:

$$C_{dVdt}(pF) = \frac{42000}{SR(V/ms)} \quad (4)$$

Using C_{SS} = 1000 pF, SR = 42 mV/us. Therefore, the ramp up time for VOUT to rise from 0 to 6.8V is, tss = 6.8 V/ 42 V/ms = 0.162 ms.

Calculate the inrush current using Equation 5:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{SS}} \quad (5)$$

With C_{OUT} = 44 µF, I_{INRUSH} = 1.848 A.

The resistor R3 serves as pullup for the open-drain output driver at the pin FLTb. The current sunk by this pin should not exceed 10 mA. C_{IN} (C1 in the reference design) is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise.

For detailed design, thermal shutdown, power dissipation during inrush, and ramp-up time to avoid the thermal shutdown during start up, see *TPS2596 2.7 to 19 V, 0.13 to 2-A, 85-mΩ eFuse With Accurate Current Monitor and Fast Overvoltage Protection*.

2.3.3 DRV8847 Driving Bipolar Stepper

Figure 4 shows the DRV8847 schematic to drive a bipolar stepper motor. The DRV8847 device has four half bridges and the midpoint of each half bridge is connected to motor winding through OUT1, OUT2, OUT3, and OUT4. There are four input pins, IN1 to IN4 for controlling the half bridges. Configure the bipolar stepper control through the DRV8847 device for a 4-pin interface or 2-pin interface.

In the 4-pin interface, the DRV8847 device is configured to drive a bipolar stepper motor with full functional modes. The 4-pin interface uses the IN1, IN2, IN3, and IN4 pins to control the drivers. In this mode the stepper or brushed DC motor can operate with all four modes (forward, reverse, coast, and brake mode) because the stepper motor can operate in either full-stepping mode or the non-circulating half-stepping mode.

In the 2-pin interface, the DRV8847 device is configured to drive a stepper motor with a decreased number of pins and functionality. In a 2-pin interface use the IN1 and IN2 pins to control the driver. In this mode the stepper motor can operate in only two modes (forward mode and reverse mode) because the stepper motor operates only in full-step mode. This 2-pin interface is very useful for low GPIO applications.

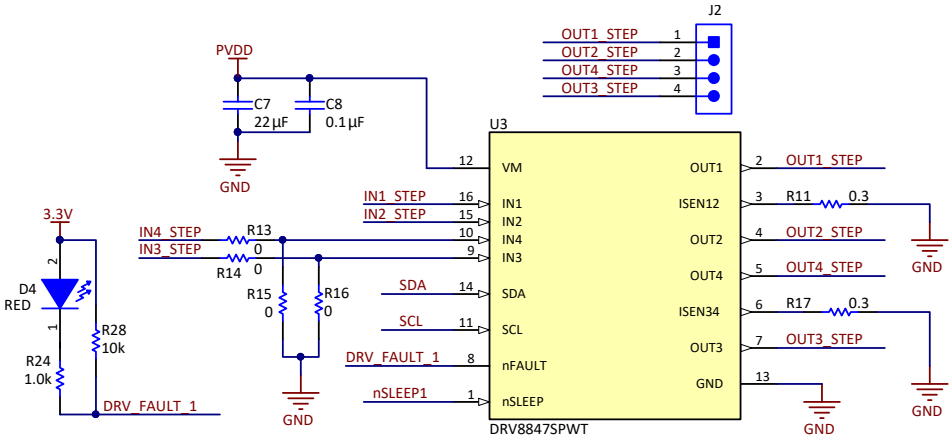

Figure 4. Schematic of DRV8847 Driving a Bipolar Stepper

The reference design is primarily targeted to show the 2-pin interface of the DRV8847 device, where the device is controlled through IN1 and IN2 issued by the MCU. The interface MODE is set by programming the registers of DRV8847 through I^2C. Also connect R15 and R16 to pull the IN4 and IN3 pins to ground and remove the R13 and R14 resistors.

The device goes to functional mode if the nSLEEP pin is pulled to logic high and the pin is controlled by the MCU GPIO pin.

The current regulation threshold is designed by the current sense resistors (R_{SENSE}) R11 and R17 connected to the ISEN pins as defined by Equation 6.

$$I_{TRIP} = \frac{V_{TRIP}}{R_{SENSE}} \tag{6}$$

From *DRV8847 Dual H-Bridge Motor Driver*, the current limit threshold voltage, V_{TRIP} = 0.15 V typical (0.135 V minimum to 0.165 maximum). In the reference design, the required current limit, I_{TRIP} = 0.5 A. Therefore, using Equation 6, R11 = R17 = 0.3 Ω.

Power loss in each R_{SENSE} = $I_{TRIP}^2 \times R_{SENSE}$ = 75 mW. The reference design uses 0.3 Ω, 0.5 W, 1% current sense resistors. C7 and C8 are the power supply capacitors and are rated to handle the maximum supply voltage. The FAULT output is pulled up through a resistor and LED. Use a pullup resistor of more than 1 kΩ, to make sure that the current consumption in the FAULT pin is limited within the recommended current.

2.3.4 DRV8847 Driving Independent Loads

In the independent bridge interface, the DRV8847 device is configured for independent half-bridge operation. In this configuration, use IN1, IN2, IN3, and IN4 pins to independently control the OUT1, OUT2, OUT3, and OUT4 pins respectively. Only two output states of the OUTx pin can be controlled (either connected to VM or connected to GND). This mode is used to drive independent loads such as relays, solenoids, and actuators.

Use this interface option for the following loads:

- Relay or solenoid coils connected to the VM pin or ground
- Single- or dual-BDC motor (with or without current regulation) with reduced functional BDC modes (forward, reverse, and braking mode only)

Figure 5 shows the schematic of the DRV8847 device driving independent loads.

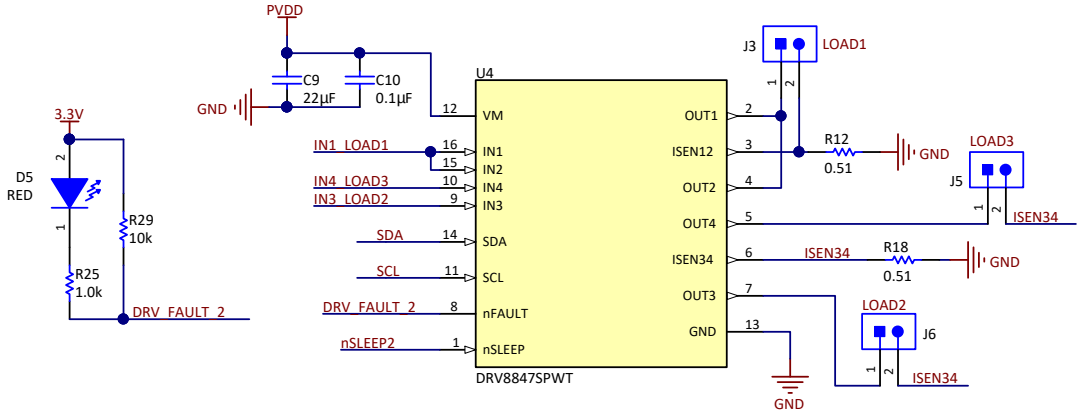

Figure 5. Schematic of DRV8847 Driving Independent Loads

The resistors R12 and R18, are used as current limit resistors and will act for two half bridges together, like OUT1 and OUT2 together and OUT3 and OUT4 together. The values of R12 and R18 are selected to 0.51 Ω each to limit the combined current for two half bridges to within approximately 0.3 A . Use Equation 6 to calculate the current limit.

The nSLEEP pin of the device is controlled through the MCU and the nFAULT pin is pulled up through a resistor and LED.

2.3.5 DRV8847 Driving Brushed DC Motor Using Output Paralleling

Figure 6 shows the DRV8847 schematic driving a brushed DC motor using two half-bridge paralleling.

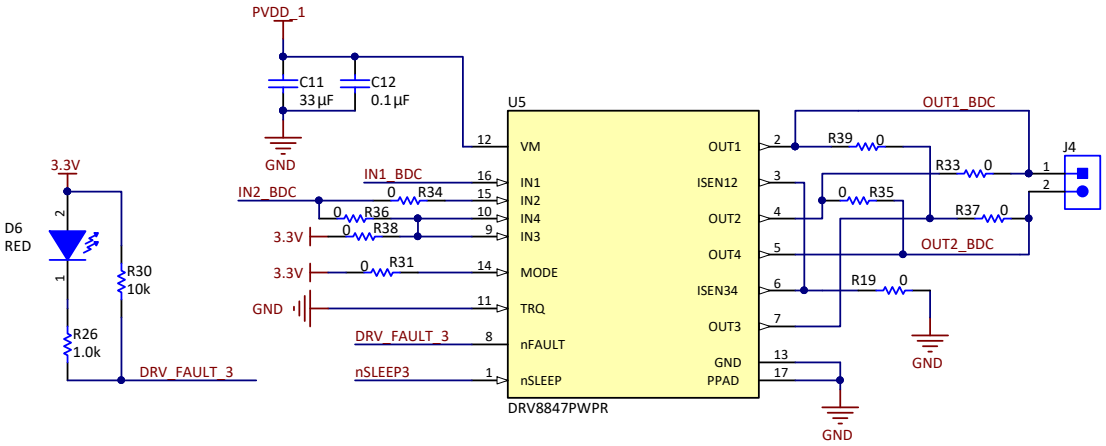

Figure 6. Schematic of DRV8847 Driving Brushed DC Motor With Options of Paralleling

The reference design has the following options:

- OUT1 and OUT2 in parallel and OUT3 and OUT4 in parallel to drive a brushed DC motor in uni-direction or bidirection. Achieve this by connecting R33 and R37 at the output and leave R39 and R35 open. At the input, connect IN1 and IN2 together at the pin, connect R36 and remove R34 and R38. Remove R31 to leave the MODE pin Hi-Z to select the independent bridge interface mode.
- OUT1 and OUT3 in parallel and OUT2 and OUT4 in parallel to drive a brushed DC motor in uni-direction or bidirection. Achieve this by connecting R39 and R35 at the output and leave R33 and R37 open. At the input, remove R36 and connect 34 and R38. Connecting R38 enables 3.3 V at the MODE pin and the device enters the parallel interface mode along with R31.

Set the current limit with R19. The reference design does not use any current limit from the DRV8847 device; therefore, a 0-Ω resistor is populated.

The nSLEEP pin of the device is controlled through the MCU and the nFAULT pin is pulled up through a resistor and LED.

2.3.6 Interface to the MCU - MSP430FR5739

Figure 7 shows the configuration of the MSP430FR5739 MCU. The reference design uses 10-µF decoupling capacitors (C3, C14) at the AVCC and DVCC pins. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency.

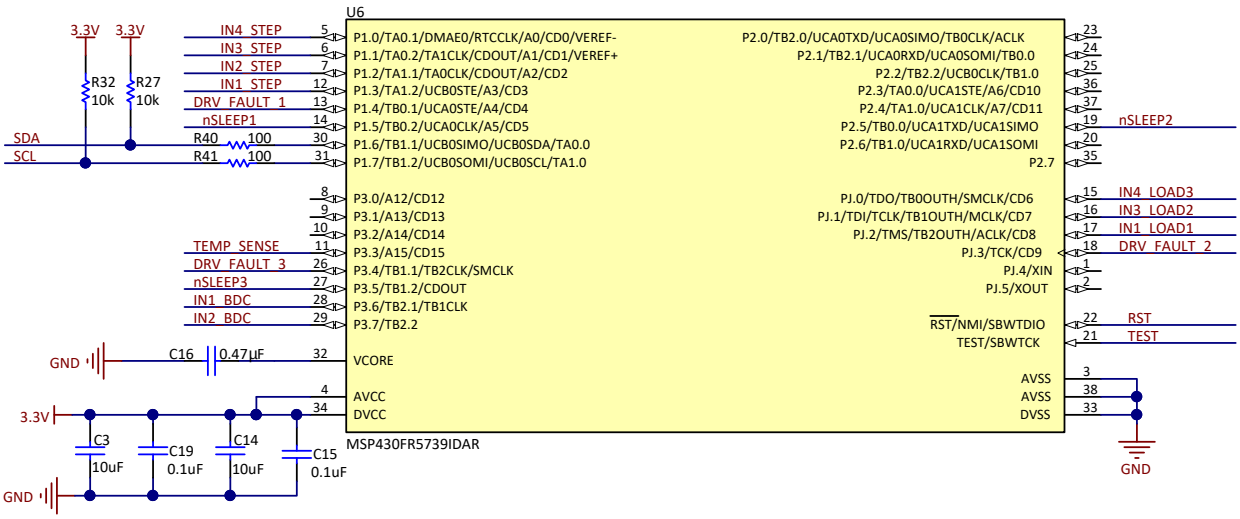

Figure 7. MSP430FR5739 Schematic

The two I²C-variant DRV8847S are controlled by MSP430FR5739 in multi-slave configuration. The MSP430 is configured as a single master and the two DRV8847S chips forms two slaves. The SDA and SCL lines are connected to the MCU with 10-kΩ pullups on each line.

The TIMER TA1 controls the bipolar stepper driver in the 2-pin interface. The TA1.1 and TA1.2 are configured to produce 90 degree phase-shifted signals to the DRV8847. The TIMER TB2 is configured to generate the PWM signals to control the brushed DC motor driver DRV8847PWP.

The temperature information from the external temperature sensor is connected to the ADC pin of the MCU.

2.3.7 Temperature Sensor Interface

Figure 8 shows the temperature sensor interface option to the board. For example, to control the damper in a refrigerator, where the damper controls the air flow between the freezer and rest of the compartment, the temperature information of the freezer and other compartments is required. The ESD protection TPD1E10B06D connected near J7 provides protection under ESD events as high as ±8-kV contact discharges.

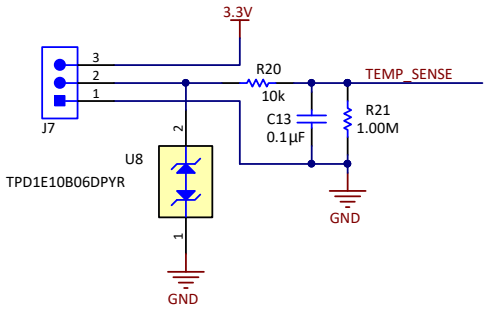

Figure 8. Temperature Senor Interface

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Figure 9 shows the connector configuration of this reference design, which features:

- Two-terminal input for power supply (J1): This is used to connect the input 12-V DC supply. Figure 9 identifies the positive and negative terminals.
- Four-terminal output for bipolar stepper motor winding connection (J2): The OUT1 to OUT4 connections from the DRV8847 are available at J2 to connect to the four winding terminals of a bipolar stepper.
- Two-terminal outputs J3, J5 and J6: These terminals are connected to the DRV8847 device which is driving independent loads. Uni-directional brushed DC motor, solenoids, valves, heaters, and so forth, can be driven by these terminals.
- Three-pin connector J7: This connector interfaces the temperature sensor output. Use the 3.3-V pin to supply power to the external temperature sensor. Connect the temperature sensor output to the midpoint marked TEMP.
- Four-pin connector J8: This is the programming connector for the MSP430FR5739 MCU. The two-wire Spy-Bi-Wire protocol is used to program the MSP430FR5739. See the *development tools* of the MSP430FR5739 for programming options with an external JTAG interface.
- Three-pin connector J9: This connector interfaces the TIDA-01447 external board to this reference design board. The TIDA-01447 is the DC/DC converter for generating the 3.3-V supply from the 12-V line.
- Two-pin connector J4: Connect the external brushed DC motors winding terminals to J4.

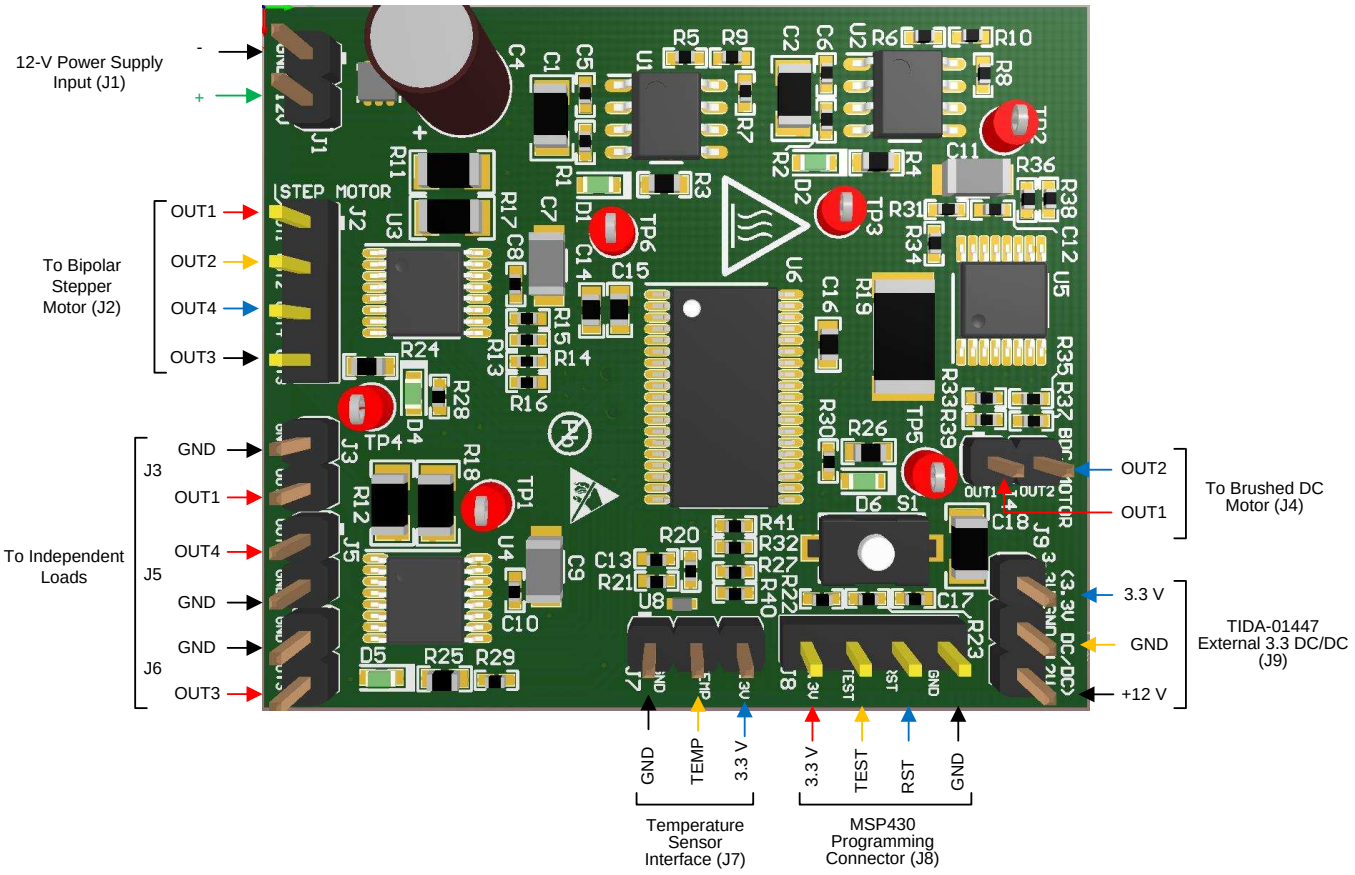

Figure 9. TIDA-010004 PCB Connectors

Follow this procedure for board bring-up and testing:

1. Remove the motor connections from the board, and power on the input DC supply.
2. Program the MCU. Make sure that the configuration in the program is done as per Section 3.1.2.
3. Remove the programmer, and switch off the DC input supply.
4. Connect the motor winding connections and other loads to the motor.
5. Apply 12-V DC to the board using a current-controlled DC power supply. Set the current limit of the power supply to 4 A.

3.1.2 Software

3.1.2.1 High-Level Description of Application Firmware

The TIDA-010004 firmware offers the following features and user-controllable parameters:

- 2-pin or 4-pin control of the DRV8847 device driving a bipolar stepper motor.
- Multi-slave I^2C communication with the two DRV8847S drivers. The MCU configures the registers of two DRV8847S drivers and also the fault diagnosis of the DRV8847 drivers.

The TIDA-010004 firmware system components are tabulated in Table 3.

Table 3. TIDA-010004 Firmware System Components

SYSTEM COMPONENT	DESCRIPTION
Development and emulation	*Code Composer Studio* version 7.2
Target controller	MSP430FR5739
Oscillator clock frequency	16 MHz
PWM generation- Timer configuration	TA1.1 and TA1.2 controlling IN1 and IN2 of DRV8847 driving bipolar stepper motor. TA0.1 and TA0.2 controlling IN3 and IN4 of DRV8847 enabling bipolar stepper motor 4 pin control along with IN1 and IN2. TB2.1 and TB2.2 controlling IN1 and IN2 of DRV8847PWP, driving the brushed DC motor by half-bridge paralleling.
I^2C communication	UCB0SDA and UCB0SCL are configured to communicate to DRV8847 through I^2C in single master multiple slave configuration, up to 400 kHz speed.
ADC configuration	A15 ->Temperature measurement feedback signal
MCU digital Inputs/Output	The GPIOs control the nSLEEP pins of multiple DRV8847 devices. Reads the nFAULT pin of DRV8847 devices. The MCU GPIOs also drive the INx pins of the DRV8847 device configured in independent mode.

3.1.2.2 Customizing the Reference Code

Select the main.c file. The parameters at the top of the file can be optimized and are included as the configuration variables. The following section of code shows these parameters:

```
/************ Speed setting of BDC and bipolar stepper motor ************/
#define BDC_PWM_PERIOD        400   // PWM Frequency for BDC motor = 16MHz/((2*PWM_PERIOD)-1)
#define BDC_PWM_DUTY          360   // BDC Duty Cycle = BDC_PWM_DUTY/BDC_PWM_PERIOD.(360/400=0.8)
#define STEPPER_SPEED_COUNT   2000  // Stepper motor speed, TA1_CLK=125kHz(ACLK=1MHz,pre-scalar=8)
                                    // Stepper rotation freq.= 125 kHz/((2*STEPPER_SPEED_COUNT)-1)

/******* Register setting of DRV8847 controlling bi-polar stepper motor *******/
#define STEP_SLAVE_ADDR       0x50  // Slave Address of DRV8847 driving bi-polar stepper
#define STEP_REG_IC1_CON      0x01  // Control register 1(IC1_CON) value
#define STEP_REG_IC2_CON      0x05  // Control register 2(IC2_CON) value
#define STEP_REG_SLR_STATUS1  0x40  // Slew rate and Status register 1 value

/******** Register setting of DRV8847 controlling bi-polar stepper motor *******/
#define INDEP_SLAVE_ADDR      0x70  // Slave Address of DRV8847 driving independent loads
#define INDEP_REG_IC1_CON     0x83  // Control register 1 (IC1_CON) value
#define INDEP_REG_IC2_CON     0x04  // Control register 2 (IC2_CON) value
#define INDEP_REG_SLR_STATUS1 0x40  // Slew rate and Status register 1
```

For detailed understanding of the register mapping and bit details, see *DRV8847 Dual H-Bridge Motor Driver*.

Multi-slave operation is used to control multiple DRV8847S devices through one I^2C line. The default device address of the DRV8847 device is 0x60 (7-bit address). Therefore, any DRV8847S devices can be accessed using this address. The steps for multi-slave configuration for programming device-1 out of 2 connected devices are as follows

1. The DRV8847S device variant is configured for multi-slave operation by writing the DISFLT bit (IC2_CON register) of all connected devices to 1b. This step disables the nFAULT output pin of all DRV8847S devices, to avoid any race condition between master and slave I^2C device.
2. Pull the nFAULT pin (nFAULT2 pin) of the other device-2 to low to release the I^2C buses of the slave device-2. Now only device-1 is connected to master.
3. Since, only one device, DRV8847S (1), is connected to the controller, and, therefore, its slave address can be reprogrammed from default 0x60 (7-bit address) to another unique address.
4. Similarly, the slave address (SLAVE_ADDR) of the other device can be reprogrammed sequentially to unique addresses by a combination of nFAULT pins.
5. When all slave addresses are reprogrammed, resume the DISFLT bit to 0b (IC2_CON register). This will enable the nFAULT output pin for fault flagging.
6. All the nFAULT pins are released and a multi-slave setup is complete. Now all connected slave devices can be accessed using the newly reprogrammed address.
7. Repeat the previous steps for any device in case of a power reset (nSLEEP).

3.1.2.3 4.9 Controlling the DRV8847 Using I2C Lines only Without Using INx Pins

The DRV8847 can be used to control the bipolar stepper motor and other loads by using only the I2C pins. In this case the DRV8847 bridges are controlled by configuring the INx bits of the IC1 control register and the INx pins of the device are left open. This means only two pins of the DRV8847 (the SDA and SCL lines for I2C) help in controlling the load, reading the fault status and also to run the fault diagnosis, saving the pins from the MCU. In this I2C control, the MODE bits of the IC1 control register can be set for 4-pin interface.

For bipolar stepper motor half stepping control, the following sequence steps setting can be written to IC1 control register one by one to control the OUTx pins:

Sequence step 1: IN1 = 0, IN2 = 0, IN3 = 0, IN4 = 1

Sequence step 2: IN1 = 1, IN2 = 0, IN3 = 0, IN4 = 1

Sequence step 3: IN1 = 1, IN2 = 0, IN3 = 0, IN4 = 0

Sequence step 4: IN1 = 1, IN2 = 0, IN3 = 1, IN4 = 0

Sequence step 5: IN1 = 0, IN2 = 0, IN3 = 1, IN4 = 0

Sequence step 6: IN1 = 0, IN2 = 1, IN3 = 1, IN4 = 0

Sequence step 7: IN1 = 0, IN2 = 1, IN3 = 0, IN4 = 0

Sequence step 8: IN1 = 0, IN2 = 1, IN3 = 0, IN4 = 1

With 100% torque scaling, the sequence of the IC1 control register vales are: {0x44, 0x4C, 0x0C, 0x2C, 0x24, 0x34, 0x14, 0x54}.

Each step corresponds to 45 degree electrical, and the time period of each step determines the speed of the motor. A periodic time-based interrupt subroutine can be used to write the DRV8847 control register as per the required INx bit values.

From the I2C write sequence frame of the DRV8847, which includes the START, 7-bit address, R/W, ACK, 8-bit register address, ACK, 8-bit data, ACK, STOP signals, the total length of the frame is 29 bits. With the allowed maximum SCL clock frequency of 400 kHz, the latency for one write cycle is 72.5 µs (= 29 / 400 kHz). Each write corresponds to 45 degree electrical in bipolar motor half step control. Considering a margin, assuming 100 µs write latency in the programming, it takes 800 µs to complete 360 degree electrical (8 write cycles). This means, when the motor is controlled via I2C, the maximum speed achievable is approximately 1.25 kHz. However, if a read cycle for the fault signal is also incorporated after the write cycle, the maximum achievable speed reduces. The register read latency can be found in a similar way by looking at the read sequence frame.

The designer has to calculate the latency and maximum achievable speed as per the clock used and other functions used in firmware.

3.2 Testing and Results

3.2.1 Test Setup

Figure 10 shows the test setup in the lab, where the reference design is driving multiple loads including a bipolar stepper motor, multiple brushed DC motors, and resistive-inductive (RL) loads.

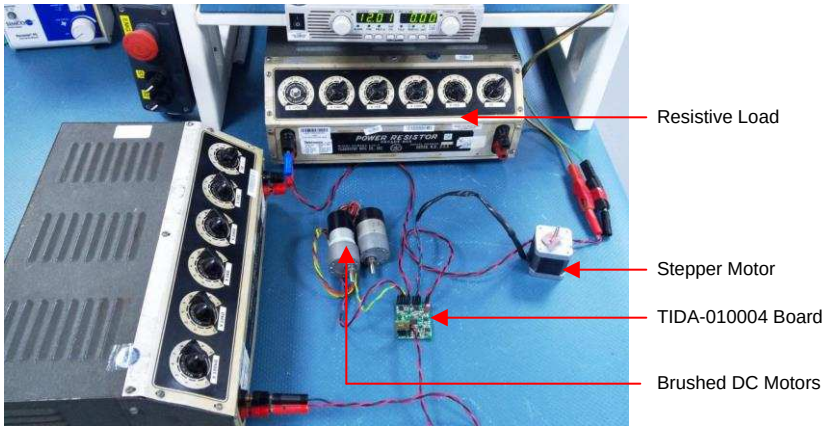

Figure 10. Test Setup With TIDA-010004 Reference Design

3.2.2 Test Results

3.2.2.1 3.3-V Power Supply Generated by TIDA-01447

Figure 11 shows the 3.3 V generated from the LDO. The ripple in the 3.3-V rail is less than 15 mV.

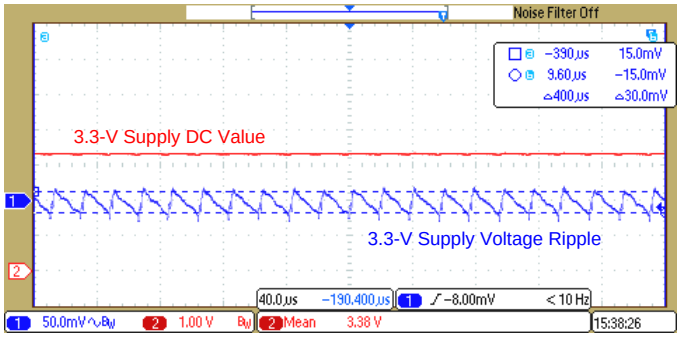

Figure 11. 3.3 V Generated by TIDA-01447 Board

3.2.2.2 Testing for Power Limit With eFuse

The eFuse TPS259631 circuit is designed to limit the current consumption to 1.11 A, which will limit the power to 15 W at 13.5-V supply input.

Figure 12 shows the test results with current and power limit operation of the eFuse. The test results show the peak current is limited to 1.12 A. The input voltage is 12 V, and the output voltage got reduced to 9 V which depends on the output load impedance.

In eFuse during overload conditions, the internal current-limit amplifier regulates the output current to I_{LIMIT}. The output voltage droops during current-limit regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold (TSD), the internal FET is turned off. When the TPS259631 detects thermal overload, the device will remain off until it has cooled down to TSD_{HYS}. Once the TPS259631 has cooled down by TSD_{HYS}, the device will remain off for an additional delay of $t_{TSD,RST}$ after which the device will automatically retry to turn on if the device is still enabled. During thermal shutdown, the fault pin FLT pulls low to signal a fault condition. Figure 12 shows once the thermal shut down happens, the internal FET turns off and hence the output voltage and current goes to zero.

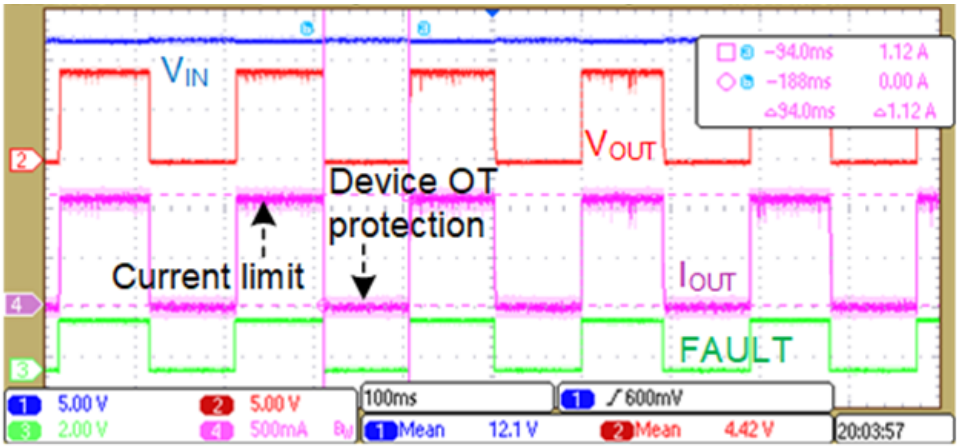

Figure 12. Accurate Current and Power Limit by eFuse TPS259631 and Device Shutdown Due to Overtemperature

The current limit can be observed as 1.12 A against a set current limit of 1.1119 A, which means the error is 0.7 %.

3.2.2.3 Controlled Start up With eFuse Reducing Inrush Current

The TPS259631 device is designed to control the in-rush current. This limits the voltage sag on the supply voltage and prevents unintended resets of the system power. A slew rate controlled startup also helps to eliminate conductive and radiated interference. An external capacitor from the dVdt pin to GND defines the slew rate of the output voltage at power on (see Figure 13).

This reference design uses a 1000-pF capacitor at the dVdt pin. With 6.8-V undervoltage lock out and substituting 6.8 V in Equation 5, the startup delay t_{SS} = 0.162 ms. The test results shows a startup delay of 0.4 ms. The difference is because during the startup period, the input current reaches current limit and hence the ramp up time is more than 0.162 ms.

Figure 13. Controlled Start-up Slew Rate With eFuse

Figure 14 shows the inrush current in the circuit without using eFuse. Observe that inrush current is uncontrolled, as the input current increases with input voltage and at one point, inrush spikes up due to some capacitive switching in the circuit. Figure 15 shows the inrush current with eFuse. The presence of the eFuse eliminates any inrush due to capacitive switching or start enable. The eFuse controls the inrush current making sure that there are no undesirable voltage dips and undervoltage lock outs due to heavy inrush current.

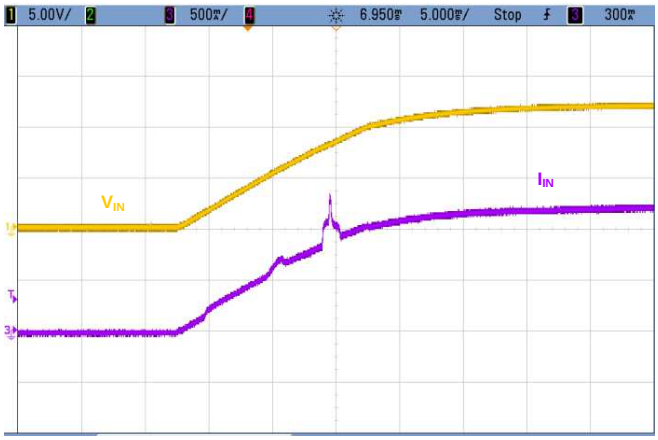

Figure 14. Inrush Current Without eFuse

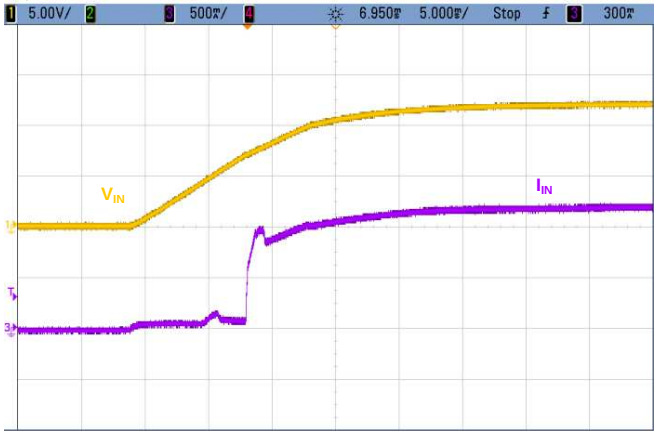

Figure 15. Inrush Current With eFuse

3.2.2.4 Thermal Evaluation of eFuse at the Rated Load

Figure 16 shows the voltage and current waveforms at the eFuse terminals under the rated load of 1.12 A and 12 V input.

From the test result capture, V_{IN} = 12.1 V and I_{IN} = 1.12 A.

Input power to the eFuse = $V_{IN} \times I_{IN}$ = 12.1 × 1.12 =13.55 W.

Approximate $R_{DS(on)}$ of TPS259631 at 25°C = 85 mΩ

Estimated power loss in the eFuse, $P_{LOSS} = I^2 \times R_{DS(on)} = 1.12^2 \times 0.085 = 0.107$ W.

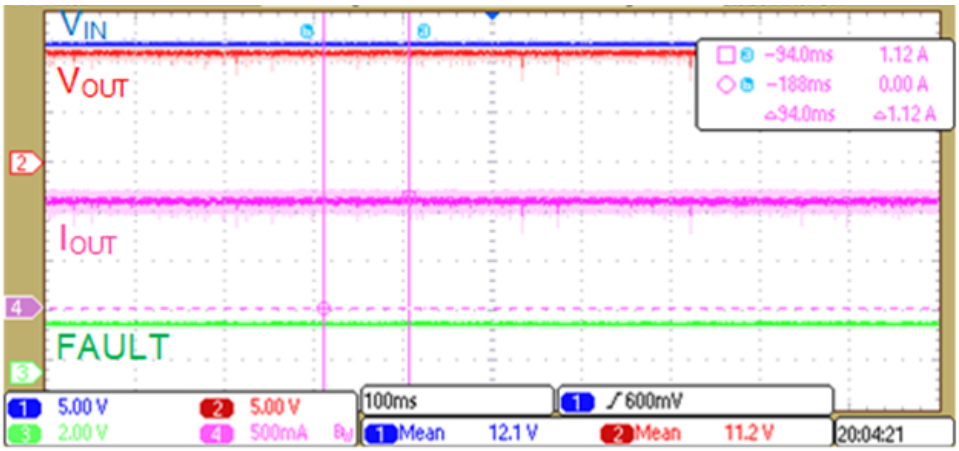

Figure 16. eFuse Input and Output Voltage and Current

3.2.2.5 Testing With Short-Circuit at the Output of eFuse

Figure 17 shows the test results with the external short circuit on the output of eFuse. The testing is done at 12-V DC input. Fast short circuit limit of TPS259631 quickly protect the circuit against hard shorts circuits. When a short circuit is detected, the device quickly throttles the FET to first decrease the current to an intermediate value before it can regulate the current to the programmed I_{LIM} value. While the device is in current limit, there's significant power dissipation inside the part due to higher voltage drop across the FET, causes thermal shut down. The thermal shutdown is reported on the FAULT pin.

The eFuse enables reliable protection with overcurrent protection and power limit under abnormal conditions.

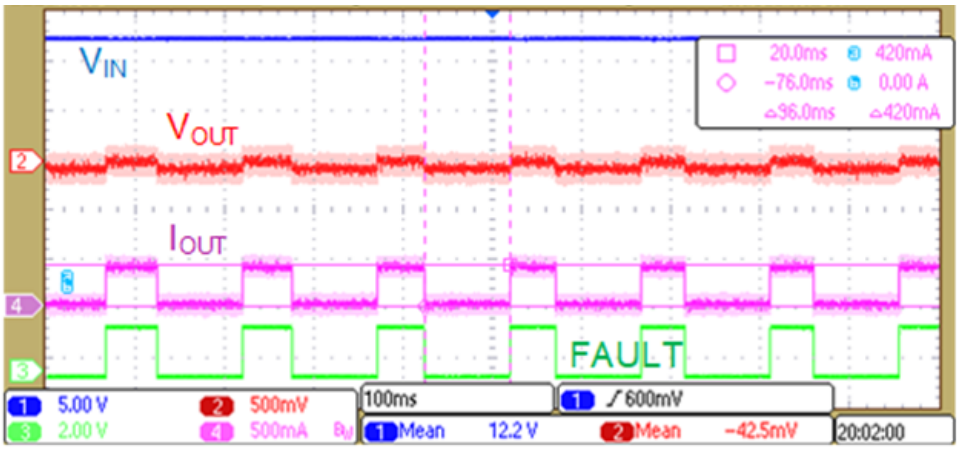

Figure 17. Test Results With Short Circuit on the eFuse Output

3.2.2.6 Overvoltage and Undervoltage Protection by eFuse

The TPS259631 device incorporates circuits to protect the system during undervoltage and overvoltage conditions. A voltage more than the V_{OVLO} threshold on the OVLO pin turns off the internal FET and protects the downstream load.

When an undervoltage or input power fail event is detected, the internal FET is quickly turned off, and FLT is asserted. The TPS259631 device also implements internal undervoltage lockout (UVLO) circuitry on the IN pin. The device gets disabled when the IN terminal voltage falls below internal UVLO threshold V_{UVLO}.

The reference design is designed with overvoltage protection voltage of 13.5 V, and undervoltage protection voltage of 6.8 V. Figure 18 shows the overvoltage shut down at 13.5 V. When the OVLO pin reaches 1.2 V, the device shuts down and FAULT is asserted. Figure 18 also shows the undervoltage protection feature of the TPS259631 device. As the VIN voltage ramps up and once the VIN voltage reaches 6.8 V, and hence when the EN/UVLO pin voltage reaches 1.2 V, the eFuse device is enabled and the FAULT pin goes high.

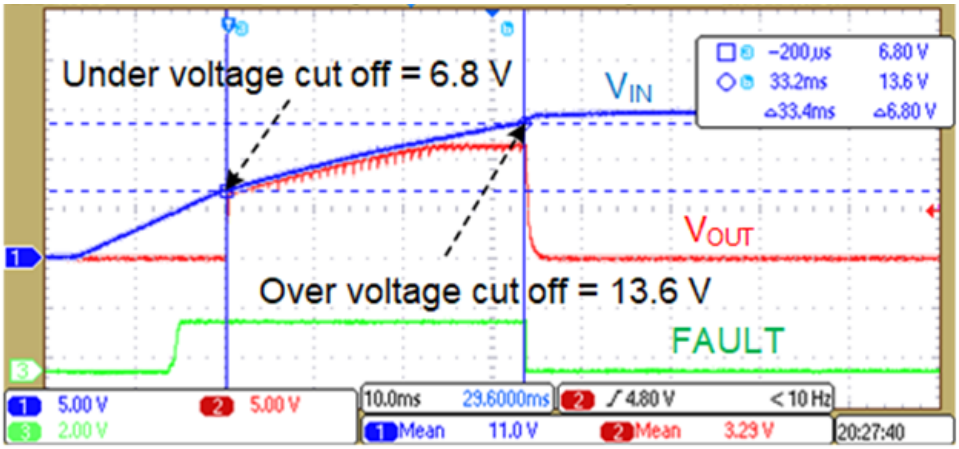

Figure 18. Undervoltage and Overvoltage Protection by eFuse at 13.5 V

If the end-equipment uses a single flyback or similar power supply with multiple outputs, a poor regulation on the 12-V line leads to large output voltage fluctuations under transients, when no eFuse is used in the system.. The downstream converters need to be designed for those variations, which lead to more design margin and hence more cost. The OV and UV protection in the eFuse will help in taking care of large voltage fluctuations. The eFuse rated from 2.7- to 20-V absolute is well-suited for a 12-V supply rail. The programmable OV-UV thresholds help in narrowing down the design specification for the downstream converters and hence saves cost.

3.2.2.7 Testing With Single-Point Failure on eFuse

Figure 19 shows the current limit test results of the eFuse with the current limit resistor, R_{LIMIT} open. The eFuse output voltage and current reduces to zero when the R_{LIMIT} resistor is open. Figure 20 shows the current limit test results of the eFuse with the R_{LIMIT} resistor shorted. The eFuse output voltage and current reduces to zero when the R_{LIMIT} resistor is short. The system with eFuse is well protected with single-point failures and still help to qualify as a low-power circuit.

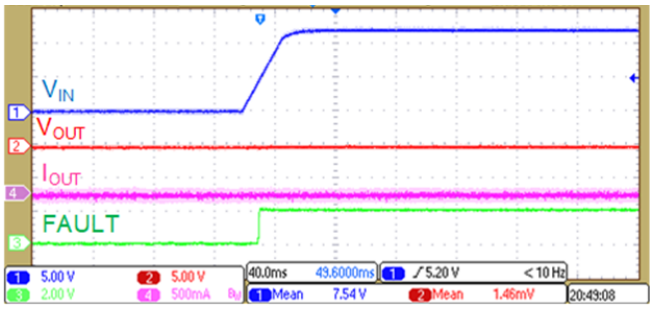

Figure 19. Testing of eFuse Circuit With Resistor R_{LIMIT} Open

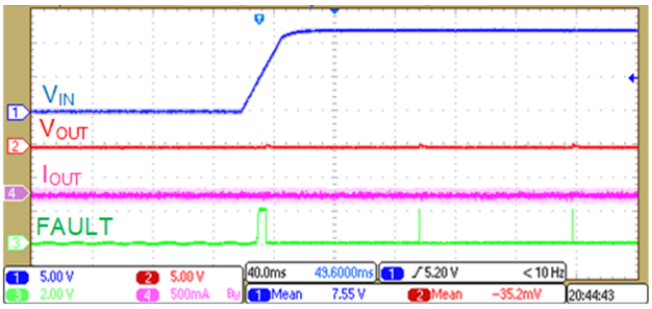

Figure 20. Testing of eFuse Circuit With Resistor R_{LIMIT} Short

3.2.2.8 Load Test of the DRV8847S Device Driving the Bipolar Stepper Motor

Figure 21 shows the load test results of the DRV8847S device driving a bipolar stepper motor in full stepping mode using a 2-pin interface. In full-stepping mode, the full-bridge operates in either of two modes (forward or reverse mode) with a phase shift of 90° between the two windings. In full-stepping mode, using the 2-pin interface, the PWM input is only connected to the IN1 and IN2 pins, and the IN3 and IN4 pins are connected to ground. Figure 21 and Figure 22 show IN1, IN2, OUT1, and OUT 2 and both the winding currents from OUT1 to OUT2 and OUT3 to OUT4. The waveforms are captured with mixed decay current regulation mode. The control signals from the MCU, IN1, and IN2 are 90° phase shifted with 100% duty cycle.

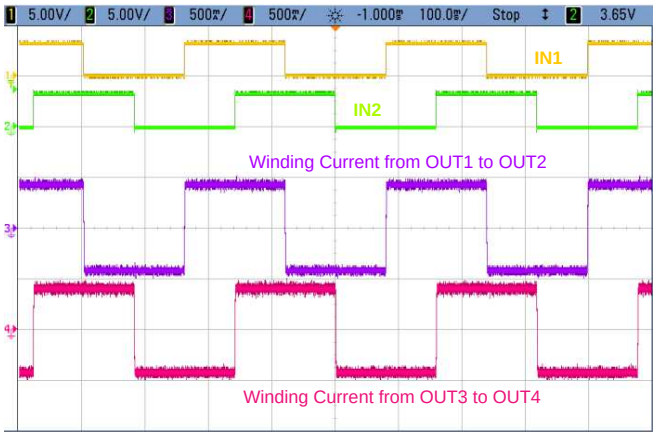

Figure 21. DRV8847 Driving a Bipolar Stepper in Full Stepping, 2-Input Mode

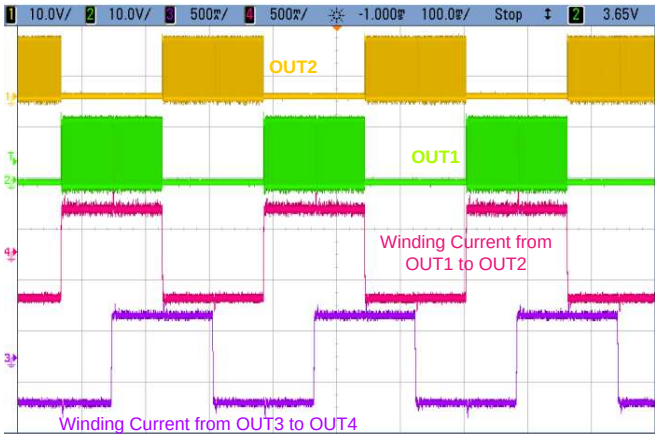

Figure 22. DRV8847 in Full Stepping Mode, Showing Current Limit Switching on OUT1 and OUT2

With the current-sense resistor, R_{ISEN12}, R_{ISEN34} = 0.3 Ω, V_{TRIP} = 0.15 V typical (0.135 V min to 0.165 maximum). The expected current limit = 0.15 V / 0.3 Ω = 0.5 A (0.45 A min to 0.55 A maximum).

Figure 23 shows the voltage across the shunt resistor during current-limit action in mixed decay mode. The current through the sense resistor is negative during the fast decay which is 25% period of total off time

Figure 23. DRV8847 Current Limit, Showing the Voltage Across Shunt

3.2.2.9 *Fast Winding Current Build up and Reversal With DRV8847*

Figure 24 shows the forward current build up from negative peak to positive peak and Figure 25 shows the reverse current build up from positive peak to negative peak when DRV8847 drives the windings of bipolar stepper motor.

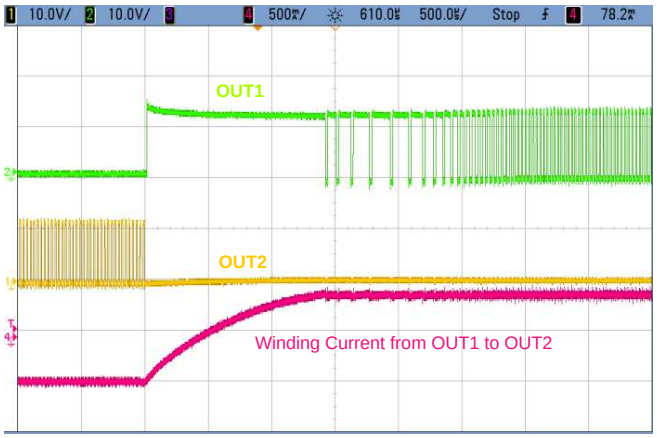

Figure 24. Current Build up From Negative Peak to Positive Peak With DRV8847

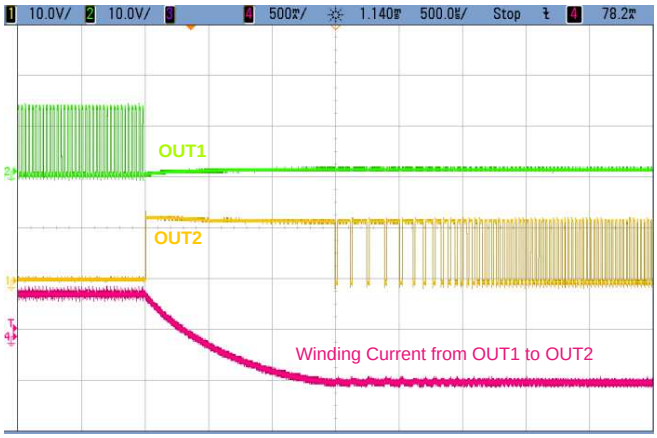

Figure 25. Current Reversal From Positive Peak to Negative Peak With DRV8847

With 100% input duty, the DRV8847 device enables fast current ramp up and decay, reducing the torque ripple in the motor and audible noise from the motor. With 100% PWM duty, the current ramps up or falls faster with full-applied voltage and once the current limit is hit, the peak current in the motor is limited by PWM switching with 20 µs off time.

3.2.2.10 Current Regulation Modes in DRV8847, Enabling the Best Current Regulation

During PWM current trip operation, the H-bridge is enabled to drive current through the motor winding until the trip threshold of the PWM current is reached. After the trip current threshold is reached, the drive current is interrupted, but because of the inductive nature of the motor, current must continue to flow for some period of time. This continuous flow of current is called recirculation current. To support this recirculation current, the DRV8847 H-bridge operates in mixed decay mode.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the anti-parallel diodes of the opposite FETs are conducting on, to let the current decay faster as shown in Figure 26 (see case 2). In slow decay mode, the winding current is re-circulated by enabling both of the low-side FETs in the bridge (see case 3 in Figure 26). Mixed decay starts with fast decay, then goes to slow decay. In the DRV8847 device, the mixed decay ratio is 25% fast decay and 75% slow decay.

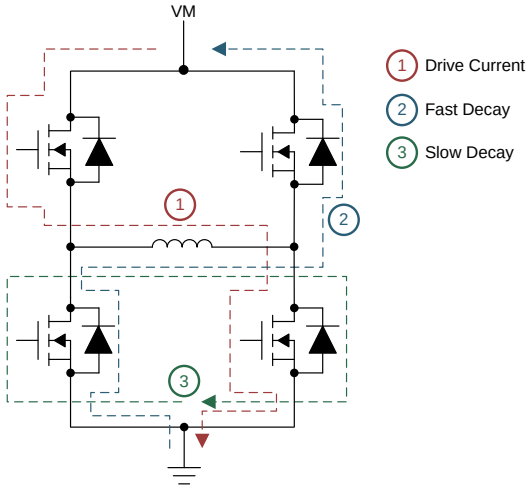

Figure 26. DRV8847 Current Regulation Flow Paths

Figure 27 shows the current regulation by the DRV8847 device with the stepper motor in mixed-decay mode. When the current reaches the threshold value, the DRV8847 device enters the fixed time off period of 20 µs. With mixed decay mode, the device enters to fast decay of 5 µs (25% of PWM off time) and then slow decay for 15 µs (75 % of PWM off time).

Figure 28 shows the current regulation in slow-decay mode where the entire 20 µs PWM off time is controlled in slow decay.

Figure 27. Current Regulation With Mixed Decay Mode

Figure 28. Current Regulation With Slow Decay Mode

Figure 27 and Figure 28 show that the switching frequency is different in both the cases. With 20-µs fixed off time, the switching frequency is lower in mixed decay compared to slow decay. Choose the decay mode based on the required frequency, motor inductance, and current ripple

3.2.2.11 Slew Rate Control and EMI Optimization With DRV8847

The DRV8847 device comes with switching slew rate options of 150 ns and 300 ns. Figure 29and Figure 30 show the OUT1 and OUT2 voltage and the winding current from OUT1 to OUT2, for the slew rates 150 ns and 300 ns, respectively.

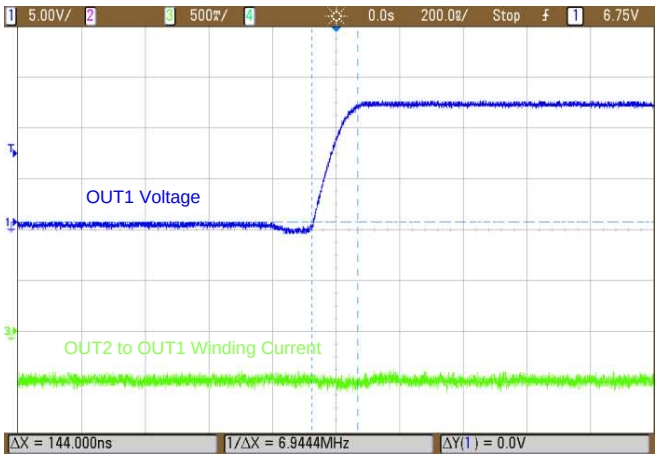

Figure 29. OUTx Voltage of DRV8847 With 150-ns Slew Rate Setting

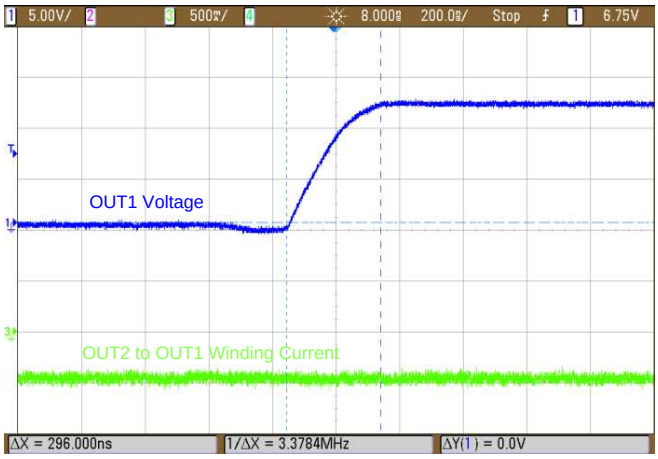

Figure 30. OUTx Voltage of DRV8847 With 300-ns Slew Rate Setting

The slew rate options help the designer to optimize EMI and switching losses according to the application requirement.

3.2.2.12 Brushed DC Motor Drive With DRV8847 OUTx in Parallel Mode

Figure 31 shows the DRV8847 current and voltage waveforms when driving a brushed DC motor with OUT1 and OUT2 connected in parallel and OUT3 and OUT4 connected in parallel. The test results shows RMS current of 1.19 A at 20-kHz PWM and 90% duty cycle.

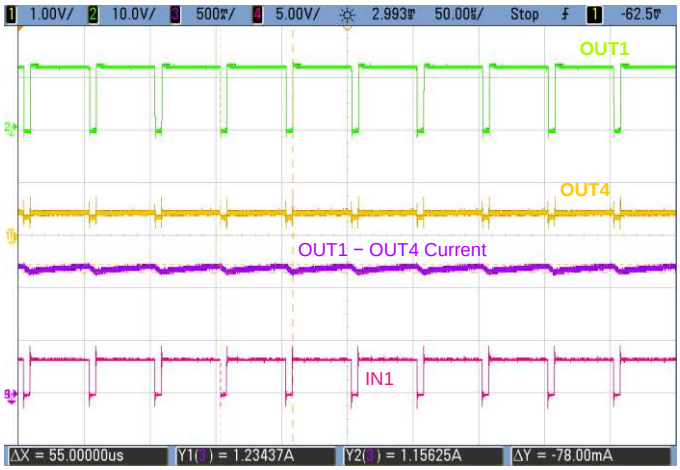

Figure 31. Test Results of DRV8847 Driving a Brushed DC Motor With Two Half-Bridges Paralleled

3.2.2.13 Efficiency of DRV8847SPW in Bipolar Stepper Driver Configuration

Table 4 shows the efficiency test results of the DRV8847S device configured in slow-decay full-stepping mode when driving a bipolar stepper motor.

Table 4. Efficiency Test Data of DRV8847 Stepper Drive

DC INPUT VOLTAGE (V)	DC INPUT CURRENT (A)	DC INPUT POWER OF DRV8847 (W)	OUT1-OUT2 WINDING CURRENT (A) (RMS)	OUT3-OUT4 WINDING CURRENT (A) (RMS)	OUTPUT POWER FROM DRV8847 (W)	EFFICIENCY (%)
11.95	0.109	1.30	0.051	0.051	1.21	92.70
11.90	0.209	2.49	0.100	0.102	2.38	95.46
12.00	0.415	4.98	0.202	0.206	4.79	96.13
12.01	0.611	7.34	0.300	0.305	7.01	95.60
11.96	0.721	8.62	0.357	0.358	8.18	94.87
11.98	0.842	10.09	0.417	0.419	9.51	94.30

Figure 32 shows the efficiency plot of the DRV8847 driver against motor winding current. The efficiency plot shows that the peak efficiency of the driver is more than 96% at 0.2-A RMS winding current. At 0.4 A, the efficiency of the driver is as high as 95% because of the low $R_{DS(on)}$ of the device.

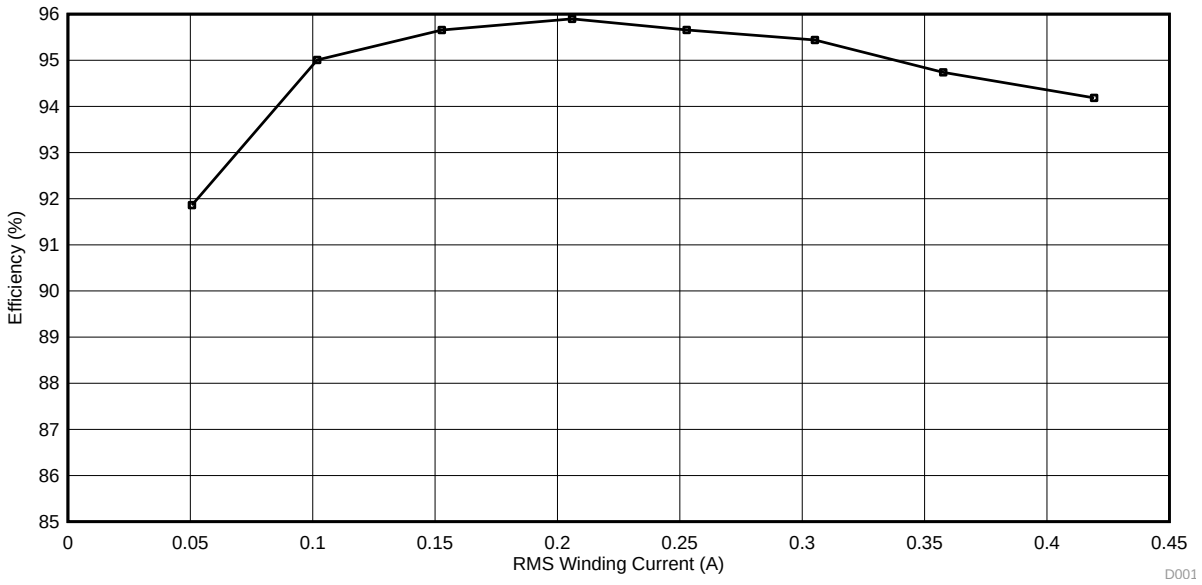

Figure 32. Efficiency Curve of DRV8847 Driving a Bipolar Stepper Motor

Figure 33 shows the thermal image of the board when the DRV8847S device is delivering 0.43-A RMS winding current at 25°C ambient temperature. The DRV8847S device was programmed to slow decay mode during the evaluation. The high efficiency of the DRV8847S device lowers the temperature rise in the device.

The temperature rise at 25°C ambient = 64.7 – 25 = 39.7°C.

Estimated absolute temperature of the DRV8847 device at 85°C with 0.43-A RMS current = 85 + 39.7 = 124.7°C.

The $R_{DS(on)}$ increase at 124.7°C may further increases the losses and temperature of the DRV8847 device and the device is rated to a junction temperature of 150°C.

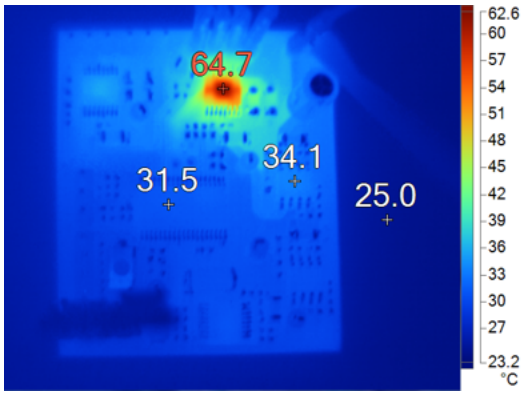

Figure 33. Thermal Image of the Board When DRV8847S is Delivering 0.43-A RMS on Each Full Bridge

3.2.2.14 Open Load Detect by DRV8847

The open load detection (OLD) feature of the DRV8847 device helps to diagnose any kind of loose wire connection or wire braking in the equipment during long time usage. The OLD diagnostic test runs at device power up or when the DRV8847 device comes out from sleep mode (rising edge on the nSLEEP pin). The OLD diagnostic test can run any time in the I^2C-variant device (DRV8847S) using the OLDOD (OLD On Demand) bit. The OLD implementation is done on the full-bridge and the half bridge. In the DRV8847 device, during an open-load condition, the half bridges, full bridge, or both bridges (depending on the MODE pin) are always operating and the nFAULT pin is pulled low. Reset the power to release the nFAULT pin by doing the OLD sequence again. In the DRV8847S device, program the full-bridge or half bridge to be in the operating mode or the Hi-Z state, whenever an open-load condition is detected by using the OLDBO (OLD Bridge Operation) bit. Moreover, the nFAULT signaling on the OLD bit can be disabled using the OLDFD (OLD Fault Disable) bit.

Figure 34 and Figure 35 show the open load test result with the open load created on OUT1 and OUT2. In Figure 34 the DRV8847S device is configured with the full bridge or half bridge to be in the operating mode even after open load detect. During power on, where VIN increases to 12 V from 0 V, OLD is detected and the FAULT pin goes down as open load is detected on OUT1. Figure 34 also shows a second OLD detection, due to the OLDOD command issued by the MCU. With the bridge in operating mode, the OUT1 operates as per the IN1 signal coming from the MCU. However, the FAULT signal is pulled low, indicating an open-load condition. Figure 35 shows the test result, when the DRV8847S device is configured with the bridges in the Hi-Z state after OLD. Even with the input signals at IN1, the OUT1 pin stays at Hi-Z.

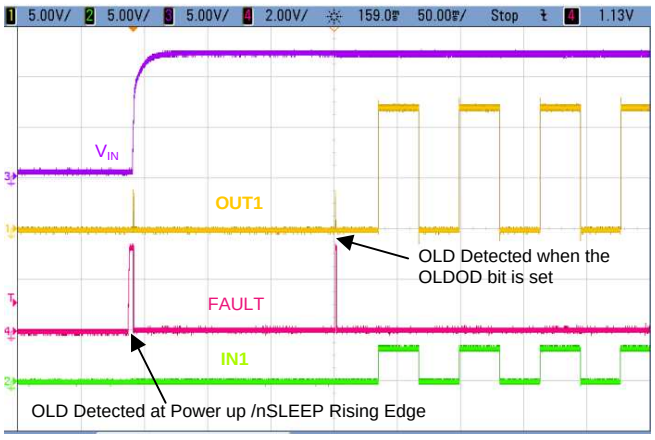

Figure 34. Open Load Detect by DRV8847S in Bridge Operating Mode After OLD

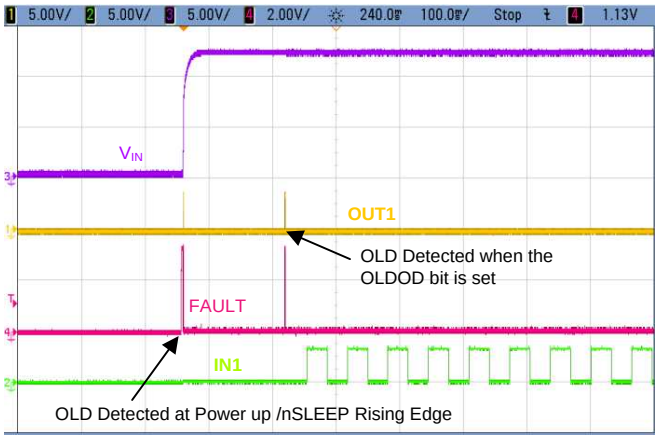

Figure 35. Open Load Detect by DRV8847S in Bridge Hi-Z Mode After OLD

3.2.2.15 DRV8847 – Short-Circuit Test

Figure 36 and Figure 37 show the reliable overcurrent protection feature by the DRV8847 device, where the OUTx pins are shorted together during the test. Figure 36 shows multiple overcurrent pulses from the OUTx pins during short circuit and the retry time of 1 ms between multiple pulses. Figure 37 shows the zoomed-in image of one short-circuit current pulse.

The integrated OCP circuit on each FET monitors the FET current and if the overcurrent detection continues for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge (or half-bridge in the independent interface) are disabled and the nFAULT pin is driven low. The DRV8847 device stays disabled until the retry time t_{RETRY} occurs, whereas the DRV8847S device has a programmable option for auto-retry or the latch mode. The 3-µs deglitch time removes false trips under noise glitches. The retry mode with 1-ms retry time protects against hot spots under short circuit.

Figure 36. Short-Circuit Protection by DRV8847 When OUT1 and OUT2 are Shorted

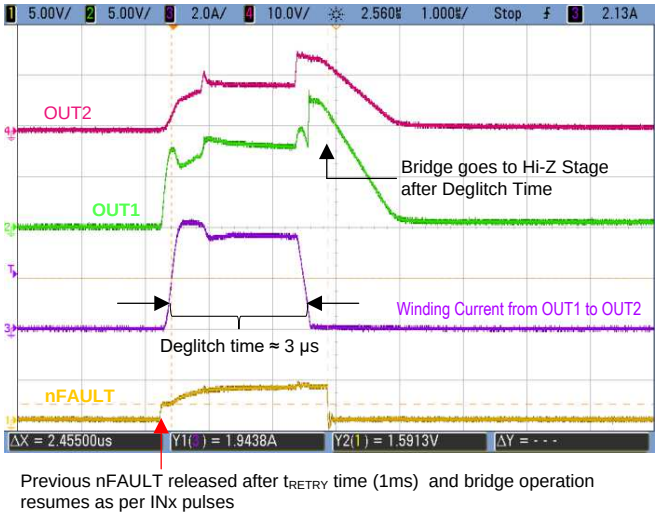

Figure 37. Short-Circuit Deglitch Time for Noise Tolerant Short Circuit Detection

3.2.2.16 Robust Protection With Single Point Failures in DRV8847

Figure 38 and Figure 39 show different single point fault conditions with the DRV8847 device. Figure 38 shows the test result when the OUT1 pin is shorted to VM while the motor is running. Initially, there was no fault and the motor is running with the proper voltage pulses at OUT1 and OUT2. When the fault is created, the OUT1 to OUT2 current is limited to set threshold and the DRV8847 device is well protected. Figure 39 shows the test result when the OUT1 pin is shorted to GND during motor running. In both the cases the system is well protected.

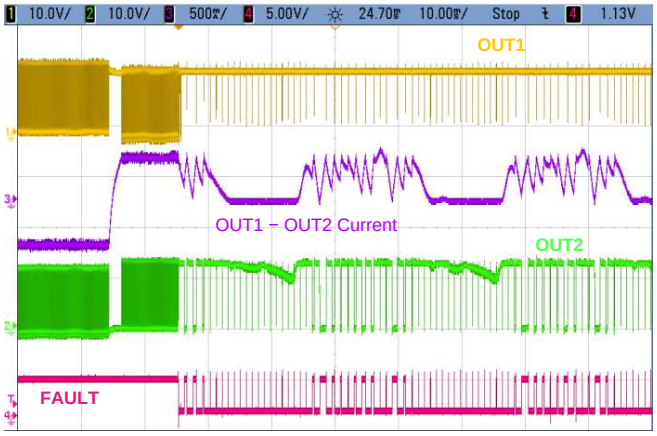

Figure 38. DRV8847 – OUT1 to VM Short During Motor Running

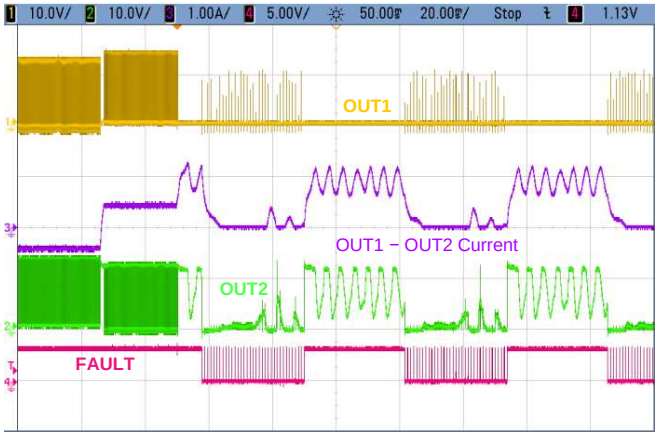

Figure 39. DRV8847 – OUT1 to GND Short During Motor Running

3.2.2.17 Surge Testing

Figure 40 shows the surge voltage test setup. The surge generator generates the required surge voltage. The surge voltage is coupled to the 12-V DC supply in a CNV504N coupling and decoupling network, where a 42-Ω impedance is also inserted on the surge voltage path with 0.5-µF coupling capacitor. The combined voltage is then applied to the reference design board 12-V input line.

Figure 41 shows the surge test results with 750-V surge and Figure 44 shows the test results with 1-kV surge voltage. In both the cases, notice that the TVS1400 device clamps the surge voltage and the voltage at the board after the TVS1400 device is clamped to 17.2 V, as per the TVS1400 specification.

The TVS1400 device ensures that any propagated surge through the front end into the 12-V line is clamped properly and the downstream circuits are well protected.

The surge testing on the reference design is done up to 1 kV. However, the TVS1400 device is specified to offer a solution to the common industrial signal line EMC requirement to survive up to ±2 kV IEC 61000-4-5 open circuit voltage coupled through a 42-Ω impedance.

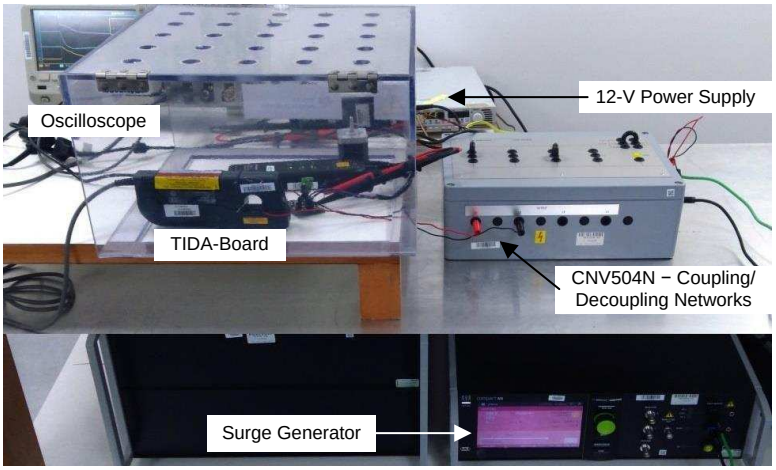

Figure 40. Surge Test Setup

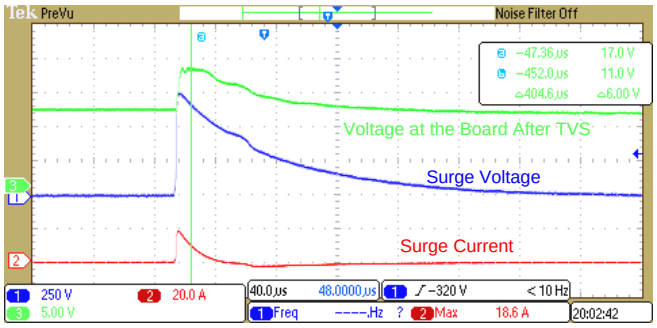

Figure 41. Surge Test Results With 750-V Surge

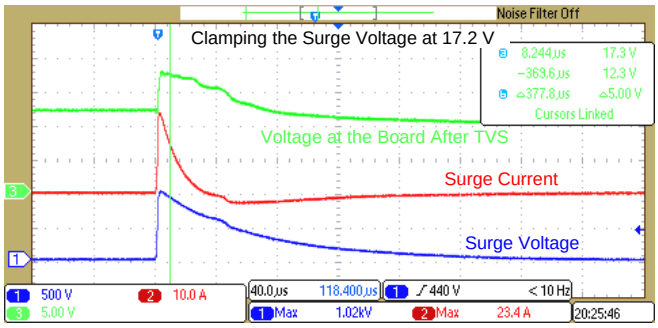

Figure 42. Surge Test Results With 1-kV Surge

3.2.2.18 ESD Testing

The reference design is tested for ESD events at multiple points. Figure 43 shows the test set up with an ESD generator gun, the reference design board, and the grounding connections.

Figure 44 shows the test points. A contact discharge is applied to:

- All the pins of the connector J2, where the OUTx pins of the DRV8847 device are connected.
- Temperature sensor interface, which is the middle pin of connector J7.
- 12-V supply input, which is the '+12V' terminal of J1.

During testing, "GND" of the TIDA-010004 board is connected to the "Earth" pin of set up. The test platform is connected to earth via two 470-kΩ resistors. The testing is done as per IEC 61000-4-2, test level 4. Ten discharges having a positive polarity and ten discharges having a negative polarity are applied to the points under test, via contact discharge when TIDA-010004 is in off state. Testing is done with an ESD contact discharge voltage of ±8 kV.

The TIDA-010004 operates as expected without any performance degradation after the ESD testing, passing with class A, as recommended by IEC 61000-4-2.

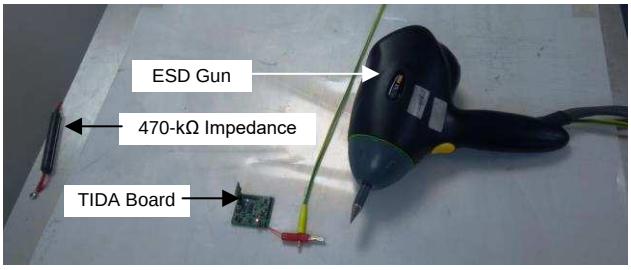

Figure 43. ESD Test Setup

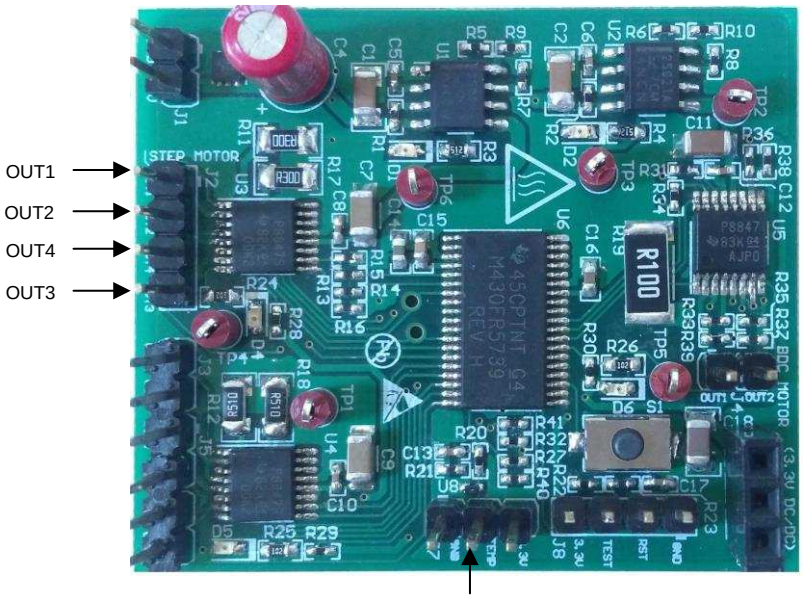

Figure 44. ESD Test Points on the Board

3.2.2.19 Testing With Increased Ambient Temperature

The reference design board is tested in a thermal chamber with ambient temperature from –10°C to 70°C. The relative humidity inside the chamber during testing was up to +85%. Figure 45 shows the test setup, where the TIDA-010004 board and the bipolar stepper motor (consuming 0.45-A RMS per phase) are kept inside the thermal chamber. The DRV8847PWP device driving the brushed DC motor is loaded externally using a resistive-inductive (RL) load consuming 1.1 A.

Figure 45. Setup for Testing the Design at Multiple Ambient Temperatures

The testing is done for duration more than sufficient to achieve the steady state conditions at different ambient conditions.

During testing, no failures or degradation in performance are observed. The current limit for the bipolar stepper was accurate as per the set limit across the temperature ranges.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010004.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010004.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010004.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010004.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010004.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010004.

5 Software Files

To download the software files, see the design files at TIDA-010004.

6 Related Documentation

1. Texas Instruments,*Small Motors in Large Appliances*

6.1 Trademarks

7 Terminology

ESD - Electrostatic discharge

BDC - Brushed direct current

PWM - Pulse width modulation

MCU - Microcontroller unit

OLD - Open load detect

UVLO - Undervoltage lockout

OVLO - Overvoltage lockout

8 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics and analog and mixed signal designs. He has system level product design experience in permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2018) to A Revision **Page**

- Changed title of document from *12-V, Highly-Protected, Single Driver-Based Stepper, Brushed DC and Actuator Drive Reference Design* to *12-V, 15-W Power Limit, Single Driver-Based Stepper, Brushed DC and Actuator Drive Reference Design* 1
- Changed TPS259631 to TPS2596 is design resources 1
- Changed range of voltage operation from *4.5 V to 16 V* to *2.7 V to 16 V* 1
- Changed error margin of input current limit from less than 2% to ±8% 1
- Changed TPS25921A to TPS259631 throughout document 2
- Changed *TIDA-010004 Block Diagram* image 4
- Changed TPS25921A in *Highlighted Products* to TPS2596 5
- Added information regarding TPS2596 5
- Changed error margin and temperature for current limit 5
- Changed threshold accuracy for UV and OV 5
- Changed design values in *Design Parameters for eFuse* table 7
- Changed *Schematic of eFuse Circuit* image 7
- Changed equations 1, 2, 3, and 4 8
- Changed 1.2 A to 1.11 A 8
- Changed 113.51 kΩ to 826.48 Ω 8
- Changed 113 kΩ to 826.48 Ω 8
- Changed 1.1945 A to 1.1119 A 8
- Changed OVP to OVLO 8
- Changed 1.40 V to 1.2 V 8
- Changed V_{ENR} to V_{OVLO} 8
- Changed 1.40 V to 1.2 V 8
- Changed 61.2 kΩ to 49.9 kΩ 8
- Changed R3 to R5 8
- Changed 60.4 kΩ to 49.9 kΩ 8
- Changed 475 kΩ to 464 kΩ 8
- Added note 8
- Added threshold voltage 8
- Changed 0.96 x V_{UV} to 6.2 V 8
- Changed 100 mA to 10 mA 8
- Changed 1.1945 A to 1.11 A 17
- Changed 12-V supply to 13.5-V supply 17
- Changed 1.18 A to 1.12 A 17
- Changed 9.44 V to 9 V 17
- Changed information in *Testing for Power Limit With eFuse* 17
- Changed *Accurate Current and Power Limit by eFuse TPS259631 and Device Shutdown Due to Overtemperature* image 17
- Deleted *upon insertion of a card into a live backplane or other "hot" power source* 17
- Changed SS to dVdt 17
- Changed 1.5 ms to 0.162 ms 17
- Changed 1.66 ms to 0.4 ms 17
- Changed *Controlled Start-up Slew Rate With eFuse* image 18
- Deleted information in *Thermal Evaluation of eFuse at the Rated Load* 18
- Added input values for rated load 18
- Changed 11.931 V to 12.1 V 18
- Changed 1.178 A to 1.12 A 18
- Changed 11.931 x 1.178 = 14.05 W to 12.1 x 1.12 = 13.55 W 18
- Changed 75°C to 25°C 18

- Changed 105 mΩ to 85 mΩ 18
- Deleted *Thermal Image of the Board When eFuse Power is 14 W* 18
- Changed *eFuse Input and Output Voltage and Current* image 18
- Changed information in *Testing With Short-Circuit at the Output of eFuse* 19
- Changed *Test Results With Short Circuit on the eFuse Output* image 19
- Added undervoltage as a system condition protected by circuits incorporated by the TPS259632 device 20
- Changed 1.4 V to 1.2 V 20
- Deleted *TPS25921A Turns ON When the Input Voltage is More Than UVLO Threshold* image 20
- Changed *Overvoltage Protection by eFuse at 13.5 V* image 20
- Changed information in *Testing With Single-Point Failure on eFuse* 21
- Changed *Testing of eFuse Circuit With Resistor R_{LIMIT} Open* image 21
- Changed *Testing of eFuse Circuit With Resistor R_{LIMIT} Short* image 21

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