TI Designs: TIDA-010023

Cost Optimized, < 1% Accurate Current Sensing and Protection for 3-Phase Inverter Reference Design

Description

This reference design demonstrates a cost optimized three-phase inverter leg (low-side shunt) current sensing solution with high accuracy and faster response for sensorless 2-shunt or 3-shunt field oriented control (FOC). For minimized audible noise drives require fast and accurate current sensing with very good noise rejection. This reference design demonstrates inverter leg current sensing with full swing response settling time close to 1-µs and accuracy error less than 1%. The design also shows very good noise rejection even with high power IGBTs switching nearby. The design implements overcurrent protection fully in hardware with less than 1.5-µs total response time. This reference design is applicable to compressor motors. The inverter power stage can work up to 2 kW.

Resources

TIDA-010023	Design Folder
TLV9064	Product Folder
UCC27712	Product Folder
TIDA-00947	Design Folder
TLV1701	Product Folder
SN74AHC367	Product Folder
TLV9001	Product Folder
TMS320F28027F	Product Folder
TPD1E10B06	Product Folder

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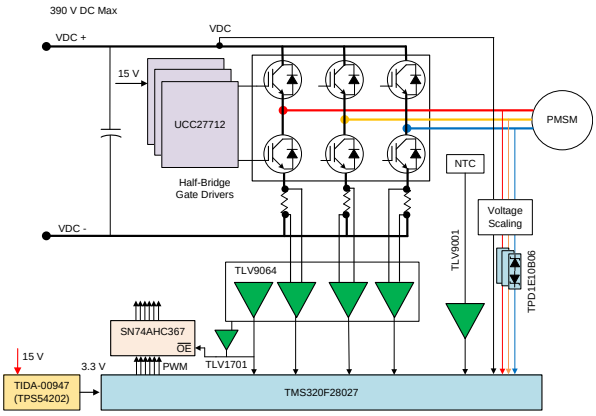
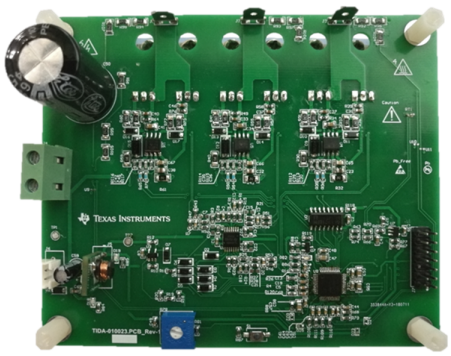
Features

- Low cost and accurate current sensing for sensorless FOC with dual and triple shunt topologies to minimize torque ripple and audible noise in motor drives
- Current sensing with < 1.25 µs settling time and < 1% calibrated accuracy enabling accurate current sensing
- Overcurrent protection fully implemented in hardware with fast response time < 1.5 µs
- Positive and negative overcurrent protection in all the three inverter legs by using only two comparators
- Protection features: motor overcurrent and overtemperature
- Three phase inverter power stage designed for 2-kW output power from and input voltage 270 V to 390 V DC

Applications

- Air Conditioners
- Washing Machines
- Refrigerators
- Appliances Compressors
- Mains Powered Tools





1 System Description

Field-oriented control (FOC) is widely used for high-performance motor control to enable smooth rotation over the whole speed range, fast accelerations and decelerations, and efficient operation during dynamic load changes. Basic idea of FOC algorithm is to decompose the 3-phase winding current into magnetic field-generating part and torque-generating part via Clark and Park transformation.

Fast and precise motor winding current sensing is required for efficient and accurate implementation of FOC and to get the best performance from the motor. The most simplest and cost effective way of measuring the winding current is by sensing the inverter leg current using a sense resistor in the inverter legs of all the three phases. This method of current sensing is much cheaper compared to hall sensor based sensing.

The delay or slow response in current sensing can lead to incorrect current estimates and hence distorted current waveform in the motor. The motor drive applications in major appliances such as a compressor motor control in air conditioners and refrigerators require accurate torque control to have the best dynamic performance and low acoustic. An inaccurate current sensing leads to distorted current waveform in the motor winding and thus produces torque ripple, which, in turn, results in inefficient and noisy performance.

Figure 1 shows three-shunt inverter leg current sensing. Three-shunt current sensing has some advantages. Contrary to the three-shunt technique, the use of a single- or two-shunt setup proves difficult to achieve circuit over modulation. Additionally, the use of a low-bandwidth op amp is sufficient. The three-shunt technique can bounce sampling between current signals, selecting two out of three phases each period, which allows long time periods for the current signals to settle, which means the current sensing window is no more limited by the minimum duty of PWM. If large current measurement windows are possible, then much slower and cheaper op amps can be used. For example, Figure 2 shows three PWM switching signals and the corresponding shunt resistor to be sampled. As Figure 2 shows, the current signal has plenty of time to stabilize.

Figure 1. Three-Shunt Current Measurement Circuit With Inverter

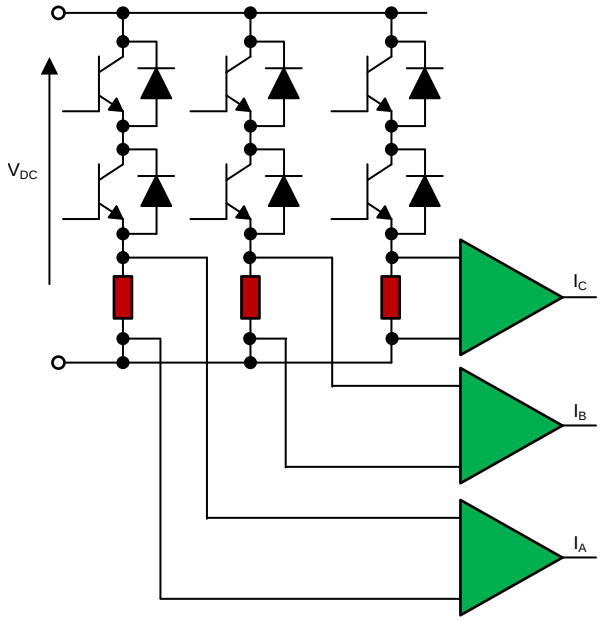
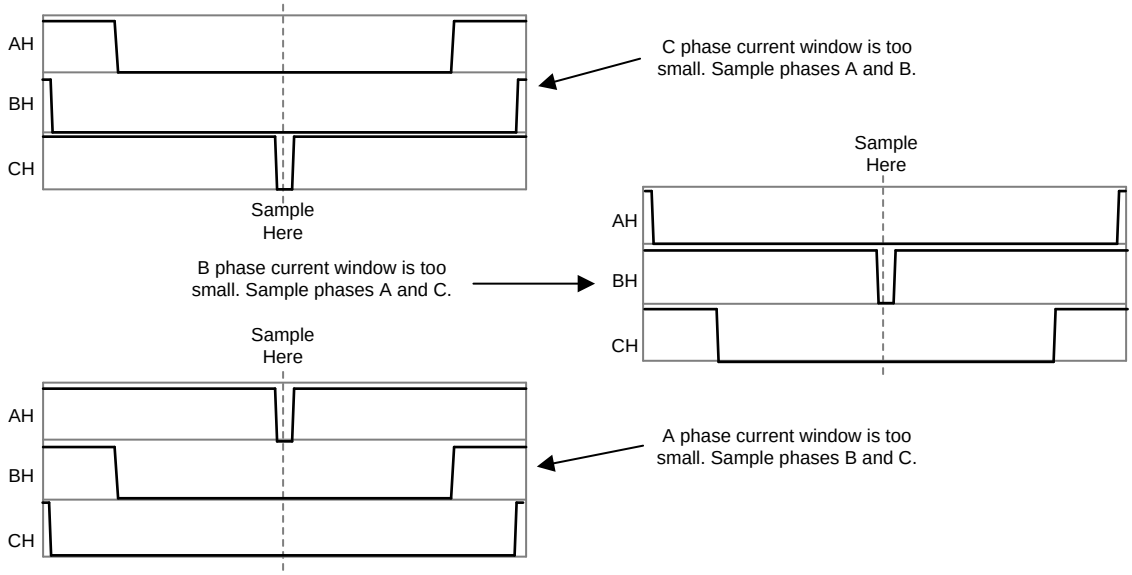
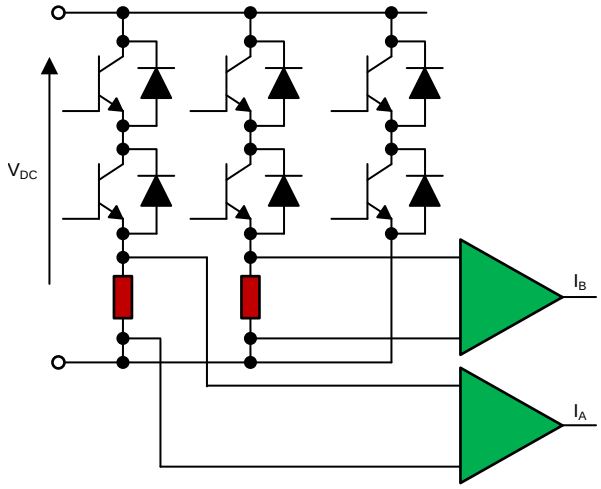


Figure 2. Using Three-Shunt Current Sampling Technique



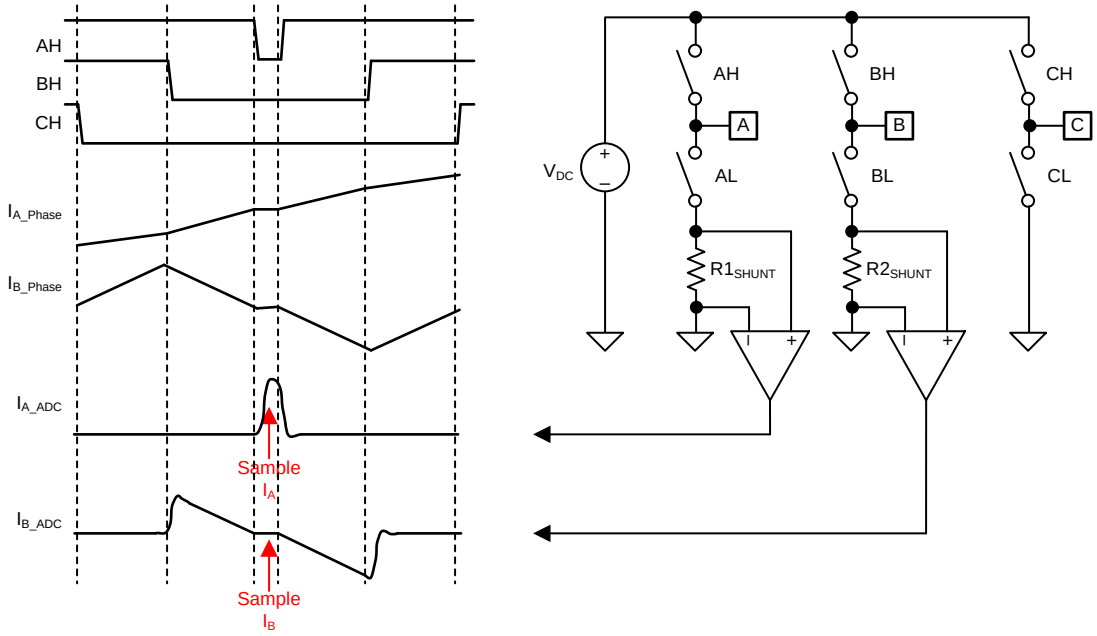
The two-shunt current measurement technique uses the principle of Kirchhoff's current law (KCL), which is that the sum of the currents into a single node equals zero. By measuring only two-phase currents, the third is calculated with KCL. Figure 3 shows a circuit for the two-shunt current measurement technique.

Figure 3. Dual-Shunt Current Measurement Circuit With Inverter



The two- and three-shunt measurement circuit has an advantage over the single-shunt circuit in that it can detect circulating currents. Figure 4 shows an example of a switching waveform and where the analog-to-digital converter (ADC) samples the current. The PWM duty cycle for IA is almost 100% in this example, which causes the IA current to rise. The PWM for IB is about 50% duty cycle and its current stays at approximately 0 A for this period. Phase current can only be measured when the lower switch of that particular phase is conducting. In the example, IA is measurable for a very short time while IB has a long time to measure. The inherent problem of using the two-shunt technique is when the measured phase is operating at PWMs near 100%. For example, when sampling IA, the measured current signal has not yet stabilized, which gives an incorrect representation of the current signal.

Figure 4. Sampling Current When Using Two-Shunt Measurement Technique



As the duty cycle increases, the time to measure voltage across the shunt resistor for the phase decreases and the current measurement must be quicker. As the duty cycle increases even more, the slew rate must be increased to properly capture the signal. Although the two-shunt current measurement technique lessens the speed requirement of the op amp as compared to the single-shunt measurement, there is a duty cycle where the slew rate has to be very large, but still less than the requirement for a single shunt.

1.1 Key System Specifications

Table 1 shows key parameters considered in the design of TIDA-010023.

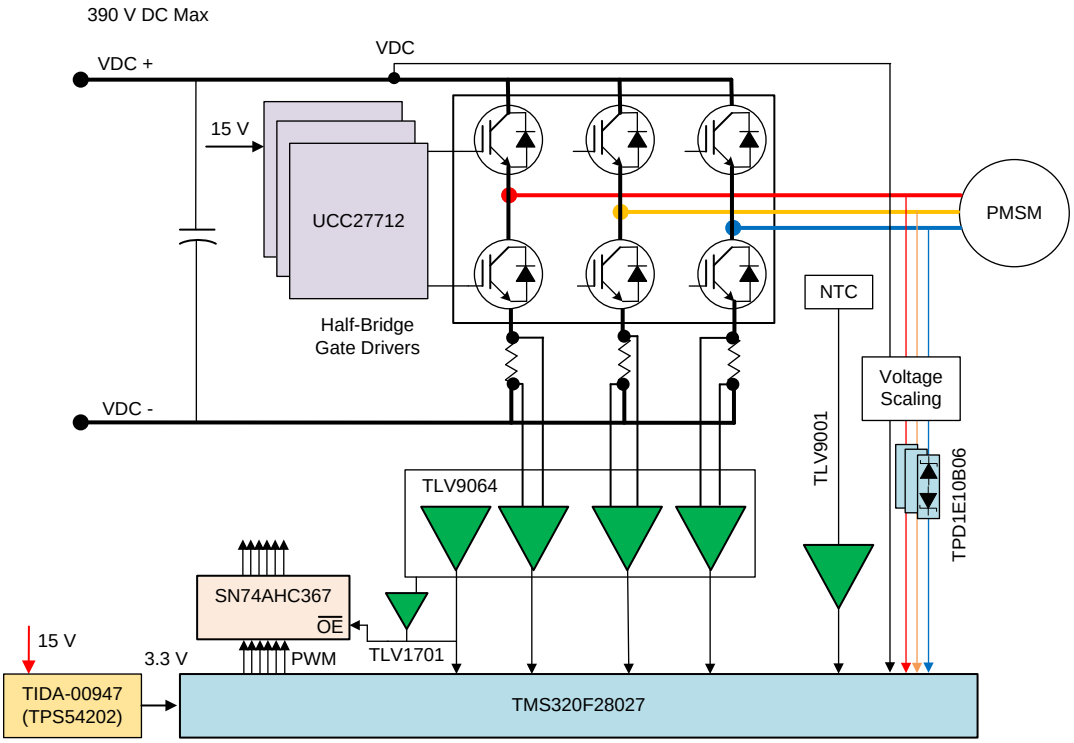
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	270-V to 390-V DC	The DC voltage derived from the 195-V to 265-V AC input with or without power factor correction
Maximum output power	2 kW	The IGBTs are selected to support a maximum 2 kW Power
RMS winding current	5.58 A	At 325-V DC delivering 2 kW at a power factor of 0.9 with space vector PWM
Peak winding current	7.89 A	At 325-V DC delivering 2 kW at a power factor of 0.9 with space vector PWM
Control method	Sensorless FOC	Designed to support InstaSPIN-FOC
Inverter switching frequency	15 kHz (adjustable from 5 kHz to 20 kHz)	Selection based on the motor inductance and desired current ripple
Feedback signals	DC bus voltage, three winding voltages, inverter leg currents	The feedback signals are required for sensorless control
Current shunt resistors used	5-mΩ shunt for inverter leg current sensing using TLV9064	See Section 2.2.2 for design aspects
Op amps gain	25	----
Inverter leg current sensing range	±13.2 A	Scaled to 0 V to 3.3 V, level-shifted with 1.65-V bias
Inverter leg current sensing accuracy (calibrated)	<1% (Calibrated)	See Section 3.2.1.3 for accuracy measurement
Protections	Positive and negative winding overcurrent, overtemperature	See Section 2.2.3 for the overcurrent protection measurement
Cooling	With external heat sink	----
Operating ambient	–20°C to 55°C	----
Board specification	120 mm × 100-mm, two-layer, 1-oz copper	----
15-V supply current for gate driver	50 mA (max)	See Section 2.2.4 for the power requirement in gate driver
3.3-V supply current	1 A (max)	For details, see *3.3-V, 1-A, Low EMI, 92% Efficiency DC/DC Module in Dual Layer TO-220 Form Factor Reference Design*

2 System Overview

2.1 Block Diagram

Figure 5. TIDA-010023 Block Diagram



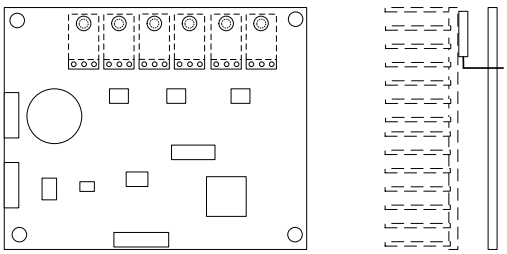
2.2 Design Considerations

2.2.1 Three-Phase Inverter

The three-phase inverter is designed to operate from the DC bus voltage up to 390 V. This design uses six IGBTs.

The designer has to adjust the position of the IGBT in the layout to fit the external heatsink. The power stage is designed to deliver up to 2-kW output power. The power stage is supplied with 390-V DC maximum and by considering the safety factor, switching spikes, and voltage build-up during regeneration, the IGBT is selected with the voltage rating equal to 600 V. Figure 6 shows the structure of the board with heatsink installed.

Figure 6. Structure of TIDA-010023 With External Heatsink



The current rating of the IGBT depends on the peak winding current. The three-phase inverter bridge is switched using SVPWM so that sinusoidal current is injected into the motor windings. The peak winding current can be calculated from the system specifications.

Inverter rated output power (POUT) = 2 kW

DC bus voltage = 325 V (rated), 270 V (minimum) – 390 V (maximum)

Power factor = 0.9 (assumed, for a low-inductance PMSM)

The nominal current in the IGBT can be calculated at the rated DC bus voltage. With space vector PWM, the maximum RMS line-to-line voltage can be 0.707 times the available DC bus voltage. For more details, see the *Space-Vector PWM With TMS320C24x/F24x Using Hardware and Software Determined Switching Patterns* application report.

$V_{LL\_RMS\ (nom)}$ = 0.707 × 325 = 229.8 V

The rated winding current can be calculated using Equation 1:

$$I_{L(nom)} = \frac{P_{OUT}}{\sqrt{3} \times V_{LL(nom)} \times \cos\varphi} = \frac{2000}{\sqrt{3} \times 229.8 \times 0.9} = 5.58 \text{ A} \quad (1)$$

The peak line current is calculated using Equation 2:

$$I_{L\_PEAK} = \sqrt{2} \times 5.58 = 7.89 \text{ A} \quad (2)$$

The maximum current in the IGBT must be calculated at the minimum DC bus voltage. (see Equation 3).

$$V_{LL\_RMS(nom)} = 0.707 \times 270 = 190.9 \text{ V}$$

$$I_L = \frac{P_{OUT}}{\sqrt{3} \times V_L \times \cos\varphi} = \frac{2000}{\sqrt{3} \times 190.9 \times 0.9} = 6.72 \text{ A}$$

$$I_{L\_PEAK} = \sqrt{2} \times 6.72 = 9.5 \text{ A} \quad (3)$$

Considering an overloading and design margin of 200%, the maximum peak winding current to design should be ≈ 19 A. For this reference design, the IGBT IXDP20N60B is used. This IGBT has a continuous collector-current-carrying capacity of 32 A at Tc = 25°C, 20 A at Tc = 90°C and a peak current capacity of 60 A.

Figure 7 shows the three-phase inverter circuit. The circuit has three shunt resistors to measure all three inverter leg currents. R44, R48, and R52 are the inverter leg shunt resistors, C24, C25, and C26 are the decoupling capacitors connected across each inverter leg.

The inverter receives the DC power supply from the connector J4. C50 is the DC bus capacitor, as Figure 8 shows. R80, R83 are the bleeder resistors for the capacitor.

NOTE: C50 is designed as the local storage capacitor. The value is not designed to meet the full capacitor requirement for a 2-kW system. The capacitors on the AC-DC power supply which precede the inverter should be high enough, based on the design requirement.

Figure 7. Three-Phase Inverter With Shunt Resistors

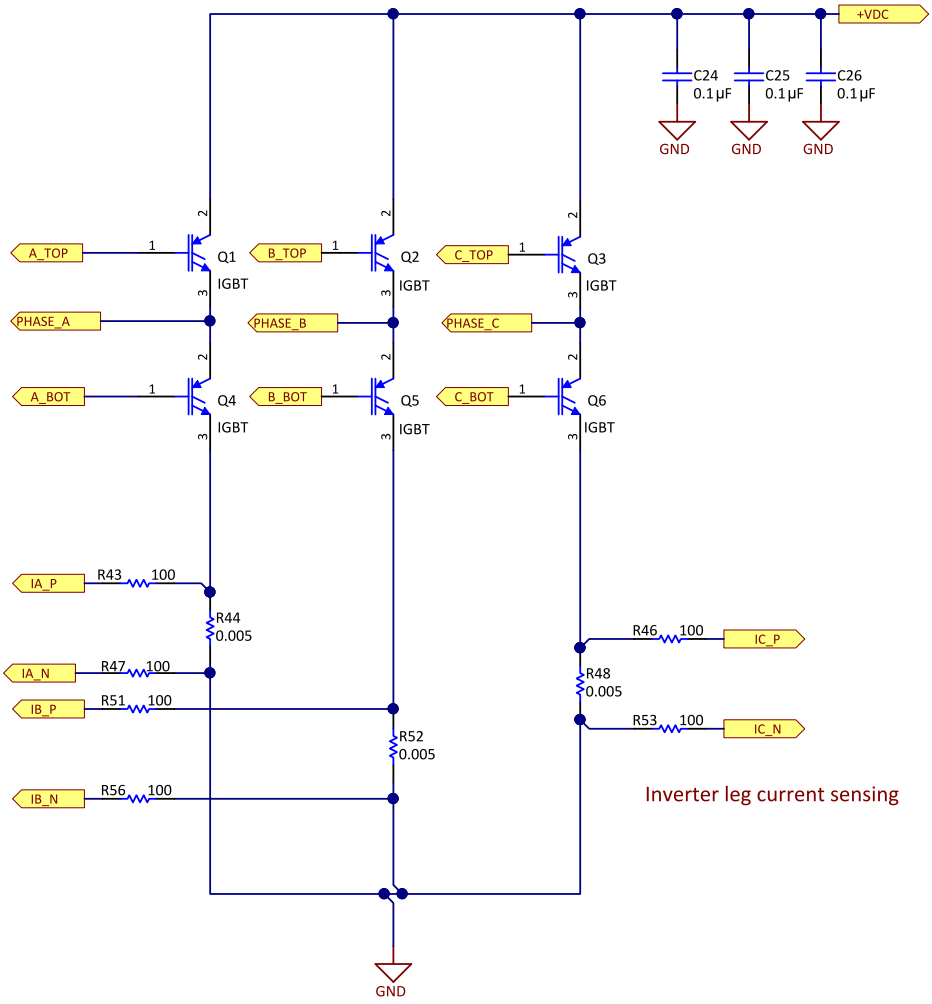
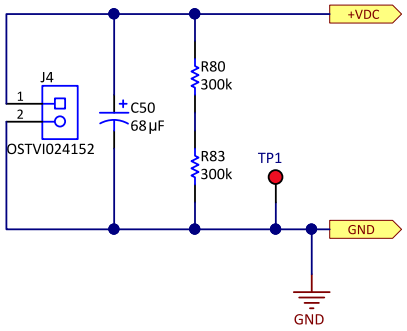


Figure 8. DC Bus Capacitor Placed in Reference Design Board

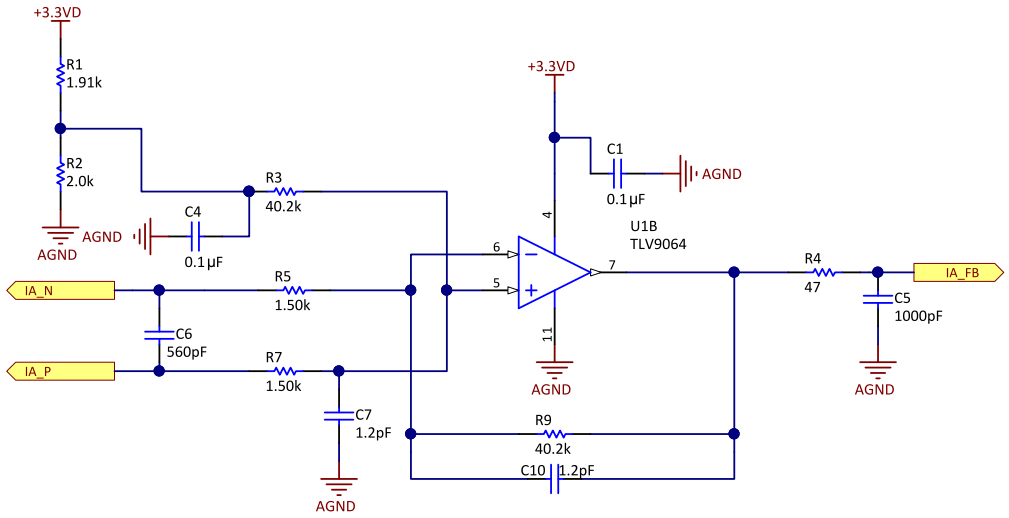


2.2.2 Current Sensing

The TIDA-010023 design has the option to use two or three shunt inverter leg current sensing. The following subsection details the design requirements and procedures for current sensing.

The TLV9064 device is used to sense and amplify the inverter leg current. The TLV906x series of devices feature rail-to-rail input- and output-swing capabilities, low input offset voltage and internal RFI and EMI filter. The TLV9064 device is a highly cost-effective solution for fast, accurate and robust current sensing. Figure 9 shows the schematic of the inverter current sensing for phase A leg.

Figure 9. Inverter Leg Sensing Circuit for Two- or Three-Shunt FOC



The current sensing circuit is designed as a non-inverting amplifier operating from unipolar single supply. The bidirectional current-sensing capability is achieved by adding a 1.65-V reference voltage level shift to the current sense amplifier output. The level shift of 1.65-V bias enables the positive current sensed at op-amp output is above 1.65-V and negative current sensed at op-amp output is below 1.65 V.

The calculation of the current-sense amplifier is as Equation 4 shows:

$$V_{OUT} = \left(I_{SENSE} \times R_{SENS} \times GAIN\right) + V_{REF} \tag{4}$$

where, $I_{SENSE}$is the current through the sense resistor, $R_{SENSE}$is the current sense resistor value, 5 mΩ is selected in this design, GAIN is set at 25, $V_{REF}$is the reference voltage of level shift, and 1.65 V is used.

The V_{REF} is generated by using divider resistors network at the non-inverter input pin of op-amp, the rules of calculation for divider resistors should follow Equation 5:

$$R1 = R2 \left\| \left(R3 + R7 + R43\right) \right. \tag{5}$$

Power consumption in sense resistors and the input-offset error voltage of op amps are important when selecting the sense-resistance values. A high sense resistance value increases the power loss in the resistors. If the current sense amplifier is used without offset calibration, select the sense resistor value such that thee sense voltage across the resistor is sufficiently higher than the op-amp input offset voltage to reduce the effect of the offset error. The low input offset voltage of TLV9064 enables to use a high gain current sense amplifier and allows the designer to use a low sense resistor value.

The nominal RMS winding current is 5.58 A. The inverter leg shunt can only carry current while the low-side switch is ON; therefore, the RMS current in the inverter leg shunt will be smaller than the RMS winding current and the value depends on the duty cycle. However, for the simplification of analysis, the winding current is considered when calculating the shunt resistor power requirement. The peak winding current is 9.5 A, as mentioned in Equation 3. The TIDA-010023 uses a 5-mΩ, 3-W sense resistor which allows sensing up to ±13.2 A with an amplifier gain of 25. The sense resistor must be selected with a low temperature drift and minimum parasitic inductance (ideally zero).

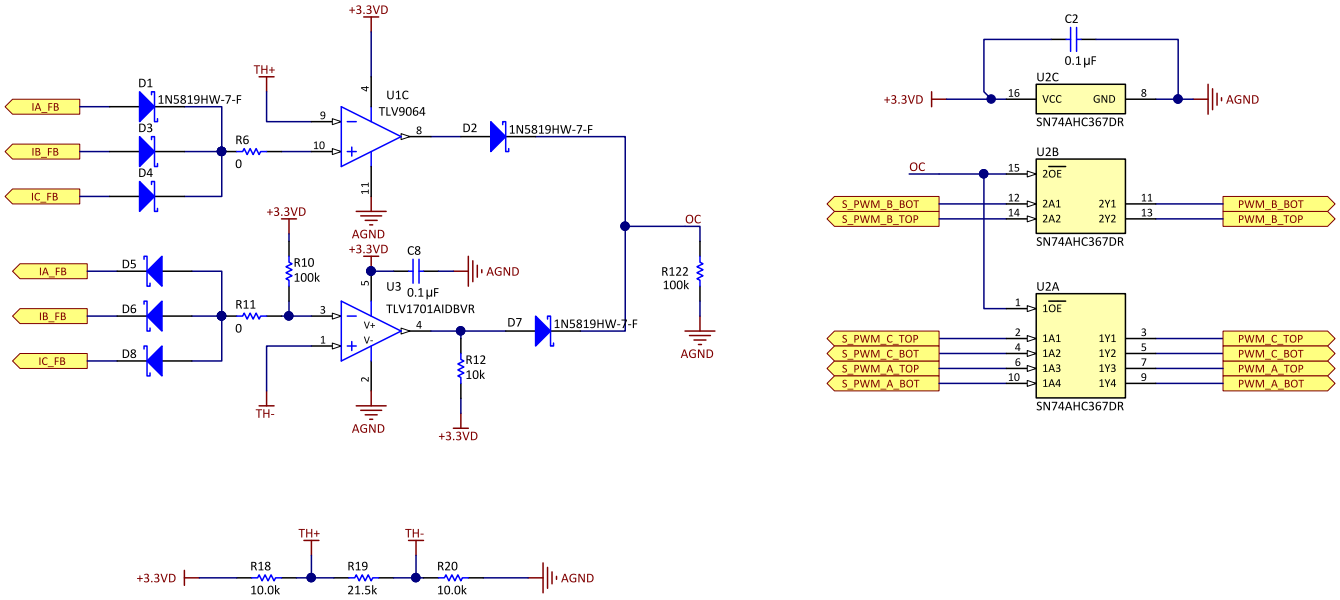
The maximum power dissipation in a single-inverter leg current sense shunt resistor equals:

$$I_{RMS}^2 \times R_{SENSE} = 6.72 \times 5\ m\Omega = 0.225\ W \tag{6}$$

2.2.3 Overcurrent Protection

Figure 10 shows the schematic of OCP for both positive and negative winding current. The circuit uses one channel of TLV9064 as a comparator and another comparator TLV1701.

Figure 10. Overcurrent Protection for Both Positive and Negative Currents



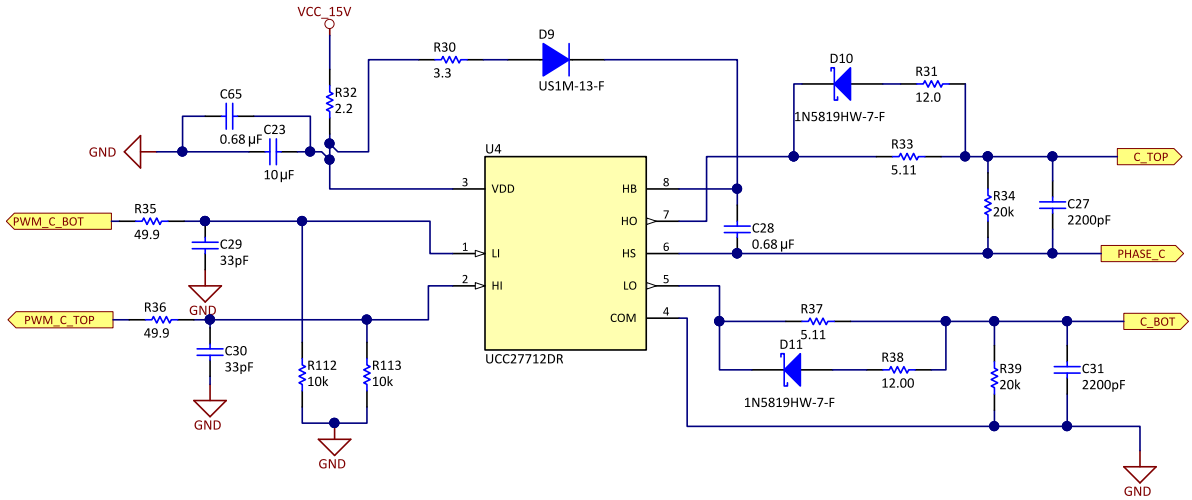
The overcurrent protection circuit output signal OC is connected to the enable pin of the line driver device - SN74AHC367. Once the overcurrent event occurs, the OC signal will be pulled up and disable the output of the line driver and hence the SVPWM signals at the input of gate driver - UCC27712. Thus, the process of protection is achieved all by hardware, which features very fast response time.

The overcurrent protection thresholds can be adjusted by changing the value of divider resistors - R18 and R20. A pullup resistor R12 is at the open-collector output of TLV1701, and meanwhile providing pull-up capability for enable signal of SN74AHC367.

2.2.4 Gate Driver Using UCC27712

Figure 11 shows the circuit diagram for a half-bridge driver using the UCC27712 device.

Figure 11. Gate Driver Schematic for Half Bridge



Selecting HI and LI Low Pass Filter Components:

A small RC filter should be added between output of line driver and input pin of UCC27712 to filter the high frequency noise. The recommend value of the RC filter is R35 = R36 = 49.9 Ω, and C29 = C30 = 33 pF.

Selecting the Bootstrap Capacitor:

The bootstrap capacitor must be sized to have more than enough energy to drive the gate of the IGBT high without depleting the bootstrap capacitor more than 10%. A good guideline is to size CBOOT to be at least ten times as large as the equivalent IGBT gate capacitance (C_g). C_g must be calculated based on the voltage driving the high-side gate of the IGBT (V_{GE}) and the gate charge of the IGBT (Q_g). V_{GE} is approximately the bias voltage supplied to VDD after subtracting the forward-voltage drop of the bootstrap diode D11 (VDBOOT). In this design example, the estimated V_{GE} is approximately 14.4 V, as Equation 7 shows.

$$V_{GE} \approx V_{DD} - V_{DBOOT} = 15\ V - 0.6\ V = 14.4\ V \tag{7}$$

The IGBT in this reference design has a specified $Q_g$of 70 nC. The equivalent gate capacitance of thee IGBT can be calculated as Equation 8 shows.

$$C_G = \frac{Q_g}{V_{GE}} = \frac{70\ nC}{14.4} \approx 4.86\ nF \tag{8}$$

After estimating the value for C_g, C_{BOOT}must be sized to at least ten times larger than C_g, as Equation 9 shows.

$$C_{BOOT} \geq 10 \times C_G \times 48.6\ nF \tag{9}$$

For this reference design, a 680-nF capacitor has been chosen for the bootstrap capacitor, as Equation 10 shows.

$$C_{BOOT} = C_{28} = 0.68\ \mu F \tag{10}$$

Selecting VDD bypass/holdup capacitor C_{VDD} and R_{bias}:

The V_{DD}capacitor (C_{VDD}) must be chosen to be at least ten times larger than C_{BOOT}. For this design, a 10-µF capacitor has been selected.

A 2.2-Ω resistor R_{BIAS}in series with bias supply and VDD pin is recommended to make the VDD ramp up time larger than 20µs to minimize LO and HO rising.

Selecting the bootstrap resistor (R_{BOOT}):

Select the resistor $R_{BOOT}$to limit the current in $D_{BOOT}$and limit the ramp-up slew rate of the voltage across the HB and HS pin. TI recommends selecting an R_{BOOT}resistor between 2 Ω and 20 Ω when using the UCC27712 gate driver. This TIDA-010023 reference design uses a current-limiting resistor of 3.3 Ω. The peak bootstrap diode current ($I_{DBOOTPK}$) is limited to approx. 4.36 A.

$$R_{BOOT} = R30 = 3.3\ \Omega$$

$$I_{DBOOT_{PK}} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} \frac{15\ V - 0.6\ V}{3.3\ \Omega} \approx 4.36\ A \tag{11}$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the bootstrap capacitor. This energy is equivalent to ½ × CBOOT × V2. This energy is also dissipated during the charging time of the bootstrap capacitor (approximately 3 × RBOOT × CBOOT). The TIDA-010023 reference design uses a 3.3-Ω, 0.125-W resistor.

Selecting the bootstrap diode:

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case a maximum of 390-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor to the 15-V VDD supply. The diode must be able to carry a pulsed peak current of 4.36 A. However, the average current is much smaller and depends on the switching frequency and the gate charge requirement of the high-side IGBT. The TIDA-010023 reference design uses a 1000-V, 1-A, fast-recovery diode.

Selecting thee-gate resistor $R_{ON}$and R_{OFF}:

Resistor $R_{ON}$and $R_{OFF}$are sized to achieve the following:

- Limit ringing caused by parasitic inductances and capacitances.
- Limit ringing caused by high voltage/current switching dV/dt, dI/dt, and body diode reverse recovery.
- Fine-tune gate drive strength to optimize switching loss.
- Reduce electromagnetic interference (EMI)

From the *UCC27712 620-V, 1.8-A, 2.8-A High-Side Low-Side Gate Driver with Interlock* data sheet:

LO and HO output pulldown resistance, $R_{HOL} = R_{LOL} = 1.5\ \Omega$

LO and HO output pullup resistance, $R_{HOH} = R_{LOH} = 3.0\ \Omega$

The TIDA-010023 reference design uses different gate resistors in the turnon and turnoff path of the IGBT. The external gate resistance in the turnon path is R33 = R38 = 5.0 Ω, and external gate resistance in the turnoff path is 5.0 Ω and 12 Ω in parallel.

Equation 12 calculates the maximum HO drive current (I_{HO_DR}):

$$I_{HO\_DR} = \frac{V_{DD} - V_{DBOOT}}{R_{HOH} + R_{ON} + R_{GFET_{Int}}} = \frac{12\ V - 0.6\ V}{3\ \Omega + 5\ \Omega + 1\Omega} \approx 1.27\ A \quad (12)$$

Equation 13 calculates the maximum HO sink current (I_{HO_SK}):

$$I_{HO\_SK} = \frac{V_{DD} - V_{DBOOT} - V_{DGATE}}{R_{HOL} + R_{ON} + R_{GFET_{Int}}} = \frac{12\ V - 0.6\ V - 0.6\ V}{1.5\ \Omega + 3.53\ \Omega + 1\Omega} \approx 1.7\ A \quad (13)$$

Equation 14 calculates the maximum LO drive current (I_{LO_DR}):

$$I_{LO\_DR} = \frac{V_{DD}}{R_{LOH} + R_{ON} + R_{GFET_{Int}}} = \frac{12\ V}{3\ \Omega + 5\ \Omega + 1\Omega} \approx 1.33\ A \quad (14)$$

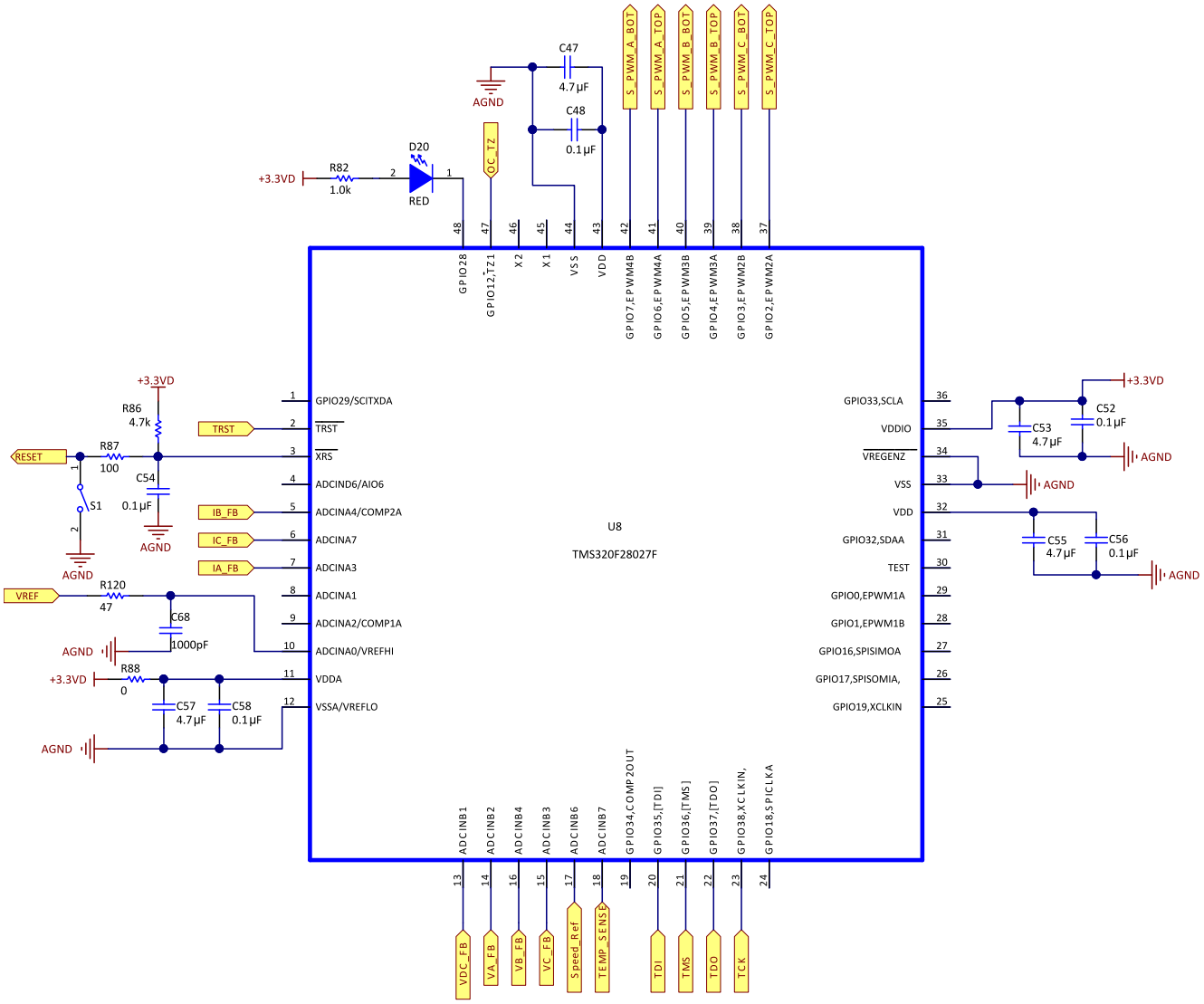
Equation 15 calculates the maximum LO sink current (I_{LO_SK}):

$$I_{LO\_SK} = \frac{V_{DD} - V_{DGATE}}{R_{LOL} + R_{ON} + R_{GFET_{Int}}} = \frac{12\ V - 0.6\ V}{1.5\ \Omega + 3.53\ \Omega + 1\Omega} \approx 1.9\ A \quad (15)$$

2.2.5 Microcontroller Unit

Piccolo TMS320F28027F MCU is used in the reference design. This MCU has special motor control software in execute-only ROM to enable InstaSPIN-FOC solution, with system software support through MotorWare™ Software. The F2802x Piccolo™ family of microcontrollers provides the power of the C28x core coupled with highly-integrated control peripherals in low pin-count devices. The digital and analog power supplies are provided with adequate decoupling. The analog power supply is decoupled through R88 resistor (the designer can choose a value up to 10 Ω) to isolate the switching currents from the digital power supply, which provides a better power supply noise rejection for the ADC of the MCU.

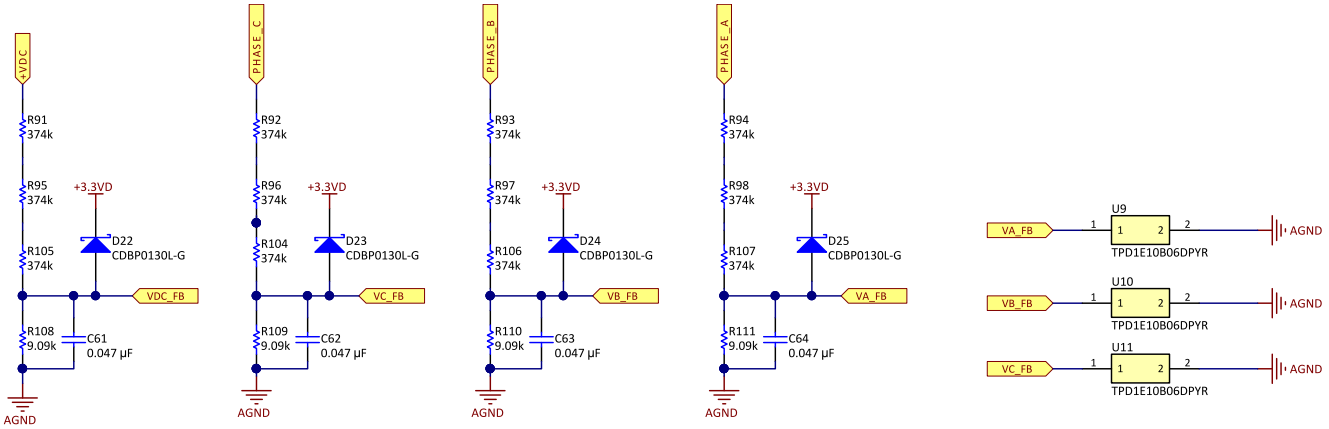
Figure 12. MCU Schematic and Peripheral Connections



2.2.6 Voltage Sensing

The voltage divider circuit that Figure 13 shows is used to measure the winding voltages and DC bus voltage. Voltage feedback is required in the FAST™ software encoder estimator of the InstaSPIN-FOC to allow the best performance at the widest speed range. In FAST, phase voltages are measured directly from the motor phases instead of a software estimate. This software value (USER_ADC_FULL_SCALE_VOLTAGE_V) depends on the voltage divider gain of the circuit, which senses the voltage feedback from the motor phases

Figure 13. DC Bus and Winding Voltage Sensing



In Figure 13, PHASE_A, PHASE_B, and PHASE_C are the phase voltages. These voltages are properly scaled and fed to the MCU through VA_FB, VB_FB, and VC_FB. The maximum phase voltage feedback measurable by the MCU can be calculated as Equation 16 shows, considering the maximum voltage for the ADC input is 3.3 V.

$$V_a^{max} = V_{ADC\_a}^{max} \times \frac{(9.09\ k\Omega + 1122\ k\Omega)}{9.09\ k\Omega} = 410.62\ V \tag{16}$$

For a motor with a maximum operating voltage of 390 V, this voltage feedback resistor divider is ideal. This divider makes sure that the ADC resolution is at the maximum for a motor working from 270-V DC to 390-V DC.

The voltage filter pole is required by the FAST estimator (see the *InstaSPIN-FOC™ and InstaSPINMOTION™* user's guide) to allow an accurate detection of the voltage feedback. The filter cutoff frequency should be low enough to filter out the PWM signals. As a general guideline, a cutoff frequency of a few hundred Hertz is enough to filter out a PWM frequency of 10 kHz to 20 kHz. The hardware filter should only be changed when ultra-high speed motors are run, which generate phase voltage frequencies in the order of a few kHz. In this reference design, consider the PMSM to have a maximum speed of approximately 3,000 RPM with eight pole pairs. This scenario gives a voltage frequency of: 3000 × 8 / 60 = 400 Hz. The voltage filter of 400 Hz should be enough cutoff frequency for this motor and speed. The filter pole setting is calculated using Equation 17.

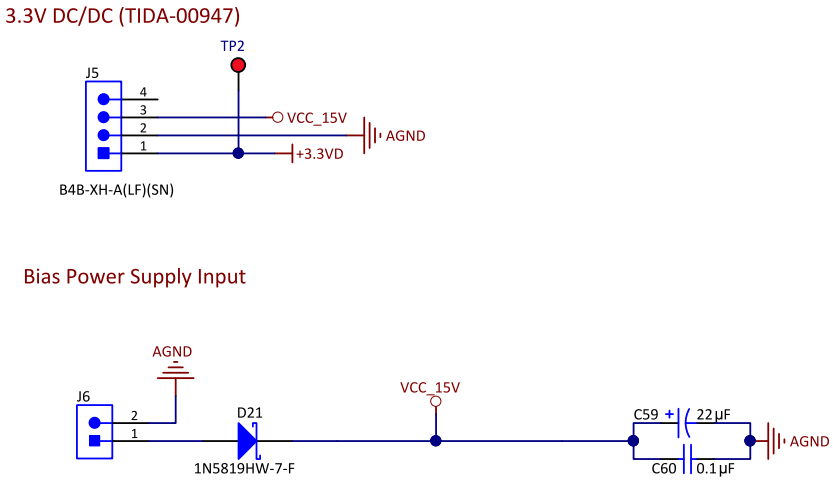
$$F_{filter\_pole} = \frac{1}{2 \times \pi \times R_{parallel} \times C} = \frac{1}{2 \times \pi \times \frac{(1122\ k\Omega \times 9.09\ k\Omega)}{(1122\ k\Omega \times 9.09\ k\Omega)} \times 0.047\ \mu F} = 375.7\ Hz \tag{17}$$

2.2.7 External Bias Power Supply and Onboard DC/DC module

The TIDA-010023 reference design board requires external 15 V, which is used for the gate driver power supply. The 3.3-V power supply for MCU, current sense amplifier, and the signal conditioning circuits is from TIDA-00947 reference design board.

The TI Design TIDA-00947 demonstrates a small, high efficiency, low EMI DC/DC module to replace LDOs in major home appliance applications. This results in drastic improvement in efficiency, saving both size and cost, as no heat sink is required. With the same input current, the TPS54202, as a power converter, enables the supplying of higher output current as well as having lower power consumption at full load, low load, and standby operation. This module is size and pin compatible with a TO-220 LDO enabling a quick evaluation and time to market.

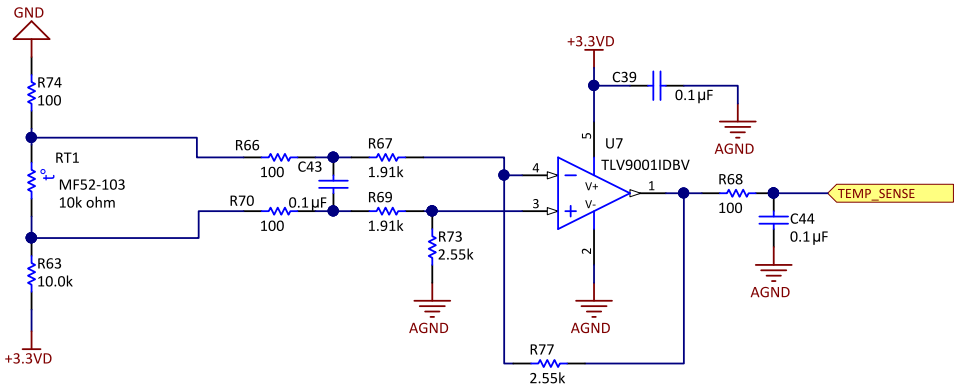
Figure 14. Bias Power Supply Connection



2.2.8 IGBT Temperature-Sensing Signal Conditioning Circuit

A NTC resistor is used and can be mounted on the heatsink. The NTC is biased using one resistor R63 (10 kΩ) to 3.3 V and one resistor R74 (100 Ω) to ground as Figure 15 shows. The 10-kΩ resistor limits the current in the circuit at the minimum temperature sensor resistance. The voltage across the NTC is connected as the differential input to the TLV9001 op amp configured as a differential amplifier.

Figure 15. IGBT Temperature-Sensing Signal Conditioning Circuit



The ADC of the MCU reads the output of the temperature sense signal-conditioning circuit and necessary action can be taken for overtemperature protection.

2.3 Highlighted Products

2.3.1 TLV9064

The major requirements in selecting the current sense amplifier are adequate gain bandwidth & slew rate, RRIO capability, good CMRR and PSRR, good EMI and RFI rejection, low offset voltage and input offset current and stable capacitive load drive.

The TLV9061 (single), TLV9062 (dual), and TLV9064 (quad) are single-, dual-, and quad- low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler.

2.3.2 TLV1701

The TLV170x family of devices offers a wide supply range, rail-to-rail inputs, low quiescent current, and low propagation delay. The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to +36 V above the negative power supply, regardless of the TLV170x supply voltage, and allows easy-wired OR structure with other fault outputs All devices are specified for operation across the expanded industrial temperature range of –40°C to +125°C.

2.3.3 UCC27712

The UCC27712 is a 620-V high-side and low-side gate driver with 1.8-A source, 2.8-A sink current, targeted to drive power MOSFETs or IGBTs. The recommended VDD operating voltage is 10-V to 20-V for IGBTs and 10-V to 17-V for power MOSFETs. The UCC27712 includes protection features where the outputs are held low when the inputs are left open or when the minimum input pulse width specification is not met. Interlock and deadtime functions prevent both outputs from being turned on simultaneously. In addition, the device accepts a wide range bias supply range and offers UVLO protection for both the VDD and HB bias supply. Developed with TI's state of the art high-voltage device technology, the device features robust drive with excellent noise and transient immunity including large negative voltage tolerance on its inputs, high dV/dt tolerance, wide negative transient safe operating area (NTSOA) on the switch node (HS), and interlock. The device consists of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap or isolated power supplies. The device features fast propagation delays and excellent delay matching between both channels. On the UCC27712, each channel is controlled by its respective input pins, HI and LI

2.3.4 TLV9001

The TLV900x family includes single (TLV9001), dual (TLV9002), and quad-channel (TLV9004) low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective solution for space-constrained applications such as smoke detectors, wearable electronics, and small appliances where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900x family is 500 pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the TLV600x devices.

The robust design of the TLV900x family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions. The TLV900x devices include a shutdown mode (TLV9002S and TLV9004S) that allow the amplifiers to switch off into standby mode with typical current consumption less than 1 µA.

2.3.5 SN74AHC367

The SN74AHC367 devices are hex buffers and line drivers designed for 2-V to 5.5-V VCC operation. These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The SN74AHC367 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable (1OE and 2OE) inputs. When OE is low, the device passes non-inverted data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2.3.6 TMS320F28027F

The F2802x Piccolo family of microcontrollers provides the power of the C28x core coupled with highly-integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code and also provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0- to 3.3-V fixed full-scale range and supports ratio-metric VREFHI and VREFLO references. The ADC interface has been optimized for low overhead and latency.

Piccolo TMS320F28027F has special motor control software in execute-only ROM to enable InstaSPIN-FOC solution, with system software support through MotorWare™. While standard C2000™ controlSUITE™ software can be used with these devices, note that this special ROM replaces the standard ROM, which means that certain software functions that controlSUITE™ projects expect to be in ROM must to be linked into the project. See the *InstaSPIN-FOC and InstaSPIN-MOTION Memory Considerations* section of the *InstaSPIN-FOC™ and InstaSPINMOTION™* user's guide or the *Memory* section of *TMS320F2802x Piccolo™ Microcontrollers* for more details.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Connector Configuration of TIDA-010023

Figure 16 shows the TIDA-010023 connector configuration, the details follow:

- Two-terminal connector for high voltage DC input (J4): This pin is used to connect the input DC supply from the preceding AC-DC power supply or the power factor correction (PFC) circuit. The positive and negative terminals can be identified as shown in Figure 16. The maximum voltage allowed at this pin is 3900 V.
- Two-terminal output connector for bias power supply (J6): This connector is used to provide external power supply to the board. The board requires an external 15-V power supply with ±10% tolerance.
- Four-terminal connector for installing TIDA-00947: This connector is used to install a LDO with TO-220 footprint or a DC/DC module such as TIDA-00947.
- Three separate connectors for motor winding connection: Figure 16 shows the phase output connections for connecting to the three-phase motor winding.
- 14-pin JTAG connector (J7): This connector is used for programming the MCU from an external JTAG interface driver.

Figure 16. TIDA-010023 PCB Connectors

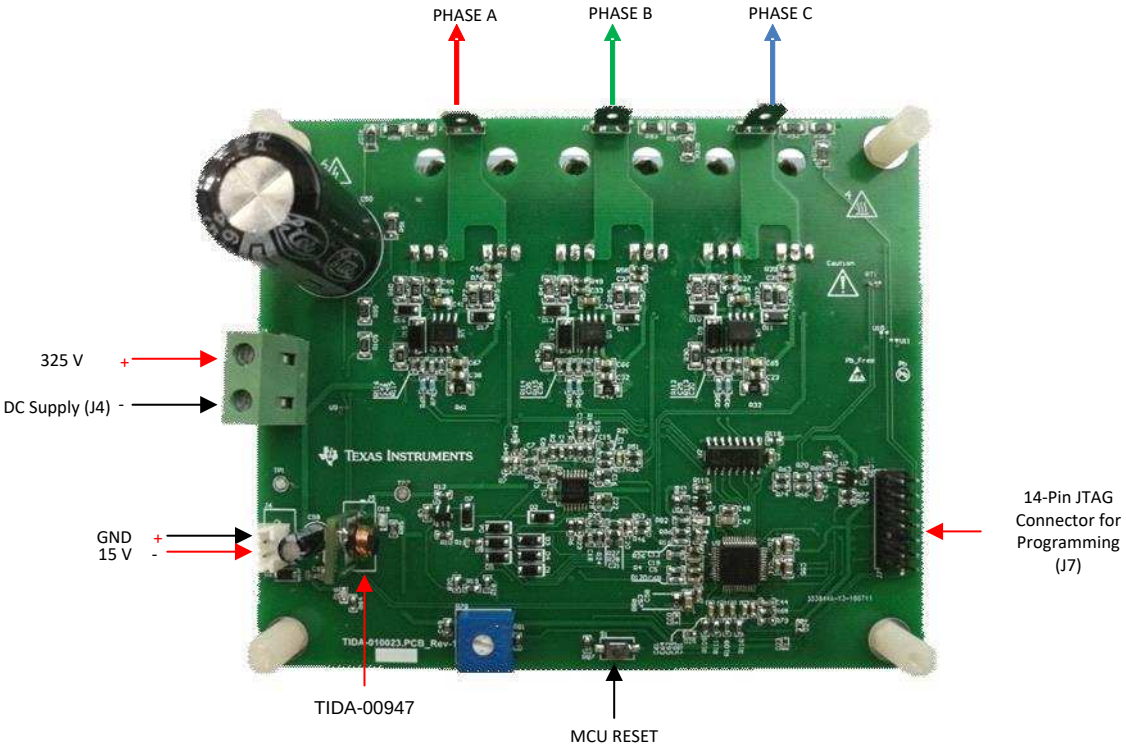


Table 2 lists the recommended operating voltages on the connectors.

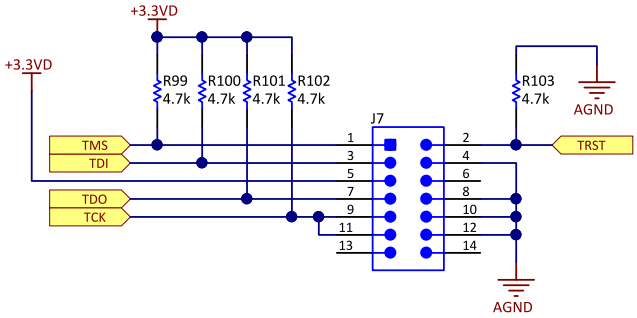
Table 2. Recommended Operating Voltage on Connectors

DESCRIPTION	VOLTAGE SPECIFICATION			MAXIMUM CURRENT
	MIN	TYP	MAX	
High: DC Input (J4)	270 V	325 V	390 V	10 A
Motor: Connection	270 V	325 V	390 V	10 A
15-V bias power supply (J6)	13.5 V	15 V	16.5 V	50 mA

3.1.1.2 Programming the TMS320F28027F

Figure 17 shows thee pin details of the 14-pin JTAG connector provided in the board.

Figure 17. MCU Programming Connector



See http://www.ti.com/product/TMS320F28027F/toolssoftware#devtools for the different programming options of the TMS320F28027.

CAUTION

Use an isolated JTAG interface for programming and real-time debugging of the board, if the board is powered from non-isolated power supplies. The use of a non-isolated JTAG interface is only permitted if all of the power supply to the system is properly isolated with sufficient safety precautions.

3.1.1.3 Procedure for Board Bring-up and Testing Using InstaSPIN-FOC™

The following list details the procedure for board bring-up and testing:

1. Remove the motor connection and high-voltage DC supply input from the board and power on the 15-V supply.
2. Use the power supply from the computer to power the JTAG driver.
3. Program the MCU as detailed in Section 3.1.1.2.
4. Connect the inverter output to the motor winding terminals.
5. Use a current-limited DC source to power up the high-voltage supply input.
6. See the *InstaSPIN-FOC™ and InstaSPINMOTION™* user's guide to understand the detailed procedure for using InstaSPIN-FOC.

3.1.2 Software

The InstaSPIN-FOC is selected as it is easy to work with motors with unknown parameters. The MCU firmware for the C2000™ is taken from MotorWare Software. MotorWare contains the required projects and libraries to use TI's InstaSPIN-FOC technology. Download the MotorWare Software from http://www.ti.com/tool/motorware.

This design is similar to the 'HVMotorCtrl+PfcKit_v2.1' hardware. Therefore, for Code Composer Studio™ projects, use the projects under "hvkit_rev1p1". After installing the MotorWare Software, the projects are found in the folder location:
...\motorware_1_01_00_18\sw\solutions\instaspin_foc\boards\hvkit_rev1p1\f28x\f2802xF\projects\ccs

Table 3 shows the hardware assignments in the TIDA-010023 reference design.

Table 3. Hardware Assignments in TIDA-010023

HARDWARE ASSIGNMENTS		DESCRIPTION
Development and emulation		Code Composer Studio software
Target controller		TMS320F28027F
PWM frequency		15-kHz PWM (default), programmable for higher and lower frequencies
PWM mode		Space vector, complimentary with dead time
Peripherals Used	PWM Generation	EPWM4A → Phase-A top-switch PWM
		EPWM4B → Phase-A bottom-switch PWM
		EPWM3A → Phase-A top-switch PWM
		EPWM3B → Phase-A bottom-switch PWM
		EPWM2A → Phase-A top-switch PWM
		EPWM2B → Phase-A bottom-switch PWM
	Overcurrent PWM shutoff trip-zone	TZ1 → Overcurrent comparator output (OC)
	ADC Channel assignment	ADCINA3 → Phase-A inverter leg current sense feedback
		ADCINA4 → Phase-A inverter leg current sense feedback
		ADCINA7 → Phase-A inverter leg current sense feedback
		ADCINB2 → Phase-A motor voltage sense feedback
		ADCINB4 → Phase-A motor voltage sense feedback
		ADCINB3 → Phase-A motor voltage sense feedback
		ADCINB1 → DC bus voltage sense feedback
		ADCINB7 → Temperature sense feedback
		ADCINB6 → Potentiometer voltage feedback
	GPIO	GPIO28 → LED indication

Before running the InstaSPIN projects, the hardware assignments should be modified in software because of the difference between this design and 'HVMotorCtrl+PfcKit_v2.1' hardware. The details of modifying the hardware assignments is provided in section 6 of 'Hardware Abstraction Layer (HAL) Module of MotorWare™' in ...\motorware\motorware_1_01_00_18\docs\tutorials\motorware_hal_tutorial.pdf.

Before running the InstaSPIN projects, the user parameters should also be modified in software. The details of modifying the user parameters is provided in chapter 4 of *InstaSPIN-FOC™ and InstaSPINMOTION™*.

The detailed procedure to build and run the lab is provided in 'InstaSPIN Projects and Labs User's Guide' in : ...\motorware\motorware_1_01_00_18\docs\labs\instaspin_labs.pdf.

3.2 Testing and Results

Table 4 lists the key test equipment. The following subsections descriptions and pictures of the test setup for specific tests.

Table 4. Key Test Equipment

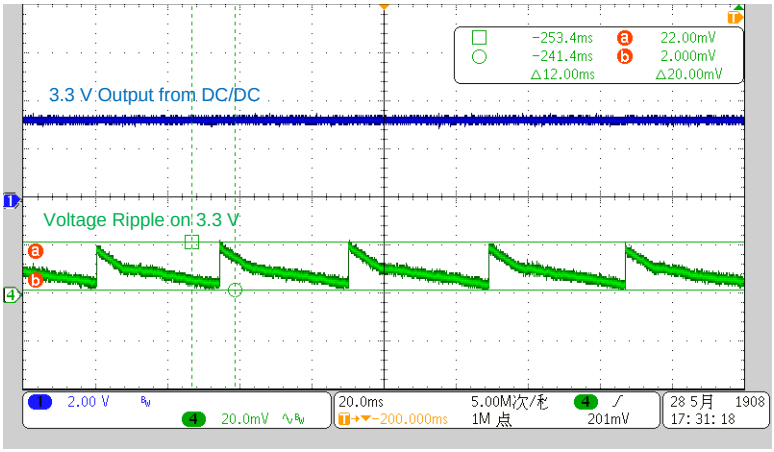
DESCRIPTION	PART NUMBER
High-speed oscilloscope	MSO4104B mixed-signal oscilloscope 1 GHz
High-voltage DC power	6260-600 digital DC power supply
Adjustable power supply	GPS-3303C laboratory DC power supply
High-current adjustable Load	Chroma 63103 DC electronic load 6 A, 60 A, 300 W
JTAG debugger	XDS100V3 emulator

3.2.1 Test Results

3.2.1.1 3.3-V Power Supply Generated by TIDA-00947

Figure 18 shows the 3.3 V generated from TIDA-00947. The ripple in the 3.3-V rail is below 20 mV at no load. For more information about DC/DC modules, see the TIDA-00947 design guide.

Figure 18. Voltage Ripple From TIDA-00947 DC/DC Module



3.2.1.2 Functional Evaluation of UCC27712 Gate Driver

The UCC27712 gate driver receives PWM signals from the line driver output of the SN74AHC367 and the corresponding gate driver voltages are generated. Figure 19 shows the low-side and high-side PWM input of the UCC27712 device and the corresponding low-side and high-side output of the UCC27712 device measured across the gate to the emitter (V_{GE}) of the IGBT.

Figure 19. Low-Side and High-Side Gate Driver Voltage from UCC27712

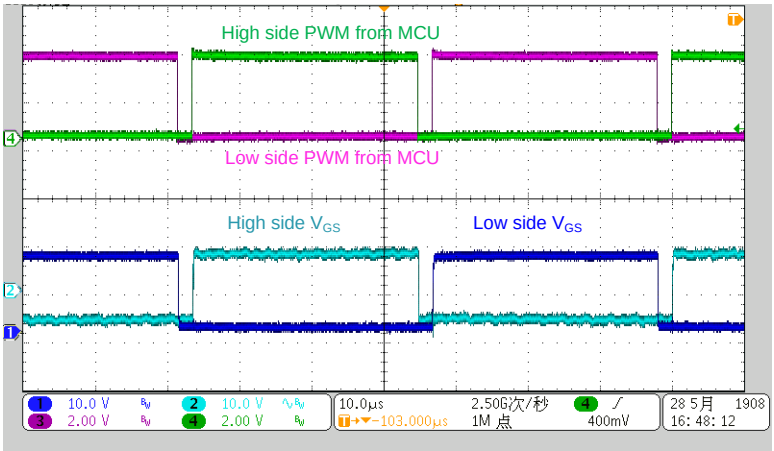


Figure 20 shows the PWM signals of high-side and low-side gate to source voltage from UCC27712, which shows that the dead time configured by the MCU at both of the edges of the PWM. The dead time is programmed to 2 µs.

Figure 20. Dead Time at Falling Edge and Rising Edge of Low-Side PWM

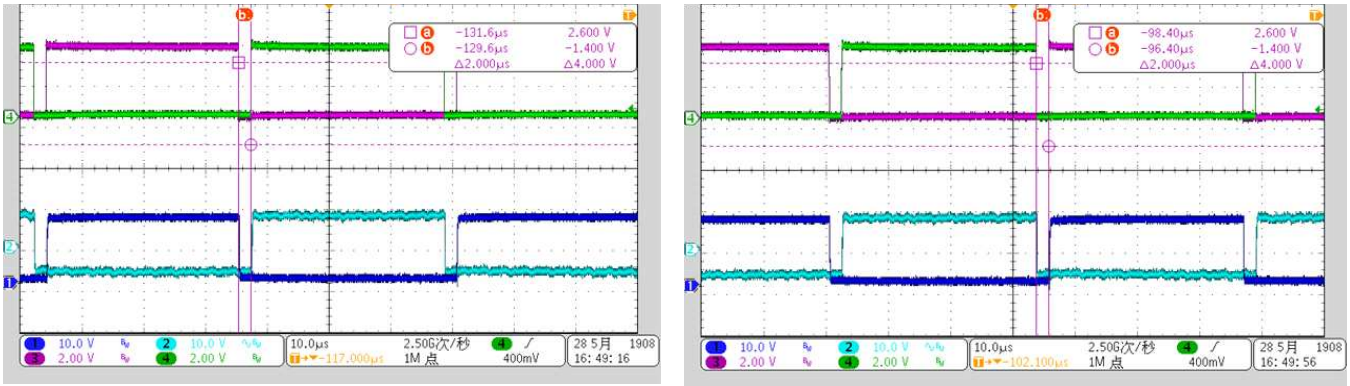


Figure 21, Figure 22, and Figure 23 show the source and sink current provided by UCC27712. The peak gate current is captured by monitoring the voltage across the gate resistors. The test conditions follow:

- $R_{G(ON)}$ = 5.0 Ω
- $R_{G(OFF)}$ = 3.53 Ω
- Gate charge (Q_g) of IGBT = 70 nC

During the testing no external capacitance is connected between the gate and source of the IGBT. The reference design is tuned to get a source current of approximately 0.85 A, and the sink current of approximately 1.7 A.

Figure 21. Source Current From Gate Driver

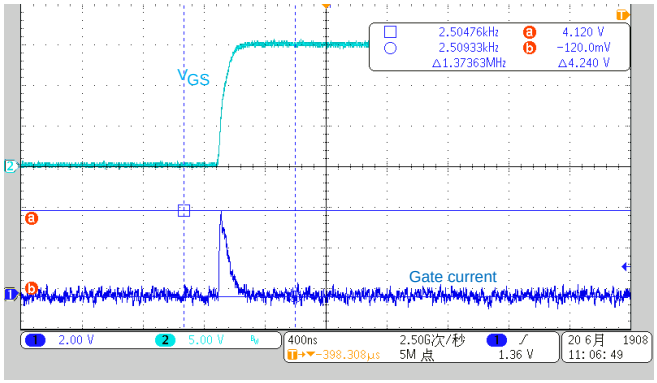


Figure 22. Sink Current From Gate Driver

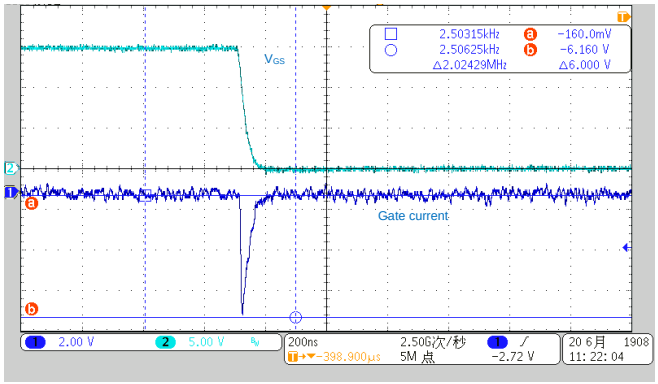
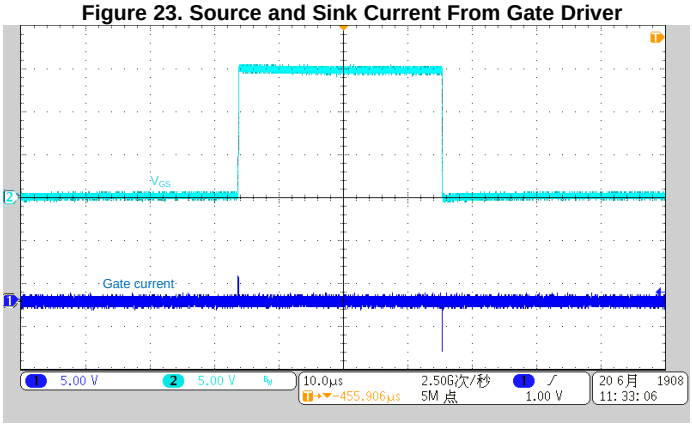


Figure 23. Source and Sink Current From Gate Driver



A bootstrap capacitor of 0.68 µF is used in the reference design. Figure 24 shows the ripple on the bootstrap capacitor. The peak-to-peak ripple voltage is 0.78 V. The test result is taken with a duty cycle of 80% and the designed bootstrap capacitor maintains voltage ripple within 5% and eliminates undervoltage lockout even in the worst conditions.

Figure 24. Voltage Ripple Across Bootstrap Capacitor

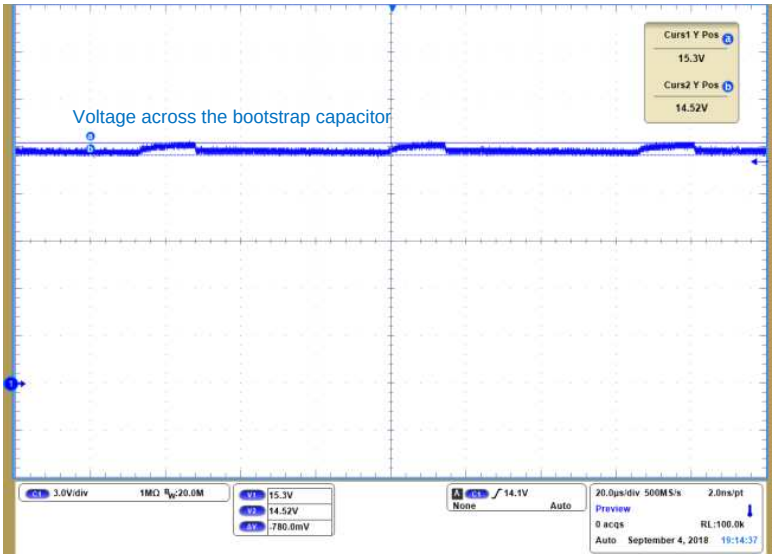


Figure 25 shows the propagation delays measured for the low-side and high-side gate drivers at rising and falling edges. The measured propagation delay is 100 ns. *UCC27712 620-V, 1.8-A, 2.8-A High-Side Low-Side Gate Driver with Interlock* specifies the propagation delay of 100 ns (typical) and delay matching of 12 ns (typical) helps in reducing the winding current distortion.

Figure 25. Gate Driver Propagation Delay During PWM Turnon and Turnoff

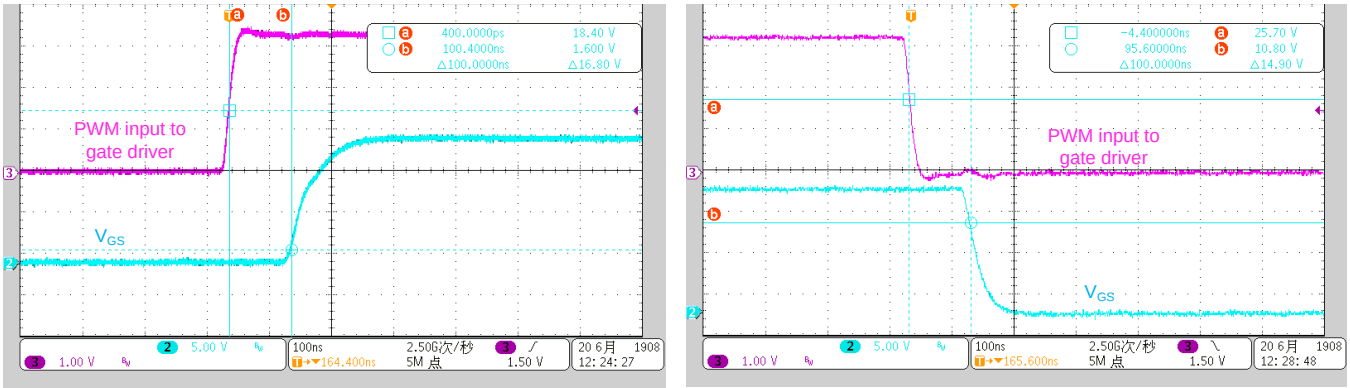


Figure 25 shows the UVLO protection of UCC27712, and the threshold voltage observed is approximately 8.4 V, which ensure that the IGBT is turned on properly with sufficient gate voltage.

3.2.1.3 Current Sensing

The transient response of the current sense amplifier is evaluated with a step change in voltage across the shunt resistor. The step change in sense voltage is created by switching the corresponding IGBTs with the motor connected, causing the winding current to flow through the sense resistor.

Figure 26 shows the simulated step response of TLV906x with the circuit as shown in Figure 9. The settling time is calculated as the time to reach steady value with 5% error. The simulation is done at 10 A and 12 A current, which corresponds to 50 mV and 60 mV voltage across the shunt resistor. The testing at 12 A shows almost full swing of the op-amp output.

Figure 26. Simulated Step Response of Current Sensing Circuit

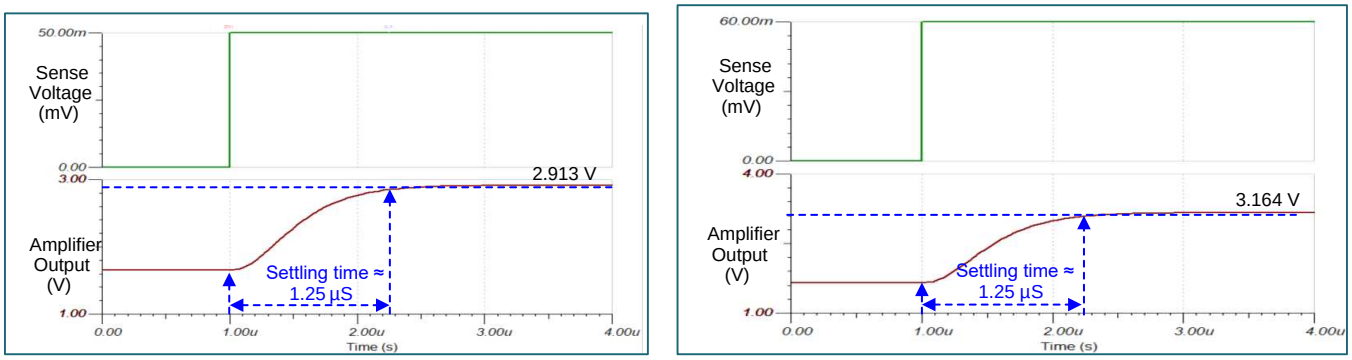


Figure 27, Figure 28, and Figure 29 show the step response with positive and negative winding current of 10 A. The test is done with R43 = R47 = 100 Ω and C6 = 560 pF. The voltage oscillations across the shunt resistor are produced mainly because of the parasitic inductance of the shunt resistor, circuit parasitic capacitance in the current path, and by the coupled noise from the IGBT switching. The input filter of the amplifier and the internal EMI filters of the amplifier helps to remove the high frequency oscillations across the shunt resistor. The full swing transient response settling time of the current sense amplifier can be observed as 1.25 us. The high 10 MHz GBW and high slew rate of the TLV9064 helps to achieve faster settling time.

Figure 27. Step Response of Current Sensing Circuit

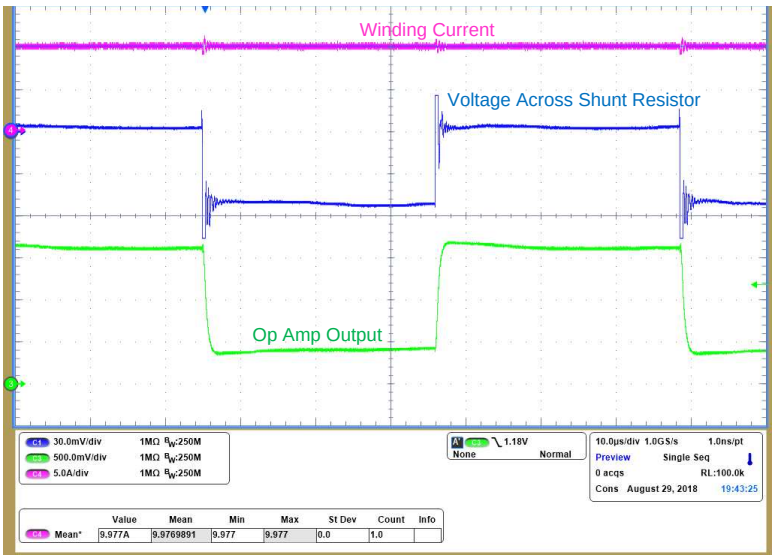


Figure 28. Step Response of Current-Sensing Circuit With 10-A Positive Current

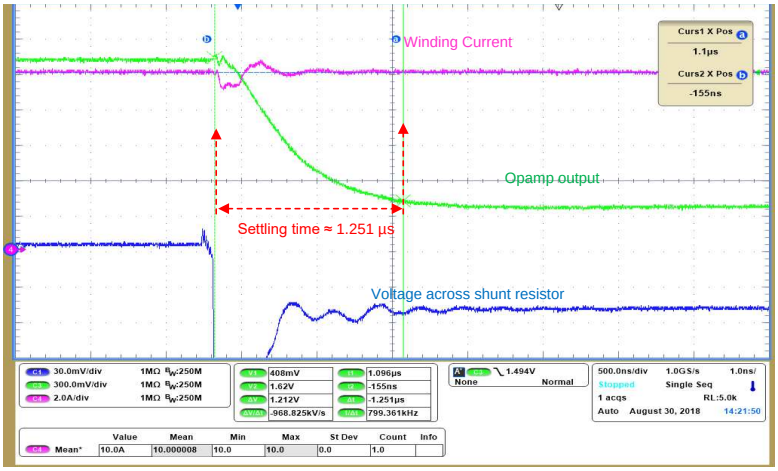


Figure 29. Step Response of Current-Sensing Circuit With 10-A Negative Current

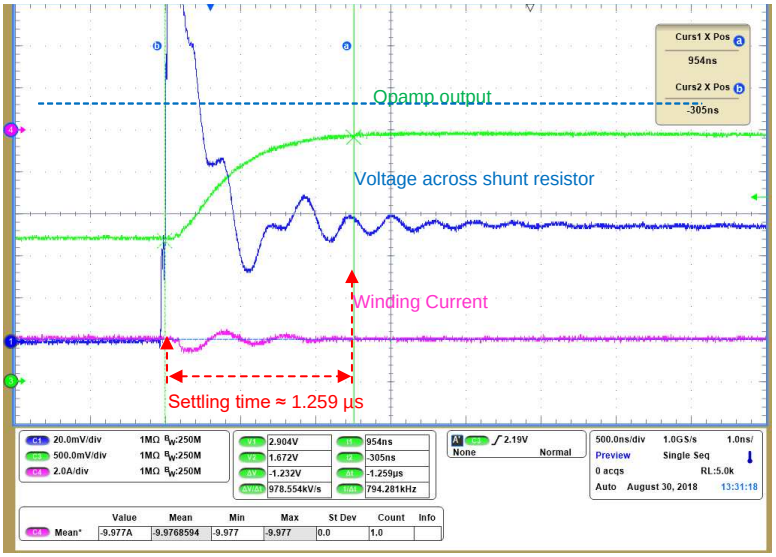


Figure 30 and Figure 31 show the step response with winding current at 12 A winding current. The settling time of current sense amplifier output is 1.34 µs. Faster settling time and rail to rail output capability helps to minimize the current sense distortion especially with 2-shunt at lower phase duty cycles.

Figure 30. Step Response of Current Sensing Circuit With 12-A Positive Current

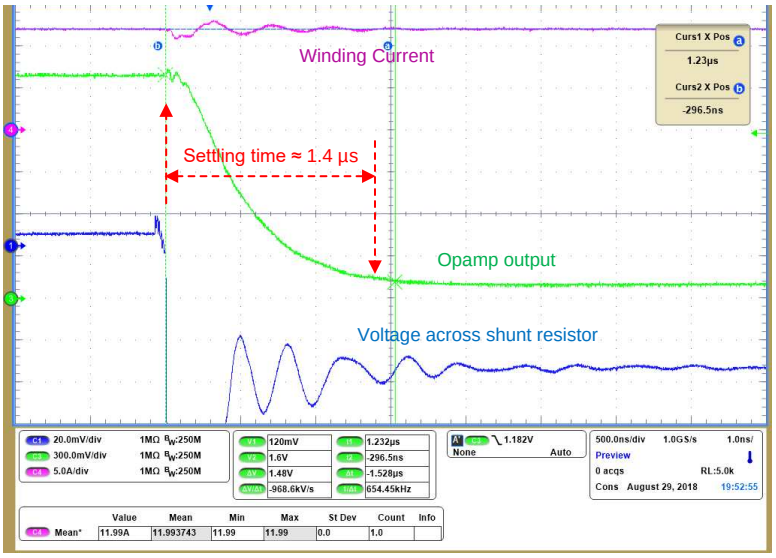


Figure 31. Step Response of Current-Sensing Circuit With 12-A Negative Current

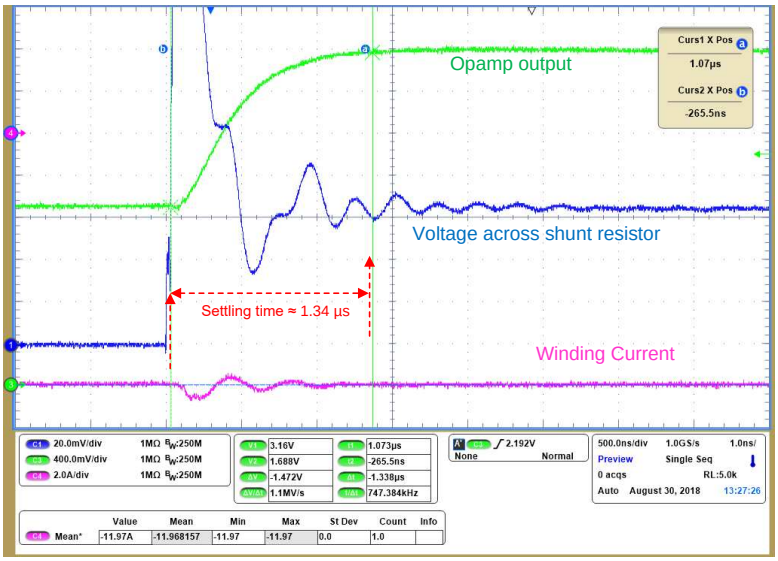
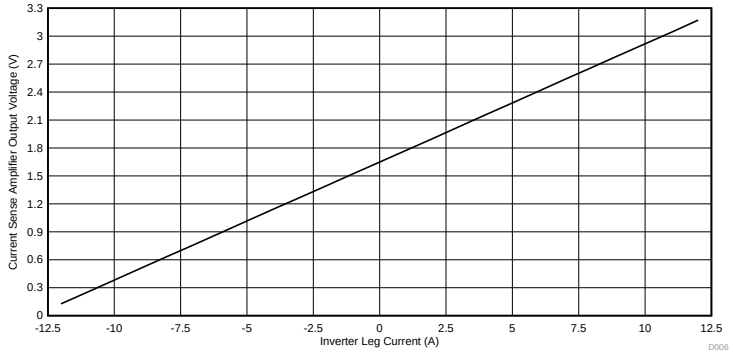


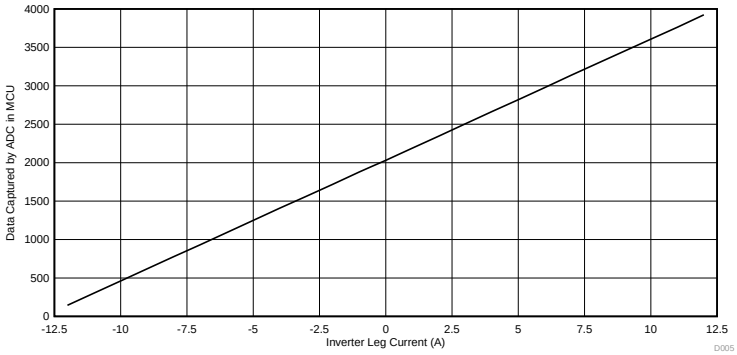
Figure 32 shows the steady-state transfer function of the inverter leg current through the 5-mΩ shunt resistor versus the output voltage of the TLV9064 amplifier. The output voltage equals 9.2 mV when the inverter leg current is zero, mainly contributed by the offset voltage of the op-amp, which can be calibrated. The test is done across the full swing range from -12 A to +12 A current. The transfer function is linear, which makes the software processing simple.

Figure 32. Inverter Leg Current vs Output Voltage Transfer Function Op Amp



With the purpose of evaluating the transfer function for actual data used in the sensorless FOC algorithm, Figure 33 shows the transfer function of the inverter leg current through the shunt resistor versus the values read from ADC data buffer of TMS320F28027F. The transfer function is linear across -12 A to +12 A current. The transfer function is also linear, which means no extra calibration algorithm needed.

Figure 33. Inverter Leg Current vs Data Acquired by ADC in MCU Transfer Function



DC accuracy of the current sense amplifier TLV9064 is done with 5-mΩ sense resistor at a gain of 25.125 V/V and at 25°C ambient temperature. The full-scale DC bus current range is –13.2 A to +13.2 A. The inverter leg current is measured with a precision 6½ digit multimeter connected in series to the inverter leg shunt and the output voltage of the current sense amplifier TLV9064 is measured with another precision 6½ digit multimeter.

The TLV9064 has low input offset voltage of ±0.3 mV, low input offset current of 0.05 pA, and high CMRR. Figure 34 shows the absolute error in inverter leg current measurement. The uncalibrated absolute error (shown in black curve in Figure 34) is less than 0.25 A (absolute value) with respect to the input current range from –12 A to 12 A. The uncalibrated error is dominated by sense resistor tolerance, offset voltage of the amplifier, feedback resistor tolerance, variation in reference voltage, and power supply ripple. The current sense amplifier output error is calibrated for offset voltage (shown in red curve in Figure 34) and the calibrated output error is less than ±0.11 A. The current sense amplifier output error is calibrated for sense resistor tolerance (shown in green curve in Figure 34) and the calibrated output error is less than ±0.02 A. Figure 35 shows the relative error [%] in measured current from the amplifier output voltage, and the calibrated relative error for offset voltage and sense resistor tolerance is less than 1%, after calibrating for op-amp offset voltage.

Figure 34. Absolute Error in Inverter Leg Current Measurement

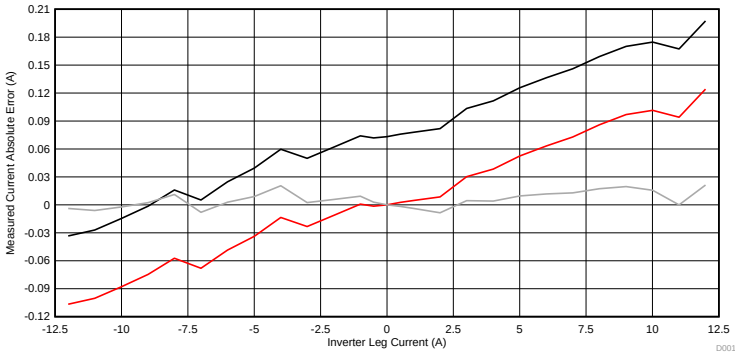
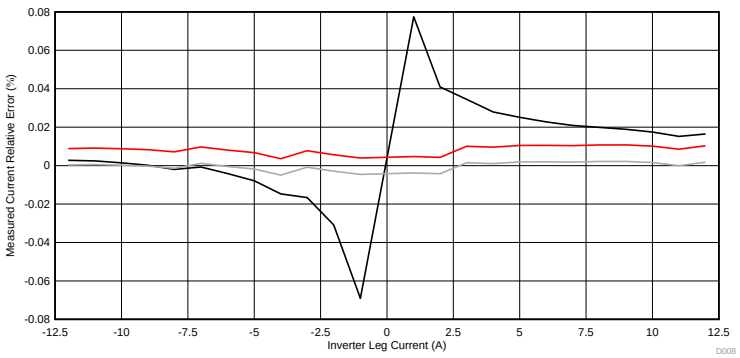


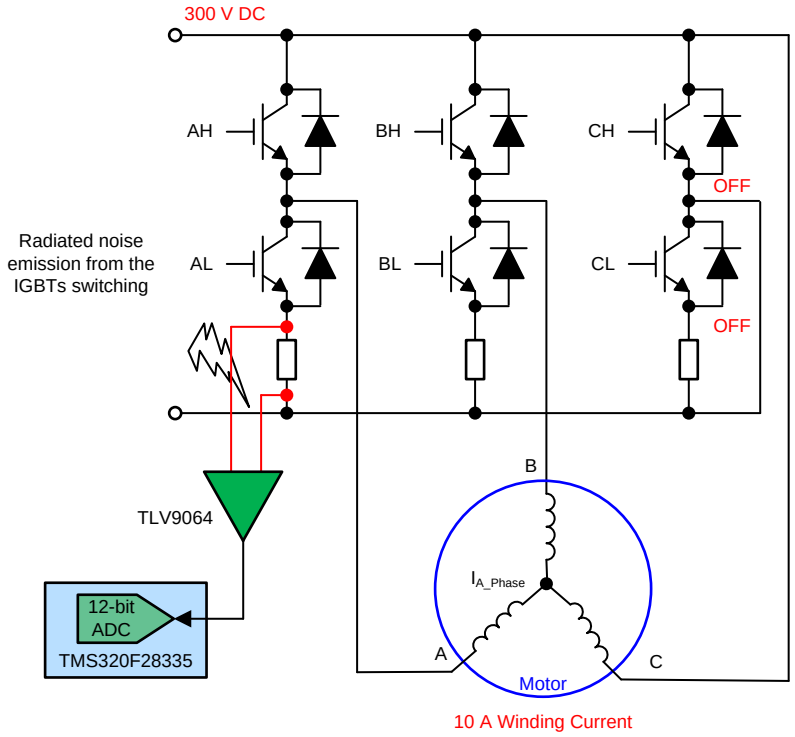
Figure 35. Relative Error [%] in Inverter Leg Current Measurement



3.2.1.4 Noise Rejection of Current Sense Amplifier

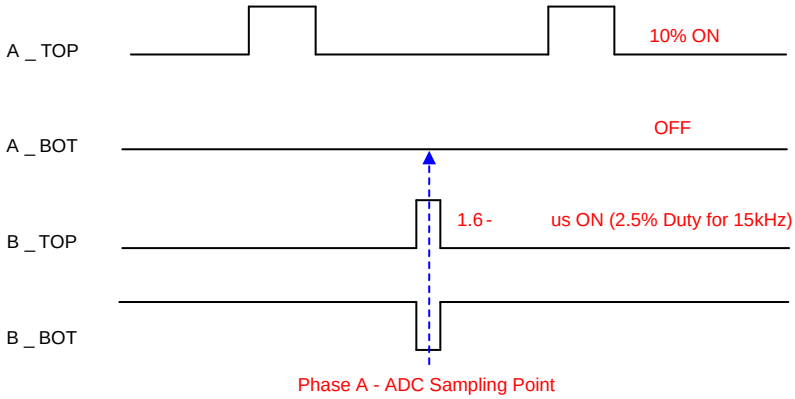
With the purpose of understanding the noise rejection by current sense amplifier, the test is done as per the set up shown inFigure 36 .

Figure 36. Test Setup for Noise Rejection of Current Sense Amplifier



The DC bus voltage is set at 300 V, and the winding current is at 10 A. PWM is applied to Phase A and Phase B. Phase C is left open. Figure 37 shows the PWM signals, the PWM signal driving the high-side IGBT for Phase A has 10% duty, and the low-side IGBT is kept off. The PWM signal driving high-side IGBT for Phase B has 2.5% duty, and the frequency is set at 15 kHz.

Figure 37. PWM Signals for Phase A and Phase B



During the testing the ADC of the MCU samples the current sense amplifier output at the middle of phase A high side off period, which is falling near the IGBT switching of phase B, meaning the noise generated during the IGBT switching will couple to the current sense amplifier circuit. The radiated noise emission signal is captured by a floating probe close to the input path of the current sense amplifier, which Figure 38 shows.

Figure 38. Floating Probe Close to Input Path of the Amplifier

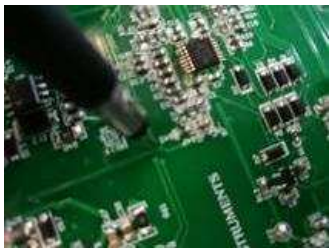


Figure 39 shows the test results of noise effect on current sense amplifier, the floating probe near amplifier input shows DC shift and noise oscillation due to IGBTs switching. Noise is also observed on the amplifier output.

Figure 39. Noise Effect on Current Sense Amplifier

The ADC converts such 500 samples over 500 PWM cycles and stores them in the MCU data buffer. The data is analyzed to understand the effect of IGBT noise coupling on the current sense amplifier output.Figure 40 and Figure 41 show the data analysis from ADC data in MCU. Figure 40 shows the maximum error is 12 codes, which corresponds to 10-mV voltage error or 0.08-A error in measured current. Figure 41 shows the error distribution is 8 codes at 96.2% of 500 points. It turned out the noise observed on current sense amplifier output is actually due to probe pick up, and the output of the amplifier is quite stable even with IGBTs switching near by.

Figure 40. ADC Sampling Accuracy

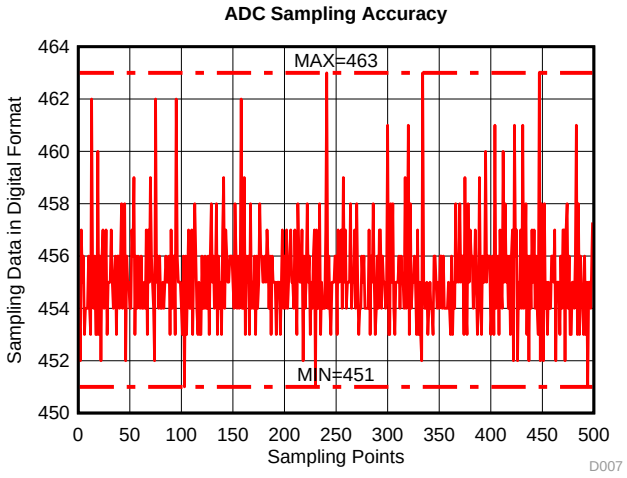
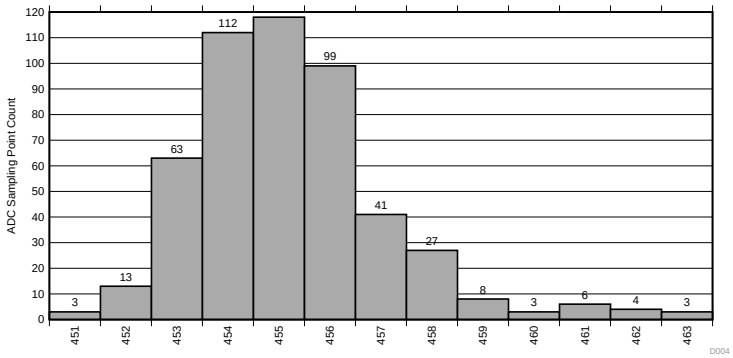


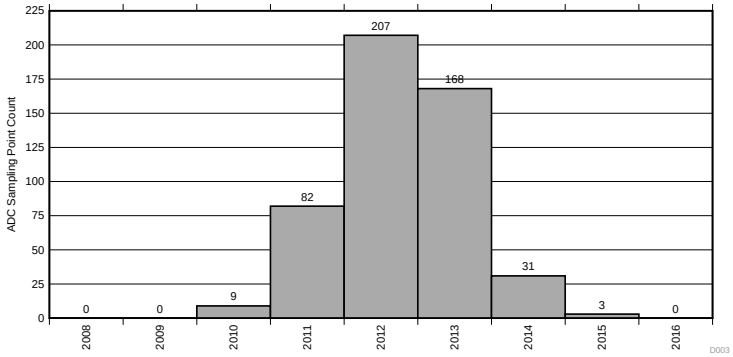
Figure 41. ADC Sampling Points Distribution



The integrated RFI and EMI filters at the input of the amplifier helps to reject the high-frequency noise coupled to the input of amplifier by nearby IGBT switching. A good PSRR of 7 µV/V, high CMRR and high stability of TLV9064 also contributes to the noise rejection on the input pins or output pins or the power supply.

With the purpose of understanding the effect of error codes in the ADC result, due to the ADC reference voltage, a LDO with voltage ripple less than 5 mV is used to replace the DC/DC. Figure 42 shows the ADC result distribution.

Figure 42. ADC Sampling Points Distribution with LDO as Power Supply



The error variation when using a LDO as the power supply is 4 codes, which means the error of the output of the amplifier is effected by the ripple in the ADC reference which is divided from 3.3-V power supply. If the designer need more accurate ADC data, it is recommended to use a LC filter at the ADC reference voltage input.

3.2.1.5 Overcurrent Protection in Hardware

As explained in Section 2.2.3, the inverter leg OCP is implemented by using one channel of the TLV9064 configured as a comparator and TLV1701 comparator.

Figure 43 shows the overcurrent detection for the positive inverter leg current (positive inverter leg current refers to negative winding current). Figure 44 shows the response time for overcurrent detection and the response time is approximately 1.5 µs.

Figure 43. Overcurrent Detection for Positive Current at 1.0 ms/div

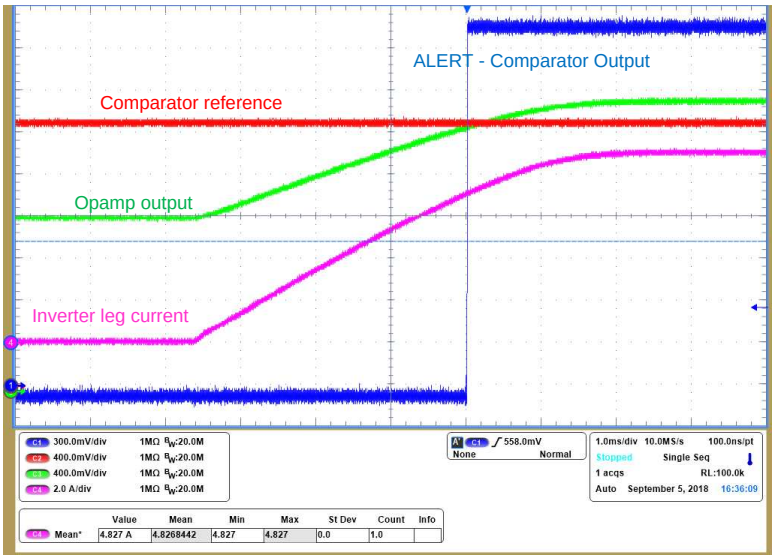


Figure 44. Overcurrent Detection for Positive Current at 2.0 µs/div

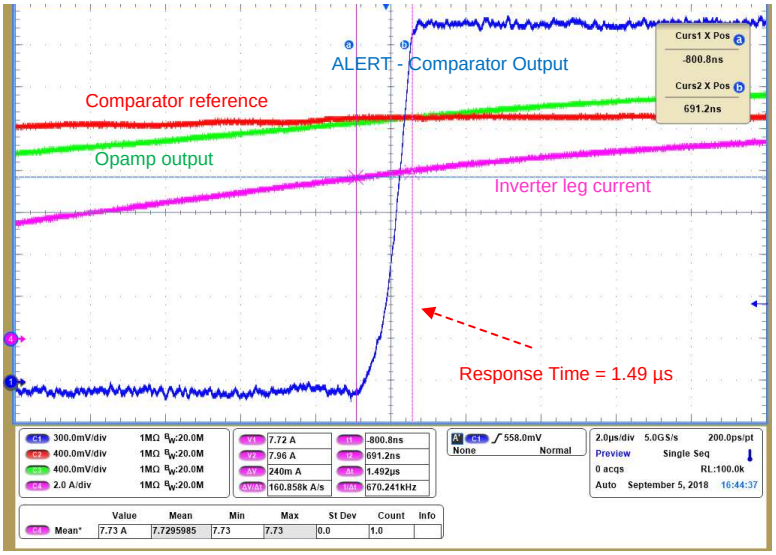


Figure 45 shows the overcurrent detection for negative inverter leg current (positive inverter leg current refers to negative winding current). Figure 46 shows the response time for overcurrent detection and the response time is approximately 1.4 µs.

Figure 45. Overcurrent Detection for Negative Current at 1.0 ms/div

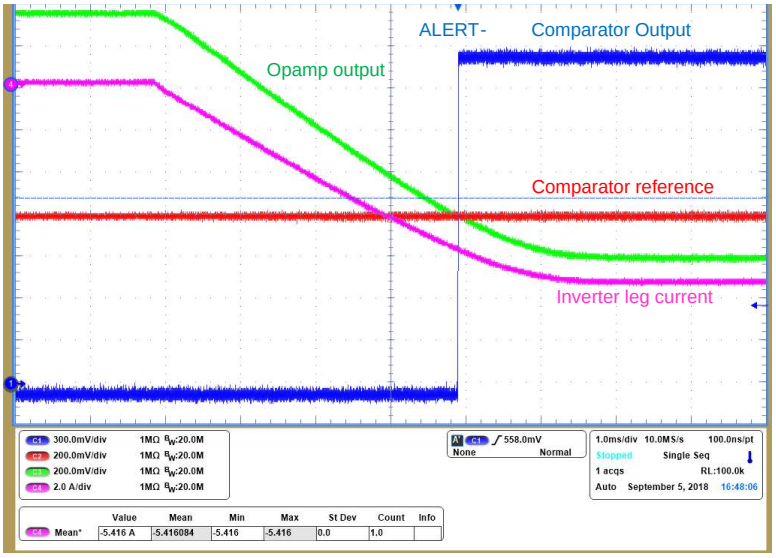


Figure 46. Overcurrent Detection for Negative Current at 2.0 ms/div

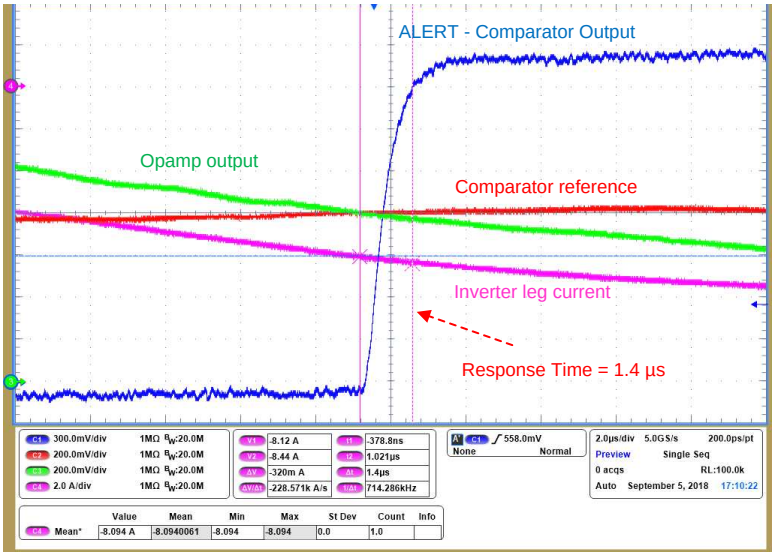


Figure 47 shows the overcurrent protection in hardware, which is achieved by pulling up the active-low enable pin of line driver SN74AHC367. Figure 48 shows the response time from overcurrent detection comparator output to the IGBT gate turn off.

Figure 47. Overcurrent Protection in Hardware

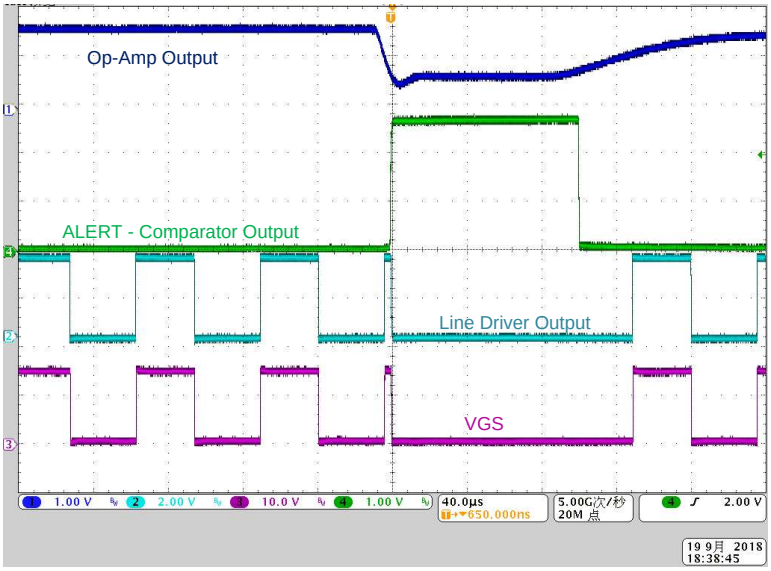
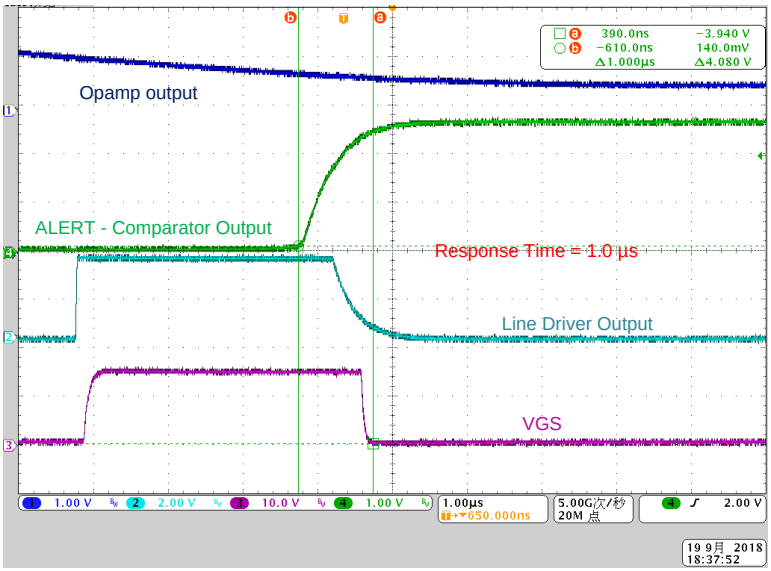


Figure 48. Response Time of Overcurrent Protection in Hardware



The response time of the overcurrent detection is less than 1.0 µs in hardware protection, which is fast enough to protect an IGBT (IGBTs typically have more than a 5-µs short-circuit capability). The lowest propagation delay of gate driver and line driver enables the fast turnoff of the IGBTs during an overcurrent event.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010023.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010023.

4.3 PCB Layout Recommendations

Use the following layout recommendations when designing the current sense layout.

- Use Kelvin connection for the sense resistor placement and sense voltage routing.
- The sense voltage signal connection to the amplifier must be connected using a symmetric differential trace routing.
- The recommended placement of the low-pass RC filter at the output of the amplifier is near the MCU.
- The recommended placement of the current sense amplifier input filter is close to the op amp.
- The creepage distance used for IGBT and gate driver layout is set within 4 mm.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010023.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010023.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010023.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010023.

5 Software Files

To download the software files, see the design files at MotorWare™ Software.

6 Related Documentation

1. Texas Instruments, *Current Sensing With < 1-µs Settling for 1-, 2-, and 3-Shunt FOC Inverter Reference Design*
2. Texas Instruments, *Space-Vector PWM With TMS320C24x/F24x Using Hardware and Software Determined Switching Patterns Application Report*
3. Texas Instruments, *InstaSPIN-FOC™ and InstaSPINMOTION™ User's Guide*

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