Design Guide: TIDA-010203

4-kW, Single-Phase Totem Pole PFC Reference Design With C2000 and GaN

Description

This reference design is a 4-kW CCM totem pole PFC using the F280049 or F280025 controlCARD and LMG342x EVM board. This design demonstrates a cost-effective and robust PFC controller, which avoids isolated current sense by putting the ground of the controller on the middle of the MOSFET leg. The benefits from non-isolation, AC current sense can be implemented with the OPA607 high-speed amplifier for reliable overcurrent protection. In this design, efficiency, thermal image, AC drop, lighting surge, and EMI CE are fully validated. The test data in this reference design illustrates the maturity of the totem-pole PFC with C2000 and GaN, and is a good platform for the PFC stage design of high-efficiency products.

Features

- Maximum power: 4000 W at 200 V–277 V nominal
- Peak efficiency: ≥ 99.1%; power factor: 0.999
- Cost-effective current sensing by non-isolated high-speed amplifier
- Single phase CCM totem pole with TI Gen2 daughter card
- Digital controlled with TMS320F28004x or TMS320F28002x control card
- FSI communication interface included

Applications

- Merchant network and server PSU
- Merchant telecom rectifiers
- Air conditioner outdoor unit

Resources

TIDA-010203	Design Folder
LMG3422R030	Product Folder
TMS320F280025C	Product Folder
OPA607	Product Folder
UCC21222	Product Folder

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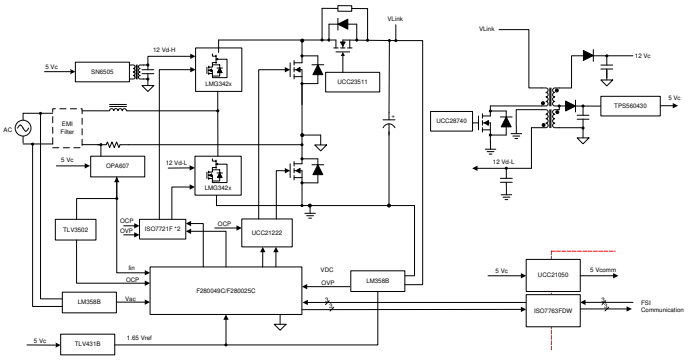
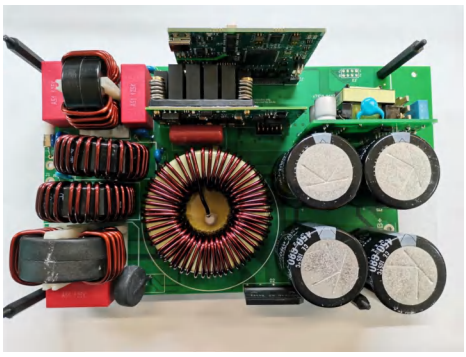




1 System Description

This reference demonstrates a 4-kW, single-phase CCM totem-pole bridgeless PFC with TI GaN and C2000, with non-isolated current sensing, isolated driving, differential voltage sensing, and an isolated FSI communication port.

Table 1-1. Key System Specifications

Parameter	Specification
Input voltage	200 V–277 V
Input current	20 A_{RMS} maximum
Output voltage	400 VDC
Output current	10 A maximum
Power rating	4 kW at single phase 200 V_{RMS}
Current THD	< 2% at 230 V_{RMS} rated load
PFC inductor	480 µH
Output capacitance	680 µF × 4

2 System Overview

This system uses the TI C2000 controlCARD TMDSCNCD280049C (TMDSCNCD280025C compatible) as the controller and the TI GaN EVM board LMG3422EVM-043 as the fast switching leg.

This design moved the C2000 reference ground to the middle point of the MOSFET leg so it can use the OPA607 non-isolated, high-speed amplifier to sense the inductor current. With this benefit, the isolated drive UCC21222 must be changed for the low-speed MOSFET leg, and the LM358B amplifier is used for DC voltage sense. The MCU ground change does not affect GaN drive, as it is generally expected to have isolators to stop the switching noise transferring from the GaN FET to the controller side. On the GaN EVM board, the LMG3422R030 is isolated by the ISO7741F and powered by the SN6505 drive isolated DC/DC.

Instead of a bulky relay, this design uses a MOSFET driven by the UCC23511 for inrush protection, which saves on PCB space.

This design has a flyback board with the UCC28740 to generate two isolated 12 V outputs; one is for the control circuits and the other 12 V is for the low-side MOSFET drive. These two 12 V outputs are designed with 500-V isolation ability with each other, which could withstand the DC link voltage when the high-side MOSFET is turned on. The 12 V output for control circuits generates the 5-V power, with the TPS650430 buck controller for MCU card and GaN card, .

Additionally, this design includes an FSI communication port with the ISO7763 isolator, powered by the UCC21050. The FSI communication allows faster communications and firmware updates.

2.1 Block Diagram

Figure 2-1 shows the block diagram and key TI parts in this design.

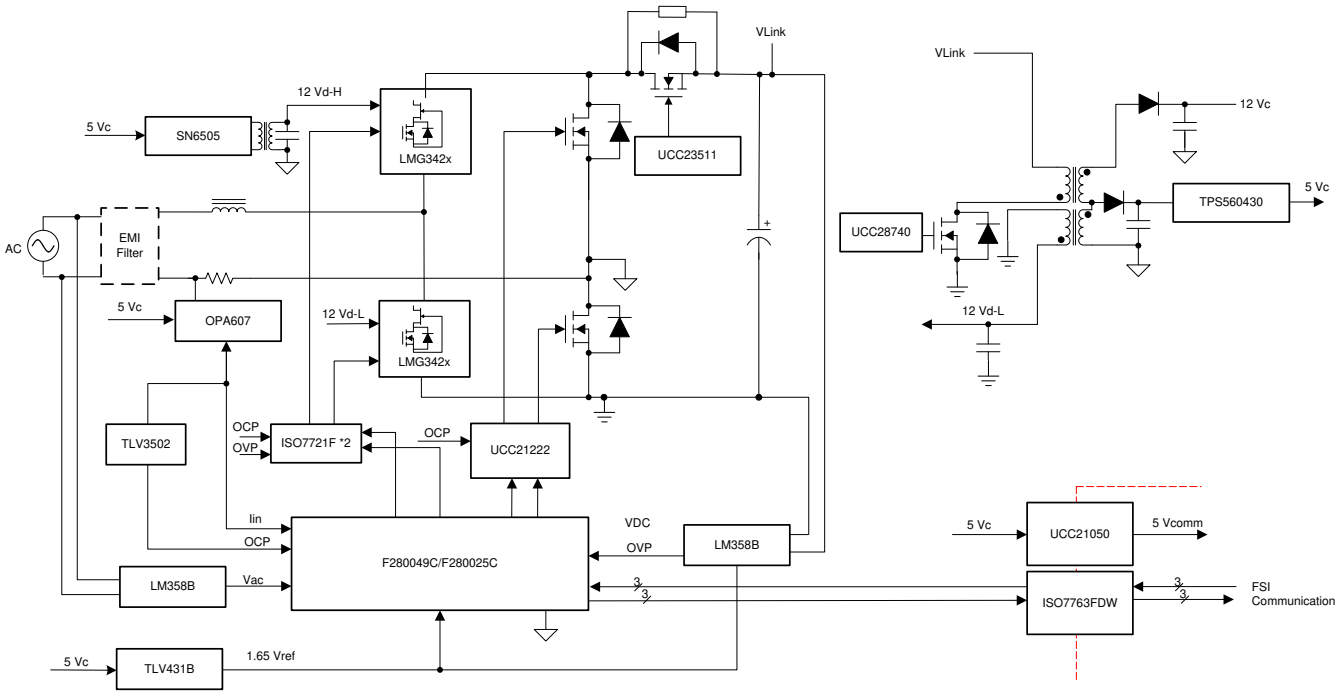


Figure 2-1. System Block Diagram

The following EVMs are used to achieve reference design operation as documented in this guide:

1. F280049C controlCARD Evaluation Module: TMDSCNCD280049C
2. LMG342x GaN EVM board: LMG3422EVM-043

2.2 Design Considerations

The digital power design includes power stage and control stage. The power stage design in this design is similar to all other boost PFC designs, similar to the design process of the *1-kW, 80 Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design (TIDA-010062)*. Figure 2-2 shows the power stage design parameters.

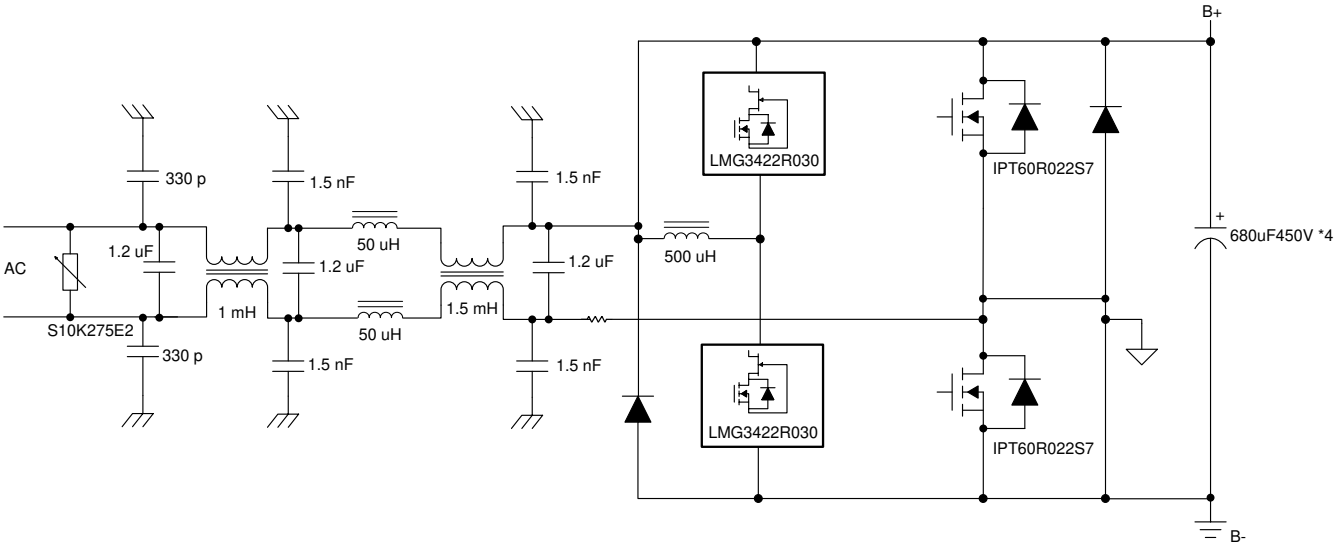


Figure 2-2. Power Stage Design Parameters

The following key considerations apply to control stage design:

- Input current sensing

  In totem-pole PFCs, most AC current sense uses isolated current sensor, such as a Hall sensor, isolated amplifier, and current transformer. In common sense, analog isolation is more challenging than digital isolation. For example, compared with a non-isolated amplifier, a Hall sensor and isolated amplifier have relatively low bandwidth and larger propagation delay. But, dealing with the PWM drive isolation is much easier. In this design, the ground of the MCU was changed to the middle point of the MOSFET leg. This small change allows use of the shunt resistor to sense the current with a non-isolated amplifier.

  The OPA607 op amp with 50-MHz GBW is selected, this high-speed amplifier helps on current loop control and overcurrent protection on the MOSFET. The input current sense ratio is set on 0.033 V/A, and the sense range is –48 A to +48 A.
- DC link voltage sensing

  After the ground of the controller is set at the middle of the MOSFET leg, the DC link has a high common-mode voltage relative to the controller ground. This common-mode voltage must be well suppressed with a resistor divider, and the CMRR of the amplifier is used to eliminate this disturbance.

  One channel of the LM358B, CMRR 20 µV/V, is used to sense the DC link voltage with differential amplifying circuits. The DC link voltage sense ratio is set to 0.0072, and the sensing range is set to 0 V to approximately 462 V.
- Input AC voltage sensing

  Because the AC line voltage is negative in a half cycle, the 0-V input must be offset to 1.65-V output. Another channel of the LM358B is used to sense the AC line voltage, which performs the scale and introduces 1.65-V offset at the same time. The AC voltage sensing ratio is set to 0.0037, and the sensing range is set to –471 V to +471 V.
- Input OCP (overcurrent protection)

  Input OCP can be realized by the CMPSS module integrated in the C2000, but an extra hardware OCP for the MOSFET leg is redundant in this design. Because the input current is bidirectional, the protection

needs a dual-channel comparator. This design uses the TLV3502 to set both direction current protection with hysteresis loop. The protection threshold is set at –48 A and +50 A, with hysteresis.

- DC bus OVP (overvoltage protection)

  Because overvoltage of the DC bus is very dangerous and causes damage to property, a hardware OVP is included in this reference. This is strongly recommended before the firmware OVP is verified functionally good. This hardware OVP is easily implemented with one channel of the LM358B, and the OVP threshold is set on 445 V with 15-V hysteresis.
- GaN FET driving

  This design uses the LMG3422EVM-043 GaN half bridge EVM as the switching leg. The EVM board includes two isolator ISO7741s and two SN6505 isolated DC/DC, for both high-side and low-side GaN FET. So the GaN bridge can be directly driven by the MCU.

  Note

  For the EVM board: LMG3422EVM-043 uses 5 V on the MCU side of the V_{CC} of the ISO7741. This is functionally workable with 3.3-V MCU logic, but needs to change to 3.3 V for matching on the logic level.
- MOSFET driving

  Because the ground of the controller is set at the middle of the MOSFET leg, the low-side MOSFET has –400 V when the high-side MOSFET turns on, a functional isolated driver is required in this situation. The UCC21225A with VLGA package can be used when PCB layout space is very limited, but in this design, the UCC21222 with SO-16 package is the most cost-effective choice. Both the UCC21222 and UCC21225A can realize interlock function using dead-time configuration.
- Inrush protection

  All PFC stages need to deal with the inrush current during AC power on. A mechanical relay and a resistor or PTC are often used to perform the current limitation. But, when the current is greater than 16 A, relay becomes very bulky and hard to choose. So, in this design, inrush relay is replaced by a MOSFET with isolated drive. Because of the MOSFET body diode, it cannot block the current from source to drain, and to avoid this, it must use two back-to-back MOSFETs, the inrush MOSFET is placed on the DC link side.

2.3 Highlighted Products

2.3.1 LMG342xR030

The LMG342xR030 GaN FET with integrated driver and protection enables designers to achieve new levels of power density and efficiency in power electronics systems.

The LMG342xR030 integrates a silicon driver that enables switching speed up to 150 V/ns. TI's integrated precision gate bias results in higher switching SOA compared to discrete silicon gate drivers. This integration, combined with our low inductance package, delivers clean switching and minimal ringing in hard-switching power supply topologies. Other features, including adjustable gate drive strength for EMI control, overtemperature, and robust overcurrent protection with fault indication, provide optimized BOM cost, board size, and footprint.

Advanced power management features include digital temperature reporting and TI's ideal diode mode. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which enables the system to optimally manage loading. Ideal diode mode maximizes efficiency by reducing third-quadrant losses by enabling adaptive dead-time control.

2.3.2 TMS320F28002x

The TMS320F28002x (F28002x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high-power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 100 MHz of signal processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Trigonometric Math Unit (TMU) and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

High-performance analog blocks are integrated on the F28002x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Fourteen PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to advanced multi-level power topologies.

2.3.3 OPA607

The OPAX607 is a decompensated (gain = 6 V/V stable), general-purpose complementary metal oxide semiconductor (CMOS) operational amplifier (op amp) that provides low noise of 3.8 nV/√Hz and a wide gain bandwidth of 50 MHz. The low noise and wide bandwidth of the OPAX607 make the device attractive for general-purpose applications that require a good balance between cost and performance. The high-impedance CMOS inputs make the OPAX607 an ideal amplifier to interface with sensors with large output impedance (for example, piezoelectric transducers).

The OPA607 features a power-down mode with a maximum quiescent current of less than 1 µA, making the device excellent for use in portable battery powered applications. The rail-to-rail output (RRO) of the OPA607 can swing up to 10 mV from the supply rails, enabling maximum dynamic range.

This op amp is optimized for low-voltage operation as low as 2.2 V (±1.1 V) and up to 5.5 V (±2.75 V), and is specified over the temperature range of –40°C to +125°C

2.3.4 UCC21222

The UCC21222 device is an isolated dual channel gate driver with programmable dead time. It is designed with 4-A peak-source and 6-A peak-sink current to drive power MOSFET, IGBT, and GaN transistors.

The UCC21222 device can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. Five-ns delay matching performance allows two outputs to be paralleled, doubling the drive strength for heavy load conditions without risk of internal shoot-through.

The input side is isolated from the two output drivers by a 3.0-kV RMS isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI).

Resistor programmable dead time gives the capability to adjust dead time for system constraints to improve efficiency and prevent output overlap. Other protection features include: Disable feature to shut down both outputs simultaneously when DIS is set high, integrated deglitch filter that rejects input transients shorter than 5-ns, and negative voltage handling for up to –2-V spikes for 200-ns on input and output pins. All supplies have UVLO protection.

3 Hardware, Testing Requirements, and Test Results

This section details the hardware and explains the different sections on the board and how to set them up for the experiments as outlined in this design guide.

3.1 Hardware Requirements

Daughter board

1. C2000 controlCARD Evaluation Module: TMDSCNCD280049C/ TMDSCNCD280025C
2. LMG342x GaN EVM board: LMG3422EVM-043

Equipment

1. Programmable AC source
2. Isolated high-voltage electrical DC load
3. 12V1A isolated DC source, ×2
4. Air cooling fan

3.2 Test Setup

This reference design includes a flyback stage which provides two 12 VDC with 600-V functional isolation for independent operation. But, during the firmware test process, the setup with an axillary power board is not expected, because no power is expected to exist on the DC bus when operating the firmware.

The following steps show the common setup with external V_{CC} power supply:

1. Remove or disconnect the flyback board, if it is assembled
2. Make sure C2000 and GaN board is well assembled
3. Connect 12VDC1 to '12Vc' and 'GND-c'; Connect another 12VDC2 to '12V-L' & 'B-'; (12VDC1 and 12VDC2 must have 500 VDC isolation ability to each other)
4. Connect the AC source cable to the input terminal, but do not power up
5. Connect the DC load to output terminal (pay **attention** for the DC **polarity**. And, the load **must be** isolated with grid and PE line)
6. Use forced-air cooling fan to cool the board
7. Insert power meter with current and voltage meter, before testing efficiency. (Make sure all voltage probes are near to the board side.)

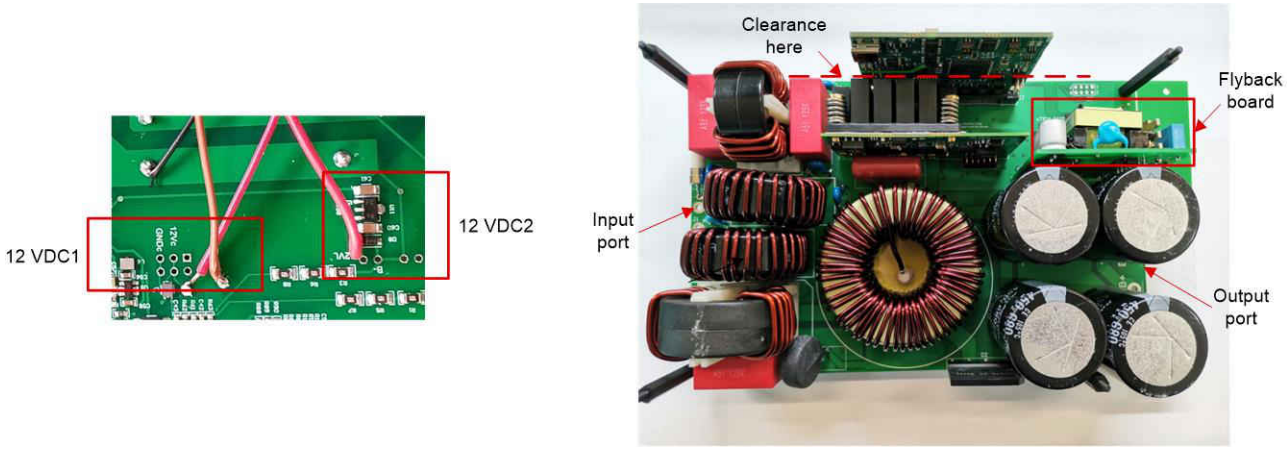


Figure 3-1. Board Setup

3.3 Test Results

3.3.1 Test Procedures

Figure 3-2 shows the EUT setup.

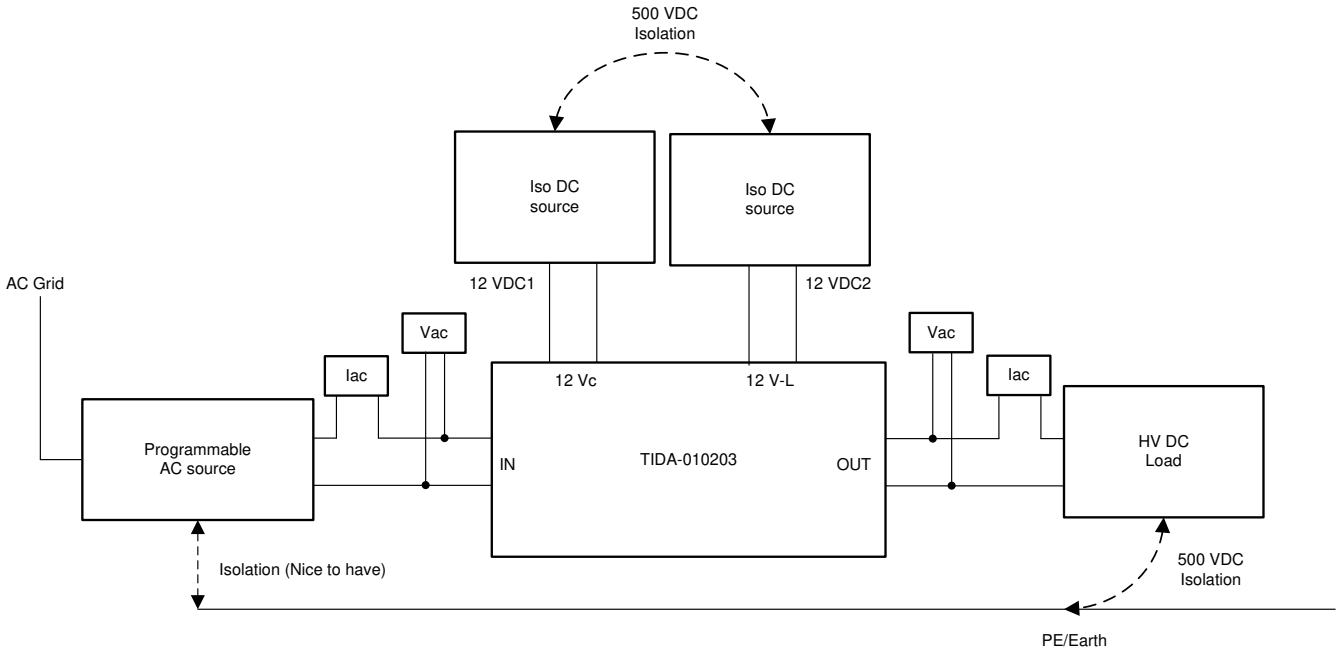


Figure 3-2. EUT Setup

Power on procedure:

1. Power on the FAN for cooling
2. Power for 12VDC_1, power consumption should be near 0.13 A
3. Power for 12VDC_2, power consumption should be smaller than 0.01 A
4. Set the DC load to CC mode, 0.5 A, load on
5. Power on the AC source (200 VAC–277 VAC), will see DC output gradually increase to 400 VDC
6. Adjust DC load between 0–10A, for test

Power off procedure:

1. Reduce the load to 1A
2. Power off the AC input
3. Power off the 12VDC_1 and 12VDC_2
4. Turn off the cooling FAN

3.3.2 Performance Data: Efficiency, iTHD, and Power Factor

Table 3-1 shows the efficiency, iTHD, and power factor data with 230-V input, without including the control and driving power loss. Figure 3-3 shows the related 230-V efficiency curve.

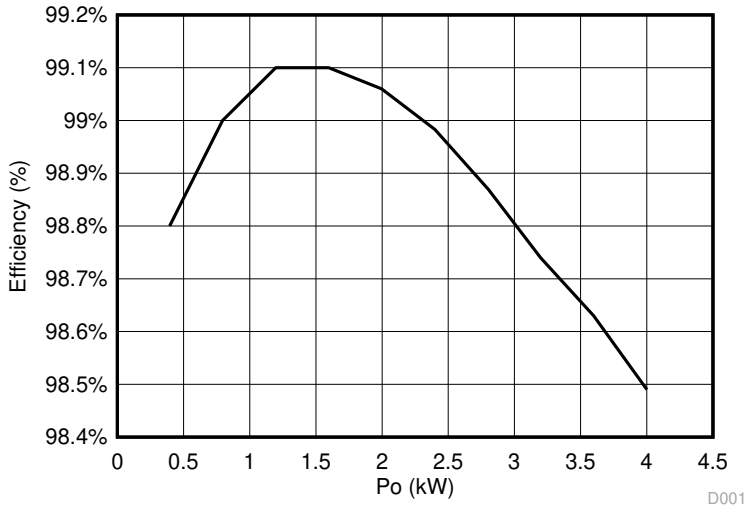


Figure 3-3. Efficiency Curve, 230 V 175

Table 3-1. Efficiency, iTHD, and Power Factor Data With 230-V Input

Vin /Vac	Iin /Aac	Pin /kW	Vout /V	Iout /A	Pout /kW	Eff.	iTHD	PF
228.3	1.924	0.4005	401.17	0.984	0.3946	98.80%	13.65%	0.984
226.11	3.651	0.8021	401.22	1.982	0.7951	99.00%	7.53%	0.996
226.89	5.37	1.2071	401.19	2.982	1.1964	99.10%	5.56%	0.998
226.06	7.158	1.6109	401.21	3.979	1.5963	99.10%	4.20%	0.999
225.71	8.956	2.0158	401.11	4.978	1.9966	99.06%	3.18%	0.999
224.82	10.802	2.4236	401.26	5.978	2.3986	98.98%	3.02%	0.999
223.2	12.711	2.8329	401.28	6.98	2.8009	98.87%	2.75%	0.999
222.89	14.545	3.238	401.28	7.967	3.1968	98.74%	2.49%	0.999
222.23	16.438	3.649	401.34	8.968	3.599	98.63%	2.22%	0.999
221.38	18.37	4.062	401.12	9.967	4.0008	98.49%	2.10%	0.999

Figure 3-4 shows the related 200-V and 277-V efficiency curves.

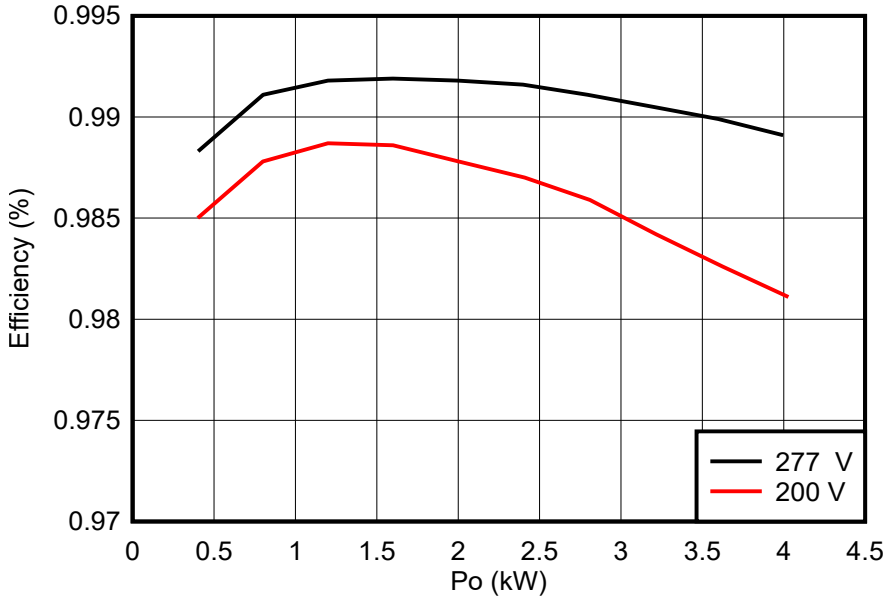


Figure 3-4. Efficiency Curve, 200 V and 277 V

Table 3-2 and Table 3-3 show the efficiency with 200-V and 277-V input, respectively, without including the control and driving power.

Table 3-2. Efficiency With 200-V Input

Pin/kW	V_{OUT}/V	I_{OUT}/A	P_{OUT}/kW	Efficiency
0.4006	396.12	0.996163	0.3946	98.50%
0.8004	396.14	1.995759	0.7906	98.78%
1.2002	396.16	2.995254	1.1866	98.87%
1.6008	396.16	3.994851	1.5826	98.86%
2.0029	396.16	4.994194	1.9785	98.78%
2.4093	396.27	6.000959	2.378	98.70%
2.8091	396.25	6.989022	2.7694	98.59%
3.2165	396.27	7.988745	3.1657	98.42%
3.6249	396.27	8.988568	3.5619	98.26%
4.0285	396.25	9.974763	3.9525	98.11%

Table 3-3. Efficiency With 277-V Input

Pin/kW	V_{OUT}/V	I_{OUT}/A	P_{OUT}/kW	Efficiency
0.4028	396.2	1.004796	0.3981	98.83%
0.8013	396.21	2.004493	0.7942	99.11%
1.2	396.2	3.003786	1.1901	99.18%
1.5991	396.22	4.003331	1.5862	99.19%
1.9984	396.2	5.002776	1.9821	99.18%
2.3983	396.18	6.002575	2.3781	99.16%
2.7949	396.22	6.991066	2.77	99.11%
3.1961	396.22	7.989753	3.1657	99.05%
3.5982	395.22	9.012449	3.5619	98.99%
3.9961	396.21	9.976275	3.9527	98.91%

3.3.3 Functional Waveforms

3.3.3.1 Current Sensing and Protection

Figure 3-5, Figure 3-6, and Figure 3-7 show the OPA607 current-sensing waveforms with 100 kHz, 500 kHz, and 1 MHz, respectively. The 220-ns phase delay, intentionally introduced to filter high-frequency noise, can be optimized with system requisitions.

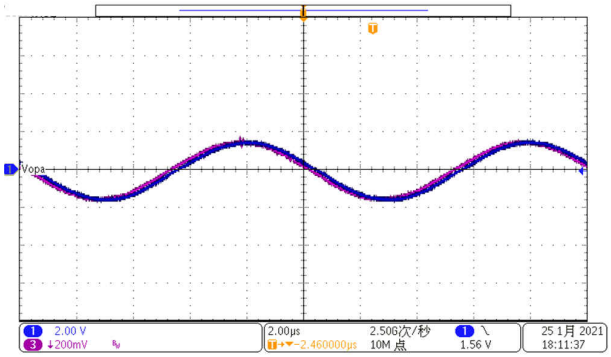


Figure 3-5. 100-kHz Waveform

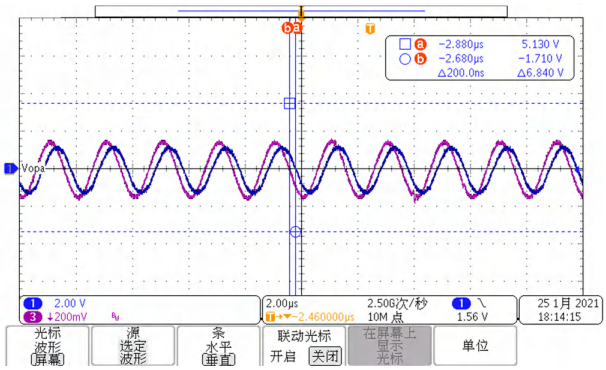


Figure 3-6. 500-kHz Waveform

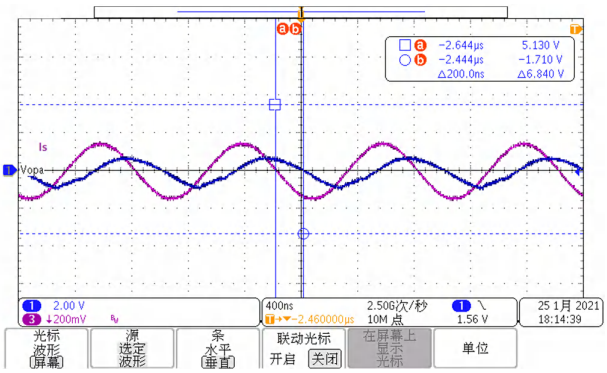


Figure 3-7. 1-MHz Waveform

With the OPA607 amplifier and TLV3502 comparator, overcurrent protection for MOSFET response is validated as in Figure 3-8 shows the negative direction OCP response time and Figure 3-9 shows the positive direction OCP response time.

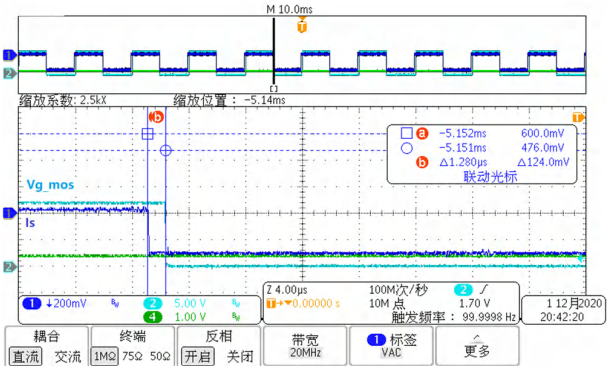


Figure 3-8. Negative OCP Action

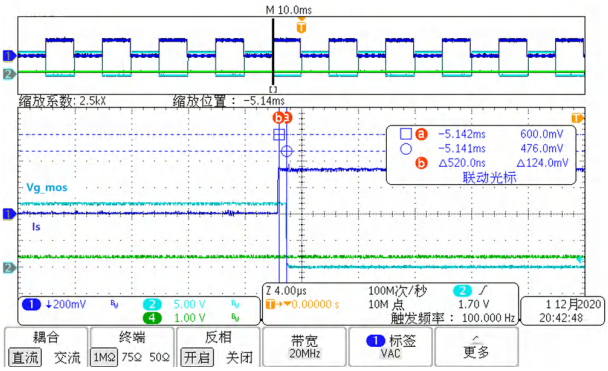


Figure 3-9. Positive OCP Action

3.3.3.2 Power Stage Start-Up and Input Waveforms

Figure 3-10 shows the start-up waveform with light load.

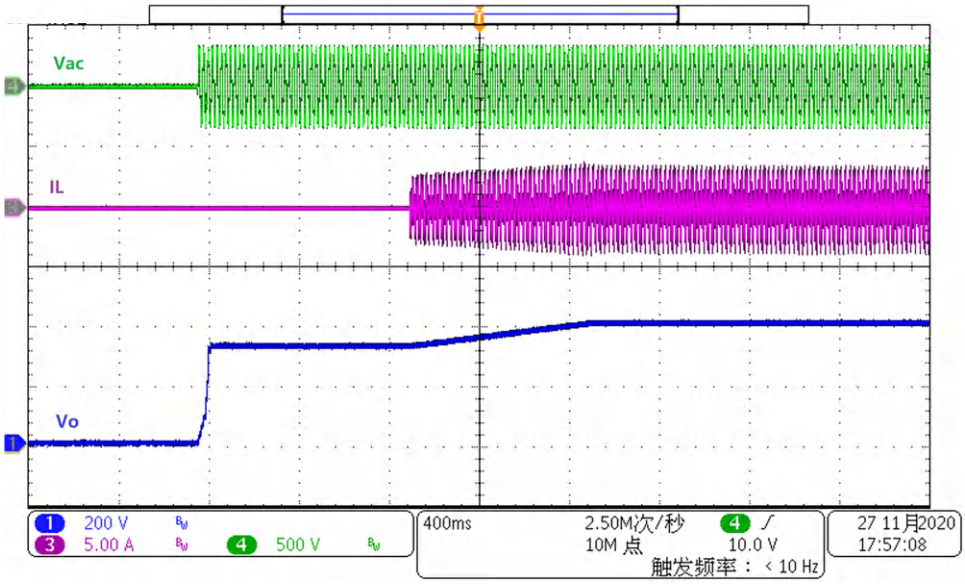


Figure 3-10. Start-Up Waveform With Light Load

Figure 3-11 shows the input current and voltage waveform under 200-V input and 4-kW load conditions.

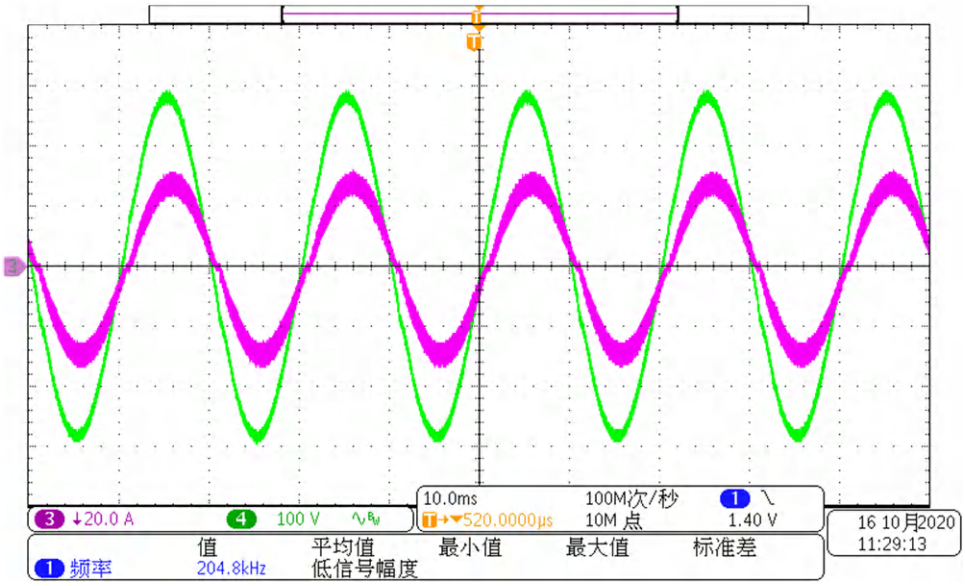


Figure 3-11. Input Current and Voltage Waveform, 200-V Input and 4-kW Load

Figure 3-12 shows the input current and voltage waveform under square AC input.

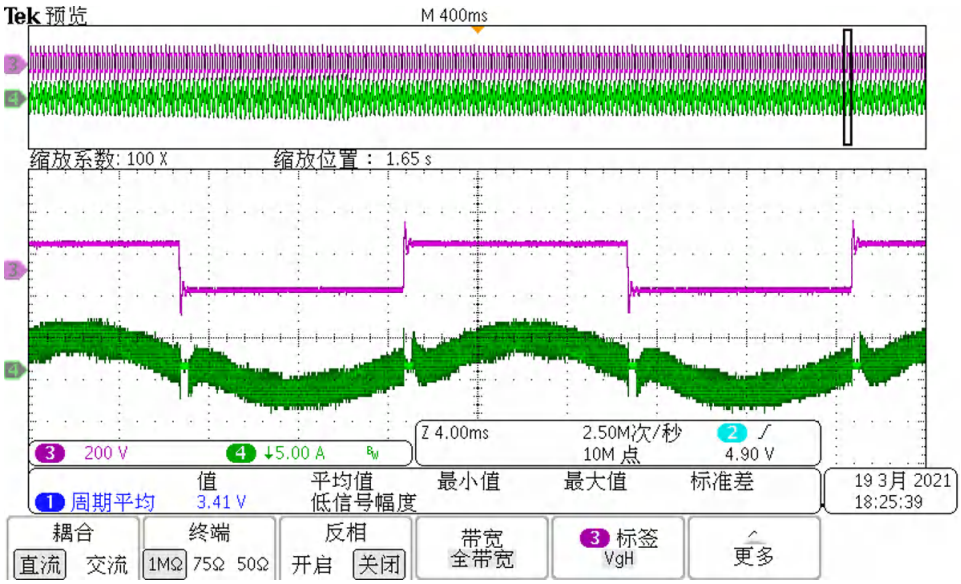


Figure 3-12. Input Current and Voltage Waveform, Under 230-V Square AC Input

3.3.3.3 AC Drop Test

In this design, the power stage was tested acting under AC 45°C drop with 2.8-kW load conditions. The test results show that control logic is not disturbed by AC distortion. The results are illustrated in the waveform in Figure 3-13.

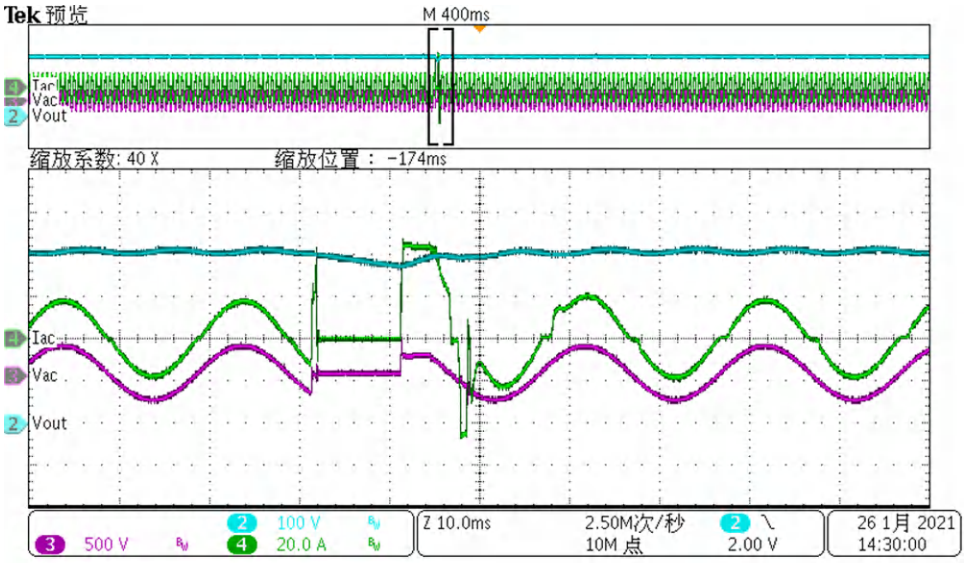


Figure 3-13. AC Drop Test

3.3.3.4 Surge Test

A lighting surge test between ACL and ACN was performed on this design. Figure 3-14 shows the 3-kV line to neutral surge voltage waveform when EUT is not connected.

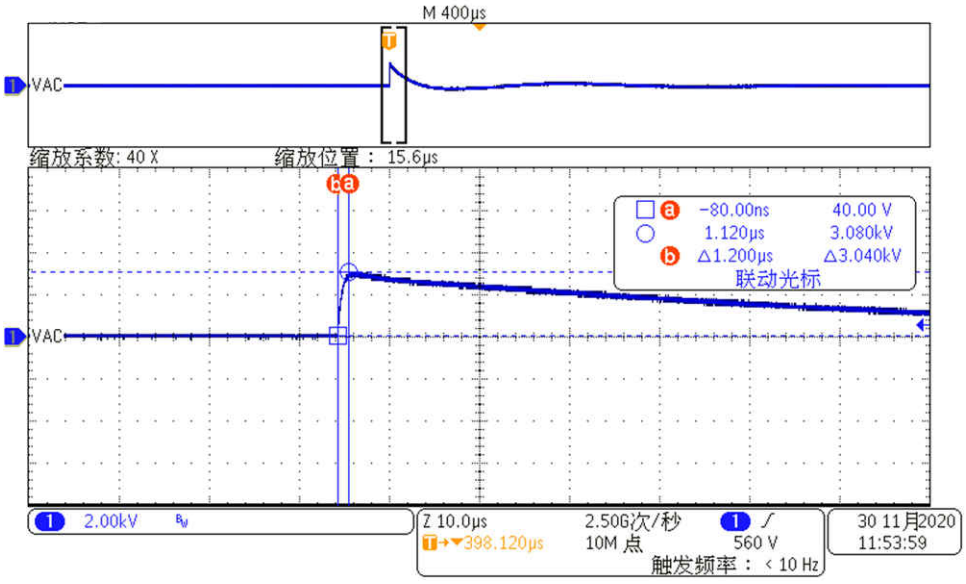


Figure 3-14. Surge Voltage Waveform

With this surge waveform, the input current and the PFC choke current which is same with the current flow through GaN FET was tested. The result shows the surge current is fully bypassed by the inrush diodes clearly, and no risk to GaN FET (see Figure 3-15).

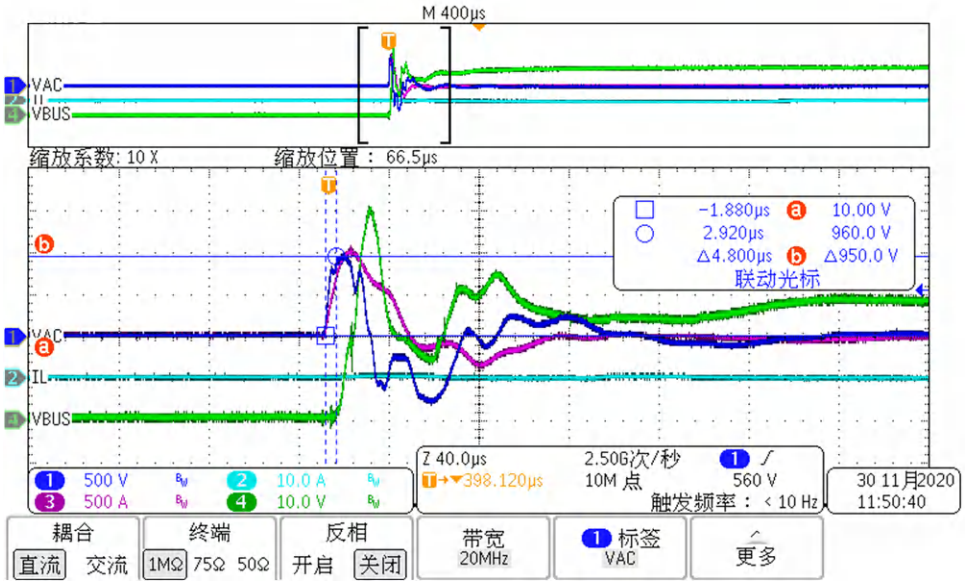


Figure 3-15. GaN FET, Choke Current in Surge Test

The surge current flow through MOSFET is a threat. As the test waveform in Figure 3-16 shows, the current under 3-kV surge exceeded the maximum peak current specification of the MOSFET.

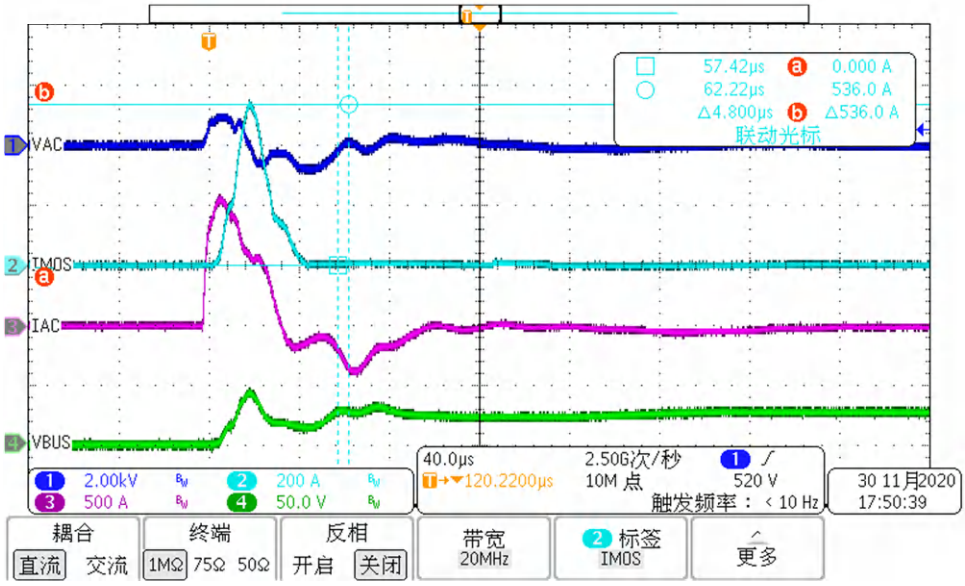


Figure 3-16. Surge Current Through MOSFET

Experiments show that the power stage is survived at the ±3-kV surge, but the MOSFET leg is broken at the –4-kV surge. Figure 3-17 and Figure 3-18 illustrate the surge waveforms under ±3-kV, respectively.

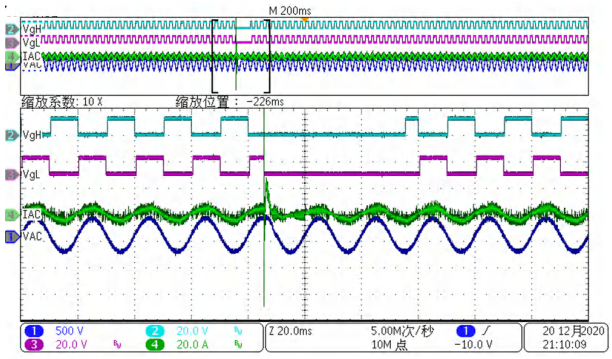


Figure 3-17. Surge Test at +3 kV, 90 Degrees

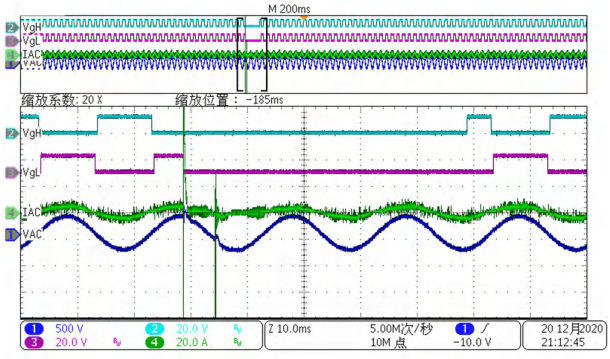
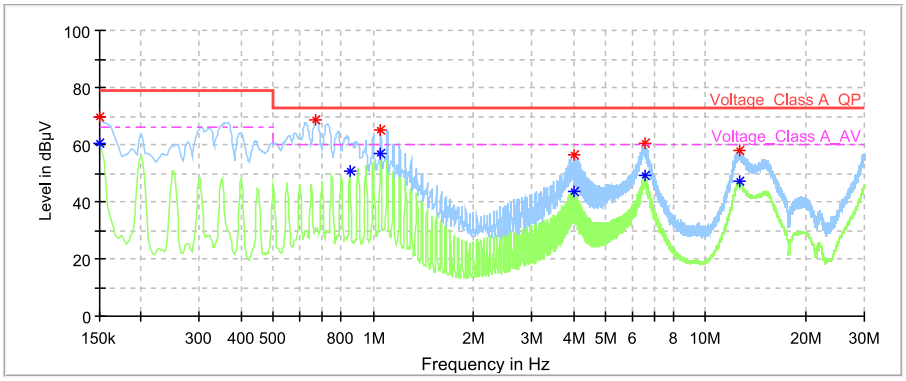


Figure 3-18. Surge Test at –3 kV, 90 Degrees

3.3.3.5 EMI Test

This reference design must deal with EMI CE, there is a 1.1-MHz and 5.5-MHz CM noise which can be suppressed with an shielding on PFC choke. Figure 3-19 shows the board CE test result after adding a shielding copper to the PFC choke at 230 VAC and 40-R resistance load.



Critical_Freqs

Frequency (MHz)	MaxPeak (dBµV)	Average (dBµV)	Limit (dBµV)	Margin (dB)	Meas. Time (ms)	Bandwidth (kHz)	Line	Filter	Corr. (dB)
0.15	69.96	---	79.00	9.04	---	---	L1	ON	19
0.15	---	60.41	66.00	5.59	---	---	L1	ON	19
0.67	68.81	---	73.00	4.19	---	---	L1	ON	19
0.85	---	50.89	60.00	9.11	---	---	L1	ON	19
1.05	---	56.79	60.00	3.21	---	---	L1	ON	19
1.05	65.17	---	73.00	7.83	---	---	L1	ON	19
4.00	---	43.76	60.00	16.24	---	---	L1	ON	19
4.00	56.56	---	73.00	16.44	---	---	L1	ON	19
6.55	---	49.22	60.00	10.78	---	---	L1	ON	19
6.55	60.42	---	73.00	12.58	---	---	L1	ON	19
12.59	---	47.15	60.00	12.85	---	---	L1	ON	19
12.67	57.99	---	73.00	15.01	---	---	L1	ON	19

Figure 3-19. EMI CE Result After Adding Shielding Copper with 230 Vac, 40-R Load

Note

This reference design must deal with EMI CE, there is a 1.1-MHz and 5.5-MHz CM noise which can be suppressed with a shielding on PFC choke. Figure 3-19 shows the board CE performance after adding a shielding copper to the PFC choke with 230 VAC and 40-R resistance load.

3.3.4 Thermal Test

Thermal performance is validated in this design. The test conditions are the following:

- 200 VAC with 4-kW load
- Cooling FAN: 27CFM, 24 V 2.64 W
- Thermal balanced after 10 minutes

Figure 3-20 illustrates the test results.

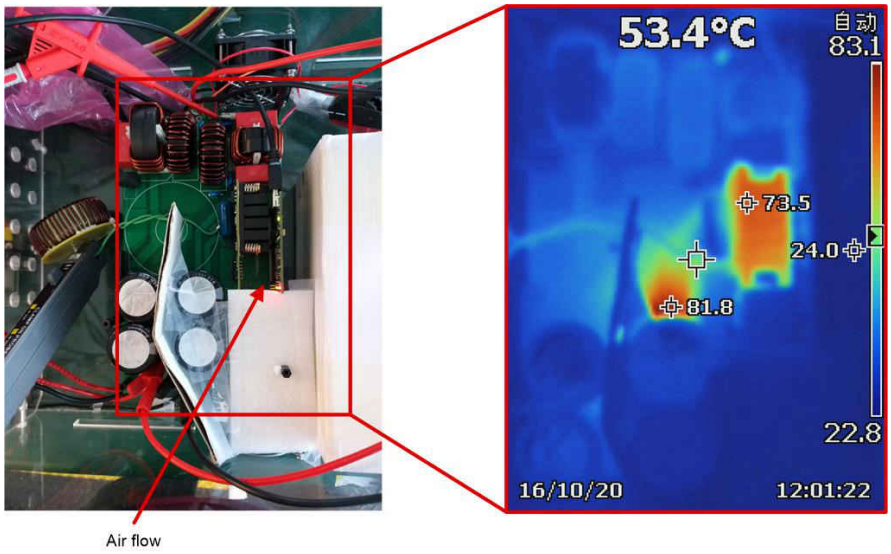


Figure 3-20. Thermal Performance Test

3.3.5 GaN FET Switching Waveform

Figure 3-21 shows the LMG3422R030 GaN FET switching waveform. This waveform shows 100 V/ns slew rate with very small under shoot during hard switch when turning on.

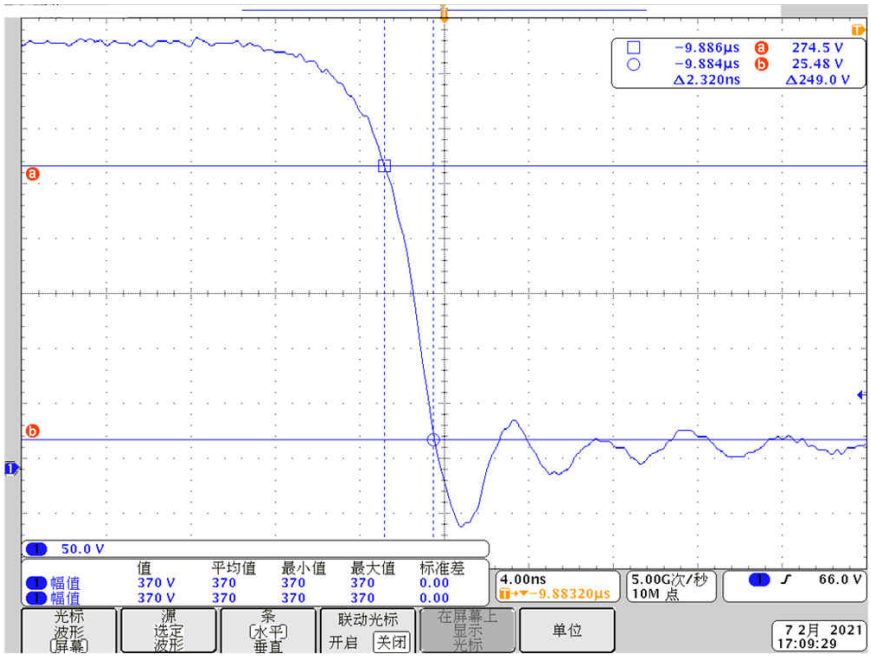


Figure 3-21. LMG3422R030 Switching Waveform

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010203.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010203.

4.2 Documentation Support

1. Texas Instruments, *1-kW, 80 Plus Titanium, GaN CCM Totem-Pole Bridgeless PFC and Half-Bridge LLC Reference Design*
2. Texas Instruments, *Bidirectional Interleaved CCM Totem Pole Bridgeless PFC Reference Design Using C2000™ MCU Design Guide*
3. Texas Instruments, *LMG342XEVM-04X User Guide*
4. Texas Instruments, *LMG342xR030 600-V 30-mΩ GaN FET with Integrated Driver, Protection, and Temperature Reporting Data Sheet*
5. Texas Instruments, *TMS320F28004x Microcontrollers Data Sheet*
6. Texas Instruments, *TMS320F28004x Real-Time Microcontrollers Technical Reference Manual*
7. Texas Instruments, *Piccolo F280049 controlCARD Information Guide*

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

DESHENG GUO is a System Application Engineer at Texas Instruments, where he is responsible for developing power solutions as part of the power delivery, industrial segment. Desheng earned his master degree from Harbin Institute of Technology with Power electronics in 2007, and worked in DELTA before joining TI.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (April 2023)	Page
• Updated Efficiency Curve, 200 V and 277 V graph	9

Changes from Revision * (April 2021) to Revision A (June 2022)	Page
• Updated *EMI CE Result After Adding Shielding Copper with 230 Vac, 40-R Load* image	16
• Added note	16

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