

IBIS Model Correlation Report

TPS65381-Q1

IBIS Version = 1.0

Report Version = 1.0

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[12/09/2013]

This correlation report is mainly subdivided into three important sections. Section A contains Datasheet correlation where one table contains C_{comp} and C_{package} information per model and Datasheet Capacitance value wherever available. This section also contains rise and fall ramp information wherever model contains V-T table. Section C contains IBIS vs. Spice correlation where IBIS waveforms simulated using HSPICE and spice netlist simulated using TISPIICE are compared graphically and waveforms for two settled periods, rising and falling edge with percentage of mismatch duly presented. The third section D gives the report revision history

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1 IBIS CORRELATION REPORT

Design ID: TPS65381-Q1

IBIS File Name and Version: tps65381-q1.ibs 1.0

Correlation Report Name and Version: TPS65381-Q1_Wipro_CorrRpt.pdf 1.0

IBIS Checklist name and version: TPS65381-Q1_Wipro_CheckList.xls 1.0

Available package types: HTSSOP

Marketing part Number(s): TPS65381QDAPRQ1

IBIS Zip File Name: tps65381-q1.zip, zip contains IBIS checklist, model & Correlation report

Date: Dec 9, 2013

Datasheet Title: Multi-Rail Power Supply for Microcontrollers in Safety-Critical Applications

Datasheet Revision: SLVSBC4 -MAY 2012

Datasheet Link: <http://focus.ti.com/lit/ds/symlink/tps65381-q1.pdf>

Contact IBIS modeling Support at elab_scm_ibis@list.ti.com for questions

2 IBIS MODEL CORRELATION

2.1 Datasheet Correlation

Compare c_comp with datasheet's input capacitance spec. Table provides data comparing c_comp for all models and all package combinations

Component Name = TPS65381-Q1							
Model Name		IBIS			Datasheet		
		Min(pF)	Typ(pF)	Max(pF)	Min(pF)	Typ(pF)	Max(pF)
diag_out_3p3	C.Comp	2.744	3.036	3.188	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	2.744	3.036	3.188	NA	NA	NA
diag_out_5p0	C.Comp	2.708	3.078	3.211	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	2.708	3.078	3.211	NA	NA	NA
endrv_nres_3p3	C.Comp	1.508	1.872	2.07	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	1.508	1.872	2.07	NA	NA	NA
endrv_nres_5p0	C.Comp	1.384	1.702	1.872	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	1.384	1.702	1.872	NA	NA	NA
error	C.Comp	0.3215	0.3865	0.3942	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	0.3215	0.3865	0.3942	NA	NA	NA
ncs_iovdd3p3	C.Comp	0.4988	0.5965	0.6512	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	0.4988	0.5965	0.6512	NA	NA	NA
ncs_iovdd5p0	C.Comp	0.7804	0.8028	0.8085	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	0.7804	0.8028	0.8085	NA	NA	NA
sclk_sdi	C.Comp	0.7804	0.8028	0.8085	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	0.7804	0.8028	0.8085	NA	NA	NA
sdo_3p3	C.Comp	1.597	1.636	1.694	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	1.597	1.636	1.694	NA	NA	NA
sdo_5p0	C.Comp	1.5	1.53	1.599	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	1.5	1.53	1.599	NA	NA	NA
sel_vdd3_vdd5	C.Comp	0.3208	0.3884	0.3942	NA	NA	NA
	C_package	NA	NA	NA	NA	NA	NA
	C_total	0.3208	0.3884	0.3942	NA	NA	NA

Table 1: C Comp IBIS vs DataSheet Table

If slew rate specifications (Rise slew and Fall slew) are available, table compares slew rates from SPICE simulation to that of Datasheet

Table 2: Slew Rate IBIS vs DataSheet Table

Model Name	Slew Rate	IBIS			Datasheet		
		Min	Typ	Max	Min	Typ	Max
diag_out_3p3	Rising(V/ns)	0.6594/141.6520	0.9089/90.4547	1.1208/52.1138	NA	NA	NA
diag_out_3p3	Falling(V/ns)	0.5708/113.1400	0.8726/75.0915	1.1316/45.5703	NA	NA	NA
diag_out_5p0	Rising(V/ns)	1.3326/111.7800	1.6633/68.5404	1.9100/41.4141	NA	NA	NA
diag_out_5p0	Falling(V/ns)	1.0594/83.8137	1.4728/54.1618	1.8007/34.1907	NA	NA	NA
endrv_nres_3p3	Rising(V/ns)	0.8236/15.1855	0.9258/12.0186	1.0609/9.2477	NA	NA	NA
endrv_nres_3p3	Falling(V/ns)	1.8788/1.4176	1.9617/0.7636	2.0411/0.4653	NA	NA	NA
endrv_nres_5p0	Rising(V/ns)	1.2602/13.9513	1.4027/11.0370	1.5929/8.4549	NA	NA	NA
endrv_nres_5p0	Falling(V/ns)	2.8745/1.5107	2.9723/0.8111	3.0647/0.4909	NA	NA	NA
sdo_3p3	Rising(V/ns)	0.5990/130.9190	0.9068/90.0516	1.1999/55.1625	NA	NA	NA
sdo_3p3	Falling(V/ns)	0.6285/122.8230	0.9841/84.1734	1.2850/50.5554	NA	NA	NA
sdo_5p0	Rising(V/ns)	1.2289/104.3460	1.6400/66.1691	1.9981/41.3176	NA	NA	NA
sdo_5p0	Falling(V/ns)	1.2957/102.2200	1.7442/63.5082	2.0985/38.8255	NA	NA	NA

2.2 Measurement Correlation

1. For Output or I/O model compare IOH and IOL data from measurements to those of IBIS model. Measurement data and simulations in SPICE are compared across Process, Voltage and Temperature corners. Any special conditions used for simulating or measurements need to be included.

Simulation Tools and version used:

Measurement conditions used:

Model simulation conditions used:

Measured IOH vs. IBIS IOH

Measured IOL vs. IBIS IOL

2. Compare IBIS C.comp with measured C.comp. Table provides comparison for all models and all package types.
Component Name

Table 3: C Comp IBIS vs DataSheet Table

Model Name		IBIS			Measurement		
		Min(pF)	Typ(pF)	Max(pF)	Min(pF)	Typ(pF)	Max(pF)
	C_Comp						
Input	C_Package						
	C_Total						
	C_Comp						
Output	C_Package						
	C_Total						

3. Clamp data if available, include for all models.

GND CLAMP data compared between IBIS and Silicon measurements. Sweep between -VCC to 2*VCC (if possible).

4. If slew rate measurements (Rise slew and Fall slew) are available, table compares slew rates from SPICE simulation to that of measurements.

Table 4: Slew Rate IBIS vs DataSheet Table

Model Name	Slew Rate	IBIS			Measurement		
		Min(pF)	Typ(pF)	Max(pF)	Min(pF)	Typ(pF)	Max(pF)
Output	Rising						
Output	Falling						

2.3 IBIS vs SPICE Correlation

2.3.1 diag_out_3p3

Model Type : 3-state

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 5: Corners of Validation

TISPICE engine used to generate and correlate IBIS models:

P.S: SPICE type could be Spectre, TISPICE, TISPICED, HSPICE, HSPICED

Generation:

TISPICE

Correlation

SPICE Netlist Simulation : TISPICE

IBIS Model Simulation : HSPICE

For all buffers correlate V-T transient simulations using IBIS(B-element) in HSPICED and SPICE netlist to ensure correlation. Include screen shot of test setup used for correlation. SimDE test setup with recommended load conditions may be used.

- Use node naming convention of IBIS_<corner> and SPICE_<corner>.
- Run simulation for all corner cases and maximum allowable speed grade, if multiple speed grades or drive strengths are allowed, please include separate correlation waveforms for each case. Include waveforms here. Re-use C.1.i and C.1.ii as needed for multiple buffers and or configurations. Include any correlation metrics if available

Test Frequency: 4MHz

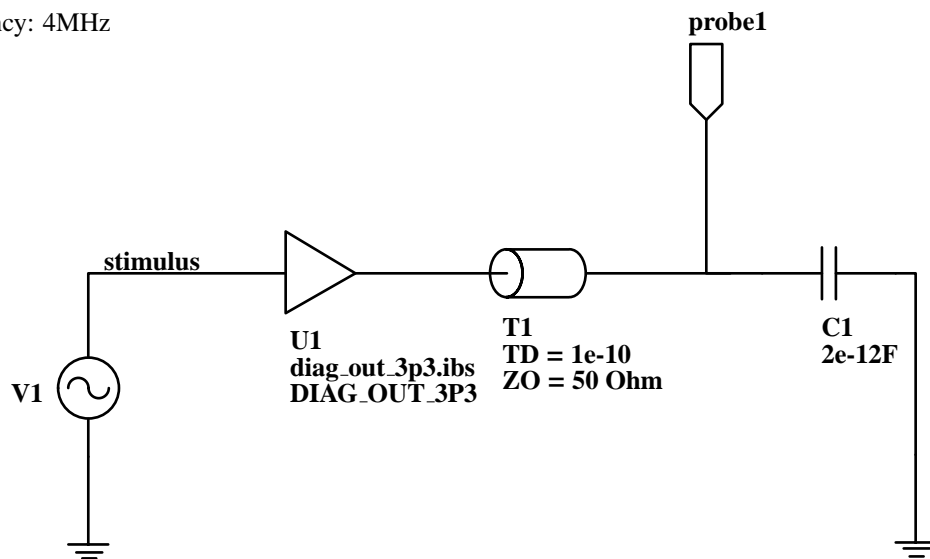


Figure 1: Validation Waveform for model diag_out_3p3

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	15.07%	1.52%	100.00%	5.29697e-01	5.32841e-02	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	16.69%	1.10%	100.00%	6.06834e-01	4.00338e-02	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	8.89%	1.37%	100.00%	2.98945e-01	4.59690e-02	1.49000e-06

Figure 2: Correlation Table for model diag_out_3p3

Figure 3: IBIS Correlation Waveform MultiCycle Image

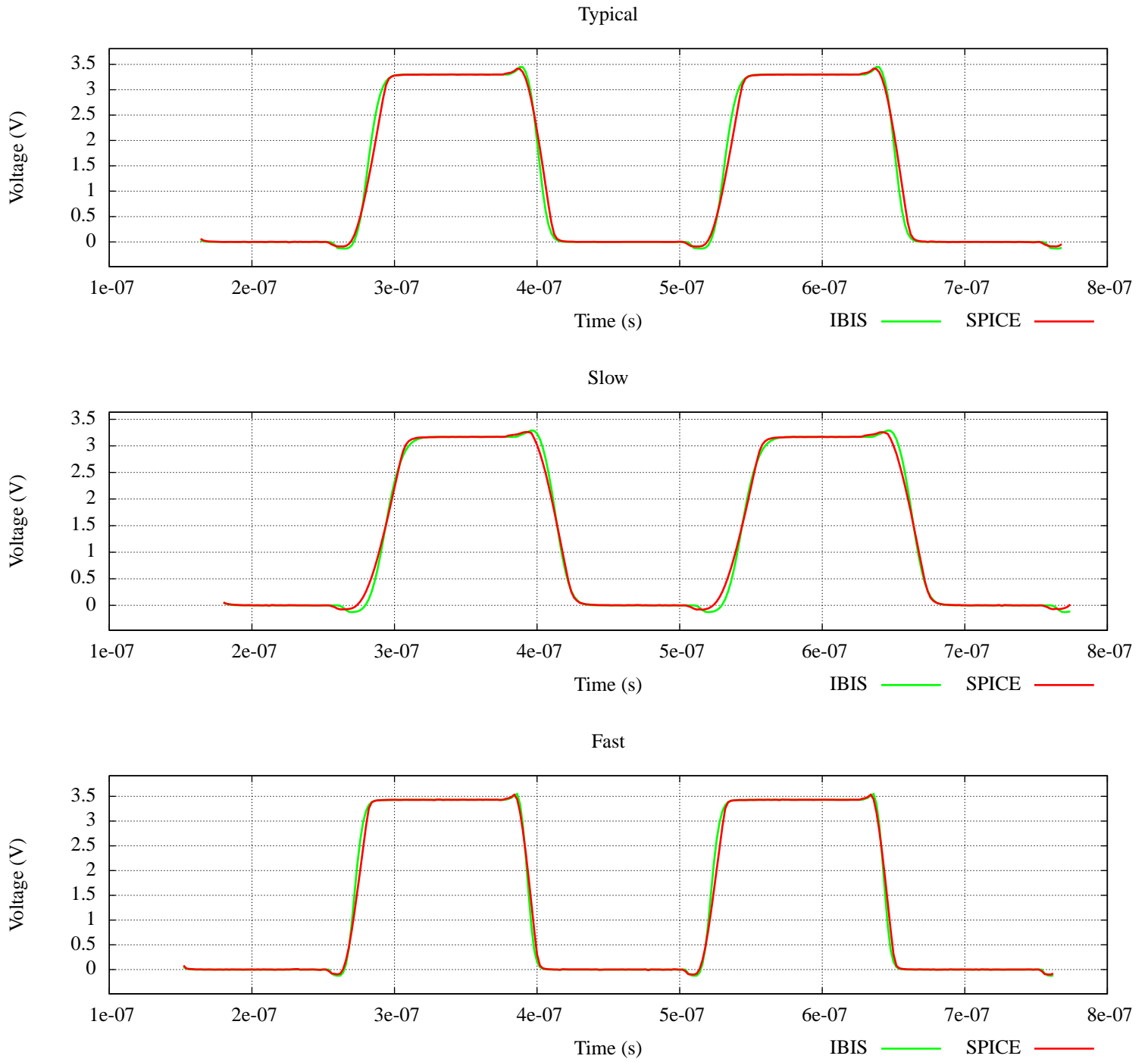


Figure 4: IBIS Correlation Waveform Rising Edge Image

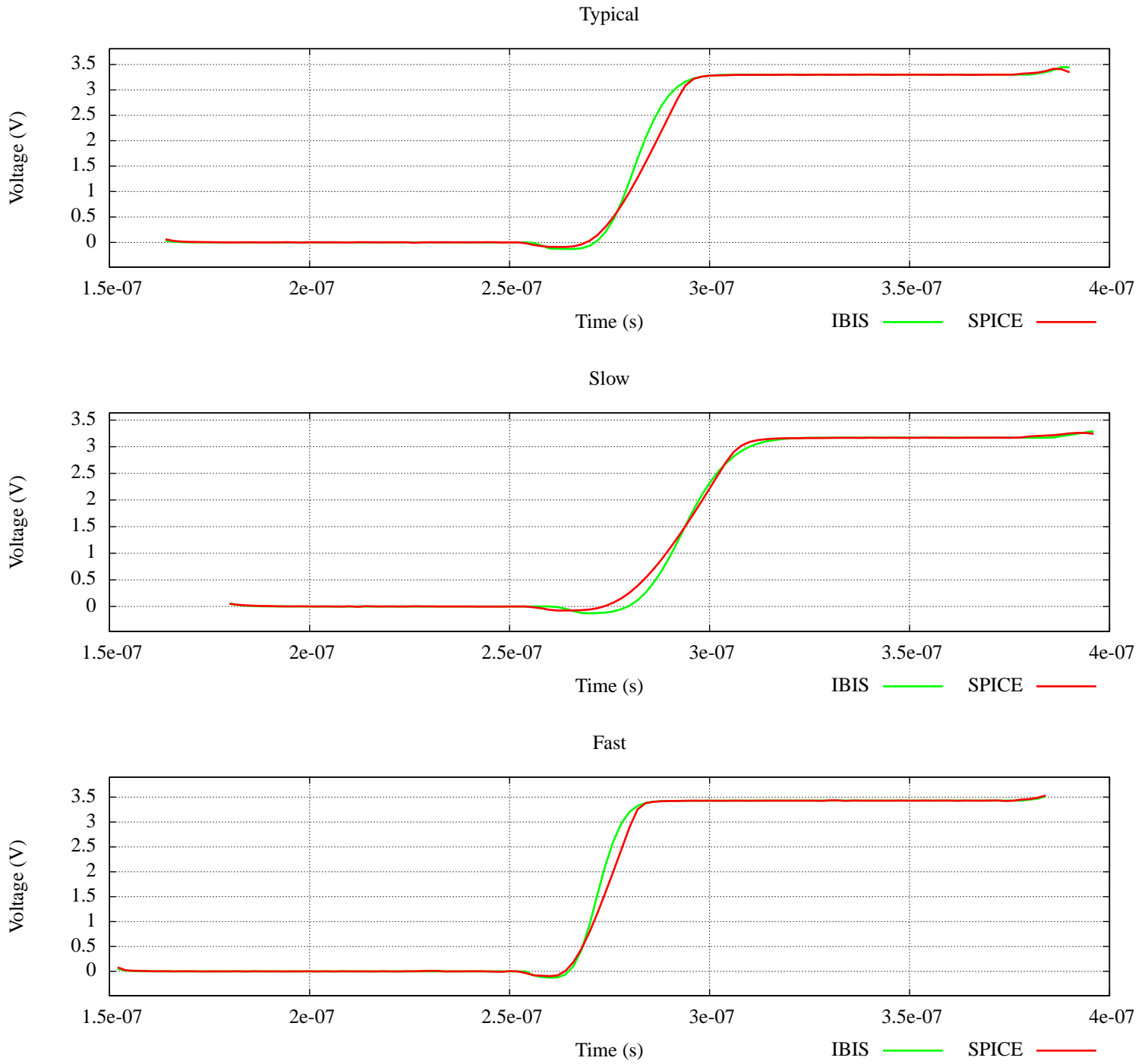
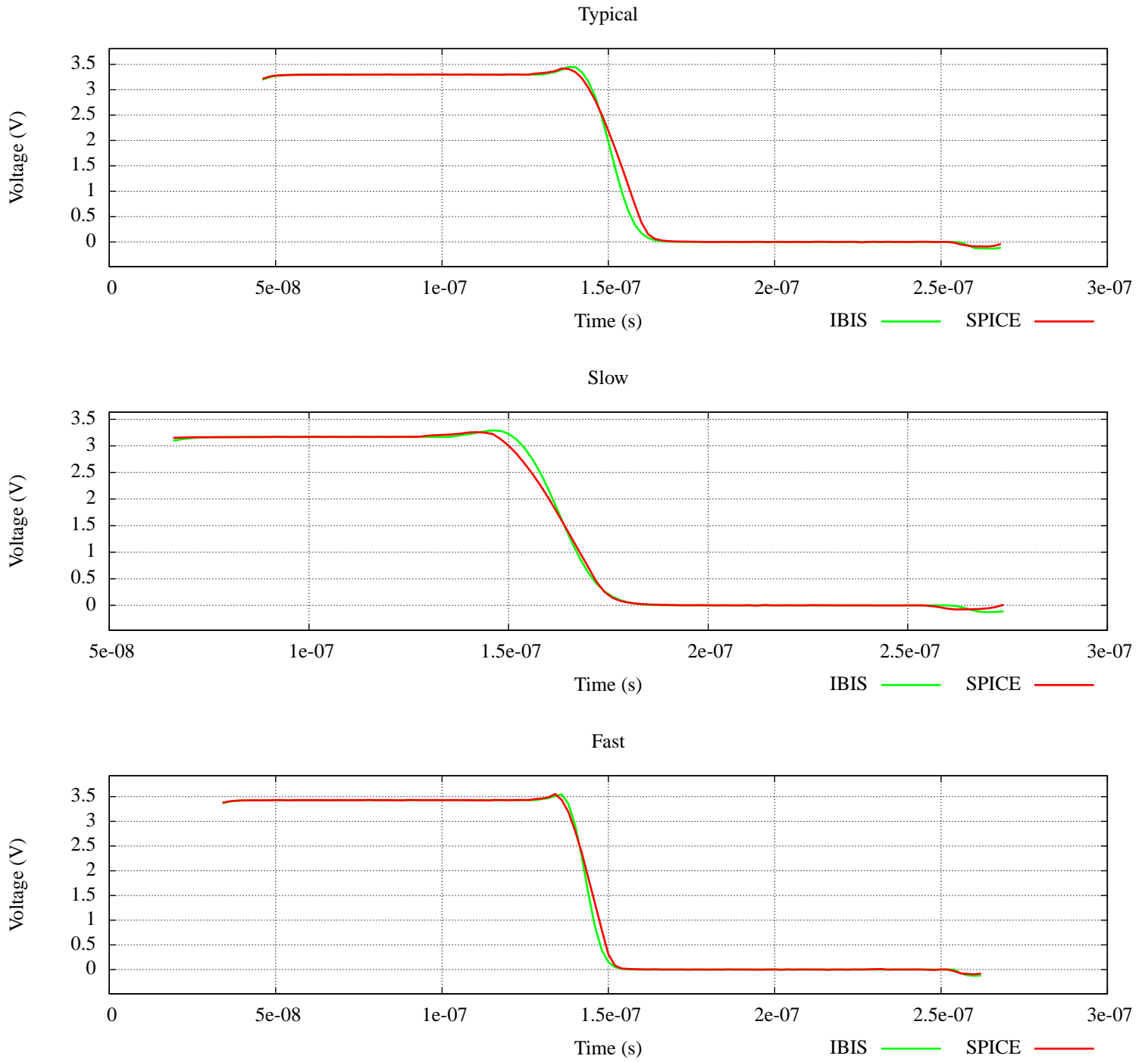


Figure 5: IBIS Correlation Waveform Falling Edge Image



2.3.2 diag_out_5p0

Model Type : 3-state

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	5.0	27
2	Weak	4.85	150
3	Strong	5.15	-40

Table 6: Corners of Validation

TISPICE engine used to generate and correlate IBIS models:

P.S: SPICE type could be Spectre, TISPICE, TISPICED, HSPICE, HSPICED

Generation:

TISPICE

Correlation

SPICE Netlist Simulation : TISPICE

IBIS Model Simulation : HSPICE

For all buffers correlate V-T transient simulations using IBIS(B-element) in HSPICED and SPICE netlist to ensure correlation. Include screen shot of test setup used for correlation. SimDE test setup with recommended load conditions may be used.

- Use node naming convention of IBIS_<corner> and SPICE_<corner>.
- Run simulation for all corner cases and maximum allowable speed grade, if multiple speed grades or drive strengths are allowed, please include separate correlation waveforms for each case. Include waveforms here. Re-use C.1.i and C.1.ii as needed for multiple buffers and or configurations. Include any correlation metrics if available

Test Frequency: 4MHz

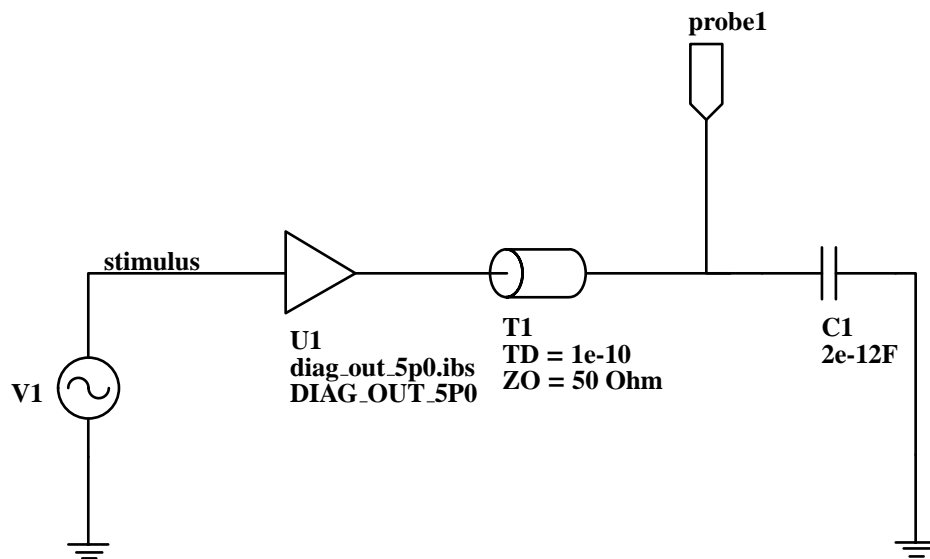


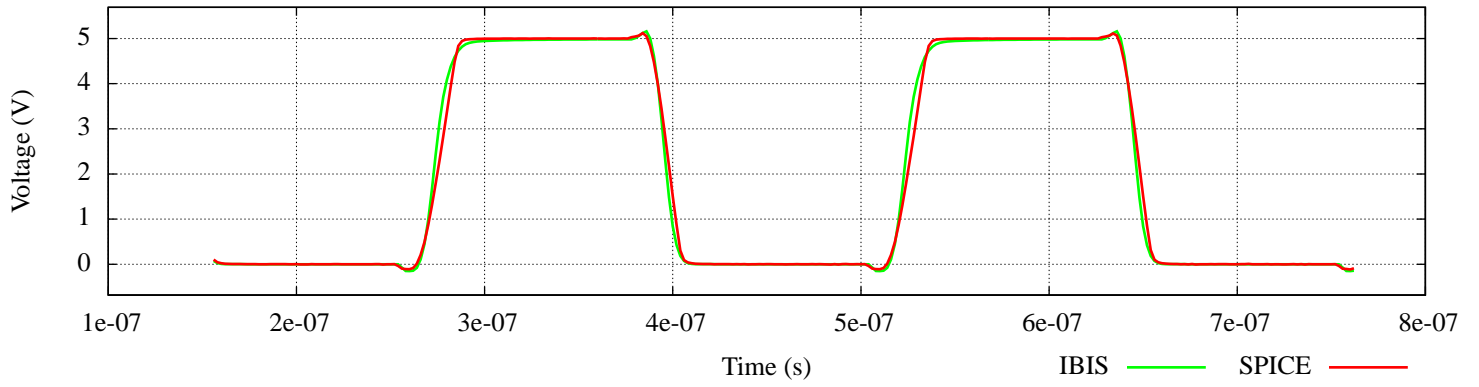
Figure 6: Validation Waveform for model diag_out_5p0

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	16.63%	1.46%	100.00%	8.70596e-01	7.63274e-02	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	9.62%	0.89%	100.00%	5.14933e-01	4.73563e-02	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	11.69%	1.42%	100.00%	5.89725e-01	7.14197e-02	1.49000e-06

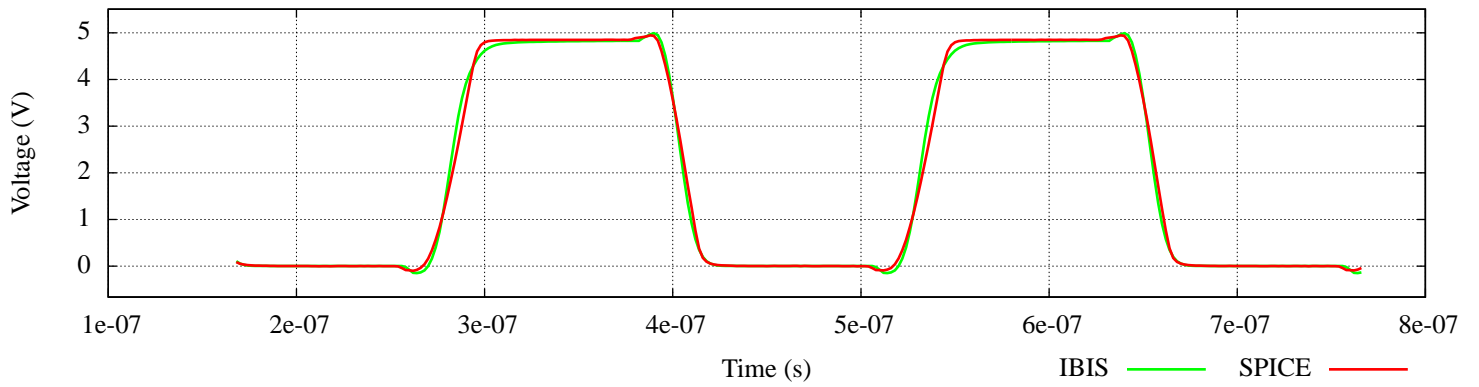
Figure 7: Correlation Table for model diag_out_5p0

Figure 8: IBIS Correlation Waveform MultiCycle Image

Typical



Slow



Fast

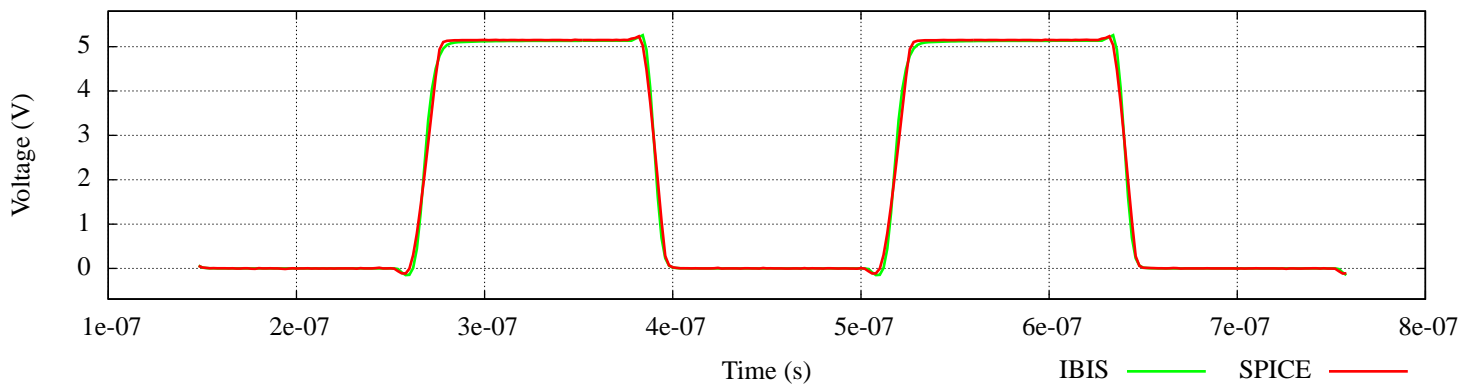


Figure 9: IBIS Correlation Waveform Rising Edge Image

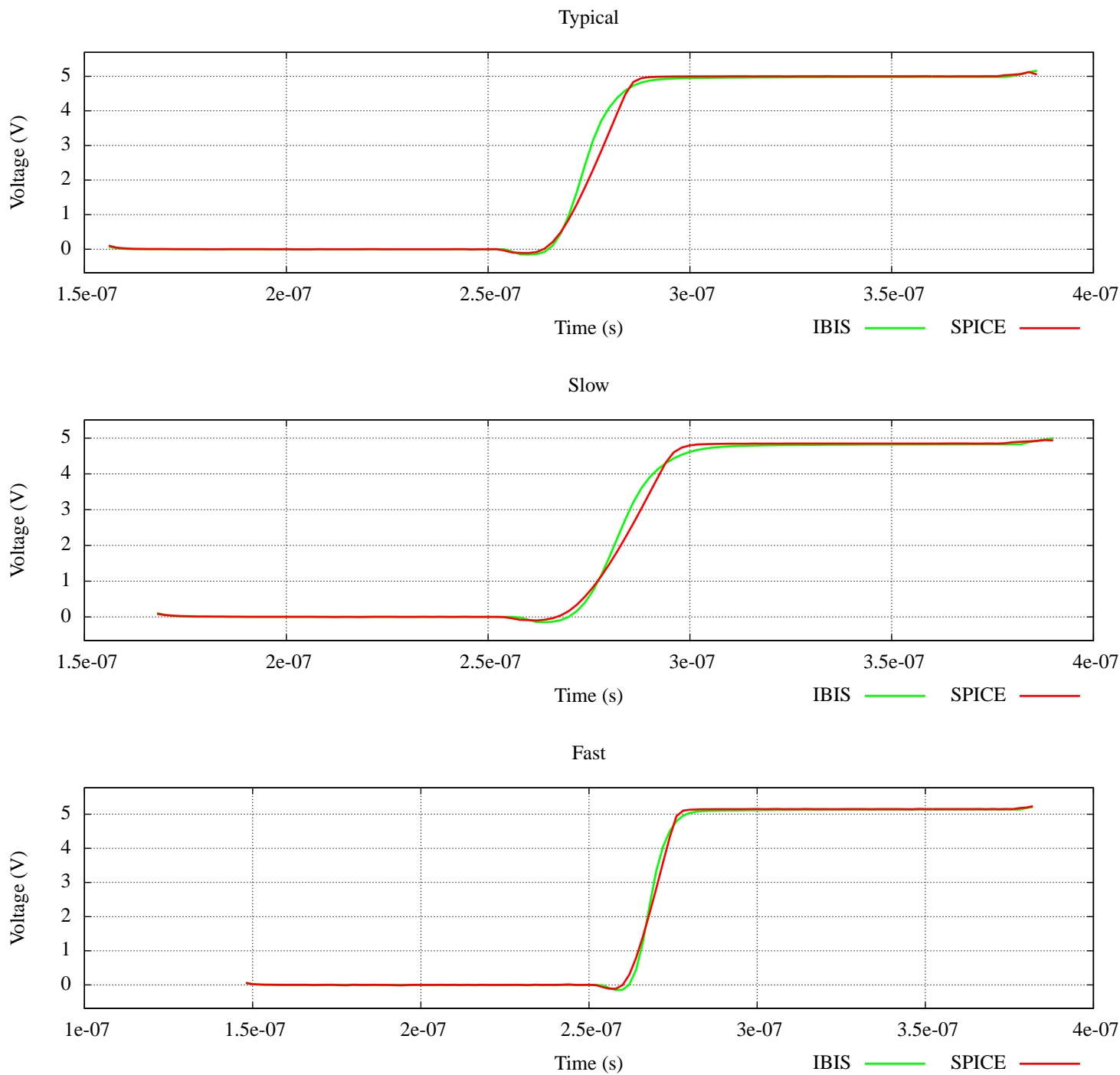
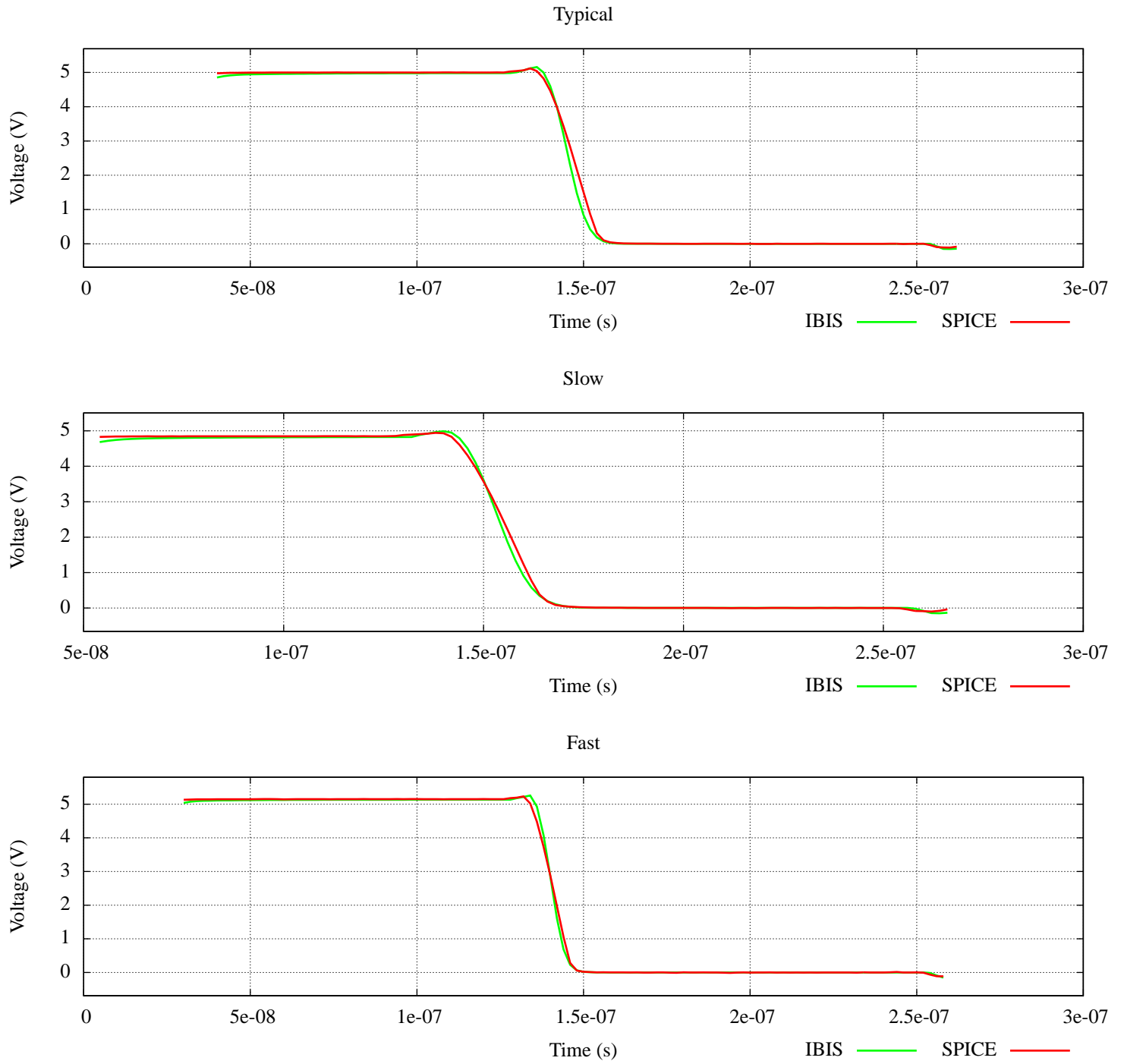


Figure 10: IBIS Correlation Waveform Falling Edge Image



2.3.3 endrv_nres_3p3

Model Type : Output

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 7: Corners of Validation

TISPICE engine used to generate and correlate IBIS models:

P.S: SPICE type could be Spectre, TISPICE, TISPICED, HSPICE, HSPICED

Generation:

TISPICE

Correlation

SPICE Netlist Simulation : TISPICE

IBIS Model Simulation : HSPICE

For all buffers correlate V-T transient simulations using IBIS(B-element) in HSPICED and SPICE netlist to ensure correlation. Include screen shot of test setup used for correlation. SimDE test setup with recommended load conditions may be used.

- Use node naming convention of IBIS_<corner> and SPICE_<corner>.
- Run simulation for all corner cases and maximum allowable speed grade, if multiple speed grades or drive strengths are allowed, please include separate correlation waveforms for each case. Include waveforms here. Re-use C.1.i and C.1.ii as needed for multiple buffers and or configurations. Include any correlation metrics if available

Test Frequency: 1000KHz

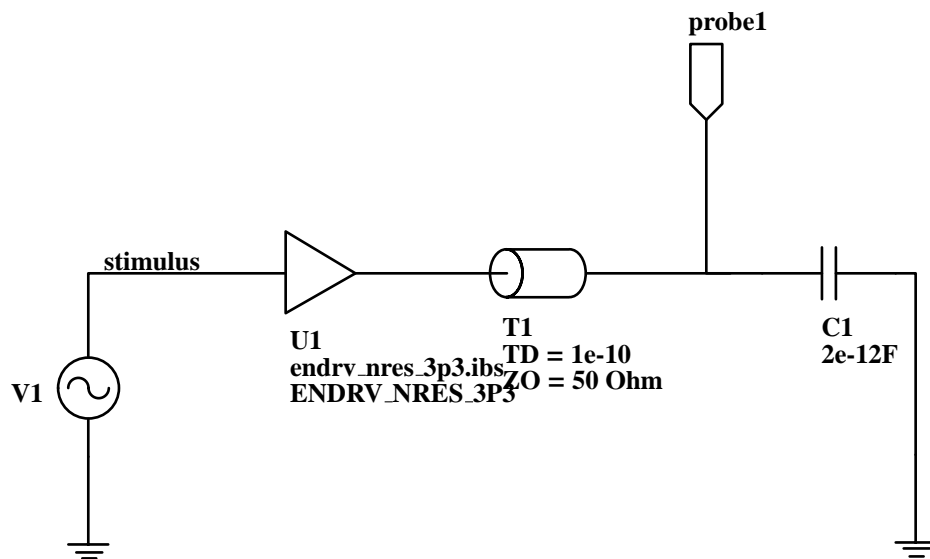


Figure 11: Validation Waveform for model endrv_nres_3p3

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	9.01%	0.46%	100.00%	2.98500e-01	1.51950e-02	5.99000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	51.67%	0.74%	100.00%	1.77819e+00	2.55426e-02	5.99000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	82.72%	1.50%	100.00%	2.62122e+00	4.74426e-02	5.99000e-06

Figure 12: Correlation Table for model endrv_nres_3p3

Figure 13: IBIS Correlation Waveform MultiCycle Image

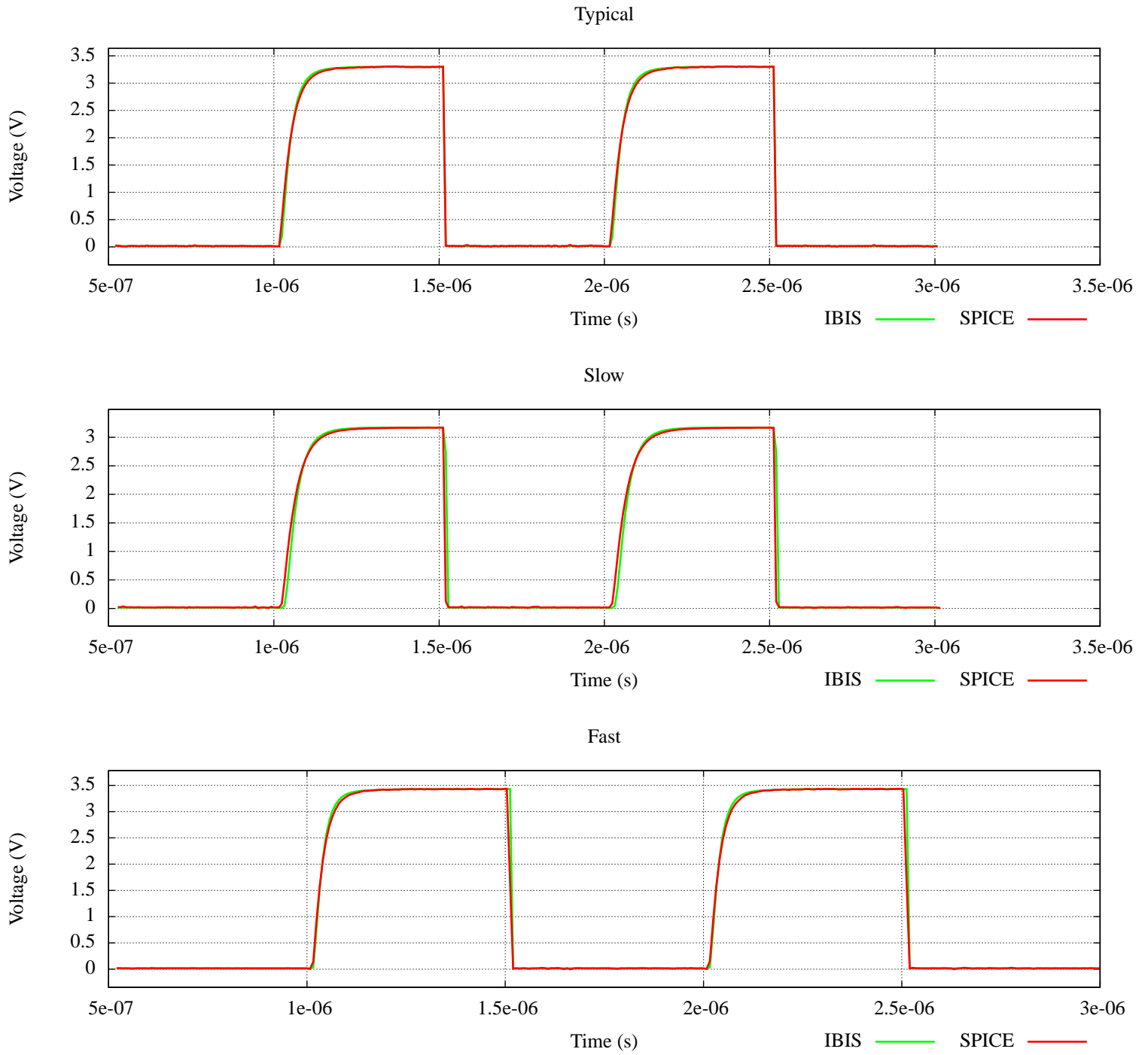


Figure 14: IBIS Correlation Waveform Rising Edge Image

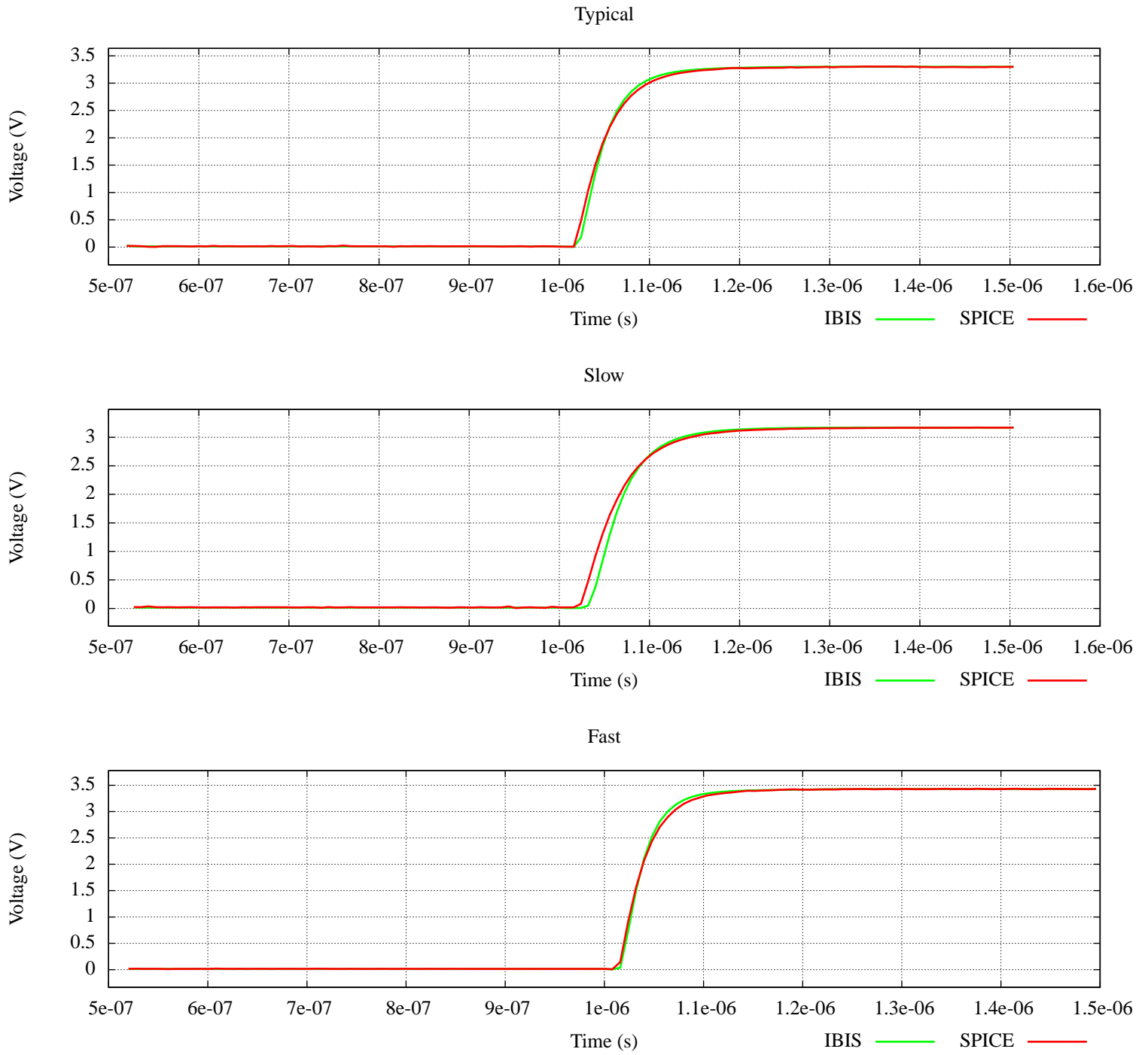
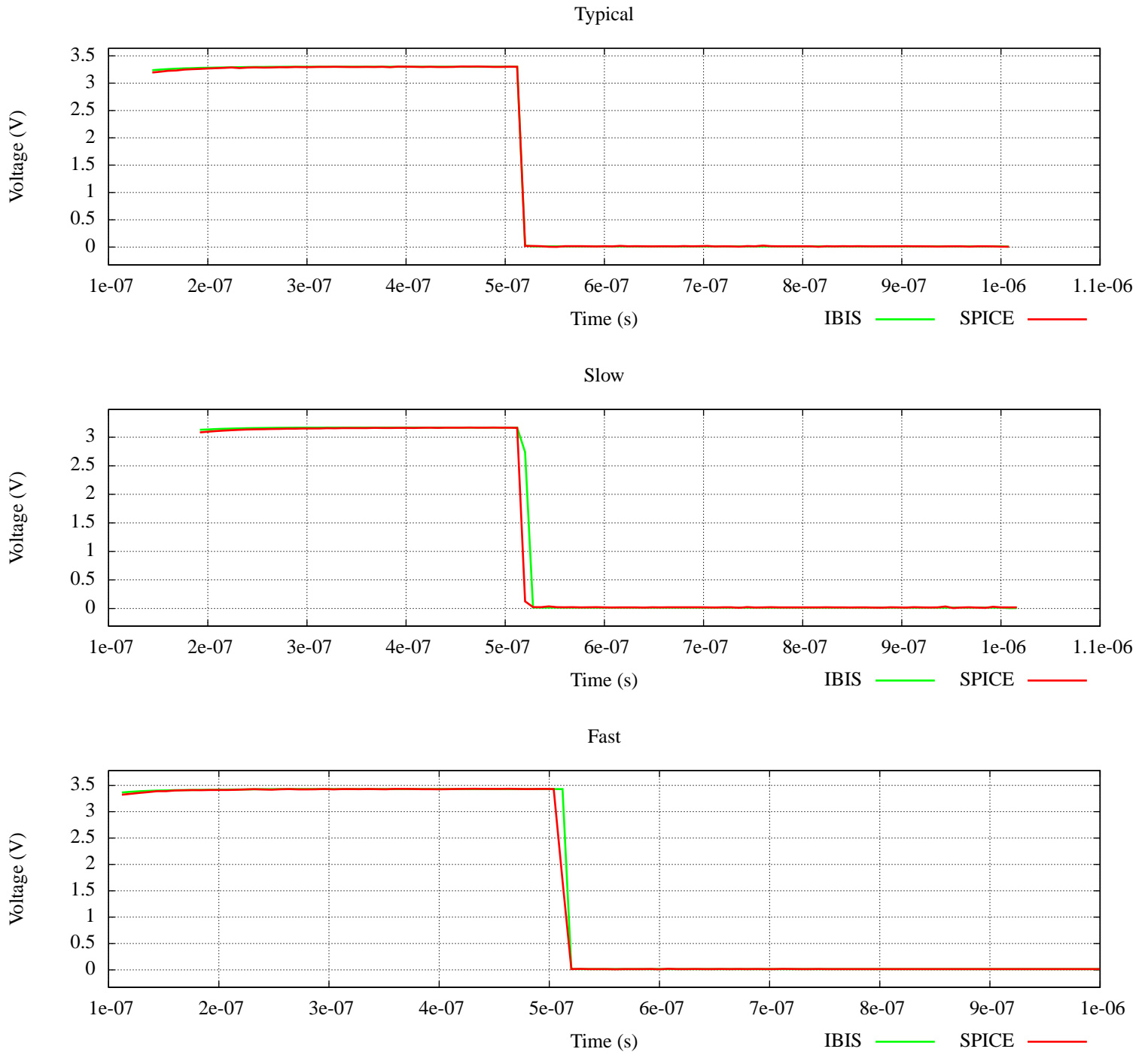


Figure 15: IBIS Correlation Waveform Falling Edge Image



2.3.4 endrv_nres_5p0

Model Type : Output

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	5.0	27
2	Weak	4.85	150
3	Strong	5.15	-40

Table 8: Corners of Validation

TISPICE engine used to generate and correlate IBIS models:

P.S: SPICE type could be Spectre, TISPICE, TISPICED, HSPICE, HSPICED

Generation:

TISPICE

Correlation

SPICE Netlist Simulation : TISPICE

IBIS Model Simulation : HSPICE

For all buffers correlate V-T transient simulations using IBIS(B-element) in HSPICED and SPICE netlist to ensure correlation. Include screen shot of test setup used for correlation. SimDE test setup with recommended load conditions may be used.

- Use node naming convention of IBIS_<corner> and SPICE_<corner>.
- Run simulation for all corner cases and maximum allowable speed grade, if multiple speed grades or drive strengths are allowed, please include separate correlation waveforms for each case. Include waveforms here. Re-use C.1.i and C.1.ii as needed for multiple buffers and or configurations. Include any correlation metrics if available

Test Frequency: 1000KHz

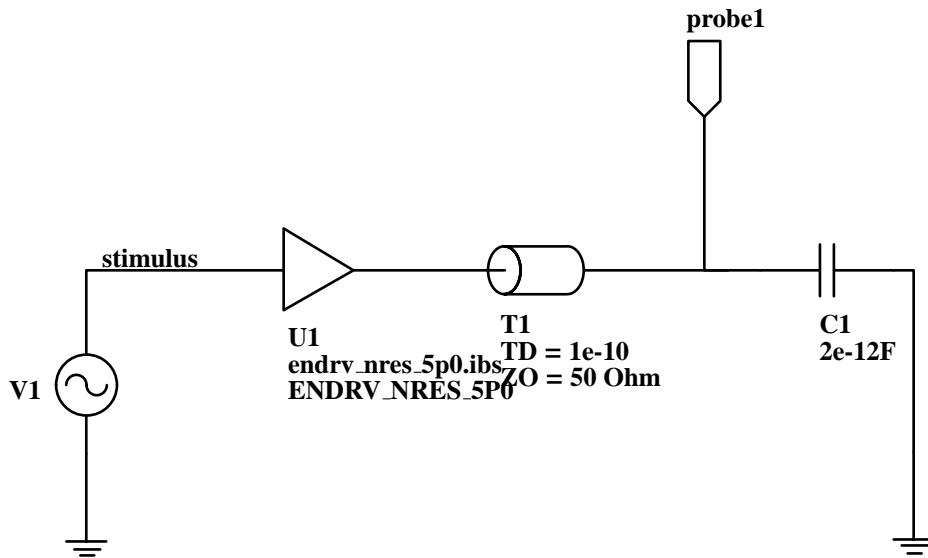


Figure 16: Validation Waveform for model endrv_nres_5p0

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	9.56%	0.37%	100.00%	4.77814e-01	1.87223e-02	5.99000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	43.22%	0.60%	100.00%	2.22917e+00	3.10238e-02	5.99000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	83.87%	1.42%	100.00%	4.06441e+00	6.87654e-02	5.99000e-06

Figure 17: Correlation Table for model endrv_nres_5p0

Figure 18: IBIS Correlation Waveform MultiCycle Image

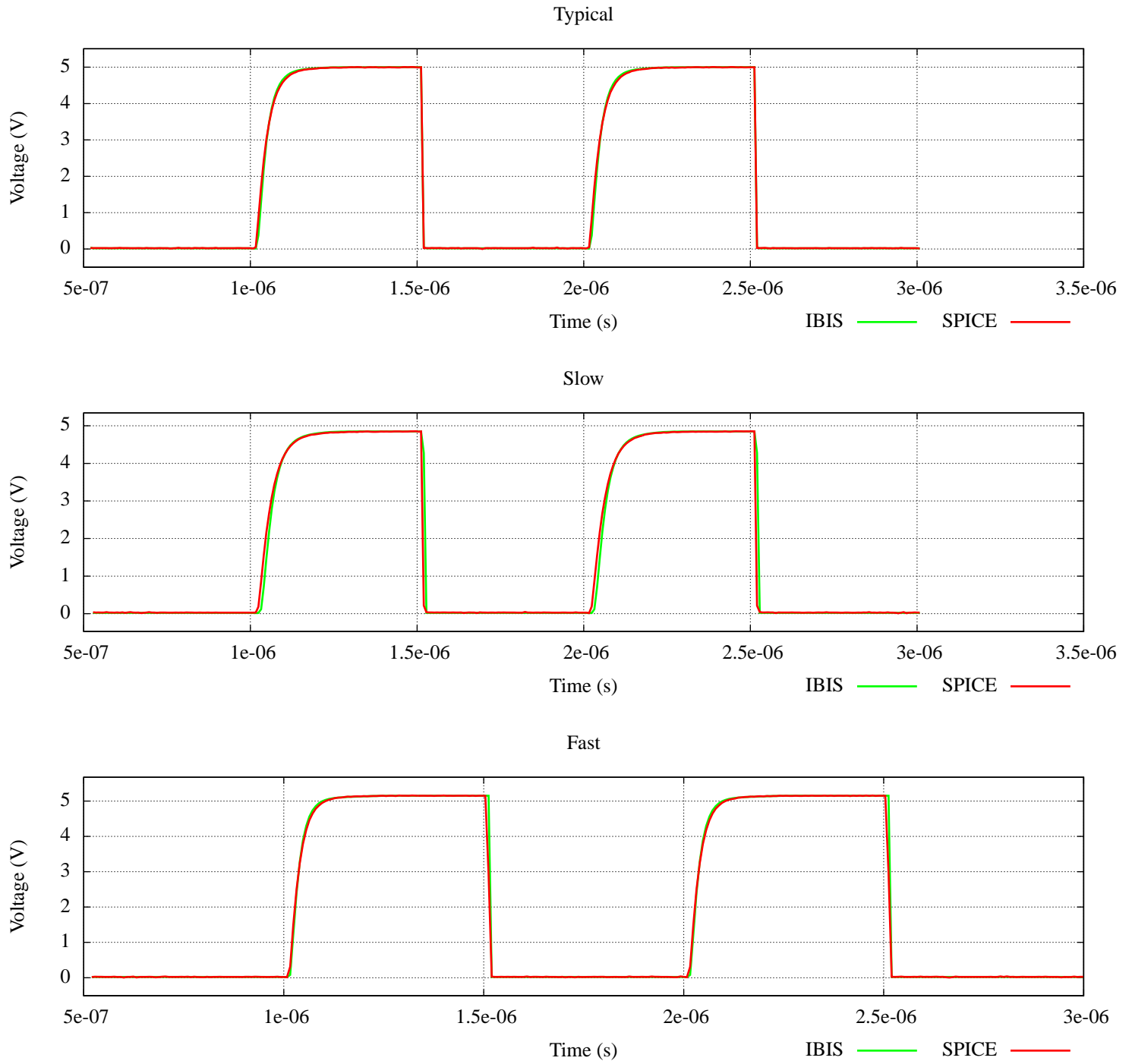


Figure 19: IBIS Correlation Waveform Rising Edge Image

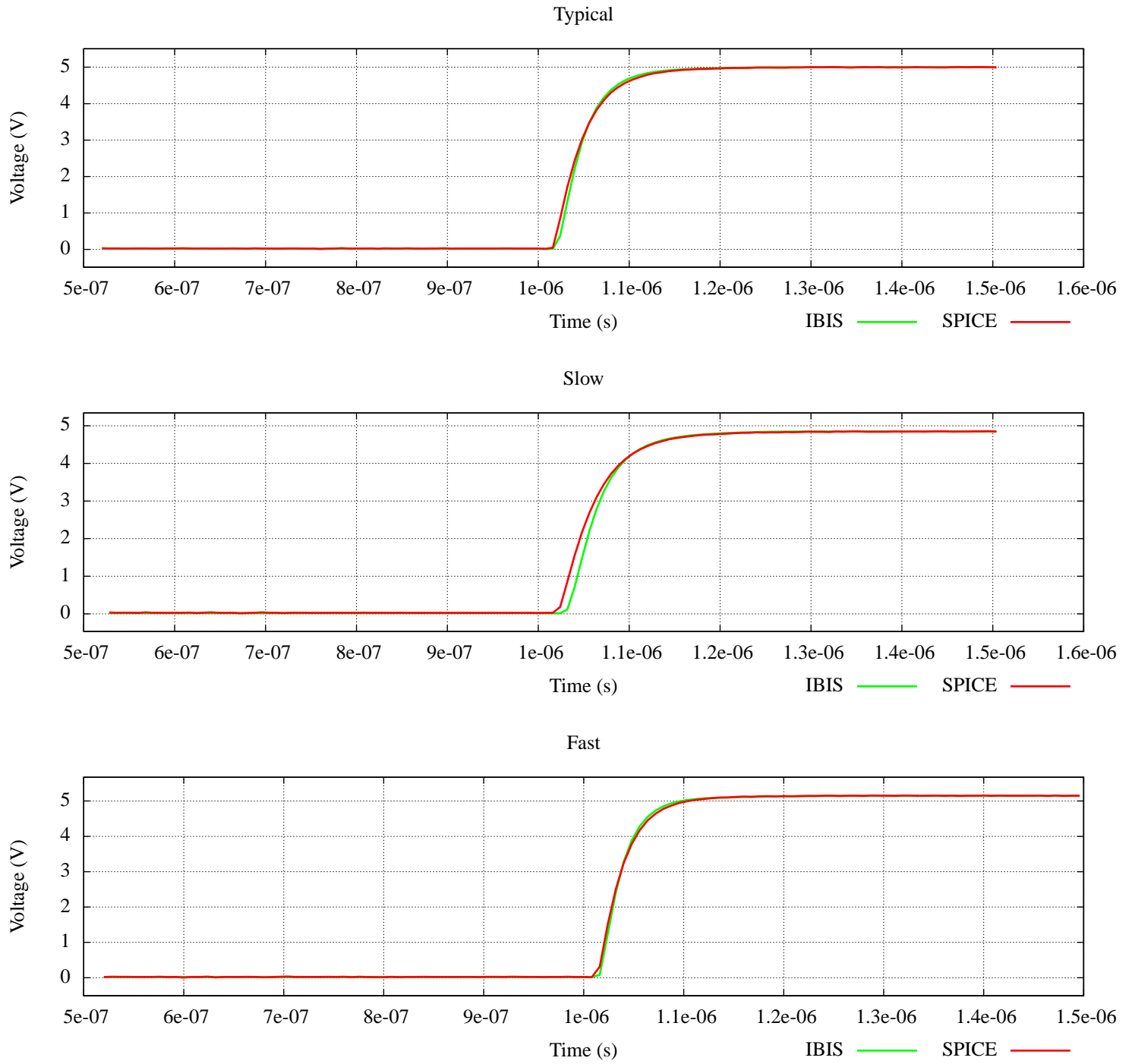
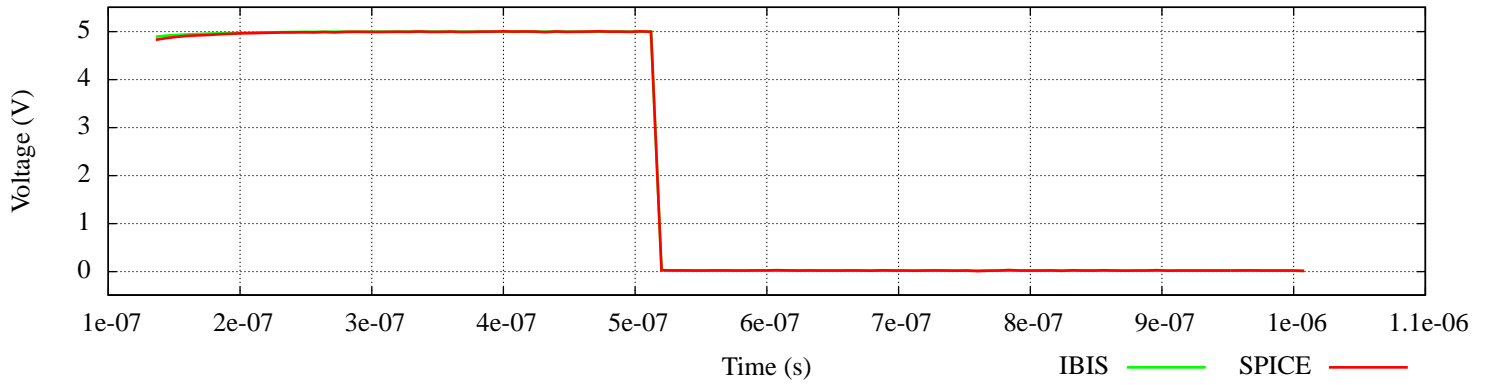
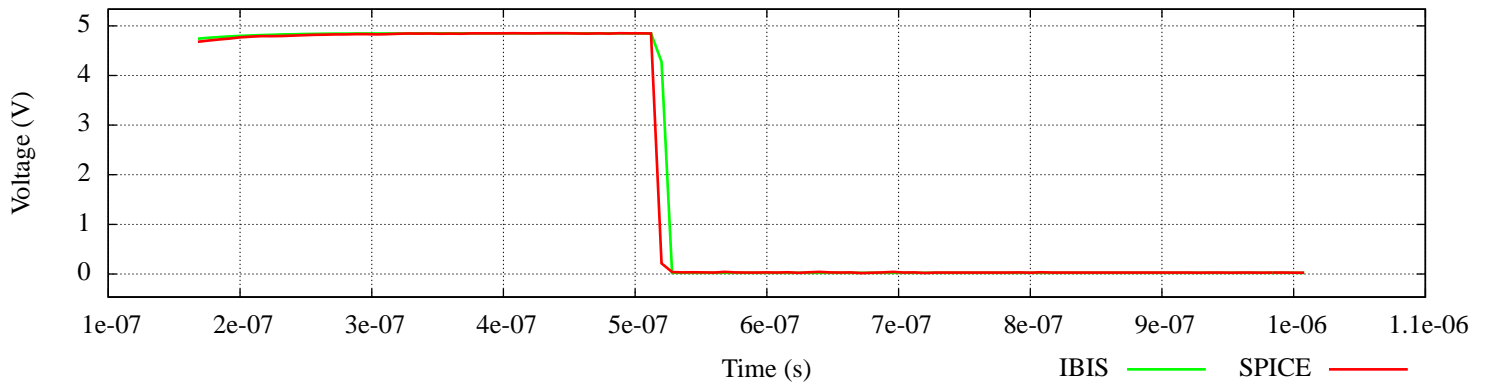


Figure 20: IBIS Correlation Waveform Falling Edge Image

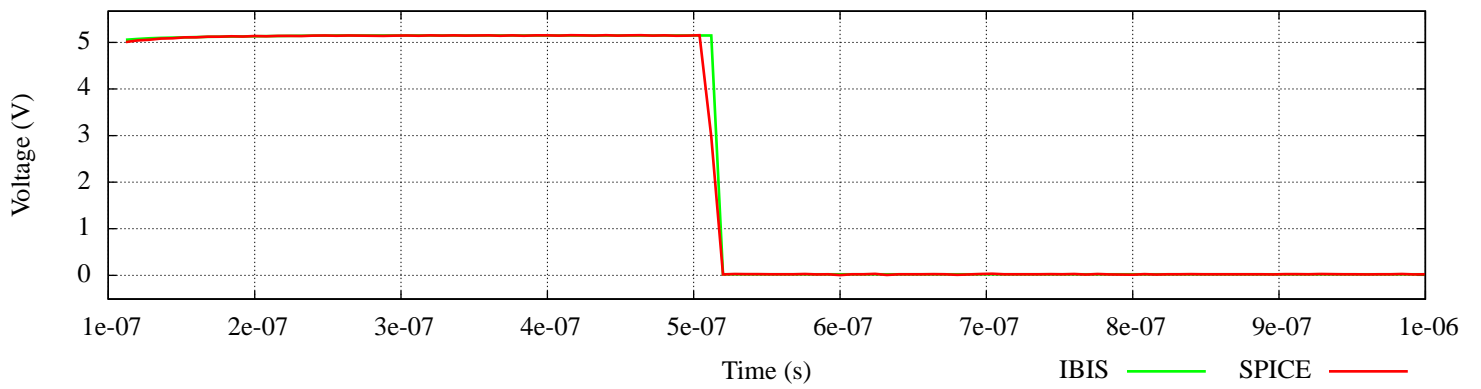
Typical



Slow



Fast



2.3.5 error

Model Type : Input

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 9: Corners of Validation

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	4.79%	0.21%	100.00%	1.60711e-01	7.04668e-03	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	3.12%	0.22%	100.00%	1.09492e-01	7.74905e-03	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	1.80%	0.21%	100.00%	5.77389e-02	6.69256e-03	1.49000e-06

Figure 21: Correlation Table for model error

2.3.6 ncs_iovdd3p3

Model Type : Input

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 10: Corners of Validation

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	4.76%	0.35%	100.00%	1.63338e-01	1.19137e-02	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	9.35%	0.39%	100.00%	3.31121e-01	1.37070e-02	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	6.96%	0.32%	100.00%	2.28299e-01	1.04074e-02	1.49000e-06

Figure 22: Correlation Table for model ncs_iovdd3p3

2.3.7 ncs_iovdd5p0

Model Type : Input

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 11: Corners of Validation

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	5.40%	0.30%	100.00%	1.82997e-01	1.02898e-02	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	5.93%	0.29%	100.00%	2.10432e-01	1.02295e-02	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	6.66%	0.35%	100.00%	2.19935e-01	1.16081e-02	1.49000e-06

Figure 23: Correlation Table for model ncs_iovdd5p0

2.3.8 sclk_sdi

Model Type : Input

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 12: Corners of Validation

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	6.19%	0.32%	100.00%	2.11242e-01	1.10879e-02	7.49900e-07
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	5.61%	0.33%	100.00%	2.00673e-01	1.19482e-02	7.49900e-07
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	6.27%	0.33%	100.00%	2.08540e-01	1.08046e-02	7.49900e-07

Figure 24: Correlation Table for model sclk_sdi

2.3.9 sdo_3p3

Model Type : IO

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 13: Corners of Validation

TISPICE engine used to generate and correlate IBIS models:

P.S: SPICE type could be Spectre, TISPICE, TISPICED, HSPICE, HSPICED

Generation:

TISPICE

Correlation

SPICE Netlist Simulation : TISPICE

IBIS Model Simulation : HSPICE

For all buffers correlate V-T transient simulations using IBIS(B-element) in HSPICED and SPICE netlist to ensure correlation. Include screen shot of test setup used for correlation. SimDE test setup with recommended load conditions may be used.

- Use node naming convention of IBIS_<corner> and SPICE_<corner>.
- Run simulation for all corner cases and maximum allowable speed grade, if multiple speed grades or drive strengths are allowed, please include separate correlation waveforms for each case. Include waveforms here. Re-use C.1.i and C.1.ii as needed for multiple buffers and or configurations. Include any correlation metrics if available

Test Frequency: 4MHz

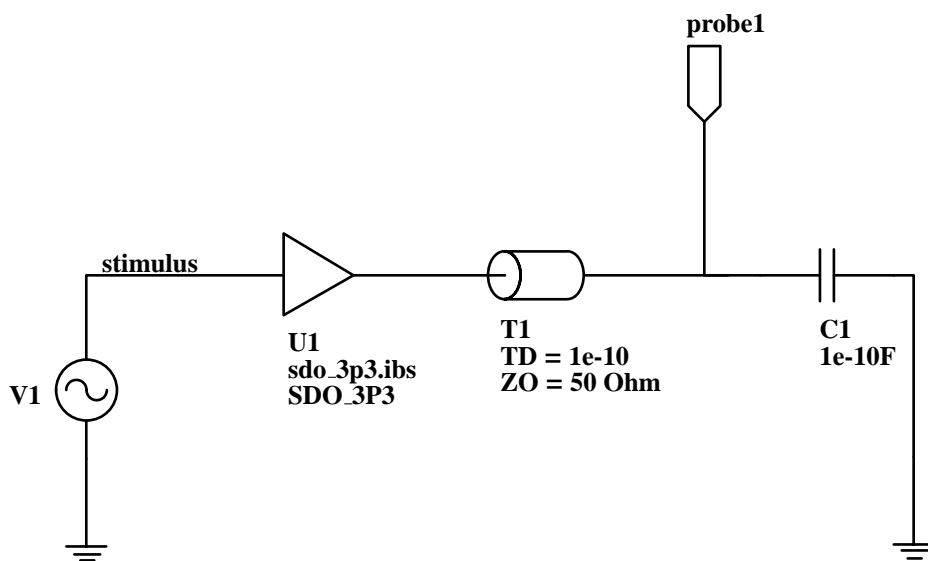


Figure 25: Validation Waveform for model sdo_3p3

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	5.26%	1.27%	100.00%	1.75311e-01	4.24058e-02	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	10.05%	1.32%	100.00%	3.48745e-01	4.57915e-02	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	3.78%	1.53%	100.00%	1.19234e-01	4.84114e-02	1.49000e-06

Figure 26: Correlation Table for model sdo_3p3

Figure 27: IBIS Correlation Waveform MultiCycle Image

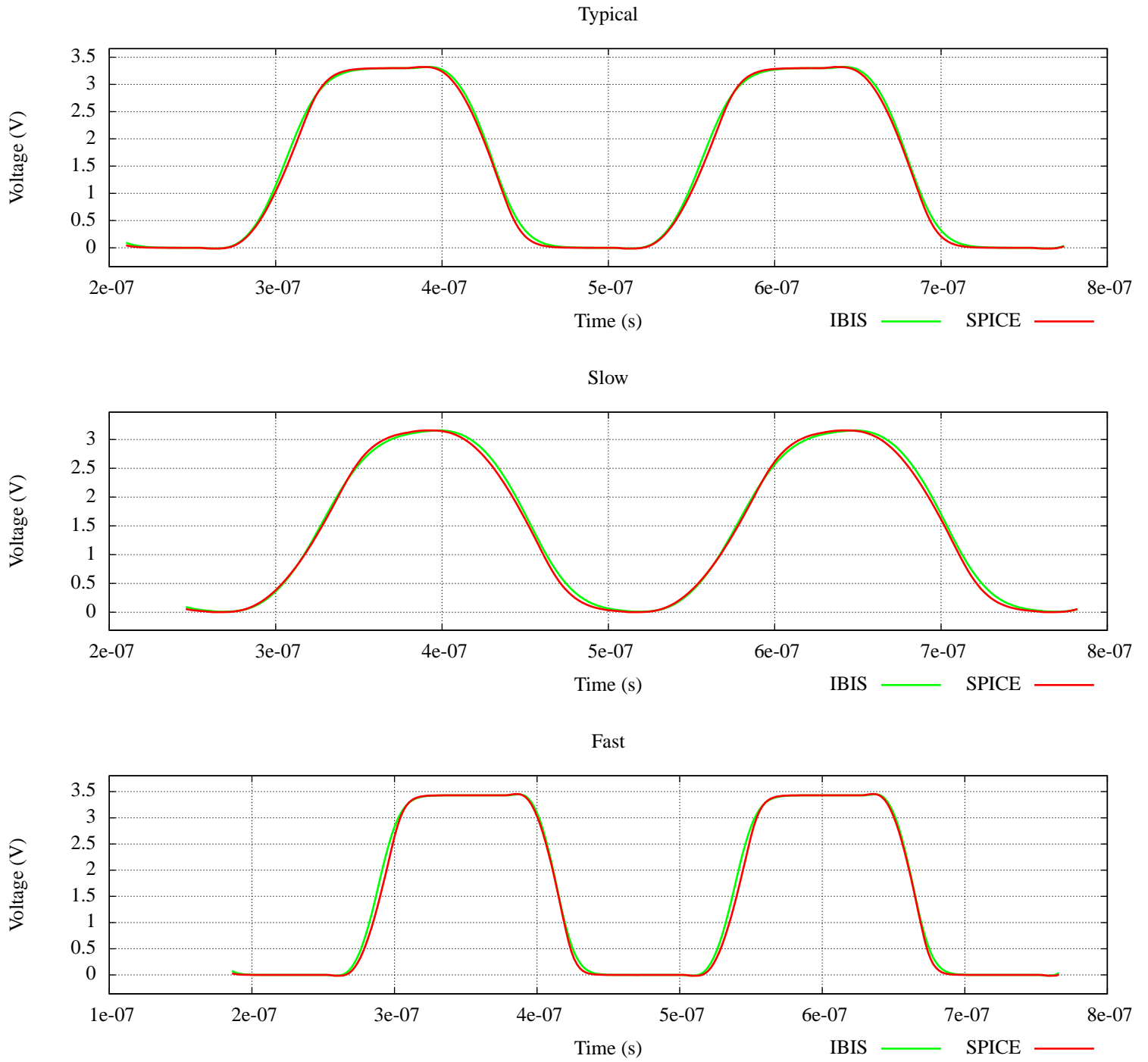


Figure 28: IBIS Correlation Waveform Rising Edge Image

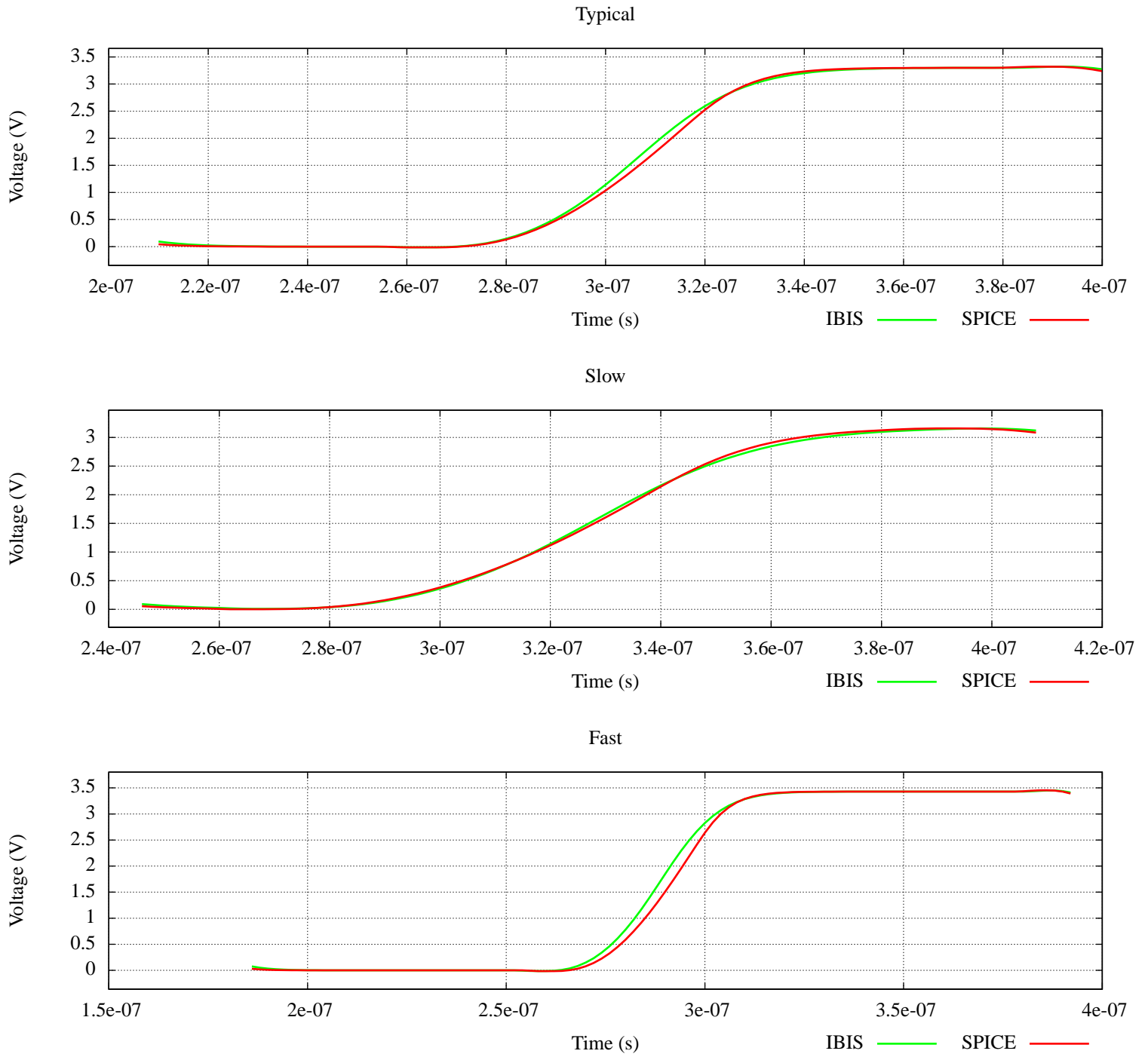
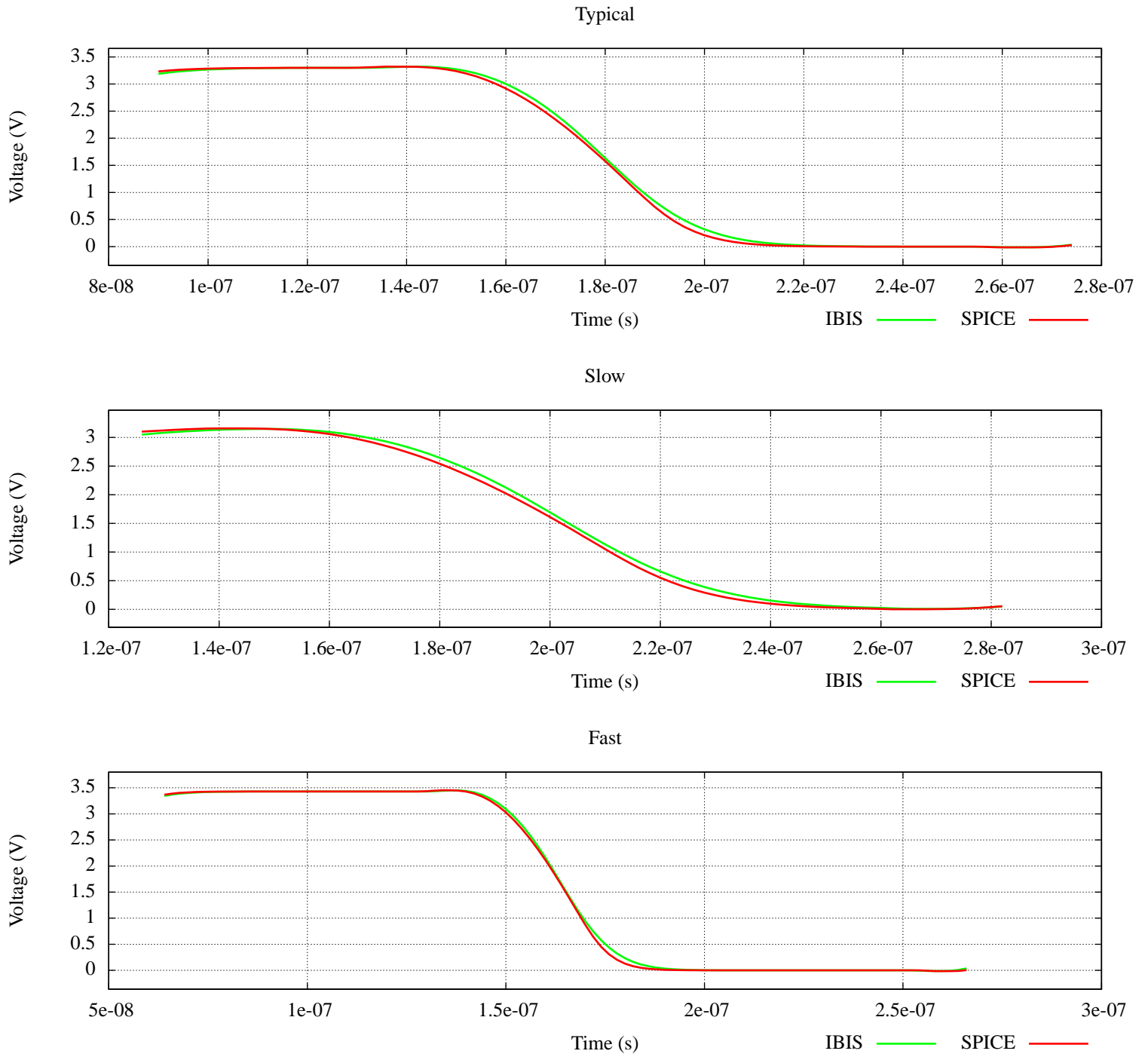


Figure 29: IBIS Correlation Waveform Falling Edge Image



2.3.10 sdo_5p0

Model Type : IO

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	5.0	27
2	Weak	4.85	150
3	Strong	5.15	-40

Table 14: Corners of Validation

TISPICE engine used to generate and correlate IBIS models:

P.S: SPICE type could be Spectre, TISPICE, TISPICED, HSPICE, HSPICED

Generation:

TISPICE

Correlation

SPICE Netlist Simulation : TISPICE

IBIS Model Simulation : HSPICE

For all buffers correlate V-T transient simulations using IBIS(B-element) in HSPICED and SPICE netlist to ensure correlation. Include screen shot of test setup used for correlation. SimDE test setup with recommended load conditions may be used.

- Use node naming convention of IBIS_<corner> and SPICE_<corner>.
- Run simulation for all corner cases and maximum allowable speed grade, if multiple speed grades or drive strengths are allowed, please include separate correlation waveforms for each case. Include waveforms here. Re-use C.1.i and C.1.ii as needed for multiple buffers and or configurations. Include any correlation metrics if available

Test Frequency: 4MHz

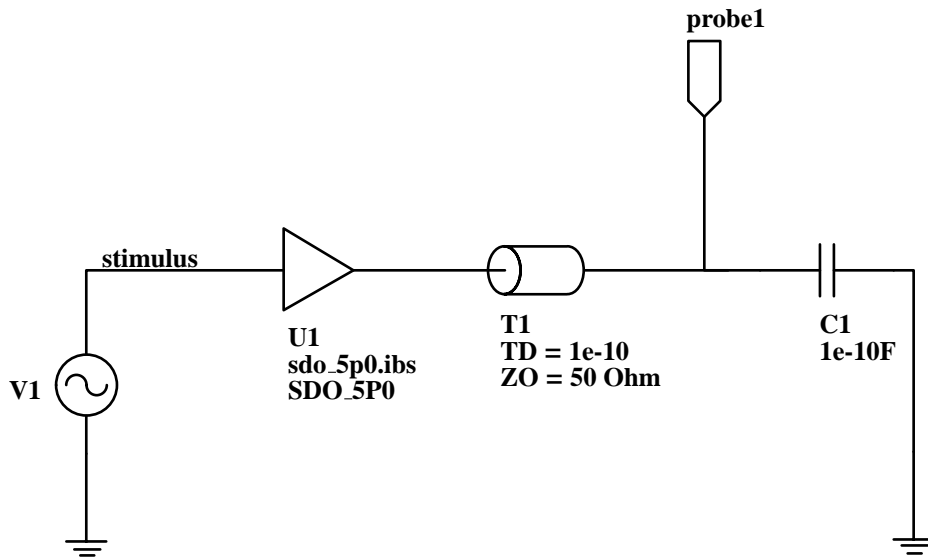


Figure 30: Validation Waveform for model sdo_5p0

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	6.37%	1.47%	100.00%	3.21701e-01	7.41930e-02	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	9.01%	1.23%	100.00%	4.69046e-01	6.42820e-02	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	5.04%	1.77%	100.00%	2.46698e-01	8.63709e-02	1.49000e-06

Figure 31: Correlation Table for model sdo_5p0

Figure 32: IBIS Correlation Waveform MultiCycle Image

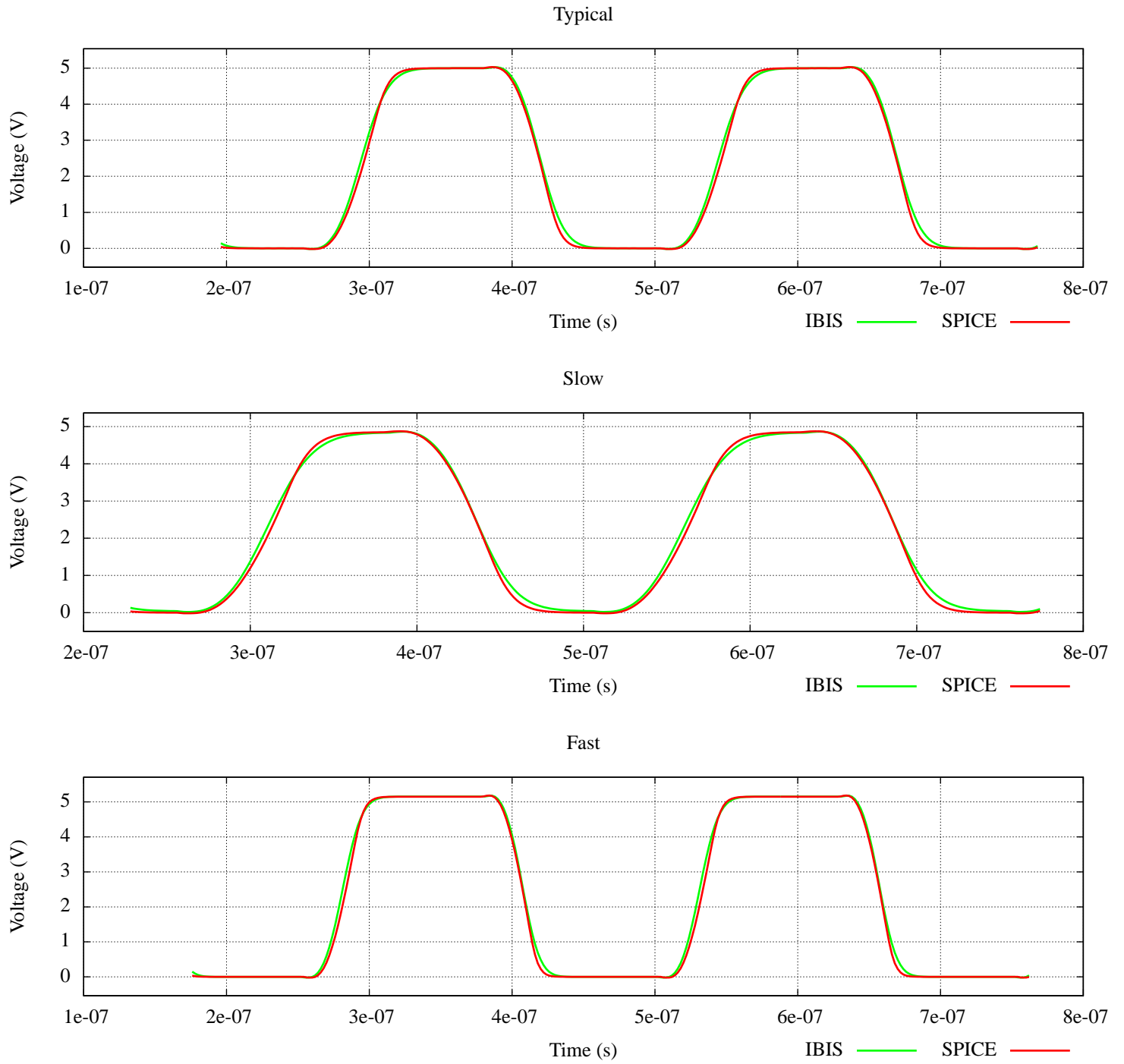


Figure 33: IBIS Correlation Waveform Rising Edge Image

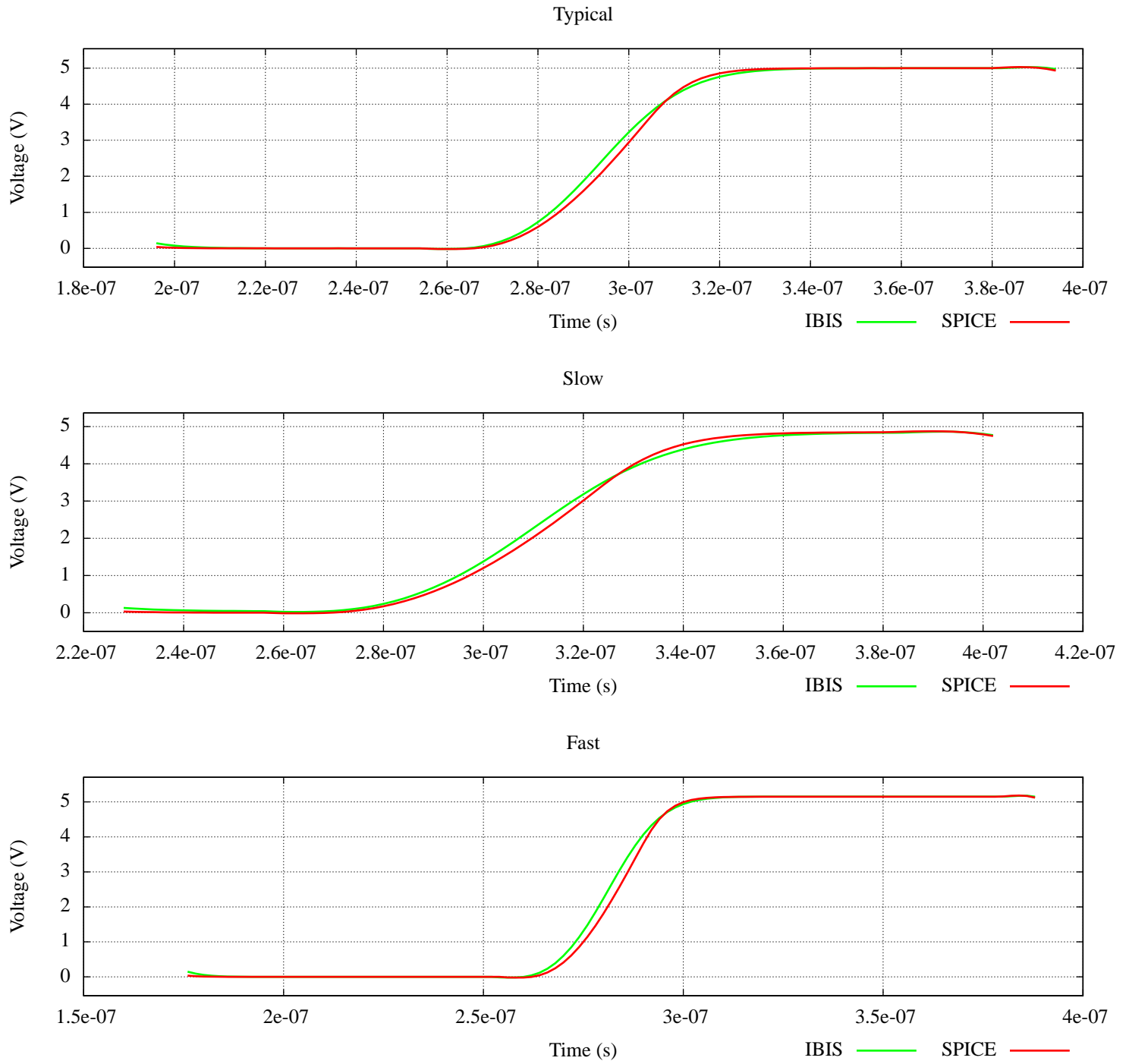
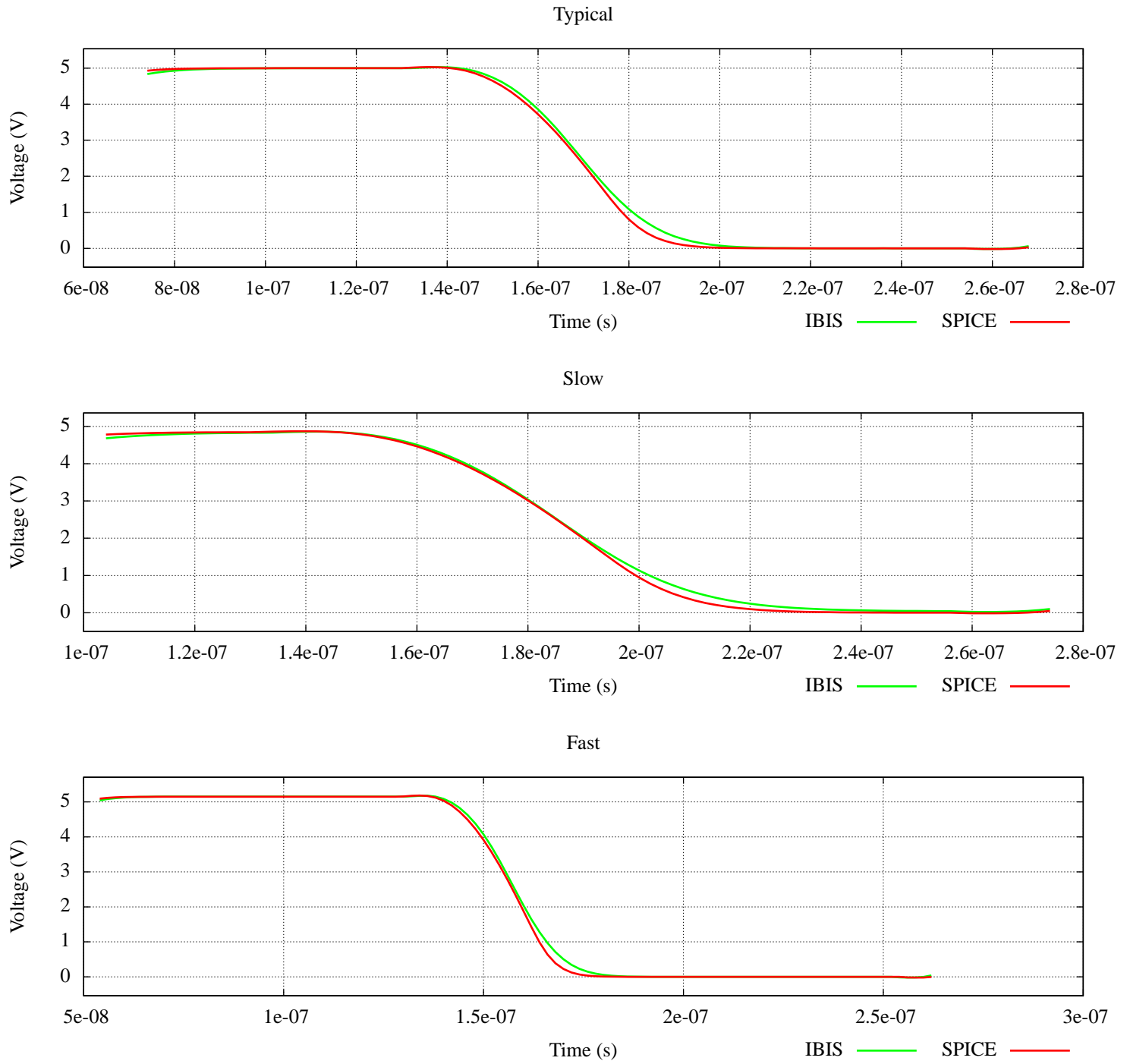


Figure 34: IBIS Correlation Waveform Falling Edge Image



2.3.11 sel_vdd3_vdd5

Model Type : Input

Corner No.	Process	Power Supply(V)	Temp(degC)
1	Nominal	3.3	27
2	Weak	3.17	150
3	Strong	3.43	-40

Table 15: Corners of Validation

Output										
	Type	Reference Waveform	Compare Waveform	Offset	DPI(%)	DAI(%)	DLI(%)	DP	DA	DL
1	Vertical	SPICE_TYP	ibis_typ	-0.00000e+00	3.50%	0.22%	100.00%	1.17092e-01	7.21191e-03	1.49000e-06
2	Vertical	SPICE_FAST	ibis_fast	-0.00000e+00	2.77%	0.22%	100.00%	9.68603e-02	7.58815e-03	1.49000e-06
3	Vertical	SPICE_SLOW	ibis_slow	-0.00000e+00	2.91%	0.22%	100.00%	9.36020e-02	7.00372e-03	1.49000e-06

Figure 35: Correlation Table for model sel_vdd3_vdd5

3 Correlation Report Revision History

Rev 1.0: 12/09/2013

-First release from Wipro.

4 TIPS

-If data is unavailable for any of the sections, please type "UA". If a section is not applicable for a model category please type "NA".

5 Template Revision History

Rev 1.0: 01/22/2009

- Initial revision based on IBIS Quality Spec 1.0

Rev 1.1: 07/10/2009

-Template updated based on IBIS Quality Spec 1.1as (draft) dated 06/02/2009

-New Quality Checklist added

Rev 1.2: 12/30/2009

-Template updated to meet IBIS Quality Spec 2.0 ratified on 10/30/2009

Rev 2.0: 02/15/2010

-Renamed template as IBIS_Correlation_Report_template_2p0.doc

-Removed IBIS Model Checklist from the report. This report is only for correlation purposes. Use IBIS Model Checklist for Quality Analysis

Rev 2.1: 06/02/2010

-Template updated to meet AEDC requirements

Rev 2.2: 07/08/2010

-Updated file naming convention for correlation report and quality checklist

Rev 2.3: 09/02/2010

-Updated how correlation waveforms should convey clear edge correlation using an example waveform correlation picture. This example correlation picture should be deleted in the final correlation report.

-Updated file naming convention for correlation report and quality checklist.

Rev 2.4: 09/15/2010

-Updated correlation waveforms format both for single-ended and differential buffers