REVISIONS			
REV	DESCRIPTION	APPRVD	DATE
A	INITIAL RELEASE		
D	TO IMPROVE SIGNAL INTEGRITY		03-21-08
F	MADE SCHEMATIC CHANGES TO U4.1,2,3 AND 4		06-25-08
G	CHANGED FOOTPRINTS SWITCHES, RES ARRAYS, LMH0346SQ. CHANGED DWG NO.	J. Jones	08-01-08

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: PER IPC-4101/24
   - A. LAMINATE: TYPE GFN, GRADE A, CLASS 2, AND TYPE FR-4
   - B. LAMINATE: TYPE GFN, GRADE A, CLASS 2, AND TYPE ISOLA-408 ER= 3.7 BETWEEN LAYERS 1 AND 2.
   - C. FINISHED BOARD: PER SHEET 3
   - D. ALL COPPER LAYERS MUST BE SPACED PER DETAIL A .
   - E. BOARD THICKNESS IS MEASURED INCLUDING TOP AND BOTTOM SIDES FINISHED COPPER AND GOLD PLATING. .058 MIN TO .064 MAX. SOLDERMASK AND SILKSCREEN LEGEND MUST NOT BE INCLUDED IN THE FINISHED BOARD THICKNESS.
   - 1F. ALL INNER LAYERS MUST BE OXIDE COATED.
2. THE CONDUCTOR PATTERN MUST BE ETCHED USING ARTWORK 880600090-001 REV G, SUPPLIED.
3. ALL CONDUCTOR LAYERS MUST BE REGISTERED WITHIN +/- .005 INCH FROM TRUE POSITION.
4. ALL EXTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0015 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
   ALL INTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0010 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
5. BOARD MUST BE NC DRILLED USING DRILL DATA SUPPLIED.
6. DRILL TOLERANCES AND HOLE SIZES ARE FOR FINISHED BOARD:
7. ALL HOLES MUST BE REGISTERED WITHIN +/-.003 INCH FROM TRUE POSITION.
8. MINIMUM ANNULAR RING MUST BE .002 INCH.
9. PLATING:
   - A. PER MIL-C-14550, PLATED THROUGH HOLES MUST BE PLATED WITH .0008 MIN. TO .0015 INCH MAX. THICK COPPER.
   - B. PER MIL-G-45204, IMMERSION GOLD .000002 TO.000007 INCHES OVER .000150 TO .000200 INCHES OF ELECTROLESS NICKEL. NO INTERNAL LAYERS ARE TO BE GOLD PLATED.
10. IMPEDANCE PER SHEET 3: ***+/- 50 +/- 5% AND 75 +/- 5% OHM IMPEDANDE REQUIRED*** USE STREAMLINE LAYER STACK-UP 551600090-001-STREAM LINE.pdf
11. DO NOT REMOVE SPACING GAUGE AT BOARD EDGE.
12. WARP AND TWIST OF FINISHED BOARDS MUST NOT EXCEED .007 INCH PER INCH.
13. SOLDERMASK: PER IPC-SM-840
    - A. SOLDERMASK BOTH TOP AND BOTTOM SIDES.
    - B. SOLDERMASK MUST CLEAR ALL LANDS SHOWN ON GERBER SOLDERMASK LAYERS.
    - C. COLOR BLUE AND SOLVENT FREE.
    - D. LIQUID PHOTO-IMAGEABLE MUST BE .0002 MIN. TO .0008 MAX. INCH THICK
14. SILKSCREEN TOP AND BOTTOM SIDES USING A GLOSSY WHITE, NONCONDUCTIVE, EPOXY BASED INK. NO SILKSCREEN ALLOWED ON GOLD AREAS, ON PADS OR IN HOLES.
15. ROUT BOARD OUTLINE, PER DRAWING DIMENSIONS.
16. VENDOR MUST ENTER VENDOR'S IDENTITY, DATE CODE AND ANY OTHER IDENTIFICATION MARKS ON BOTTOM SIDE ETCH APPROXIMATELY WHERE SHOWN.
17. OTHER VENDOR NOMENCLATURE OR MARKINGS SHOULD NOT BE ETCHED OR SILKSCREENED ON BOARD WITHOUT PRIOR PERMISSION.
18. ALL VENDOR IN-PROCESS MARKINGS, QA STAMPS, ETC. MUST BE PLACED ON THE BOTTOM SIDE OF BOARD.
19. FINISHED BOARD MUST MEET UL94V-0 RATING AND RoHS COMPLIANCE.
20. BOARDS MUST BE NETLIST TESTED FOR OPENS AND SHORTS USING: TESTPOINT REPORT FOR 600090.ipc.
21. DOCUMENTATION THAT MUST BE DELIVERED WITH BOARDS:
    - A. CROSS SECTION REPORT (SPACING BETWEEN COPPER LAYERS AND COPPER THICKNESS)
    - B. ELECTRICAL TEST CERTIFICATION OF COMPLIANCE (ACCORDANCE WITH IPC-ET-652 CLASS II)
    - C. CERTIFICATION OF COMPLIANCE (BOARD HAS BEEN MANUFACTURED TO DRAWING REQUIREMENTS)
    - D. RoHS CERTIFICATE OF COMPLIANCE.
    - E. IMPEDANCE REPORT (REQUIRED IMPEDANCE TRACES PER NOTE 10)
    - F. MICROSECTION CROSS SECTION
22. MUST DELIVER SOLDER SAMPLE BOARD FOR MECHANICAL CHECKING.

BOARD FABRICATION INFORMATION		
	NOMINAL	SMALLEST
AIR GAP	.007	
TRACE SIZE	.010	
HOLE SIZE	.015	
PAD SIZE	.030	
SURFACE MOUNT TOP SIDE ONLY		

UNLESS OTHERWISE SPECIFIED		
DO NOT SCALE DRAWING	DRAWN BY:	DATE
DIMENSIONS ARE IN INCHES	VIRGIL HUTCHINS	6-25-08
TOLERANCES ON: 2 PL DECIMALS +/- .01 3 PL DECIMALS +/- .005 ANGLES 1 DEGREE	CHECKED BY: John Jones	6-25-08
	APPRVD BY: John Jones	08-01-08
MATERIAL: SEE NOTES	APPRVD BY:	
FINISH: SEE NOTES		

National Semiconductor™
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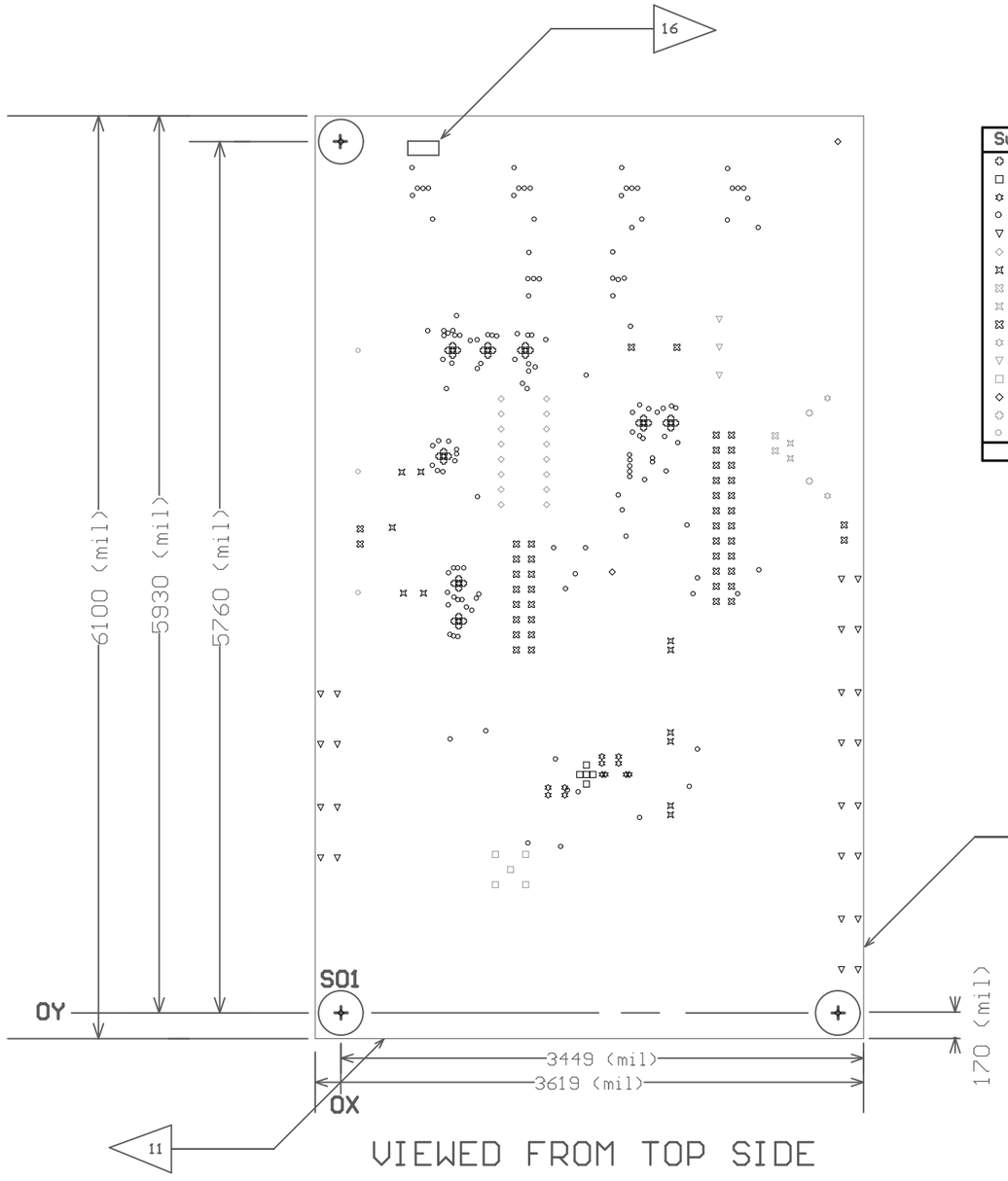
PCB FABRICATION DRAWING
SD346 EVK

B	DWG 551600090-000	G
SCALE: NONE	SHEET 1 OF 3	REV

HOLE DIAMETER (MILS)	DIAMETER TOLERANCE (IN.)
< 25	+.001/-.010
25-125	+/-.003
> 125	+/-.005

6

Symbol	Hit Count	Tool Size	Plated	Hole Type
✪	40	7.874mil (0.2mm)	PTH	Round
□	5	7.992mil (0.203mm)	PTH	Round
✡	12	8mil (0.2032mm)	PTH	Round
○	135	10mil (0.254mm)	PTH	Round
▽	24	13mil (0.3302mm)	PTH	Round
◇	16	25mil (0.635mm)	PTH	Round
⌑	11	28mil (0.7112mm)	PTH	Round
⊠	2	37.008mil (0.94mm)	PTH	Round
⌑	2	37.008mil (0.94mm)	PTH	Round
⊠	46	40mil (1.016mm)	PTH	Round
✡	2	59.843mil (1.52mm)	PTH	Round
▽	3	60mil (1.524mm)	PTH	Round
□	5	63mil (1.6002mm)	PTH	Round
◇	5	125mil (3.175mm)	PTH	Round
✪	2	127.953mil (3.25mm)	PTH	Round
○	3	146mil (3.7084mm)	PTH	Round
	313 Total			



VIEWED FROM TOP SIDE

VIEW FROM TOP SIDE

23 DO NOT CUT BACK GND (LAYERS 2) FROM BOARD EDGE

24 MAY CUT BACK CONNECTOR TOP ETCH PAD FROM BOARD EDGE .005 MAX TO AVOID PEEL BACK BROM BOARD EDGE.

880600090-001 Rev G - Mech Layer 1(Board Outline)

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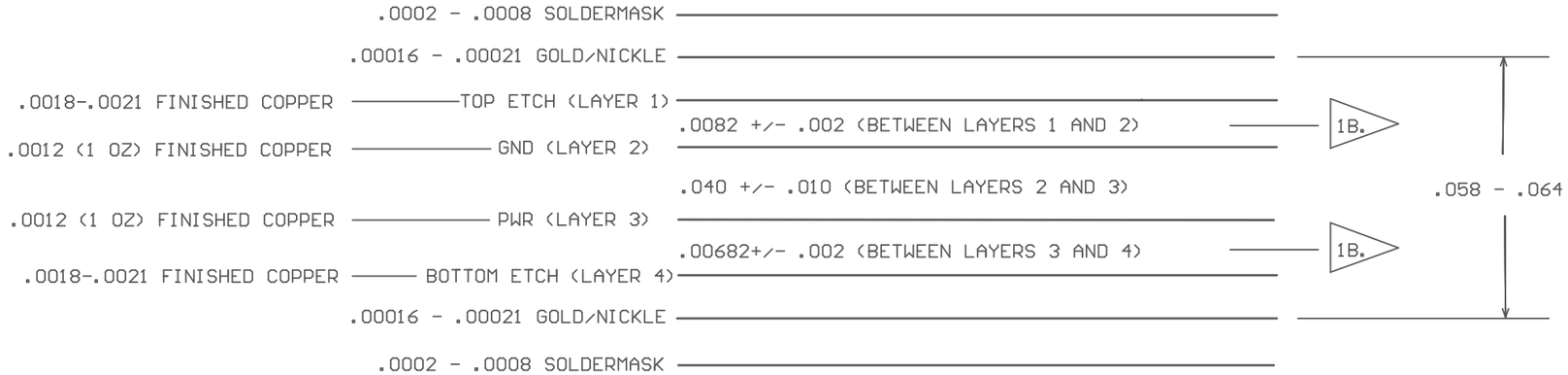
PCB FABRICATION DRAWING
SD346 EVK

B	DWG 551600090-000	G
SCALE: NONE	SHEET 2 OF 3	REV

10 1B. SEE SHEET 1 NOTE 10

IMPEDANCE	LAYER	TRACE	SPACE BETWEEN TRACES	TRACE
5% 100 OHM DIFFERENTAL	T-ETCH (TOP SIDE)	10	10	XX
5% 50 OHM SINGLE END	T-ETCH (TOP SIDE)	13.5	XX	XX
NONE	OTHERS	OTHERS	XX	XX



DETAIL A

LAYER STACK-UP
SCALE: NONE

1A. 1O. 1B. 9B. 1C. 1D.

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PCB FABRICATION DRAWING
SD346 EVK

B	DWG 551600090-000	G
SCALE: NONE	SHEET 3 OF 3	REV