QFN PACKAGE Q&A

Q. What is a QFN?

A: Quad Flatpack No lead (QFN) is a leadless package with peripheral terminal pads, and an exposed die pad for mechanical and thermal integrity. The package can be either square or rectangular.

Q: What applications should I consider using QFN packages in?

A: QFN package could be used in a variety of applications. Applications requiring low standoff heights, improved thermal performance, reduced size or reduced weight are good candidates for QFN design-in. Cell Phones, PDAs , Portable Music and Video players can significantly benefit from this package.

Q: How does QFN pin-out compare to TSSOP, SOIC or SSOP?

A: The new QFN package offerings from Texas Instruments allow for a conventional pin-out scheme similar to traditional dual in-line packages. Function to pin number assignments in QFN are assigned the same pin number as in TSSOP and other dual in-line packages

Q: Is this a lead-free (Pb-free) package?

A: Yes, these QFN packages are Pb-free with matte tin finish, and comply with lead-free environmental policies. The finish is two-way compatible, meaning that both Pb-free pastes and SnPb pastes solder well. The Pb-free solder recommendation is the Sn-Cu-Ag metallurgy. Check with your local TI Field Sales representative for sample availability.

Q: Is there a concern with tin-plating and whiskers?

A: Matte tin finish is a different process than conventional tin-plating, and has shown to be resistant to tin-whiskering.

Q: What size land pad should I design on my board for these packages?

A: Land pad and exposed pad design is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in the application note. Experimentation with QFN packages of similar size has shown that these packages can easily withstand greater than 1000 cycles from -40 to 125°C (15 minute dwell) on a 0.8 mm thick PCB with OSP pads with the exposed pad soldered. Data has shown characteristic life values of >3000 cycles.

Q: What routing choices do I have when using QFN packages?

A: The pad design is wide enough to allow for via-in-pad routing techniques to be employed on an economical basis. Single layer routing or standard via outside the package outline is also feasible because of flow-through design.

Q: Can I mount QFN packages on the bottom side of the PCB board?

A: Yes you can. The ideal 2nd reflow profile is the same as the 1st (reflow profile is recommended in the application note). The package is adequately secured during the second reflow as long as the exposed pad is soldered. TI recommends designing stencils per the application note, which complies with IPC-7525.

Q: Can the packages be reworked on the boards?

A: Yes, there are rework and repair tools and equipment available. Rework processes will not differ significantly from BGA processes.

Q: How do board assembly yields of QFN compare to BGA's?

A: The yields have been proven to be similar due the ability of both of these packages to self align during reflow.

Q: What alignment accuracy is possible?

A. Alignment accuracy for the 0.50-mm pitch package is dependent upon board level pad tolerance, placement accuracy, and terminal lead position tolerance. Nominal terminal lead position tolerances are specified at ± 50 microns. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q: Are there specific recommendations for SMT processing?

A: Texas Instruments recommends using a terminal lead for the alignment of QFN packages. This method is the most accurate assuming the machine is capable of indexing off the terminal lead, but this method could be slower than using the package outline for alignment. The package outline can also be used for alignment, but this could result in less accurate placement. Process characterization of placement, paste characteristics, stencil yield, and reflow parameters should be accomplished so that the placement process chosen requires minimal time, and self alignment corrects minor placement deviations.

Q: Can the solder joints be inspected after reflow?

A: Visual inspection can be used to inspect the outside part of the solder joint. Standard BGA inspection processes such as lamographic X-ray techniques can be used for a more thorough inspection.

Q: Can I probe test a mounted QFN?

A: Yes. Peripheral solder joints may be probed, and grounded exposed pads can be probed at the side of the package where the tie bar has been exposed.

Q: Do I need to solder the exposed die pad to the board?

A: Power dissipation is greatly enhanced by soldering the exposed die pad to the board, and the board level reliability during temperature cycling and other board/package stress tests is greatly improved.

Q: Can I use thermal vias under the exposed pad/PWB interface?

A: Using thermal vias enhances power dissipation by 1.5-2X. If your application requires enhanced thermal performance, thermal vias will help.

Q: Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?

A: EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:
Solid ground and power planes should be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation. Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation. Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced by using this method.

Q: What are the standard shipping quantities?

A: Currently, tape and reel quantities of 1000 units are available.