Optimal output filter design for microprocessor or DSP power supply

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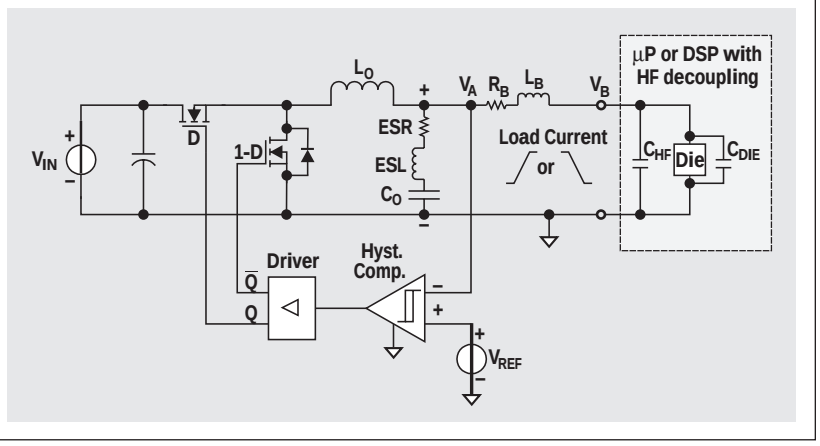
Introduction

Tight dynamic tolerances for supply voltages of next-generation microprocessors and DSPs at high slew-rate transitions from sleep mode to full-power operation and backwards require fast-transient-response power supplies along with a special decoupling technique. The analysis and optimization of synchronous-buck converters with hysteretic controllers at load-current transients has been presented in References 1 and 2. This article presents a detailed optimization procedure for output filter selection to meet the load-current transient requirements at minimum cost and size. The electrolytic, OS-CON, POSCAP, and ceramic capacitors are compared in a power supply that corresponds to Intel's VRM 8.4 requirements (see Reference 3). These design examples outline the trade-off between cost, size, and efficiency of the power supply and help the user to choose the optimal solution for any particular application.

Figure 1. Analyzed model of power distribution system during load-current transient



Microprocessor or DSP power supply model

The model shown in Figure 1 presents the microprocessor or DSP power distribution system.

The model includes a synchronous-buck converter with an ideal controller, output inductor (L_O), and output bulk capacitor (C_O) with equivalent series resistance (ESR) and equivalent series inductance (ESL). The equivalent resistor (R_B) represents the added resistance of traces and connectors and characterizes a resistive voltage drop through the supply path. The equivalent inductor (L_B) characterizes an inductive voltage drop through the traces and connectors. The ideal controller has a feedback loop without any delay and limitations on the duty cycle covering the whole possible range from zero to one. In such a case, the converter has minimum peak-to-peak output-voltage transient. The hysteretic controllers from Texas Instruments with relatively small delays and a narrow hysteresis window, such as TPS5210, TPS5211, TPS56XX, TPS56100, and others, are good approximations of the ideal controller with the optimal transient-response characteristics.

Analytical equations were derived for the voltages and currents through the main components of the model in Figure 1 as a function of time both for the load-current step-down and step-up transients. These equations were included in the MATHCAD program to view the voltage and current transient waveforms and to build optimization curves that are described later in this article. To verify the derived equations, the MATHCAD transient waveforms were compared with the measured ones under the same conditions. The measurements were fulfilled on the evaluation board TPS5210SLVP-119. As one can see from Figure 2, the theoretical and measured waveforms are very close for the load-current step-down and step-up conditions.

Impact of system parameters on transients

Dependence on switching-cycle position

The output-voltage transient response depends on the position of the switching cycle when the load-current transient occurs. If the load current steps down, the excessive energy of an output inductor has to be delivered to the output capacitor. The worst case for the step-down transition is when the transient occurs at the end of an upper FET conduction time because the inductor current has its maximum. At this moment the inductor stores the maximum energy while the output ripple voltage also has its maximum. So the transient effect is the most significant at this moment, causing the greatest output voltage spikes in comparison with any other moment (Figure 3).

By contrast, the worst case for the step-up transition is when the transient happens at the end of the switching cycle, because the inductor current and output voltage ripple have their minimum at this moment. Only the output capacitor supplies the load during the step-up transient, while the inductor restores its energy and current to the new load-current level.

Influence of supply-path parasitics

The voltage transient waveforms on the converter output pins (point V_A in Figure 1) and on the microprocessor package supply pins (point V_B in Figure 1) are different because the supply-path resistance (R_B) and inductance

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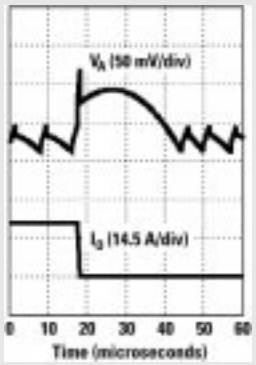
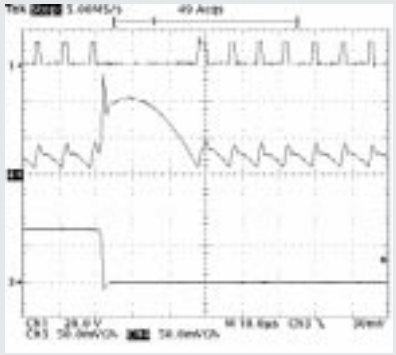
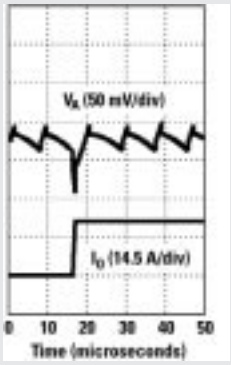
Figure 2. Theoretical (a, c) and measured (b, d) waveforms during load-current step-down (a, b) and step-up (c, d) transitions



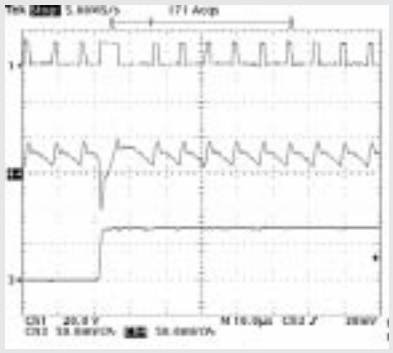
(a) Theory



(b) Measurement



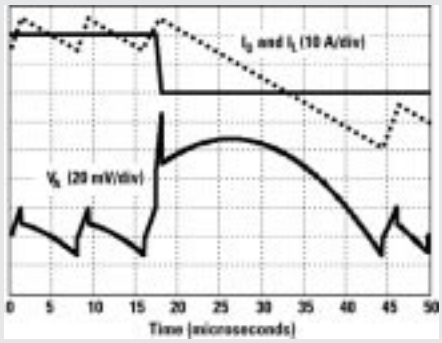
(c) Theory



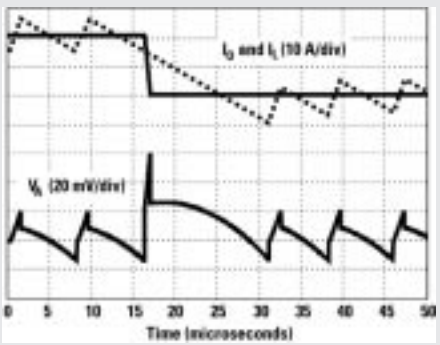
(d) Measurement

Theoretical waveforms show the output voltage (top) and load-current (bottom) transients. Measured waveforms include voltage (V_{DS}) of the low-side FET (Ch1: 20 V/div), output voltage (Ch4: 50 mV/div), and load current (Ch3: 14.5 A/div).

Figure 3. Output voltage (bottom curve) and inductor current (dashed) waveforms for the different instants when the load-current (top, solid) step-down transition occurs



(a) Worst case: Transient occurs at the end of the upper FET's conduction time



(b) Best case: Transient occurs at the end of the switching cycle

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(L_B) cause the additional voltage drop. If the output current step (ΔI_O) and slew rate (SR) are defined as

$$\Delta I_O = I_{O(MAX)} - I_{O(MIN)} \text{ and} \quad (1)$$

$$SR = \Delta I_O / t_O , \quad (2)$$

where t_O is the output current transition duration, then the additional voltage drop (V_B) through the supply paths is defined by

$$V_B = VR_B + VL_B = \Delta I_O \times R_B + SR \times L_B . \quad (3)$$

Assume that R_B = 1.5 mohm; L_B = 1.0 nH; ΔI_O = 23.8 A; and SR = 20 A/µs in accordance with the VRM 8.4 requirements. Then the voltage drop through the supply path is

$$V_B = 35.7\,mV + 20\,mV = 55.7\,mV.$$

For the 1.65-V output power supply, this means almost 3.8%. This example shows why it is important to keep the output filter capacitors as close as possible to the microprocessor package to avoid a significant voltage drop due to supply-path parasitics.

Optimal output inductor

It seems obvious that the lower output inductor value enables better transient-response characteristics because of faster inductor current change to the new level after the load-current transient occurs. The example in Figure 4 shows that, in reality, after some optimal point (Figure 4b), further decreasing of the inductor value increases the peak-to-peak transient amplitude because the output ripple rises significantly. As shown later, the optimal inductor value depends on switching frequency and the type of output bulk capacitors.

Two extreme values of an output-voltage transient

Typical load-current transient waveforms are shown in Figure 5. The output-voltage waveform has two extreme values, Vm1 and Vm2. For most applications, the transient slew rate of the load current is much higher than the maximum slew rate of the output inductor current. Because of that, the first extreme value, Vm1, depends mainly on the output capacitor and supply-path parasitics. It is not affected significantly by the controller transient-response characteristics.

The second extreme value, Vm2, depends on resistive components ESR and R_B, capacitive component C_O, inductor value L_O, and the converter characteristics, including switching frequency and type of control. Vm2 does not exist if the following inequality is fulfilled:

$$ESR \times C_O > m \times t_s \times \left(\frac{1}{2} + \frac{\Delta I_O}{\Delta I_L} \right), \quad (4)$$

where t_s is a switching cycle, and ΔI_L is a peak-to-peak ripple portion of the output inductor current. The parameter m depends on the type of transient. For the worst-case step-down transient, m = 1 – D, and for the worst-case step-up transient, m = D. Of course, only the first spike has to be considered in this situation during the design.

Assume that the output filter capacitors are connected in parallel and that each capacitor has the characteristics C_O1, ESR1, and ESL1. The number "1" after a parameter means that that parameter relates to one of many capacitors connected in parallel. It is shown in Reference 2 that if ΔVreq is the maximum allowable peak-to-peak transient tolerance, then the required number of output bulk capacitors, N1 and N2, to meet the conditions Vm1 = ΔVreq and Vm2 = ΔVreq, respectively, can be defined as in Equations 5 and 6 at the bottom of this page. Equations 5 and 6 can be used for the optimal output filter design.

Active droop compensation

One can see from Equations 5 and 6 that the number of capacitors can be lowered by increasing ΔVreq. The active droop compensation is an effective technique to do that. The droop compensation means that the dc output-voltage level of the converter is set to the highest level within the specification window at no-load condition and to the lowest level at full-load. This approach degrades the static load regulation but increases the output-voltage dynamic tolerance by as much as twofold, thus reducing the number of bulk capacitors required. For the same output filter, this technique allows a decrease in the peak-to-peak output-voltage transient response. The popularity of this idea is confirmed by the fact that it has numerous names like "Programmable Active Droop™," "Active Voltage Positioning," "Adaptive Voltage Positioning," "Summing-Mode Control," etc. The transient waveforms with and without active droop compensation are shown in Figure 6. One can see that without droop compensation (Figure 6a), the output-voltage peak-to-peak amplitude is 146 mV and exceeds the requirements, as shown by the cursors. With droop compensation (Figure 6b), the peak-to-peak transient is only 78 mV, keeping the

$$N1 = \frac{\frac{ESL1}{t_O} + ESR1 + \frac{t_O}{2 \times C_O 1} + \left(ESR1 + \frac{t_O}{2 \times C_O 1} \right) \times \left(1 - \frac{t_O}{m \times t_s} \right) \times KL}{\frac{\Delta Vreq}{\Delta I_O} - \frac{L_B}{t_O} - R_B} \quad \text{and} \quad (5)$$

$$N2 = \frac{\frac{1}{2} \times \left[\frac{m \times t_s}{C_O 1} - \frac{t_O}{C_O 1} + \left(ESR1 + \frac{ESR1^2 \times C_O 1}{m \times t_s} + \frac{m \times t_s}{4 \times C_O 1} \right) \times KL + \frac{m \times t_s}{C_O 1} \times \frac{1}{KL} \right]}{\frac{\Delta Vreq}{\Delta I_O} - R_B}, \quad (6)$$

where $KL = \frac{V_{OUT} \times (1-D) \times t_s}{L_O \times \Delta I_O}$, and $D = V_{OUT}/V_{IN}$ is a duty cycle.

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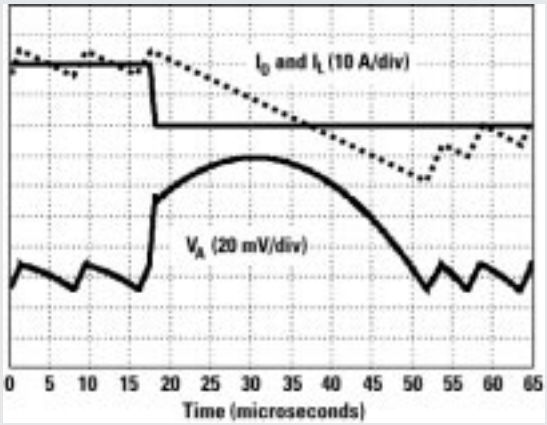
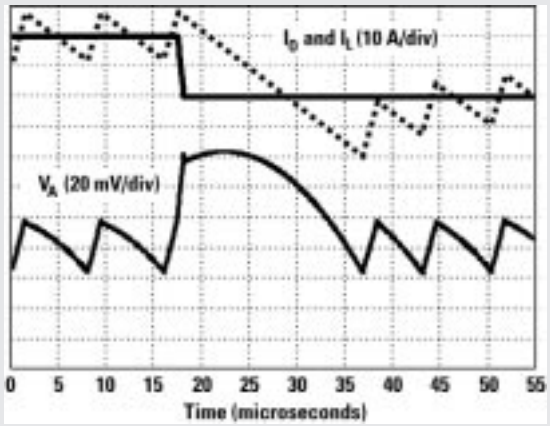
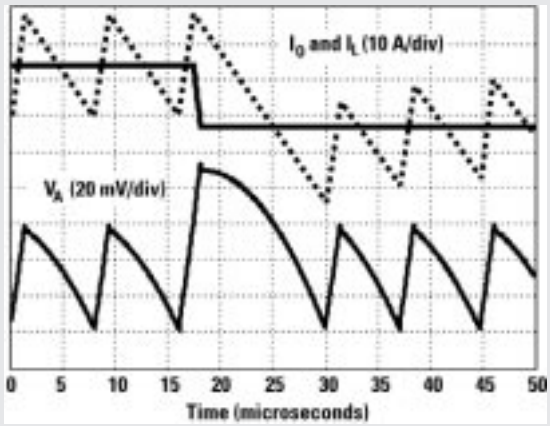
Figure 4. Transient waveforms with different inductor values (L_O)



(a) L_O = 1.6 µH, $V_{O(MAX)}$ = 79 mV, t_{recov} = 34 µS



(b) L_O = 0.8 µH, $V_{O(MAX)}$ = 62 mV, t_{recov} = 19 µS



(c) L_O = 0.4 µH, $V_{O(MAX)}$ = 72 mV, t_{recov} = 12.5 µS

Figure 5. Typical load-current transient waveforms

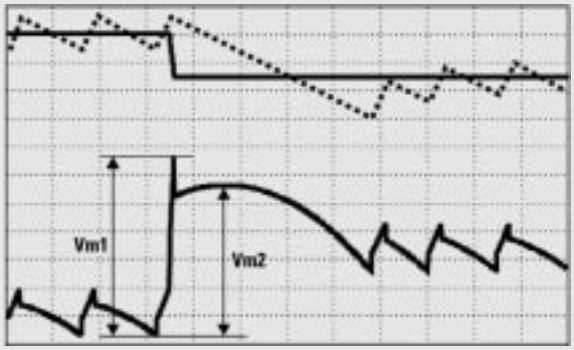
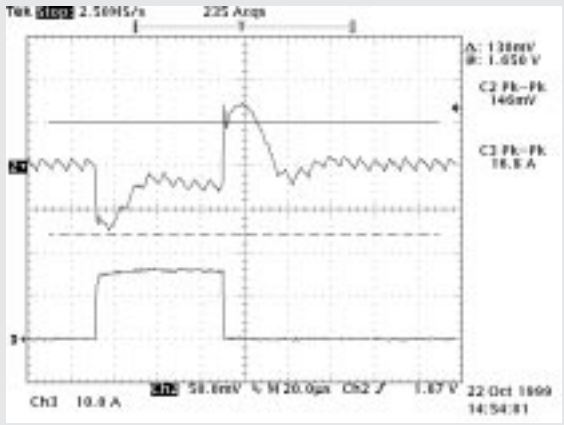
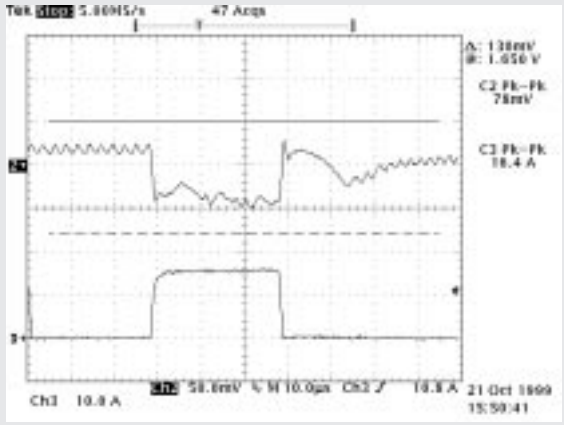


Figure 6. Active droop compensation technique



(a) Without droop compensation ($V_{OUT(P-P)}$ = 146 mV)



(b) With droop compensation ($V_{OUT(P-P)}$ = 78 mV)

Channel 2 shows output voltage (50 mV/div.), Channel 3 shows load current (10 A/div.), and the cursors show the required limits for the output voltage.

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output voltage well within the requirements for the same load-current transient conditions.

Optimal output filter selection procedure

The following step-by-step design procedure shows how to select output capacitors, an inductor value, and a switching frequency that are optimized for a specific application. For this design the typical VRM 8.4 requirements are used as an example:

V_{IN} = 5 V, V_{OUT} = 1.65 V, ΔV_{OUT} (dc) = –80 mV ÷ +40 mV, ΔV_{OUT} (ac) = –130 mV ÷ +80 mV, $I_{O(MAX)}$ = 26 A, $I_{O(MIN)}$ = 2.2 A, ΔI_O = 23.8 A, ΔVreq = 180 mV, SR = 20 A/µs, R_B = 1.5 mΩ, and L_B = 1 nH.

1. Definition of the worst-case transient

Select which type of transient, a load-current step-up or step-down, is the most important to optimize. The transient, caused by the load-current transition, is completed when the inductor current has reached the new steady-state current level. The inductor current slew rate depends on the voltage applied to the inductor. This voltage is equal to $V_{IN} – V_{OUT}$ during a load-current step-up, or to V_{OUT} during a load-current step-down. For most microprocessor and DSP applications, usually $(V_{IN} – V_{OUT}) > V_{OUT}$. This means that the worst case is defined by the load-current step-down transition because the lower voltage, V_{OUT}, changes the inductor current more slowly. In such a case the load-current step-down has to be optimized first; then, after the output filter selection, the load-current step-up transient has to be verified to meet requirements.

2. Maximum peak-to-peak dynamic tolerance

An accurate output-voltage budget needs to be done to determine a maximum dynamic output-voltage tolerance, ΔVreq. The dynamic and static supply-voltage limits have to be compared with all potential tolerances, including set-point accuracy, time and temperature variation, and line and load regulation. Use the droop compensation and adjust the nominal output voltage to get the maximum possible ΔVreq. Figure 7 shows the output-voltage budget calculation for this particular example. For the step-down transient, the required window is:

Vreq = 1,730 mV – 1,570 mV – 2 mV – 2 × 6 mV – 50 mV = 96 mV

For the step-up transient, it is:

Vreq = 1,690 mV – 1,520 mV – 2 mV – 2 × 6 mV – 50 mV = 106 mV

The required droop compensation is:

Droop = 106 mV – 16 mV – (1,570 mV – 1,520 mV – 2 mV) = 42 mV

Table 1. Comparison of different types of capacitors

TYPE	VENDOR	PART NUMBER	V_{dc} (V)	CAPACITANCE (µF)	ESR (mohm)	ESL (nH)	SIZE (mm)	RELATIVE COST
Aluminum electrolytic	Rubycon	6.3ZA1000	6.3	1000	24	4.8	∅10 x 16	1
OS-CON	Sanyo	4SP820M	4	820	8	4.8	∅10 x 10.5	6
POSCAP	Sanyo	4TPC150M	4	150	40	3.2	7.3 x 4.3 x 1.9	3
Ceramic	Murata	GRM235Y5V226Z10	10	22	20	0.5	3.2 x 2.5 x 1.35	0.7

Figure 7. Output-voltage budget for VRM 8.4 power supply (not scaled)

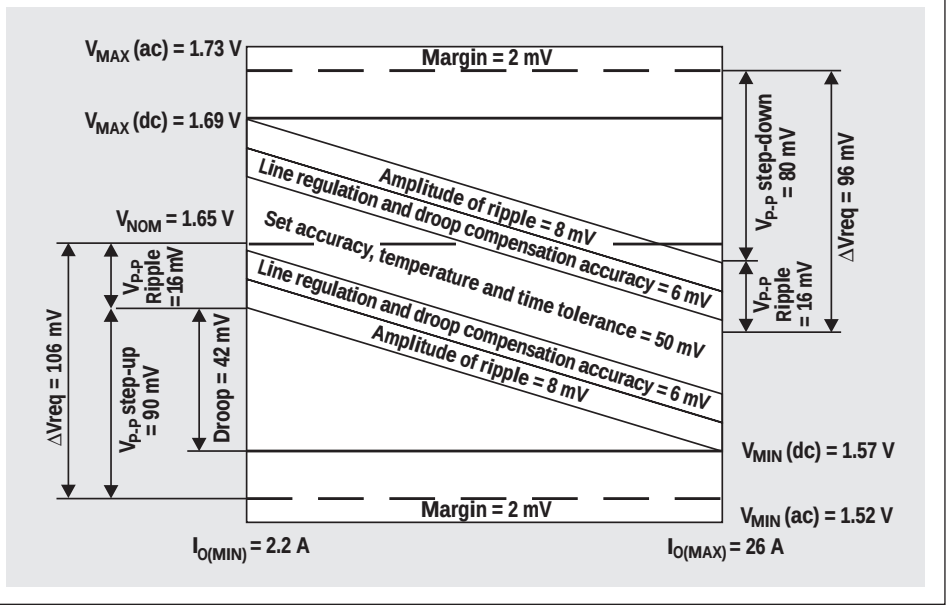
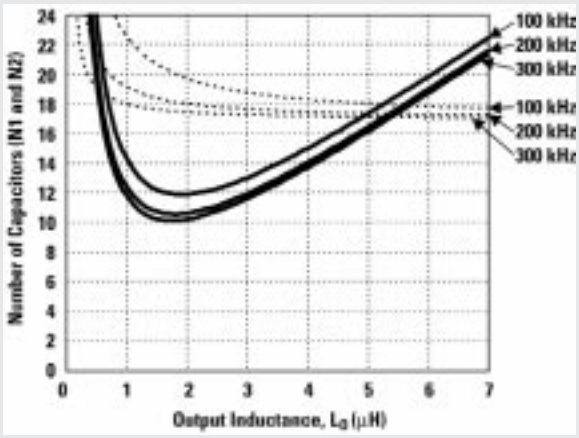
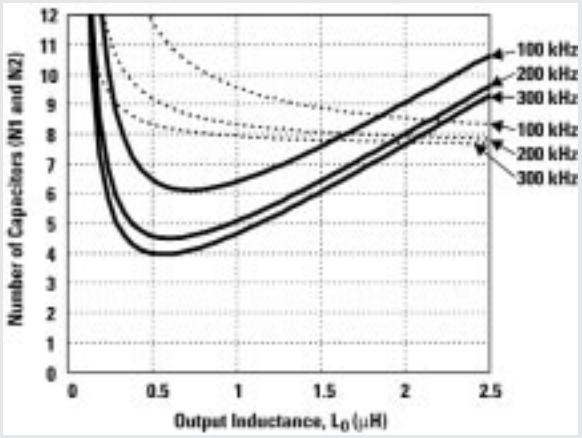


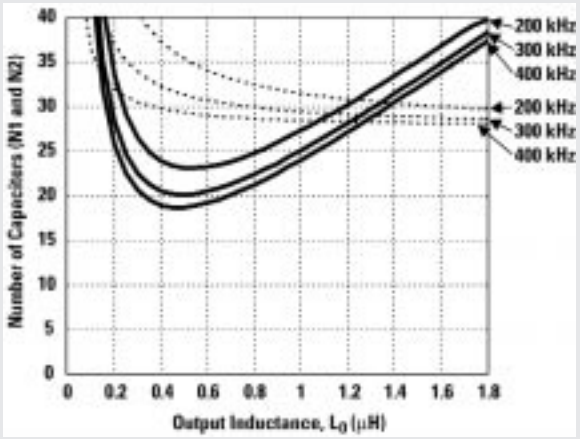
Figure 8. Optimization curves N1 (dashed) and N2 (solid) as a function of output inductance (L_O) and switching frequency (f_s) for different types of capacitors



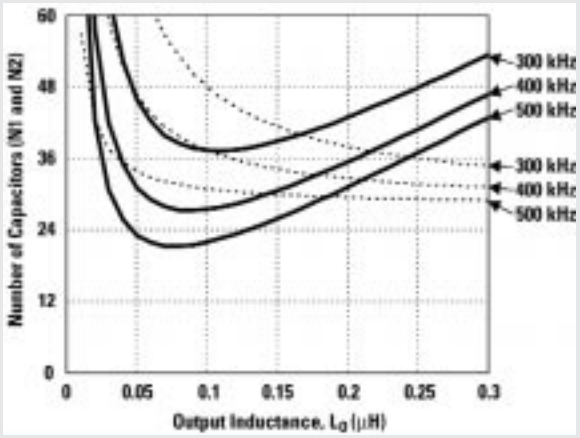
(a) Aluminum electrolytic



(b) OS-CON



(c) POSCAP



(d) Ceramic

3. Output bulk capacitor selection

Equations 5 and 6 show that the number of output bulk capacitors, N1 and N2, can be decreased if capacitors with low ESL1, ESR1, and high enough capacitance, C_O1, are used. Electrolytic, OS-CON, POSCAP, and ceramic capacitors are the most popular candidates for this application. Table 1 shows the main characteristics of capacitors that have been selected for the comparison in this design. This table does not restrict the list of capacitors and vendors, and the selected capacitors illustrate only the trade-off between different types based on cost, size, reliability, and efficiency. The capacitor vendors usually provide the impedance and ESR curves based on measurements with sinusoidal waveforms. The ESL value usually is not specified. For better design accuracy, the ESR and ESL have to be estimated by measuring capacitor reaction on the high-slew-rate linear charge or discharge current if the capacitor is intended for use in microprocessor or DSP power supplies. Because of this, some numbers in the table may differ from the specification data.

For the ESL and ESR estimate, the parasitic inductance and resistance of the traces and vias required for capacitor mounting have to be included. Usually, many smaller capacitors connected in parallel yield lower ESL and ESR compared with larger capacitors. Small surface-mount capacitors can be located as close as possible to the microprocessor or DSP package. This is important to minimize R_B and L_B values.

4. Output filter optimization curves

The number of capacitors, N1 and N2, as a function of output inductance (L_O) and switching frequency ($f_s = 1/t_s$) are shown in Figure 8 for the electrolytic, OS-CON, POSCAP, and ceramic capacitors.

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One can see that the first spike curves, N1 (dashed), do not have an extreme value and increase rapidly at low output inductance. The second spike curves, N2 (solid), have minimum value at some output inductance. In most cases the curves N1 cross the curves N2 at two points. The lowest-integer number of output capacitors, which is still higher than the cross-section of curves N1 or N2, is the minimum number that satisfies the requirements. The inductance has to be selected as close as possible to the cross-section points of both curves, or in-between. To avoid variation in the transient response due to component tolerances, it is wise to select the inductance in the region where the slew rate of the curves is not too high.

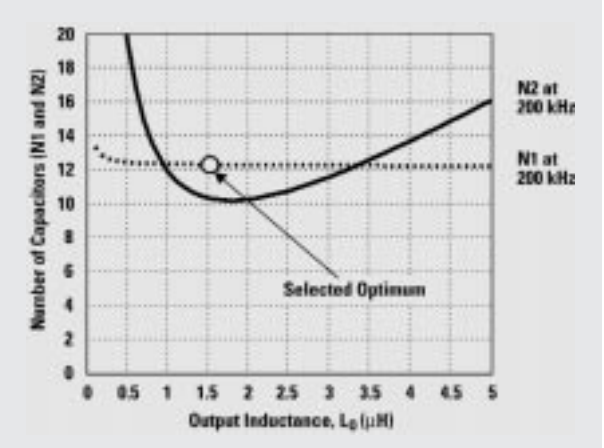
It is shown that the number of aluminum electrolytic and OS-CON capacitors does not drop significantly at frequencies higher than 200 kHz. The POSCAP capacitors work effectively at up to 350 kHz. The ceramic capacitors work well at 500 kHz and at higher frequencies. Here, the switching frequency is rather restricted by the power losses in semiconductors.

One can see that, for the aluminum electrolytic and OS-CON and partly for the POSCAP capacitors, the curve N1 is typically higher than the curve N2. This is because they have relatively high ESL1 and large capacitance C_O1. The number of capacitors N1 also rises rapidly if the supply-path stray inductance is too high. The additional high-frequency decoupling helps to decrease equivalent ESL and to reduce the number and cost of bulk capacitors.

In accordance with this design example, aluminum electrolytic and OS-CON capacitors in the 100- to 200-kHz switching-frequency range and with the output inductance value around 1 to 2.0 µH are preferable for applications requiring low power losses. The POSCAP capacitors have lower ESL1, but their number is higher because of relatively high ESR1 and low capacitance C_O1. Their preferable application is low-height DC-DC converters with a switching-frequency range from 250 to 300 kHz. The optimal value for the output inductor is around 0.7 µH. The number of ceramic capacitors might be too large at frequencies lower than 500 kHz. Their preferable application area is minimum-size, high-frequency converters. One can see that their ESL1 is very low, but the impact of the second extreme value is significant because of the low capacitance C_O1. The system cost, temperature range, available space, reliability, cooling conditions, and life of the product have to be considered during final selection of the output filter.

Assume that the aluminum electrolytic capacitor has been selected for further consideration. Figure 8a shows that, at 200-kHz switching frequency and with a 2-µH inductor, the required number of capacitors is 18 because of the high first spike. The number of electrolytic capacitors in this case can be decreased if a few high-frequency decoupling capacitors are added to decrease the impact of ESL and L_B. Seven 805-size ceramic capacitors of 1 µF each have been added. Each capacitor has an ESL1 of 2.6 nH, including inductance of vias and traces. The equivalent inductance of 7 capacitors placed very close to the microprocessor is 2.6 nH/7 = 0.37 nH. For this design, the load-current slew rate and supply-bus inductance are SR = 20 A/µs and

Figure 9. Optimization with aluminum electrolytic capacitors



New optimization curves N1 and N2 for the aluminum electrolytic capacitors with additional high-frequency decoupling

L_B = 1 nH. Adding the high-frequency decoupling capacitors decreases the slew rate roughly three times in this case:

$$SR_{new} = SR \times (0.37\ nH/1\ nH) = 7.4\ A/\mu s$$

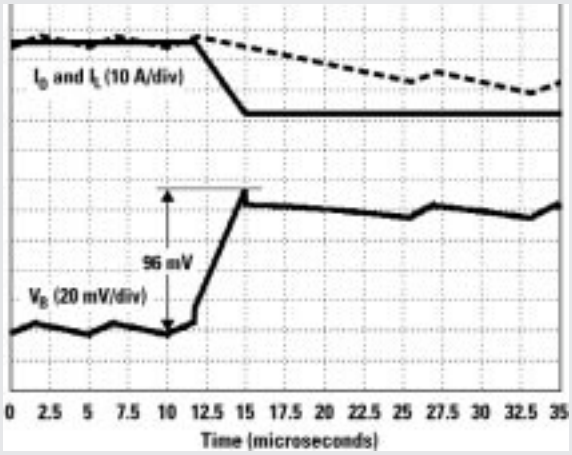
The new optimization curves for the aluminum electrolytic capacitors with high-frequency decoupling are shown in Figure 9. One can see that curves N1 and N2 are much closer to each other because the high-frequency decoupling lowers the effect of inductive parasitics. The optimal inductor value, 1.5 µH, is selected, and the number of capacitors is 12 instead of 18 without the additional 7 ceramic capacitors of 1 µF each.

The transient waveforms based on this design are shown in Figure 10. One can see that the output voltage at low load is shifted at higher levels because of active droop compensation. Both step-up and step-down transients are acceptable for microprocessors in accordance with the VRM 8.4 requirements.

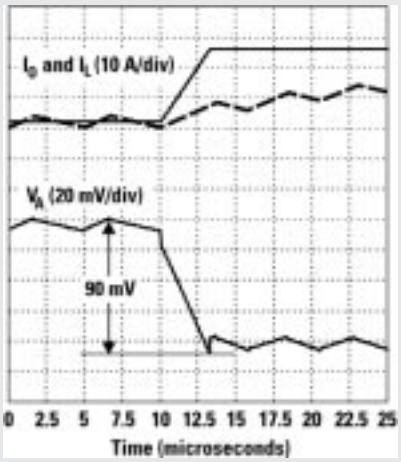
Conclusion

A power-supply system for powering high-slew-rate transient loads, such as a microprocessor or DSP, was analyzed. The selected model, based on practicality and accuracy, included a synchronous-buck converter with the controller, output inductor, output bulk capacitor with parasitics, and power-supply traces between the bulk capacitors and the microprocessor or DSP package. The accuracy of the model and derived equations was confirmed by comparison with the measurement results. It was shown how the different parameters of the model influence transient-response characteristics. A step-by-step optimal design procedure for the minimum-size and least costly output filter was suggested based on the derived equations. A design example of a DC-DC converter in accordance with the VRM 8.4 requirements was presented, and different types of bulk capacitors like aluminum electrolytic, OS-CON, POSCAP, and ceramic were compared.

Figure 10. Transient waveforms of an optimized output filter with aluminum electrolytic capacitors



(a) Load-current step-down



(b) Load-current step-up

References

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Related Web sites

http://power.ti.com
www.ti.com/sc/docs/tools/analog
www.ti.com/sc/select