Reducing PCB design costs: From schematic capture to PCB layout

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Modern EDA software packages provide a host of tools that allow designers to draw schematics in order to produce printed circuit boards. Understanding the basic requirements of these tools and the interactions between them can help to reduce the cost of PCB designs.

The basics

Schematic capture packages contain various tools and features that make the process of entering a schematic and documenting a circuit easy on the designer. One common feature among popular schematic capture packages is an array of libraries. Another is the ability to output netlists that are compatible with various simulation and PCB layout packages. The schematic capture process creates a database of symbolized parts and a netlist describing the connections between the symbols.

PCB layout packages have their own suite of tools and features designed to streamline the creation, verification, and documentation of a physical printed circuit board. All the board designer needs to do is define the outline of the board, add footprints from a decal library, import the netlist, and route the connections. Netlist comparisons will verify that the board matches the schematic. Online error checking warns of open- or short-circuit conditions. Design rules can be set up to check things such as matched net lengths, routing stubs, and parallelism.

Sounds simple, doesn't it? Draw a schematic, output the netlist, and sit back to wait for your prototype assemblies. Simple, that is, until the call from the assembly shop tells you that a part does not match its footprint, or you spend hours tracking down a diode or capacitor that was laid out backwards. An understanding of the process that takes place when exporting a schematic netlist is necessary to ensure your board layout will be correct.

Figure 1. Schematic library symbols

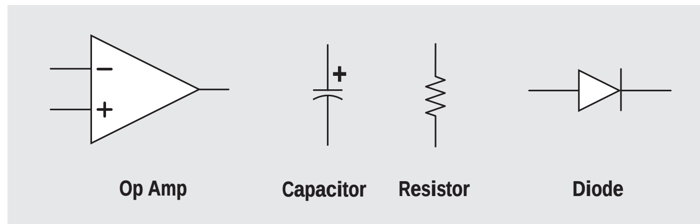
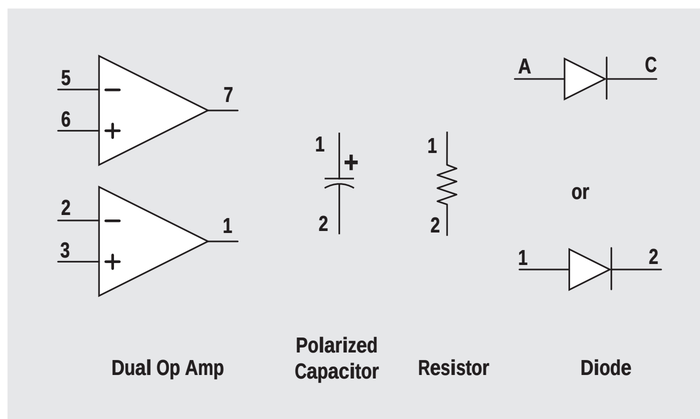


Figure 2. Component electrical pin numbers



Schematic libraries

Schematic libraries are based on familiar symbols such as those shown in Figure 1.

The symbol libraries are generic by nature. They are intended as building blocks for various part types. Schematically speaking, the same resistor symbol can be used for a 1/8-watt surface mount or a 100-watt chassis-mount device. The op amp symbol could be a single device in a 5-pin SOT package or a dual device in an 8-pin DIP. To create a valid schematic part, these symbols must, at a minimum, have electrical pin numbers assigned and be saved in a part type library.

Quite often, this is the extent of the part type libraries supplied with the schematic capture tool (see Figure 2). Enough information is given to allow the designer to create a schematic, but information required to create a printed circuit board is missing. As with the symbol library, the vendor-supplied part type libraries are intended as a starting point for a customized user library.

Customizing a vendor-supplied library requires that the user assign attributes detailing the specific part to be used in the design. A generic vendor-supplied part type "resistor," for example, could be copied to a customized user library, be given a footprint attribute "1206," and then be renamed to part type "RES_1206_SMT." When this new part is called from the user library, it would always require that a 1206-size surface-mount footprint be used to represent this device on the printed circuit board.

PCB libraries

The PCB libraries are based on the footprints designated by industry standards. They usually include common surface-mount and through-hole devices. To create a footprint, or decal, pads are arranged in a specific pattern and designated with an electrical pin number. Figure 3 is an example of some common footprints shipped with most PCB design tools.

As with the schematic symbol library, one PCB decal can be associated with many different part types. The layout database relies on the pin numbers defined in the schematic library for mapping to a footprint in the PCB library. This process allows two completely different 8-pin devices to use the same 8-pin PCB decal.

Understanding the importance of this problem becomes even more obvious when you consider parts such as diodes or electrolytic capacitors. A generic schematic part called "DIODE," for instance, could be assigned a PCB decal called "D0-41." If the diode is designated in the schematic library with electrical pin 1 as the anode and electrical pin 2 as the cathode, the associated D0-41 footprint must also have the same designations (see Figure 4). Having the pins reversed on the PCB footprint can cause serious problems that can be difficult to debug on an assembled board. Error checking will not catch this type of problem.

Figure 3. Example of common PCB footprints

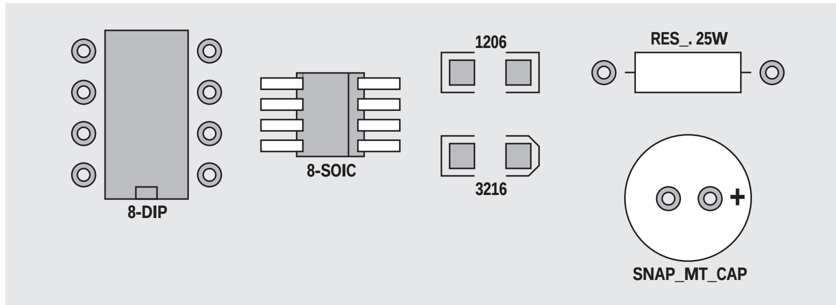
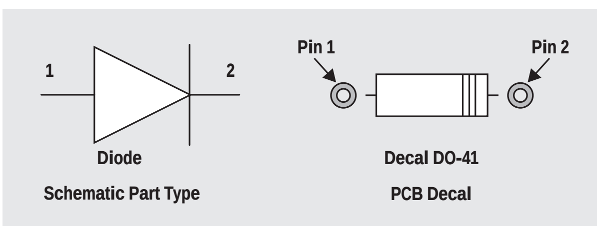


Figure 4. Diode designation



The netlist file

The netlist file is where the schematic and PCB databases come together. The output from a schematic database is formatted to meet the needs of a specific PCB layout package and contains several specialized sections.

The first section usually describes the PCB decals that are needed in the design. If a decal does not exist in the PCB library, the desired part cannot be placed on the board. All schematic part types must be assigned a valid PCB decal before the schematic netlist can be imported to the PCB design database. Most PCB design packages will immediately flag an error and stop processing the netlist file if a decal is missing.

The next section of the netlist file contains the connection, or "rubber band," information. If a decal cannot be found, there can be no connections to route. Other sections may include PCB routing directives, simulation directives, or detailed information for power and ground connections.

Save time and avoid errors

Avoid using different platforms to produce schematic and PCB designs. Most EDA vendors can provide bundled schematic capture and PCB layout packages that are designed to work together. These integrated packages provide a common shell that allows for easier verification of the schematic and board files, and makes processing engineering changes relatively painless. Integrated packages usually allow "back-annotation" as well, so that changes made in a PCB design can be reflected back to the schematic.

The use of a common library can help prevent problems. Develop a system where one regularly updated library serves the needs of all persons involved in design activities. Multiple people creating the same devices in individual libraries will only lead to errors and confusion at layout. If a new part needs to be constructed, build it in a central library so everyone can use it. Review all newly created parts and their associated PCB footprints for accuracy.

PCB layout tools will normally present an error or warning if the schematic part references a PCB footprint with fewer electrical pins than described in the schematic netlist. For example, if a 14-pin device were assigned to an 8-pin decal, there would be an error mapping pins 9 through 14 described in the schematic. If, on the other hand, a 14-pin decal is assigned to an 8-pin device, error flags are not necessarily raised. A PCB decal can have more pins than electrically represented in a schematic; mounting or alignment holes, for instance, are part of a decal. This type of error often goes unnoticed as well. It is usually found after the PCB is fabricated, when someone tries to mount a 14-pin device in a 16-pin decal.

Many companies use outside sources to design printed circuit boards. If an external design house provides your printed circuit board layouts, make sure your engineers are familiar with the tools they use. Sending out a netlist file in the correct format will save time and money. Share your libraries with your vendor so they can save time and avoid having to re-create parts. Create your schematic libraries so that they reference the PCB footprint libraries of your design house.