Product Bulletin

Clock Distribution Circuits (CDC) Family Driving High-Performance Systems

Key Features

- Expanding portfolio of clock distribution circuits (CDC) for motherboard, DIMM and wide range of telcom, automotive and industrial applications
- Cost-effective PLL-based clock buffer/drivers for DIMM applications
- Direct Rambus™ clock generator for 400-MHz differential clock source
- PLL-based clock synthesizers/drivers for multiple frequency generation
- Clock buffer/drivers provide low skew and up to 18 output signals from a single input

Today's personal computers (PC), gaming PCs, workstations, servers, telecommunications switching equipment, internetworking hubs and switches and many other systems must operate at faster speeds and higher frequencies than ever before.

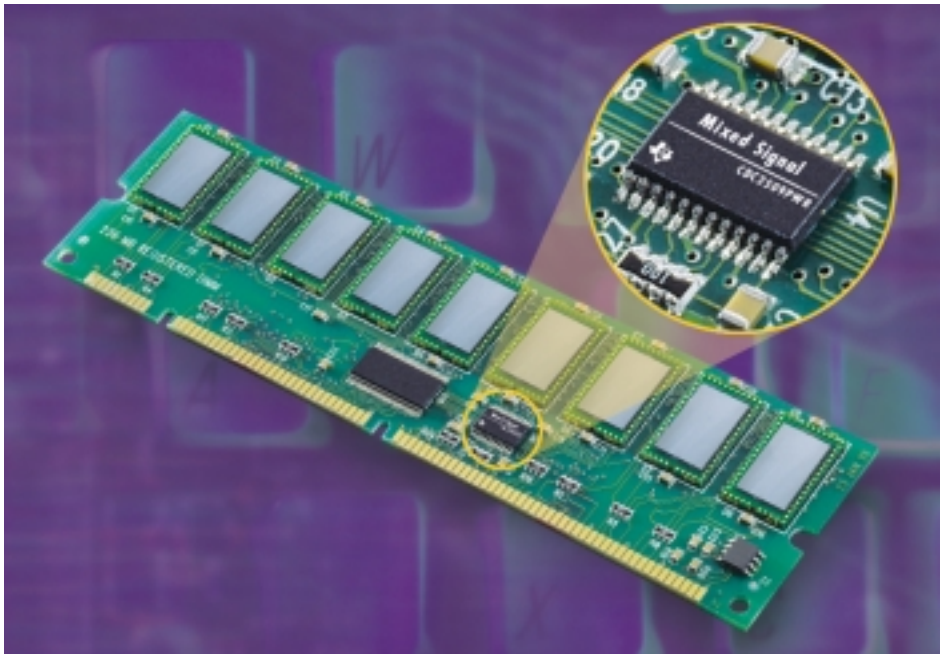
To meet these increasing performance demands, designers must pay special attention to timing delays and skews in clock signal generation, synchronization and distribution.
Designers face the challenge of creating a clocking system that meets tighter timing requirements, lower power consumption and minimized board space – all while keeping system costs in check.

CDCs from Texas Instruments (TI) keep these high-performance systems running with functions such as frequency multiplication, division and clock distribution functions, including buffering and fan out with or without Phase-Lock Loop (PLL). And most importantly, TI CDCs are designed for low skew tolerances over a wide range of output loading and operating conditions, as well as maximum clock frequencies.

To meet a broad range of system requirements, TI offers a complete portfolio of cost-effective CDCs for high-performance applications, targeting motherboards and memory modules.
TI's product portfolio includes:

- High-end Phase-Lock Loop (PLL) drivers, including PC100, PC133 and DDR compliant PLL clock drivers
- Direct Rambus™ Clock Generator
- Advanced frequency synthesizers/drivers
- Economical buffer drivers

As a family, TI CDC products provide a complete clocking portfolio for today's timing requirements.



TI's clock distribution circuits (CDC) are targeted for the high performance demands of DIMMs (shown above) and PC motherboards.

Target Applications

TI is aggressively developing new CDC products to meet the growing demand and high performance expectations of the memory module and PC motherboard markets. Currently, TI has the following products available for each application:

DIMM Applications

PLL-Based Clock Buffer/Drivers —
Specifically designed for use with synchronous DRAMS (SDRAMS), TI PLL-based clock drivers for DIMMs

are high-performance, low-skew, low-jitter, PLL clock drivers that use a PLL to precisely align, in both frequency and phase, the feedback output (FBOUT) to the clock (CLK) input signal.

PC Motherboard Applications

Clock Buffer/Drivers —
TI clock drivers are high-performance buffers that distribute one input to 18 outputs with minimum skew for clock distribution.

Clock Synthesizer/Driver —
TI provides high-performance clock synthesizers/drivers that generate all required clock signals for high-performance PC motherboard applications. The central processing unit (CPU) clock outputs (PCLKn) are programmable to multiple motherboard frequencies, including 133 MHz, 100 MHz, 66 MHz and 33 MHz.

Direct Rambus Clock Generator (DRCG) —
TI's DRCG meets the clocking requirement of systems using Rambus™ memory architecture.

Other Applications

TI also provides cost-effective clocking for general purpose applications outside the PC space. Both the CDCV304 (non-PLL) and the CDCVF2505 (PLL) are robust, 8-pin devices used in telcom, set-top boxes, automotive, industrial and a wide variety of other markets.

Device Categories

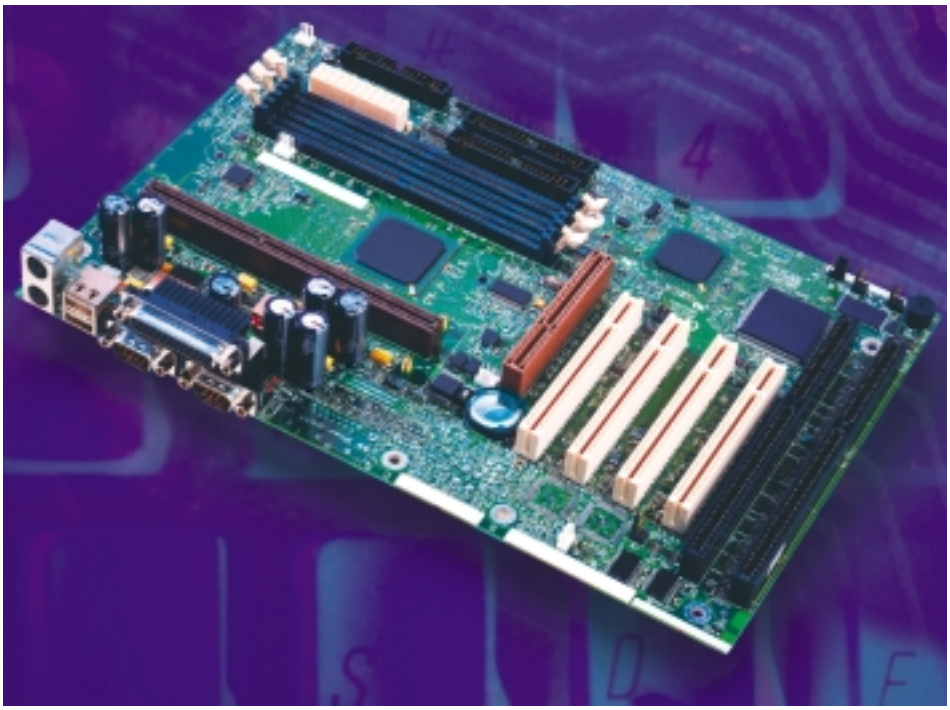
TI's CDCs can also be categorized by function and performance.

PLL-Based CDCs

Functionally, a PLL detects differences in phase and frequency between the input and feedback clock signals. Circuits with a PLL then adjust the reference voltage to the voltage-controlled oscillator in order to align the two clock signals in both frequency and phase. A PLL provides a reliable reference clock throughout the system, with an effective clock delay of zero.

TI's PLL-based CDCs give high-performance systems operating at more than 100-MHz extreme accuracy at a reasonable price. With ½ X, 1X and 2X multiply options for outputs, TI PLL CDCs reduce timing problems for components such as high-speed microprocessors and synchronous DRAMs. The low-voltage and low-power devices are optimized to reduce switching noise and to extend battery life in portable systems such as laptop PCs. Integrated series damping resistors allow PLLs to be used in point-to-point applications, while PLLs without damping resistors are designed to drive multiple memory loads.

Finally, an integrated loop filter on TI PLL clock drivers lowers system cost by reducing the need for external components.



For motherboard (shown here) and DIMM applications, TI CDCs feature low skew and high speed.

General Clock Synthesizers/Drivers

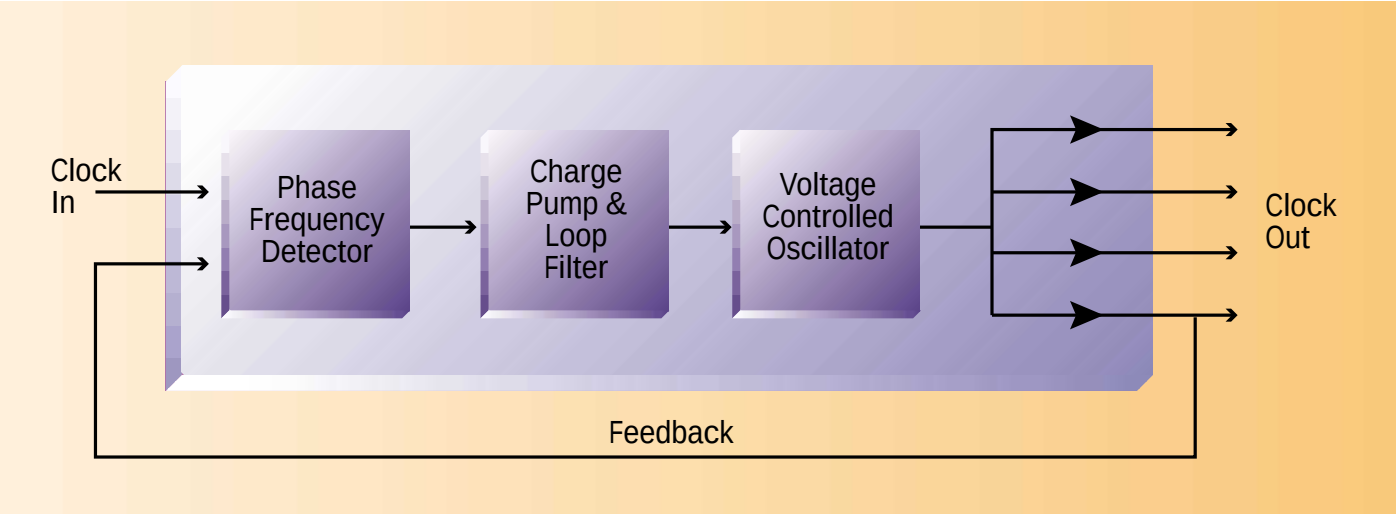
TI clock synthesizers/drivers are PLL-based frequency synthesizers that take the clock input from a reference clock or crystal and then generate multiple outputs of different frequencies. TI offers clock synthesizers for 133-MHz, 100-MHz and 66-MHz motherboards.

Performance Clock Synthesizers/ Drivers

Direct Rambus Clock Generator (DRCG) —
For systems using Rambus architecture, TI offers the CDCR81 DRCG. The 400-MHz Differential Clock Source for an 800Mb of Data Transfer Rate features Spread Spectrum Clock Tracking, which synchronizes the clock domains of the Rambus channel with an external system or processor clock. With three power operating modes, the device uses minimal power for mobile and other power-sensitive applications.

DDR-Based CDCs —
TI's new line of Double Data Rate (DDR) SDRAM clock synthesizers and PLL

PLL-Based CDCs



TI PLL clock drivers optimize DIMM applications.

buffers enable a new level of performance in PCs and servers. These clock devices have differential outputs that allow data to be clocked on every differential cross point, effectively doubling the memory throughput for a given clock frequency. This new memory technology is being adopted by most server platforms, and TI has established strong leadership in the definition and development of this new technology. TI has developed a synthesizer (CDC950) and two zero-delay PLL buffers (CDCV850, CDCV857) that are optimized for low jitter and low PLL tracking skew.

Clock Buffer Drivers

Systems that don't require the extreme accuracy of PLL can benefit from TI clock buffer drivers. Clock buffering uses an output waveform directly following an input waveform, typically exhibiting some propagation delay and skew on the outputs.

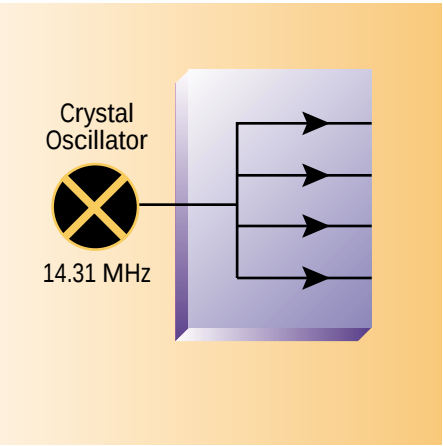
For very high-frequency systems, TI offers a range of cost-effective buffer CDCs. Specified for low skew to provide reliable clock distribution throughout the system, the family is designed to minimize I/O noise for a cleaner clock signal in motherboard applications.

TI buffer-based CDCs can fanout up to 18 signals from a single-clock input, helping to minimize loading capacitance. Some devices also feature a two-line serial interface for easy connection in a USB system. All TI buffer drivers are compatible with a number of switching standards, including low-voltage pseudo-ECL (LVPECL).

For more information

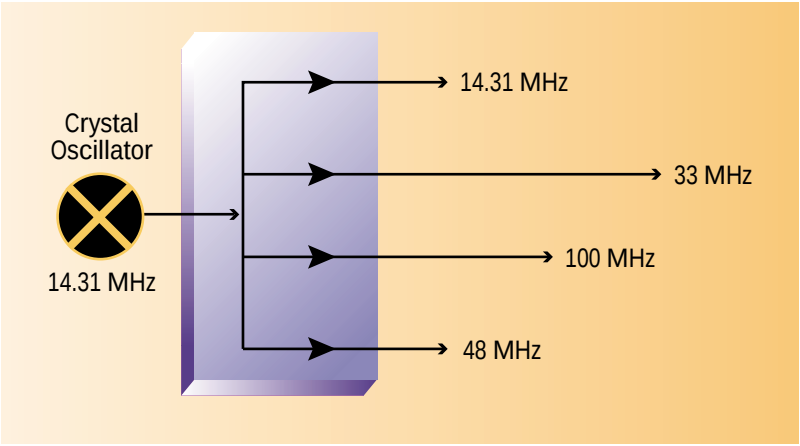
Leading-edge systems demand the leading-edge control provided by TI CDCs. If you would like more information on how TI CDCs can help give your system an advantage, please contact your local TI field sales office or visit the CDC website at: **www.ti.com/sc/cdc**

Buffer CDCs



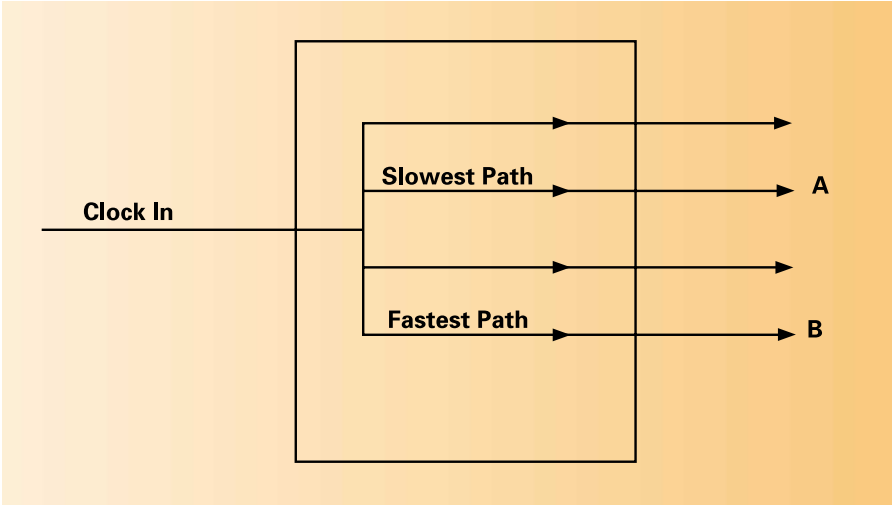
TI's buffer CDCs can distribute up to 18 outputs.

Clock Synthesizers/Drivers



TI clock synthesizers/drivers are designed for high-performance PC motherboards.

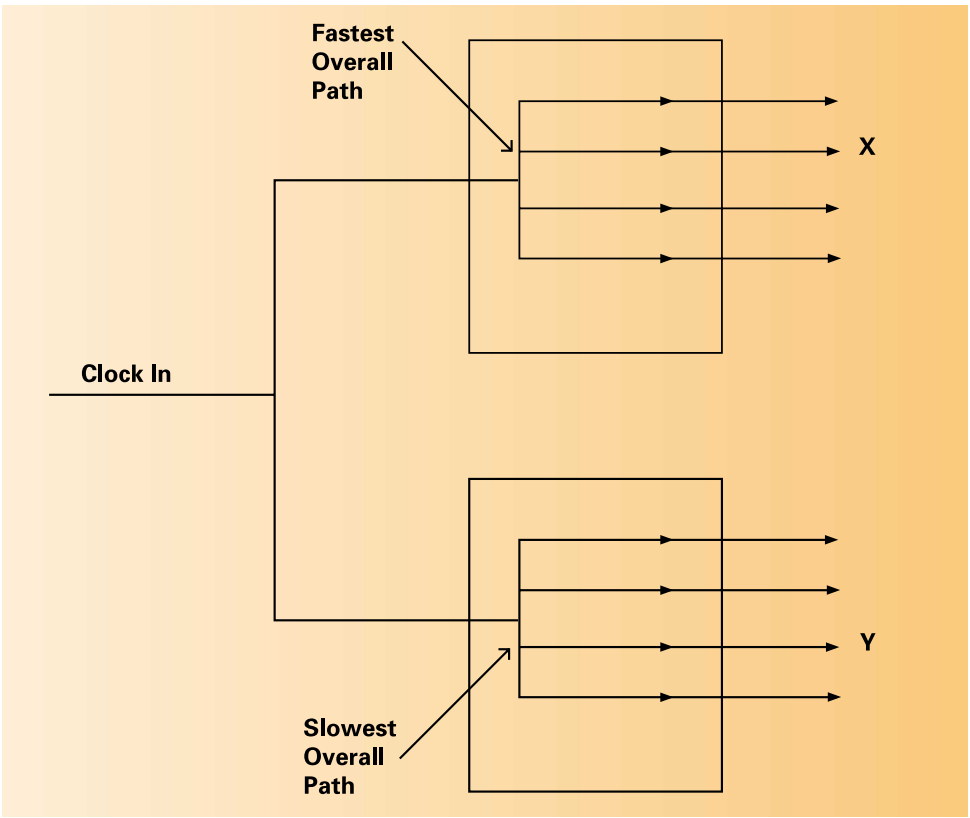
Clock Distribution Circuits (CDC) Parameters and Definitions



Output Skew: tsk(o) = | t_a-t_b |

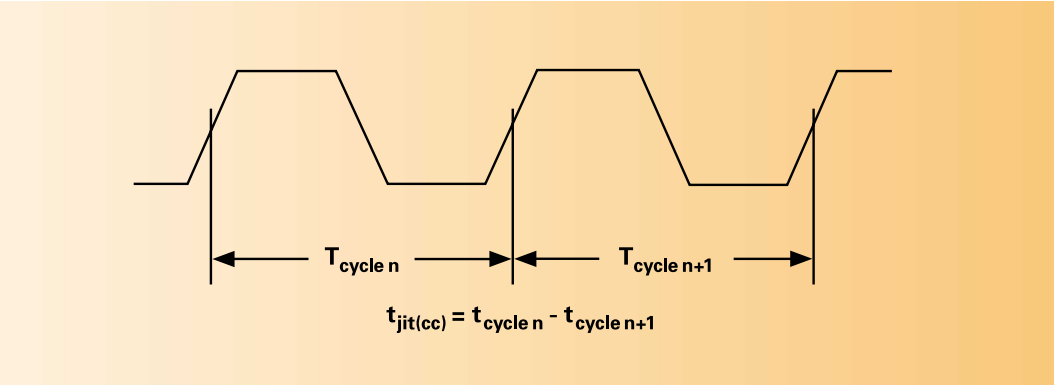
How Skew Is Defined

Although there are several parameters for skew, the two most important for CDCs are output skew, tsk(o), and part-to-part skew, tsk(pp), as defined by JEDEC Standard No. 65. After the input clock switches, not all of the outputs for each device switch simultaneously, due to slight variations among individual transistors and slight differences in signal path length inside the chip, as well as differences in lead length from die bond pad to package pin. The difference in time between the fastest switching output and the slowest in each device is the output skew.



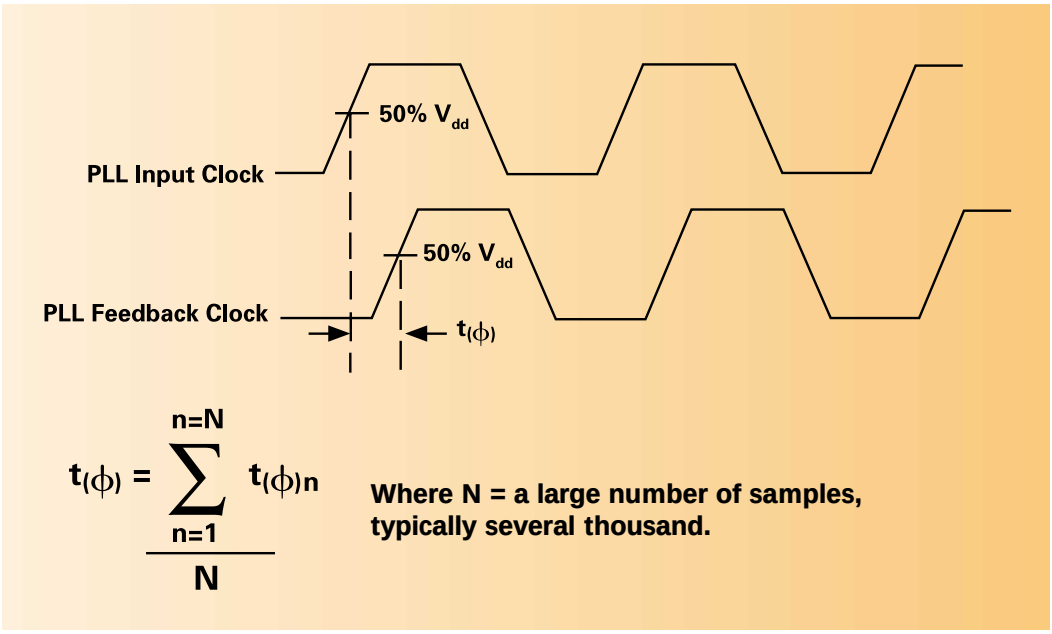
Part-to-Part Skew: tsk(pp) = | t_y-t_x |

Similarly, if the clock input pulse enters several devices simultaneously, the difference between the fastest output and the slowest output across all devices (due to manufacturing process tolerances) is called part-to-part skew, tsk(pp).
TI CDCs are designed to hold output skew and process skew to a minimum in order to keep clock pulses reliably in phase and to allow the system designer more room in the timing budget for skew between traces on the printed circuit board. Some of the new TI CDCs have output skew as low as 150 ps.



How Cycle-to-Cycle Period Jitter Is Defined

Simply defined, cycle-to-cycle period jitter, $t_{jit(cc)}$, is the period difference between two adjacent clock periods. This becomes very important as speed increases and timing budget decreases. Minimizing jitter prevents timing issues in a system. This parameter is usually reported as the largest negative displacement and the largest positive displacement over several thousand clock periods. A negative displacement occurs if period n > period n+1, and a positive displacement occurs when period n < period n+1. The newest TI PLLs can achieve a cycle-to-cycle period jitter of ±75 ps. A common misconception is that this parameter can be measured using the infinite persistence mode of an oscilloscope. Infinite persistence mode gives information about long-term peak-to-peak jitter, but not cycle-to-cycle period jitter because it is not possible to distinguish period n from period n+1 on the scope display. In the past, you needed special equipment and/or software to make this measurement, but some newer oscilloscopes have a mode that supports true cycle-to-cycle period jitter measurements.



How Static Phase Offset Is Defined

With system clock speeds increasing at a rapid pace, it becomes more difficult to use simple buffering techniques to maintain synchronization throughout the system because of propagation delay which can be as high as 1.5 ns – 5 ns, depending on device technology. One possible solution to this problem is to use a 0-delay buffer, which uses an analog PLL to phase lock the input and output clock. Of course, perfect phase alignment is not possible, and it is necessary to characterize the extent to which a PLL can maintain phase alignment. Static Phase Offset, t(ϕ) (commonly known as phase error), measures the time difference between the averaged input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable. The key point in this definition is the word "averaged." In a lab environment, you will compare the PLL input edge to the PLL feedback input edge over several thousand cycles and take the average value of this time difference. This method effectively subtracts out jitter component and is the reason this value is called static phase offset. A typical value for static phase offset is ±300 ps, but newer TI PLLs can achieve ±150 ps.

TI's CDC Products

PLL-Based Clock Distribution for DIMM Application

Device	Description	I/O Levels (Input/output)	$t_{sk(o)}$ max. (ns)	Frequency (MHz)	# Pins/ Pkg	V_{CC}
CDC516/CDC2516[1]	1:16 PLL Clock Driver w/ 3-state output	TTL/TTL	0.25	25-125	48/TSSOP	3.3 V
CDC509	1:9 PLL Clock Driver w/ 3-state output	TTL/TTL	0.25	25-125	24/TSSOP	3.3 V
CDC2509B[1]/C[1]	1:9 PLL Clock Driver w/ 3-state output with spread spectrum clock tracking	TTL/TTL	0.25	25-125	24/TSSOP	3.3 V
CDC2510B[1]/C[1]	1:10 PLL Clock Driver w/ 3-state output with spread spectrum clock tracking	TTL/TTL	0.25	25-125	24/TSSOP	3.3 V
CDC582/CDC2582[1]	1:12 LV Diff PECL PLL Clock Driver w/ (9) at 1/2x or 2x output	LVPECL/TTL	0.5	25-100	52/TQFP	3.3 V
CDC586/CDC2586[1]	1:12 PLL Clock Driver w/ (9) at 1/2x or 2x output	TTL/TTL	0.5	25-100	52/TQFP	3.3 V
CDC536/CDC2536[1]	1:6 PLL Clock Driver w/ (3) at 1/2x or 2x output	TTL/TTL	0.5	25-100	28/SSOP	3.3 V
CDC857-2/-3	1:10 SSTL-II differential	SSTL-II outputs or LVTTL/SSTL-II	0.2	66-167	48/TSSOP	2.5/3.3 V
CDCF2509	1:9 PLL Clock Driver for PC 133 Application	LV CMOS & LVTTL/LVCMOS	0.2	25-140	24/TSSOP	3.3 V
CDCF2510	1:10 PLL Clock Driver for PC 133 Application	LV CMOS & LVTTL/LVCMOS	0.2	25-140	24/TSSOP	3.3 V
CDCVF2509	1:9 low-power PLL Clock Driver for PC 133 and Beyond Application	LVTTL/LVTTL	0.1	50-175	24/TSSOP	3.3 V
CDCVF2510	1:10 low-power PLL Clock Driver for PC 133 and Beyond Applications	LVTTL/LVTTL	0.1	50-175	24/TSSOP	3.3 V
CDCVF2505	1:5 PLL Clock Driver for General Purpose	LVTTL/LVTTL	0.15	33-170	8/TSSOP/SOIC	3.3 V
CDCV850	1:10 PLL Clock Driver for DDR SDRAM Application SSC compatible with two-line serial interface	AC Coupled	0.1	60-170	48/TSSOP	2.5/3.3 V
CDCV857	1:10 Low Power Differential	SSTL2/SSTL2	0.1	60-170	48/TSSOP	2.5 V

Clock Synthesizer/Driver for Motherboard Application

Device	Description	I/O Levels (Input/output)	$t_{sk(o)}$ max. (ns)	Frequency (MHz)	# Pins/ Pkg	V_{CC}
CDC924	PC MB Clk Synthesizer/ Driver 133-MHz Max. Freq w/ spread spectrum	LVTTL/LVTTL, TTL	0.175	66, 100, 133	56/SSOP	2.5/3.3 V
CDC930	PC MB Differential Syn/Dri w/133-MHz Freq Max w/Spread Spectrum	XTL/Various	0.15	100, 133	56/TSSOP/SSOP	3.3 V
CDC943	133-MHz Clk Syn/Dri and Buffer for Mobile Application	XTL/Various	0.15	66, 100, 133	56/SSOP	2.5/3.3 V
CDC950	133-MHz Diff Clock Syn/Dri for PC Motherboards w/ 3-State Outputs	XTL/Various	0.1	100, 133	48/TSSOP	3.3 V

TI's CDC Products (Continued)

Buffer-Based Clock Distribution — All packages are available in Tape and Reel

Device	Description	I/O Levels (Input/output)	$t_{sk(o)}$ max. (ns)	Frequency (MHz)	# Pins/ Pkg	V_{CC}
CDC111	1:9 diff LVPECL	LVPECL/LVPECL	0.05	0-500	28/PLCC	3.3 V
CDC203	6:6 inverter	CMOS/CMOS	0.7	0-40	20/SOIC	3.3 V
CDC204	6:6 inverter	CMOS/CMOS	1.0	0-80	20/SOIC	3.3 V
CDC208	Dual 1:4 fanout	TTL/CMOS	1.0	0-60	20/SOIC	5 V
CDC328A	1:6 fanout w/sel polarity	TTL/TTL	0.5	0-100	16/SOIC/SSOP	5 V
CDC329A	Enhanced CDC329	TTL/CMOS	0.6	0-80	16/SOIC	5 V
CDC340	1:8 w/fast tpd fanout	TTL/TTL	0.5	0-80	20/SOIC	5 V
CDC341	1:8 w/fast tpd fanout	TTL/TTL	0.5	0-80	20/SOIC	5 V
CDC351/CDC2351[1]	1:10 w/fast tpd fanout	LVTTL/LVTTL	0.5	0-100	24/SOIC, SSOP	3.3 V
CDC319	1:10 clock driver with two-line serial interface for PC motherboard	LVTTL/LVTTL, TTL	0.25	0-100	28/SSOP	3.3 V
CDCV304	1:4 fanout for PCI-X and general applications	LVTTL	0.1	0-140	8/TSSOP/SOIC	3.3 V

Direct Rambus™ Clock Generator

Device	Description	I/O Levels (Input/output)	$t_{sk(o)}$ max. (ns)	Frequency (MHz)	# Pins/ Pkg	V_{CC}
CDCR81	400-MHz Direct Rambus Clock Generator	CMOS/RSL[2]	–	267-400	24/SSOP	3.3 V
CDCR61A	400-MHz Direct Rambus Clock Generator	RSL[2]	–	300, 400	16/TSSOP	1.8/3.3 V
CDCR62	400-MHz Direct Rambus Clock Generator	RSL[2]	–	300, 400	16/TSSOP	1.8/3.3 V

[1] With series output resistors [2] Rambus™ Signaling Levels

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