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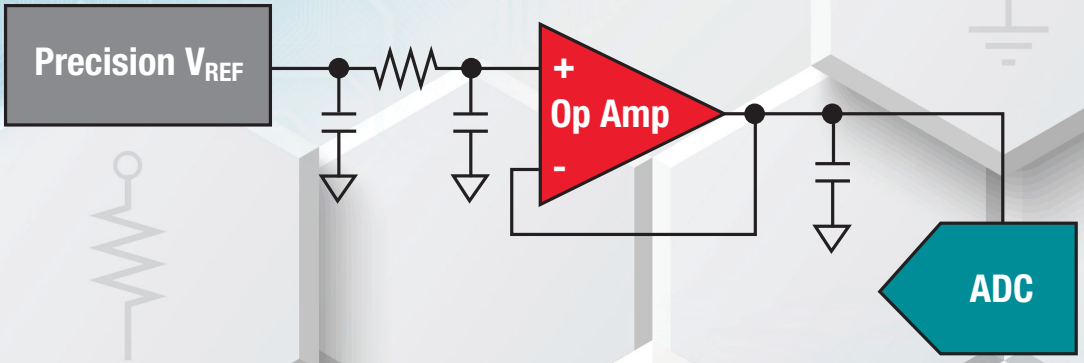


Tips and Tricks for Designing with Voltage References

Texas Instruments

Preface

The new intelligence injected into simple everyday objects and subsystems requires some sort of silicon “brain” to react predictably and desirably to various real-world conditions that could ultimately affect the behavior and performance of the system. That is where voltage references come into the picture.

A voltage reference is a precision device specifically designed to maintain a constant output voltage, even as parameters such as ambient temperature or supply voltage change. The precision of a voltage reference enables its use in several different types of applications beyond a data converter. As you will see in this document, the range of applications demonstrated show that while voltage references may not be a new concept, they are going to remain an integral part of system design moving forward.

This document provides a comprehensive overview of voltage reference basics and application design. The first chapter focuses on voltage reference essentials. The authors explore cases in which a power designer might need certain features from one topology while capitalizing on the benefits of another topology. The second chapter dives into voltage reference performance and design guidelines with data converters. The third and final chapter discusses the functional flexibility of voltage references to serve as low-drift DC voltage or current sources. Through these examples and resources, you should find useful nuggets of information to help optimize your designs.

CONTENTS

Chapter 1: Voltage Reference Essentials

1. Shunt vs. Series. Which Topology is Right for You?

By Christopher Dean

The most common way to interface with the real world is to use analog-to-digital converters (ADCs), sensors or other application-specific integrated circuits (ICs). Accurate measurements require a reference voltage that does not fluctuate with system conditions such as input voltage or ambient temperature. A voltage-reference IC provides a steady voltage that other ICs use to make measurements with the required accuracy.

There are two types of voltage references: shunt and series. Each has its own set of strengths and use cases, listed in **Table 1**.

Shunt References

A shunt reference is functionally similar to a Zener diode, where the voltage drop across the device is constant after the device reaches a minimum operating current. The shunt reference regulates the load by acting as a constant voltage drop and shunting excess current not required by the load through the device to ground. An external resistor sets the total supply current and acts as the voltage drop between the input supply and the reference voltage, as shown in **Figure 1**.

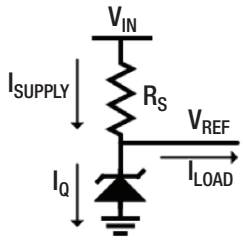


Figure 1: Positive voltage reference.

The input supply will always see the maximum load current as determined by the input voltage level and the external resistor. The shunt reference will sink more or less current as the current requirements of the load change.

The external resistor must be between $RS_{\_MIN}$ and $RS_{\_MAX}$, calculated by **Equations 1** and **2**:

$$R_{S\_MIN} = (V_{IN\_MAX} - V_{OUT}) / (I_{LOAD\_MIN} + I_{Q\_MAX}) \quad (1)$$

$$R_{S\_MAX} = (V_{IN\_MIN} - V_{OUT}) / (I_{LOAD\_MAX} + I_{Q\_MIN}) \quad (2)$$

$$\text{where } R_{S\_MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{LOAD\_MIN} + I_{Q\_MAX}} \text{ and } R_{S\_MAX} = \frac{V_{IN\_MIN} - V_{OUT}}{I_{LOAD\_MAX} + I_{Q\_MIN}}$$

You can also use a shunt reference to create floating references and negative references, and the equations remain the same. Floating references connect to another voltage potential instead of to ground. One possible use case is to combine multiple shunt references to create a higher reference voltage, such as a 15V reference with 10V and 5V shunts.

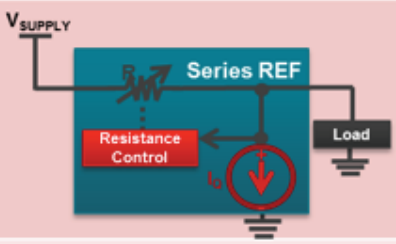
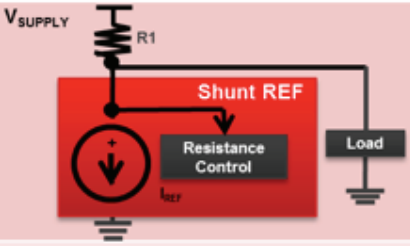
	Series References	Shunt References
Diagram		
Number of Terminals	At least 3	At least 2
Advantages	• Significantly lower power dissipation • Generally higher precision • Low I_Q • Low dropout	• Wide V_{IN} tolerant with proper resistor selection • Can be used to create negative or floating reference voltages • Inherent current sourcing and sinking
Disadvantages	• Limited max V_{IN}	• V_{IN} current fixed at max load • No shutdown mode
Key Markets	• Factory Automation, Grid, Medical, Test	• Isolated power supplies, Adapters, Automotive
TI Nomenclature	• LM41xx, REFxxxx	• LM40xx-N, LM(V)431, LM1/2/385, LM1/2/336 • ATL431, TL(V)431

Table 1: Typical comparison table of shunt vs. series voltage references.

For a negative reference, connect a negative supply rail to the anode (what was the ground pin) through a series resistor, and connect ground to the cathode (what was the output pin). Much like the positive output configuration, the output is between the resistor and the device, as shown in **Figure 2**.

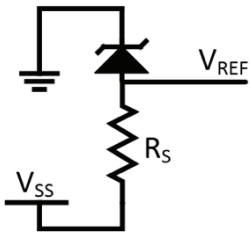


Figure 2: Negative voltage reference.

Series Reference

A series reference does not require an external resistor and only consumes as much current as required by the load, plus a small quiescent current. However, since the input voltage passes directly into the reference device instead of through a series resistor, a series reference has a maximum-rated input voltage that you must account for. **Figure 3** shows a typical series reference circuit.

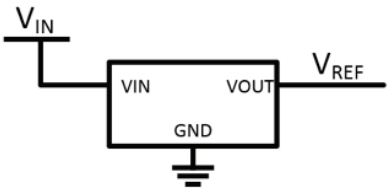


Figure 3: Typical series reference circuit.

Proper regulation for a series reference requires that the input voltage be at least the output voltage plus some headroom. The extra voltage difference between the input and output is known as the dropout voltage, and typically increases with the load current.

A series reference may include an enable pin to externally enable or disable the device to save power when the output is not needed.

When selecting a voltage reference for your next application, keep these typical use cases in mind:

- Shunt reference use cases:
  - Wide-input voltage range or high-input voltage transients.
  - Negative or floating voltage references.
- Series reference use cases:
  - Variations in load current, where the supply current decreases with the load current.
  - Reference with sleep or shutdown operations.

2. How to Achieve Ultra-Low Dropout Voltage with Shunt References

By Christopher Dean

The dropout voltage is the minimum voltage difference between V_{IN} and V_{OUT} under a given load. Have you ever needed a voltage reference that has to tolerate wide-input voltage ranges yet is still capable of low-dropout operation? For example, many series references with low dropout do not support input voltages up to 12V. This is where a shunt reference can be very handy.

In the application shown in **Figure 1**, the LM4040 shunt reference voltage is 4.096V, which is a common choice for analog-to-digital converters (ADCs) because 1mV is equivalent to one least significant bit (LSB) with a 12-bit ADC.

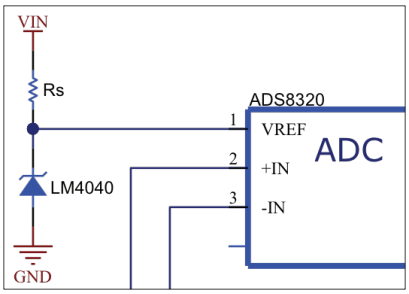


Figure 1: Driving an ADC external-reference pin with a shunt reference.

The shunt reference requires an external resistor to set the supply current. You can determine the load current for the voltage reference from the ADC data sheet. For this example, let's use the ADS8320. In the circuit shown in **Figure 1**, the maximum current draw of the external reference pin is listed as 80µA in the ADC data sheet. With an external resistor value of 576Ω, the voltage reference will remain in its operational area over an input voltage range of 4.19V to 12.75V. That's a dropout voltage of 94mV, with full reference functionality beyond 12V.

To compare the shunt reference low dropout to a series reference with the same 4.096V reference voltage, the maximum dropout voltage for the REF5040 is specified as 200mV in the data sheet.

Table 1 summarizes the voltage and current values for the LM4040 shunt reference.

R_S	I_{LOAD}	V_{IN_MIN}	I_Q at V_{IN_MIN}	V_{IN_MIN}	I_Q at V_{IN_MAX}
576 Ω	80 µA	4.16 V	71.1 µA	12.75 V	14.98 mA

Table 1: Voltage and current parameters for low dropout LM4040 shunt reference.

Very low dropout voltages are possible because the maximum load current seen by the reference device is very small at 80µA. As the load current increases, the resistor, R_S, must increase as well, forcing a higher minimum V_{IN}.

3. How to Achieve Shunt Reference Flexibility with Precision Series References

By Marek Lis

A series voltage reference is a three-terminal device: V_{IN}, V_{OUT} and GND. It is similar in concept to a low-dropout (LDO) voltage regulator but designed for a lower quiescent current and much higher accuracy. Think of it as the voltage-controlled resistance (VCR) between the V_{IN} and V_{OUT}. It regulates the output voltage by adjusting its internal resistance such that V_{IN} minus the drop across the resistance, R, equals the reference voltage at V_{OUT}; see the block diagram in **Figure 1**.

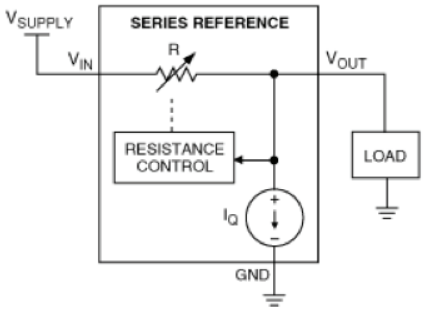


Figure 1: Series voltage reference – VCR model.

Series references generally have much better initial accuracy and temperature drift coefficients than shunt references. Thus, if you need better than 0.1 percent initial accuracy and/or less than 25ppm/°C temperature drift, you will most likely need a series voltage reference.

However, shunt references offer more flexibility in terms of V_{IN} range, as well as the option to stack multiple devices on top of one another to obtain higher reference voltages, and the ability to create negative or floating references.

How can you combine the design flexibility of shunt references with the precision of series references?

You can take advantage of the precision and stability characteristics of the low-noise, low-drift REF5050 family, by externally connecting the V_{IN} and V_{OUT} pins together. By doing so, the series voltage references in this family are essentially converted into Zener diodes, but with greatly diminished negative effects of shot noise and reverse-breakdown resistance. While you could use any of the seven devices in this family, let's focus on the REF5050 (5V output) and REF5010 (10V output).

The simplified schematic in **Figure 2** shows the REF5050's two main circuit components: BandGapAmp, with its gain stage responsible for assuring a constant V_{OUT} voltage over temperature and supply variations; and the ErrAmp output stage, capable of sinking or sourcing a minimum of 10mA of output load current with minimal effect on output voltage initial accuracy.

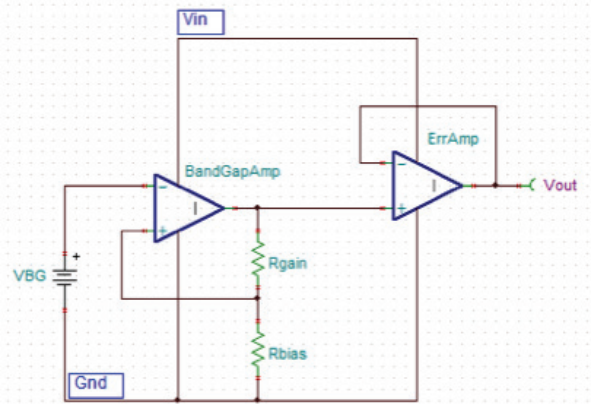


Figure 2*: Simplified schematic of the REF5050.*

To assure V_{OUT} initial accuracy and temperature drift, the Class AB output transistors must all operate in their linear region; thus, Drain-to-Source Voltage (V_{DS}) must be greater than the transistor saturation voltage, V_{SAT}. Therefore, the input voltage, V_{IN}, of a series voltage reference must be at least a dropout voltage above V_{OUT}; see the circuit in **Figure 3**. The minimum dropout voltage of the REF5050 under quiescent conditions (I_{OUT} = 0) is 200mV.

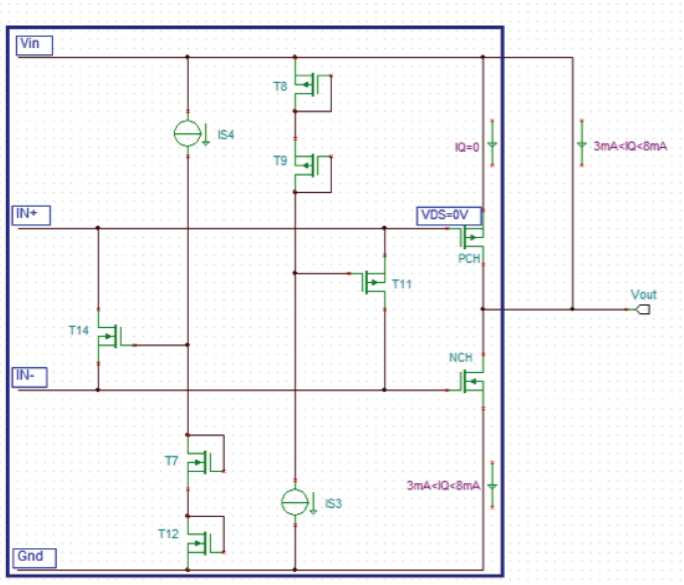


Figure 3: Placing the REF5050 ErrAmp output stage in a shunt configuration.

However, by externally connecting V_{IN} and V_{OUT} together (the right side of **Figure 3**), V_{DS} = 0V and the upper output transistor, PCH, gets completely shut off. Under such conditions the output bias current, I_Q, bypasses the PCH transistor entirely and flows directly from V_{IN} to a lower output transistor, NCH. This establishes a precision reference voltage between V_{IN} and GND.

By shorting V_{IN} and V_{OUT}, the REF5050 is effectively transformed into a two-terminal shunt voltage reference, but it maintains the DC and temperature precision of a series voltage reference. Under this arrangement, the output stage biases up at a somewhat higher quiescent current than typical, but the precision and stability of the REF5050 remain unchanged.

Figures 4 and **5** are examples of circuit configurations using the REF5050 and REF5010 as the basic building blocks.

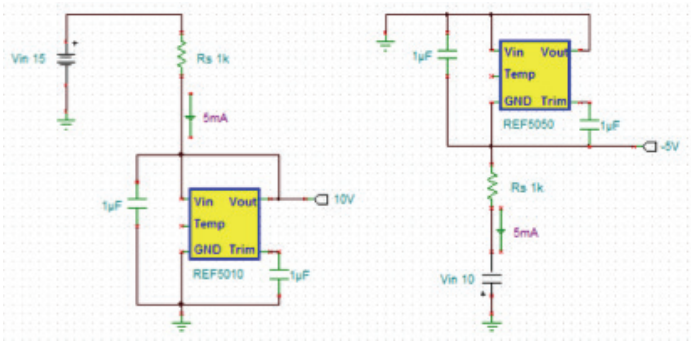


Figure 4: The REF5010 and REF5050 used in a positive and negative shunt configuration.

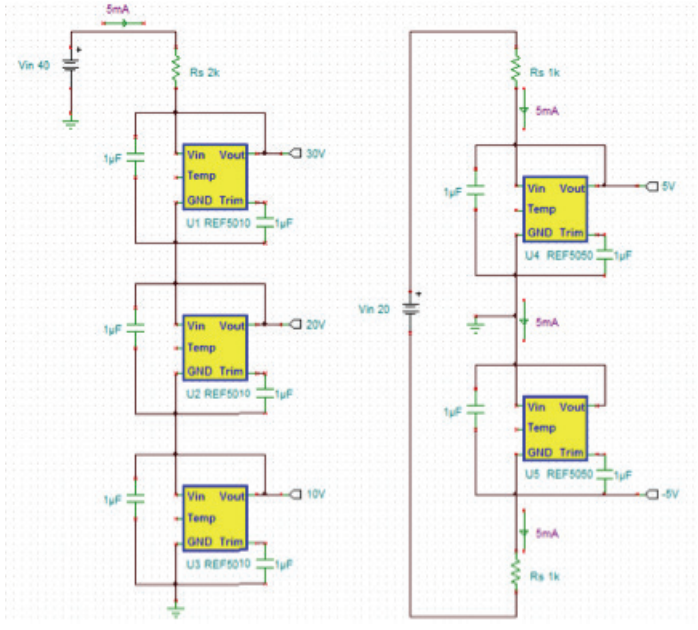


Figure 5: Stacking the REF5010 for a high-voltage and the REF5050 for a dual-voltage shunt configuration.

Given that Rs is appropriately sized for the required maximum output loading, using the REF5050 or REF5010 as a shunt reference imposes no limit on the maximum power-supply voltage, since most of the voltage drop and power will typically be dissipated in R_S. Therefore, as a simple two-terminal device, you can use the REF5050 family of series voltage references configured as a shunt in innovative circuits such as negative, dual and floating references. Additionally, you can stack multiple devices on top of each other to obtain virtually any desired reference voltage.

The two-terminal application arrangement of the REF5050 has excellent characteristics, which are closely related to an ideal Zener diode. The serial connections of REF5010 basic shunt blocks enable you to build exceptionally high-voltage references (in thousands of volts) with very high voltage precision and superb temperature stability.

4. Level-Shift of Precision Voltage References

By Marek Lis

Due to circuit topology limitations, some of the highest-precision series voltage references do not offer lower output-voltage options like 1.25V. But as long as a negative supply is available, there are ways to create a lower option by level-shifting one of the existing references as a basic building block.

A newly built voltage reference's initial accuracy and drift can closely match the performance of the original voltage reference, as long as the input voltage offset and drift of the external operational amplifier (op amp) – as well as matching of the resistors used – meet the appropriate minimum requirements.

One of the ways to generate a 1.25V precision voltage reference involves voltage-level translation, shown in **Figure 1**. The REF5025 nominal output voltage (2.5V) is level-shifted to half of its value by driving its GND pin to -1.25V with the use of the OPA376. Since the maximum input-voltage offset and drift of the OPA376 are ±25µV and ±1µV/C, respectively, as long as the matching of R1/R2 resistors is within 0.01 percent, the resulting 1.25V voltage reference initial accuracy and drift will match the REF5025's performance.

The resulting 1.25V reference can work on power supplies as low as ±1.35V or as high as ±2.75V; it can also be powered by asymmetric supplies of +1.35V/-4.15V, +4.15V/-1.35V or anything in-between, as long as the total supply voltage does not exceed the OPA376's 5.5V maximum supply.

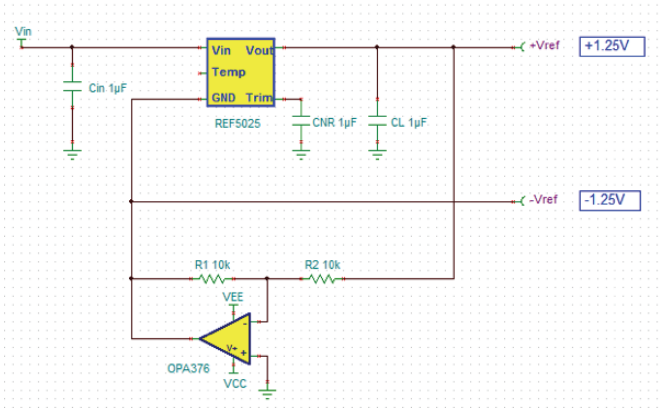


Figure 1: Creating a 1.25V precision voltage reference.

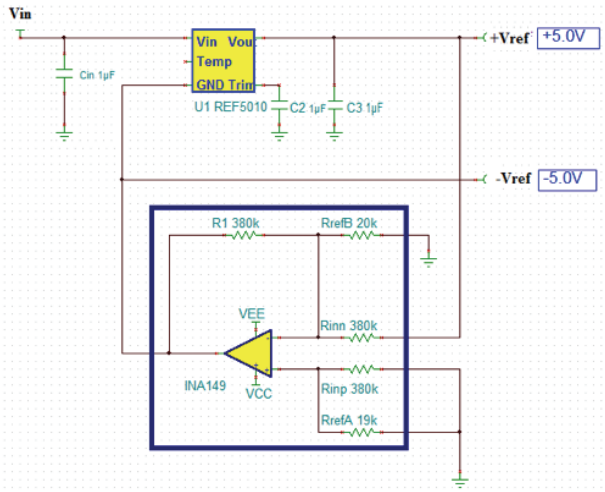


Figure 2: Using the INA149 for a dual-output precision voltage reference.

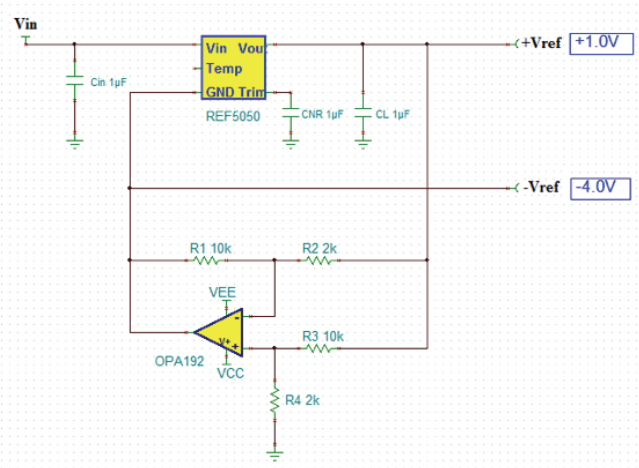


Figure 3: Using the OPA192 and REF5050 for asymmetric precision voltage references.

In order to create a higher-output precision voltage reference, you can use the REF5010 together with the INA149 difference amplifier shown in **Figure 2**. Since the INA149 is a precision unity-gain difference amplifier with a maximum gain error of 0.02 percent, as well as maximum V_{OS} and drift of 1,100µV and 15µV/°C, respectively, using it in combination with a 10V precision voltage reference results in a 0.011 percent input offset-related error (1,100µV/10V*100 percent) and 1.5ppm/°C temperature drift (15µV/°C/10V*1E+6). These parameters are within the specified maximum initial accuracy and temperature drift of the REF5010 and thus ensure that the dual-output precision voltage reference shown in **Figure 2** closely preserves the initial accuracy and drift of the REF5010 building block.

As far as power supplies go, the circuit configuration shown in **Figure 2** can work on the minimum supplies of +5.2V (limited by the 200mV maximum dropout voltage of the REF5010) and -6.5V (the output of the INA149 can operate linearly down to 1.5V of its negative supply). On the high end, the maximum positive supply can be as high as 13V (limited by the 18V maximum total supply of the REF5010), while the negative supply, Vee, is limited only by the 36V maximum total supply of the INA149, and thus can operate from 30.8V (if V_{CC} = 5.2V) or 23V (if V_{CC} = 13V).

The use of difference or instrumentation amplifiers (INAs) like the one shown in **Figure 2**, with superb laser-trimmed internal resistors and temperature coefficient matching, typically results in a higher-performance and lower-cost solution than using the external resistors shown in **Figure 1**, which can be expensive for the required matching of better than 0.1 percent.

For higher supply-voltage operations, you can build virtually any precision voltage reference using a reference option such as the REF5050, together with a high-voltage precision amplifier like the OPA192. By appropriately scaling the R1 through R4 resistors (**Figure 3**), you can split the nominal reference voltage of the basic reference block into any desirable parts. With the OPA192 maximum-input voltage offset of ±25µV and drift of ±0.5µV/C, you can ensure that the resulting precision voltage reference shown in **Figure 3** maintains the initial accuracy and drift of the REF5050 basic building block, provided that the required 0.01 percent matching of the ratios of the external resistors is not the limiting factor.

For linear operation of the circuit in **Figure 3**, the minimum positive supply of +1.2V is limited by the REF5050's dropout voltage of 200mV. The minimum negative supply of -4.3V is based on the OPA192's specified output swing of 300mV above its negative rail. The maximum positive supply of 14V is limited by the REF5050's maximum total supply of 18V, while the maximum negative supply can be as high as -34.8V (if V_{CC} = +1.2V) or -22V (if V_{CC} = 14V), limited only by the OPA192's maximum total supply of 36V.

There are a variety of ways to level-shift a precision voltage reference to virtually any required output voltage. However, you must take special care to properly choose not only external components like op amps, INAs and resistors, but also assure that the minimum/maximum operating supply voltages do not diminish the overall performance of the original circuit.

5. Adjustable Shunt Voltage References

By Jose Gonzalez Torres

Have you ever had to pick between two of your favorite desserts and thought to yourself, "Why can't I have both?" Well, the same thing happens to engineers every day when designing with programmable voltage references.

A very common goal for engineers is to come up with very low-power designs that offer a set functionality: to sense temperature, power up a computer, or even serve you your preferred choice of sweets. But did you know that in order to get to that low-power operation, the engineer is also giving up other advantages? In order to achieve low power, engineers often have to design with voltage references that offer very low current but suffer from a loss of accuracy across the operating temperature range. Is there a way for these engineers to have their cake and eat it too? I think you know the answer.

First, let's take a look at what voltage reference accuracy means and the conditions that directly impact accuracy, using the common TL431 to drive the analysis. If you have a circuit similar to **Figure 1**, you can set up R1 and R2 to get the desired cathode voltage V_{KA} output based on the voltage reference. You can find more information about how to do so in this application note.

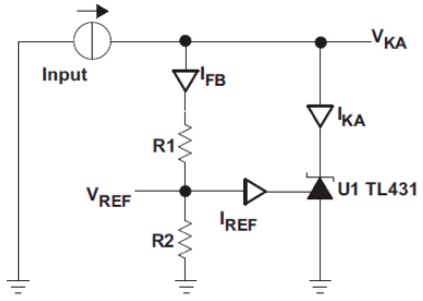


Figure 1: Power-supply current limiter.

V_{REF} is not always at its nominal; in fact, it is guaranteed to have an offset based on the device's operating conditions. **Table 1** shows the TL431 specifications table that directly affects V_{REF}.

You can use **Equation 1** to calculate the effective V_{REF} by adding the collective effects of these parameters (typical), assuming operation of V_{KA} = 5V and a cathode current of 2mA.

$$V_{REF} = V_{NOM} + \left[\left(I_{KA} - I_{NOM}\right) x Z_{KA}\right] + \left[\left(V_{KA} - V_{NOM}\right) x \frac{\Delta V_{REF}}{\Delta V_{KA}}\right] \quad (1)$$

This tells you that for the TL431, the effective V_{REF} is now 2.4899V, or 0.2 percent accurate, which is not a significant difference in plain sight. But once you cross to the maximum value, which usually happens over high temperatures, you get an effective V_{REF} of 2.539V, or 1.78 percent accuracy.

PARAMETER		TEST CONDITIONS		TL431C, TL432C			UNIT
				MIN	TYP	MAX	
V_{REF}	Reference voltage	V_{KA} = V_{REF}, I_{KA} = 10 mA		2440	2495	2550	mV
$V_{I(DEV)}$	Deviation of reference voltage over full temperature range	V_{KA} = V_{REF}, I_{KA} = 10 mA, T_A = 0°C to 70°C	SOT23-3 and TL432 devices		6	16	mV
			All other devices		4	25	
ΔV_{REF} / ΔV_{KA}	Ratio of change in reference voltabe to the change in cathode voltage	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{REF}		– 1.4	– 2.7	mV/V
			ΔV_{KA} = 10 V – V_{REF}		– 1	– 2	
I_{REF}	Reference input current	I_{KA} = 10 mA, R1 – 10 kΩ, R2 = ∞			2	4	µA
$I_{I(DEV)}$	Deviation of reference input current over full temperature range	I_{KA} = 10 mA, R1 – 10 kΩ , R2 = ∞, T_A = 0°C TO 70°C			0.4	1.2	µA
I_{MIN}	Minimum cathode current for regulation	V_{KA} = V_{REF}			0.4	1	mA
I_{OFF}	Off-state cathode current	V_{KA} = 36 V, V_{REF} = 0			0.1	1	µA
$\lvert Z_{KA} \rvert$	Dynamic impedance	V_{KA} = V_{REF}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

Table 1: TL431 electrical specifications.

How does this affect your system?

In an analog environment, where the overall voltage drift may be the necessary threshold to trigger an operational amplifier, a 44.5mV maximum/6mV minimum offset could mean the difference between regulation and standby, which could lead to system failures. But this becomes more of an issue when you consider the use of the TL431 as a reference for an analog-to-digital converter (ADC). The least significant bit (LSB) voltage is based on the converter's accuracy in number of bits. Assuming the same conditions of 5V and an ADC of 8 bits, you get an LSB of 19.53mV, which should be fine during typical operation (as you can see in **Equation 2**). But across temperature, the operation will change and the system might be reading the wrong data or performing incorrectly.

$$LSB = \frac{5V}{2^8} = 19.53mV \quad (2)$$

So how can you resolve the accuracy issues and still maintain low-power operation? One solution is the ATL431, which features lower-power operation but significantly improves accuracy. Using the ATL431 under the same conditions and design parameters as before, you will get an effective V_{REF} of 2.499V (0.95mV), or 0.03 percent accuracy. This gives you a much larger margin of error when considering analog operation, but more so, you can now use a much higher-resolution ADC (**Equation 3**):

$$2N = \frac{5V}{0.95mV} = 50263.16 \quad (3)$$

$$N \sim 12\ bits$$

In the end, a small change in the right direction can yield results that are more of a compromise with your original design around the TL431. The ATL431 is one of those solutions that provide good-enough power savings to also have an improvement in accuracy, without having to sacrifice one for the other. In the end, even with compromise, it is possible to obtain the best of both worlds.

Chapter 2: Voltage Reference Applications

1. How the Voltage Reference Affects ADC Performance: Fundamental Operation of an ADC

By Bonnie Baker and Miro Oljaca

When designing a mixed-signal system, many designers tend to examine and optimize each component separately. This myopic approach can go only so far if the goal is to have a working design at the end of the day. Given the array of different components in a system, designers must have a complete understanding of not only the individual components but also their impact on overall system performance.

When a design has an analog-to-digital converter (ADC), it is critical to understand how this device interacts with the voltage reference and voltage reference buffer. Part 1 of this series looks at the fundamental operation of an ADC independently, exactly as many designers do, and then at the performance characteristics that impact the accuracy and repeatability of the system. Part 2 delves into the voltage reference device, once again examining its fundamental operation and the details of its impact on the performance of an ADC. Part 3 investigates the impact of the voltage-reference buffer and the capacitors that follow it, and how to ensure that the amplifier is stable. We will compare assumptions and conclusions to measurement results and briefly analyze the interplay between the driving amplifier, voltage reference and converter, followed by an investigation of sources of error in the ADC's conversion results.

The Fundamentals of ADCs

Figure 1 shows the voltage reference system for the successive-approximation-register (SAR) ADC that we will examine in this three-part series. As the name suggests, the ADC converts an analog voltage to a digital code. Overall system accuracy and repeatability depend on how effectively the converter executes this process.

You can define the accuracy of the conversion with static specifications, and the repeatability with dynamic specifications. Generally, the ADC static specifications are offset-voltage error, gain error and transition noise. The ADC dynamic specifications are signal-to-noise ratio (SNR), total harmonic distortion (THD) and spurious-free dynamic range (SFDR).

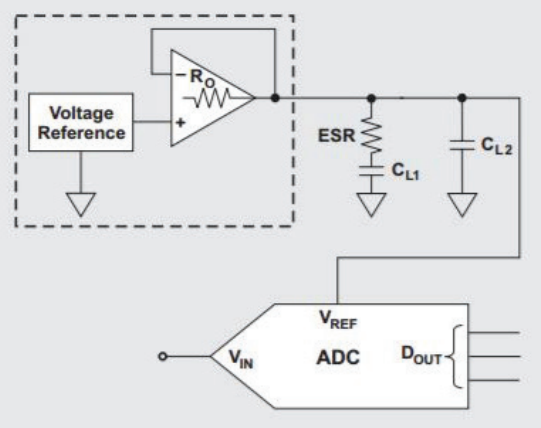


Figure 1: Voltage reference system for a SAR ADC.

Static Performance

Figure 2 shows an ideal and an actual (or nonideal) transfer function of a 3-bit ADC. The actual transfer function has an offset-voltage error and a gain error. In the example application circuit, only the ADC gain error, transition noise and SNR are of concern.

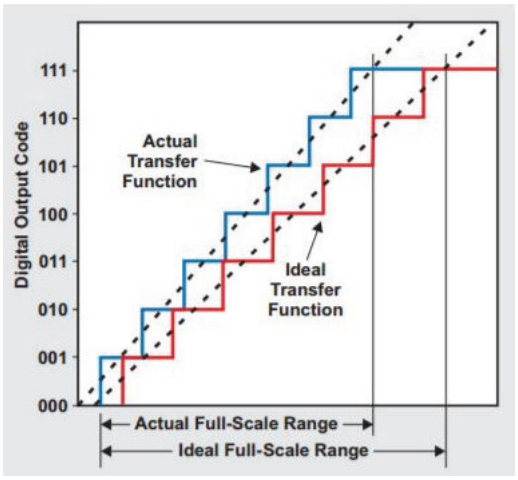


Figure 2: Ideal and actual ADC transfer functions with offset and gain errors.

Equation 1 describes the typical transfer function of the ideal (error-free) ADC:

$$Code = V_{IN} \; x \; \frac{2^n}{V_{REF}} \qquad (1)$$

where Code is the ADC output code in decimal form, V_{IN} is the analog input voltage (in volts), n is the resolution of the ADC (or number of output-code bits) and V_{REF} is the analog value of the voltage reference (in volts).

Equation 2 demonstrates that the ADC output code is directly proportional to the analog input voltage and inversely proportional to the voltage reference. **Equation 2** also shows that the output code depends on the number of bits (the converter resolution).

The DC errors of nonideal ADCs are offset-voltage error and gain error. Introducing offset-voltage error into the transfer function involves rewriting Equation 1 as **Equation 2**:

$$Code = \left(V_{IN} - V_{OS\_ADC}\right) x \frac{2^n}{V_{REF}} \quad (2)$$

where V_{OS_ADC} is the input offset voltage of the ADC. Gain error is equal to the difference between the ideal slope from zero to full scale and the actual slope from zero to full scale. The notation for gain error is a decimal or percentage. If you consider the impact of only the gain error (no offset-voltage error) on an ADC, you can rewrite Equation 1 as **Equation 3**:

$$Code = V_{IN} x \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)} \quad (3)$$

where GE_{ADC} is the gain error expressed as

$$GE_{ADC} = \frac{Actual\ Gain - Ideal\ Gain}{Actual\ Gain}$$

From **Equation 3**, you can see that the gain-error factor adds to the initial accuracy of V_{REF}. The output code is inversely proportional to the combination of the voltage reference plus the gain error. The DC error caused by noise from the voltage reference chip inversely impacts the gain accuracy of the ADC. The second part of this series will specifically show the impact of the voltage reference's errors.

Equations 2 and **3** combined show the final transfer function as **Equation 4**:

$$Code = \left(V_{IN} - V_{OS\_ADC}\right) x \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)} \quad (4)$$

To analyze ADC transition noise, you can examine the code-transition points in the ADC's transfer curve. These are the points where the digital output switches from one code to the next as a result of a changing analog input voltage. The transition point from code to code is not a single threshold but a small region of uncertainty.

Figure 3 shows the uncertainty at these transitions resulting from internal converter noise. The region of uncertainty is defined by measuring repetitive code transitions from code to code. An ADC's transition noise has a direct effect on the SNR of the converter. Since it is important to understand this phenomenon, the second part of this series will look more closely at voltage reference noise characteristics.

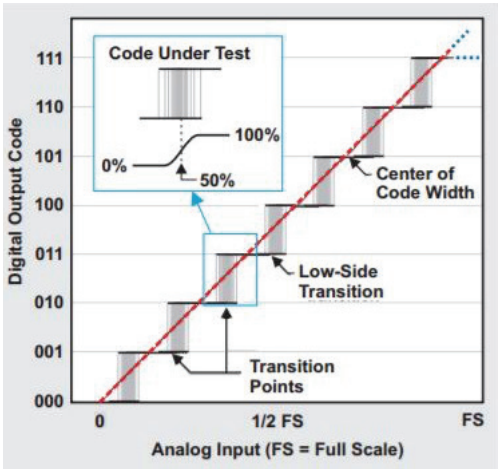


Figure 3: Transition noise with a 3-bit ADC.

Dynamic Performance

The total system noise from the circuit in **Figure 1** is a combination of the inherent ADC noise, the noise from the analog input-buffer circuitry and the reference input voltage noise. **Figure 4** shows a simplified internal circuit of a SAR ADC. To determine the dynamic performance of an ADC, you can use a fast Fourier transform (FFT) plot of the converter's output data, calculating an FFT plot from a consistent clocked series of converter outputs. The FFT plot provides the SNR, noise-floor level and SFDR.

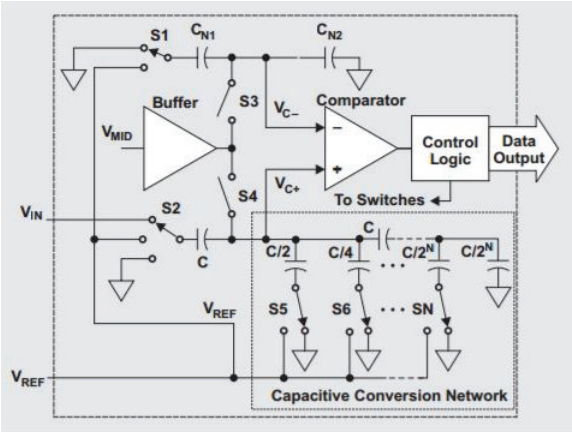


Figure 4: Simplified topology of a SAR ADC.

In the example application circuit, only the SNR specification is of interest. **Figure 5** provides an FFT plot of these specifications. A useful way of determining noise in an ADC circuit is to examine the SNR in **Figure 5**. The SNR is the ratio of the root mean square (RMS) of the signal power to the RMS of the noise power. The SNR of the FFT calculation is a combination of several noise sources, which may include the ADC quantization error and ADC internal noise. Externally, the voltage reference and the reference-driving amplifier contribute to overall system noise. The theoretical limit of the SNR is equal to 6.02n + 1.76dB, where n is the number of ADC bits.

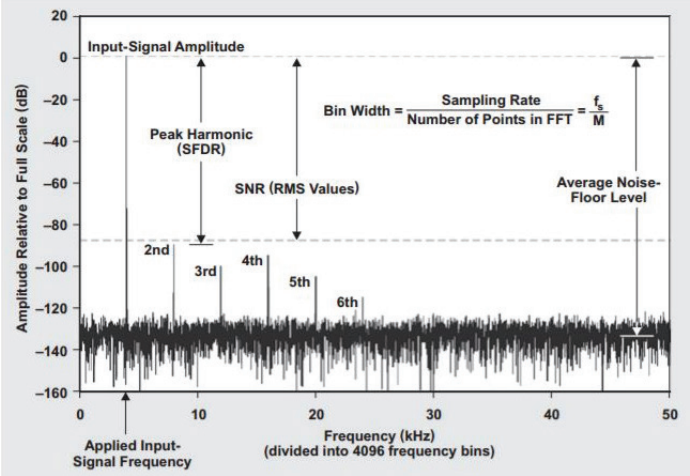


Figure 5: FFT plot with 8,192 data samples from a 16-bit converter.

The THD quantifies the amount of distortion in the system. THD is the ratio of the root sum square (RSS) of the powers of the harmonic components (spurs) to the input-signal power. For example, in **Figure 5**, the harmonic components are labeled "2nd" through "6th." An RSS calculation is also known as the square root of the sum of the squares of several values. Spurs resulting from the nonlinearity of the ADC appear at whole-number multiples of the input signal's frequency (the fundamental frequency). Most manufacturers use the first six to nine harmonic components in their THD calculations.

If the ADC creates spikes in the FFT plot, the converter probably has some integral nonlinearity errors. Additionally, spurs can come from the input signal through the signal source or from the reference driving amplifier. If the driving amplifier is the culprit, the amplifier may have crossover distortion, or it may be marginally stable, slew rate-limited, bandwidth-limited or unable to drive the ADC.

Injected noise from other places in the circuit, such as digital clock sources or the frequency of the mains, can also contribute spurs to the FFT result. The combination of the converter's SNR and THD can determine the signal to noise and distortion (SINAD) of the device. Many designers refer to SINAD as "THD plus noise" or "total distortion." SINAD is an RSS calculation of the SNR and THD; that is, it is the ratio of the fundamental input signal's RMS amplitude to the RMS sum of all other spectral components below half the sampling frequency (excluding DC). While the SAR converter's theoretical minimum for SINAD is equal to the ideal SNR, or 6.02n + 1.76dB, the working SINAD is **Equation 5**:

$$SINAD(dB) = -20\log\sqrt{10^{-SNR/10} + 10^{THD/10}} \quad (5)$$

SINAD is an important figure of merit because it provides the effective number of bits (ENOB) with a simple calculation (**Equation 6**):

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \quad (6)$$

In an FFT representation of converter data, the average noise floor (see **Figure 5**) is an RSS combination of all of the bins within the FFT plot, excluding the input signal and signal harmonics. You can choose the number of samples vs. the number of ADC bits so that the noise floor is below any spurs of interest. With these considerations, the theoretical average FFT noise floor (in decibels) is:

$$FFT\ Noise\ Floor = 6.02n + 10\log\left(\frac{3M}{\pi\ x\ ENBW}\right)$$

where M is the number of data points in the FFT and ENBW is the equivalent noise bandwidth of the FFT window function. A reasonable number of samples for the FFT of a 12-bit converter is 4,096, which will result in a theoretical noise floor of -107dB.

Conclusion

The ADC specifications that impact the application circuit in **Figure 1** are gain error, transition noise and SNR. Part 2 of this series examines the voltage reference's DC accuracy and noise contribution to system performance.

2. How the Voltage Reference Affects ADC Performance: Design and Performance of a Voltage Reference System for SAR ADCs

By Miro Oljaca and Bonnie Baker

Now that we have examined the fundamental operation of an analog-to-digital converter (ADC) independent of the voltage reference and analyzed the performance characteristics that have an impact on system accuracy and repeatability, let's focus on the design and performance of a voltage reference system for a successive-approximation-register (SAR) ADC. We will also work through an example of how to design an appropriate external reference for 8-to 14-bit ADCs.

Choosing the Correct V_{REF} Topology

Voltage references are available in two-terminal shunt or three-terminal series configurations. The left side of **Figure 1** shows a two-terminal shunt voltage reference, in which the entire integrated circuit (IC) chip of the shunt reference operates in parallel to its load. With a shunt voltage reference, an input voltage is applied to the resistor connected to the cathode. The typical initial voltage accuracy of this device can be as low as 0.5 percent or as high as 5 percent, with a temperature coefficient of approximately 50 to 100µV/°C. The shunt voltage reference can be used to create positive, negative or floating reference voltages.

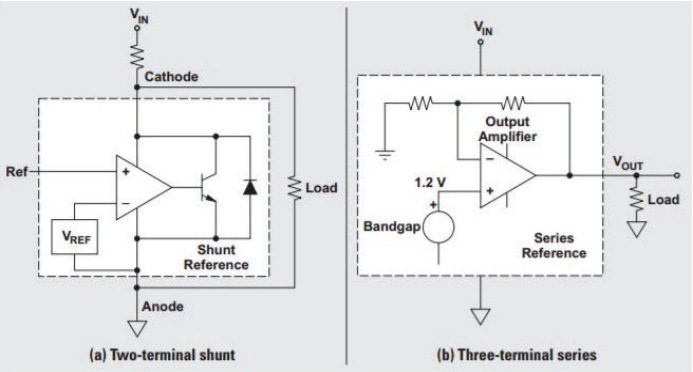


Figure 1: Voltage reference configurations.

The three-terminal series voltage reference (the right side of **Figure 1**) operates in series with its load. An internal bandgap voltage, in combination with an internal amplifier, creates the output voltage of this reference. The series voltage reference produces an output voltage between the output and ground while providing the appropriate output current to the external load. As the load current increases or decreases, the series reference maintains the voltage at V_{OUT}.

The typical initial voltage accuracy of a series-reference device can be as low as 0.05 percent or range up to 0.5 percent, with temperature coefficients as low as 2.5ppm/°C. Because of the series reference's superior initial output voltage and over temperature performance, you would use this type of device to drive the reference pins of precision ADCs. Beyond 8 or 14 resolution bits where the size of the least significant bit (LSB) is 0.4 percent and 0.006 percent, respectively, an external series voltage reference ensures that the intended precision of the converter can be achieved.

Another common application for series voltage references is sensor conditioning. In particular, a series voltage reference is useful in bridge-sensor applications as well as applications that have thermocouples, thermopiles and pH sensors.

The initial accuracy of the series voltage reference in an ADC application provides the general reference for the conversion process. Any initial inaccuracy of the output voltage can be calibrated in hardware or software. Additionally, changes in the accuracy of the voltage reference output can be a consequence of the temperature coefficient, the line regulation, the load regulation or long-term drift. The series voltage reference provides better performance in all of these categories.

Understanding Reference Voltage Noise

From Part 1 of this series, you can conclude that the ADC has only one function: to compare an input voltage to a reference voltage, or to create an output code based on an input signal and reference voltage. Part 1 presented diagrams and formulas that describe the basic transfer function of the ADC along with the device's noise characteristics. **Equation 1** expresses the typical transfer function of the ideal ADC shown in **Figure 2**:

$$Code = V_{IN} x \frac{2^n}{V_{REF}} \quad (1)$$

where Code is the ADC output code in decimal form, V_{IN} is the analog input voltage to the ADC, n is the number of ADC output bits and V_{REF} is the analog value of the reference voltage to the ADC.

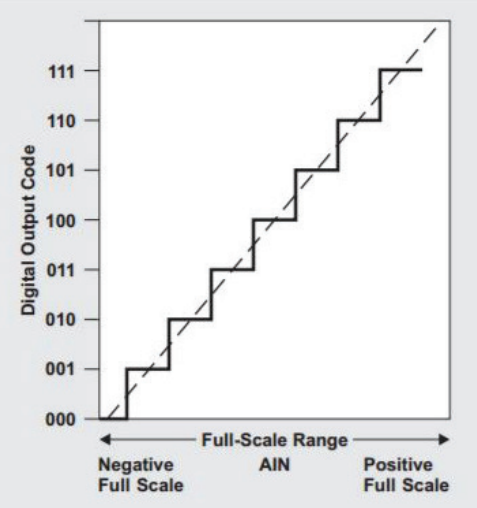


Figure 2: An ideal 3-bit ADC transfer function.

Equation 1 shows that any initial error or noise in the reference voltage translates to a gain error in the code output of the ADC. Measuring several points from the ADC's negative full-scale input to its positive full-scale input, it becomes clear that the contribution of the reference noise is a function of the ADC input voltage. To evaluate the voltage reference noise as well as the overall noise, it is necessary to measure the noise close to both the negative full scale and the positive full scale.

Figure 3 shows the results of measuring the reference noise and the ADC noise in a system. The overall noise is not constant but linearly dependent on the ADC's analog input voltage. When designing this type of system, keep the reference noise lower than the ADC's internal noise. Both reference topologies in **Figure 1** generate comparable noise over frequency. The voltage noise in series voltage references comes mainly from the bandgap and the output amplifier. Both of these elements generate noise in the 1/f region and the broadband region (see **Figure 3**)

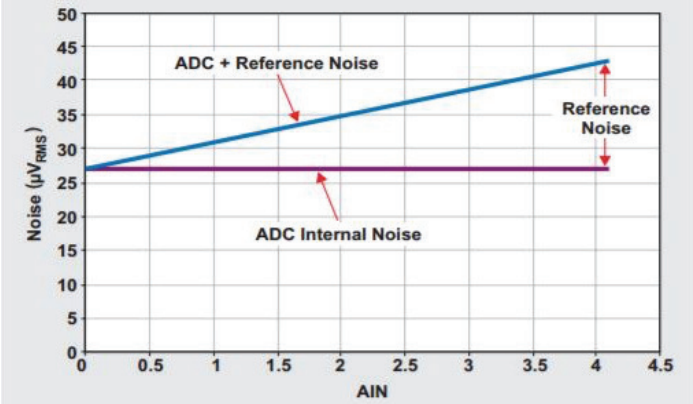


Figure 3: Total noise at ADC output as a function of ADC input voltage.

Noise in the Voltage Reference's 1/f Region

In the data sheets of most series reference devices, the specification for output voltage noise is over the frequency range of 0.1 to 10Hz, which encompasses the 1/f region in **Figure 4**. Broadband noise replaces noise in the 1/f region, often called "pink noise," in the higher frequency domain.

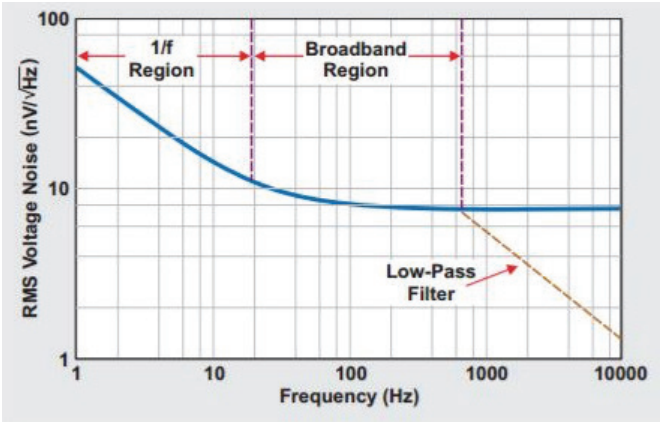


Figure 4: Voltage noise regions in the frequency domain.

Noise in the Voltage Reference's Broadband Region

Some manufacturers include specifications for the voltage reference's output noise density. This type of specification is usually for noise in the broadband region, such as the noise density at 10kHz. Broadband noise, which is present over the higher wideband frequencies, is also known as "white noise" or "thermal noise."

An added low-pass filter with an extremely low corner frequency will reduce the broadband noise at the output of the reference. This filter is designed with a capacitor, the equivalent series resistance (ESR) of the capacitor and the open-loop output impedance of the reference output amplifier (see **Figure 5**).

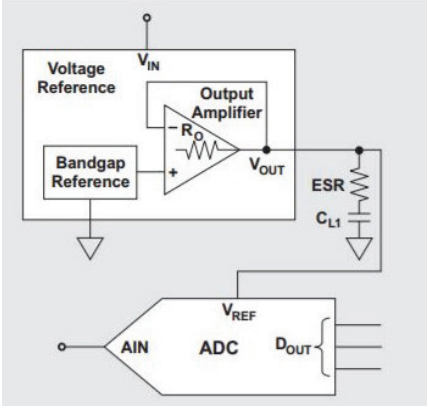


Figure 5: Low-pass filter between the series voltage reference and the ADC.

Table 1 shows the noise measured from TI's REF5040 for different frequency bandwidths, as well as for different external-capacitor values and types. These measurements demonstrate that ceramic capacitors with a low ESR of about 0.1Ω have a tendency to increase noise compared to tantalum capacitors with a standard ESR of about 1.5Ω. This tendency is the result of stability problems and the gain peaking of the reference's output amplifier.

CAPACITOR	MEASURED NOISE (μV_{RMS}) BANDWIDTHS			
	22 kHz (low-pass 5-pole)	30 kHz (low-pass 3-pole)	80 kHz (low-pass 3-pole)	>500 kHz
GND	0.8	1	1.8	4.9
1 µF (tantalum)	37.8	41.7	53.7	9017
2.2 µF (ceramic)	41.7	46.2	55.1	60.8
10 µF (tantalum)	33.4	33.4	35.2	38.5
10 µF (ceramic)	37.1	37.2	37.8	39.1
20 µF (ceramic)	33.1	33.1	33.2	34.5
47 µF (tantalum)	23.2	23.8	24.1	26.5

Table 1: Noise measured from the REF5040 for different bandwidths, capacitor values and types.

As we mentioned earlier, the two sources of noise in a reference voltage are the internal output amplifier and the bandgap. The internal schematic of the REF5040 in **Figure 6** shows that the TRIM pin provides direct access to the bandgap. Adding an external capacitor to the TRIM pin creates a low-pass filter that provides a bandgap broadband attenuation of approximately -21dB. For example, a small 1µF capacitor adds a pole at 14.5Hz and a zero at 160Hz. If you need more filtering, you can use a larger-value capacitor in place of the 1µF capacitor. For instance, a 10µF capacitor will generate a 3dB corner frequency of 1.45Hz. This low-pass filter will lower the bandgap noise. Attaching a 1µF capacitor to the TRIM pin of the REF5040 will lower the total output root mean square (RMS) noise by a factor of 2.5.

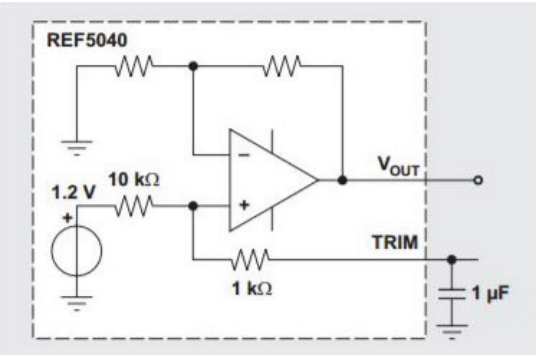


Figure 6: Using the TRIM pin to filter REF5040 bandgap noise.

Conclusion

Figure 7 shows a complete circuit diagram for a reference system configured with an 8- to 14-bit converter. The accuracy of the voltage reference in this system is important; however, you can calibrate any initial inaccuracies with hardware or software. On the other hand, eliminating or reducing reference noise will require a degree of characterization and hardware-filtering techniques.

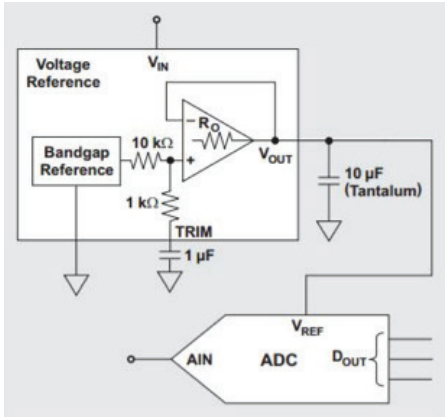


Figure 7: Voltage reference circuit for an 8- to 14-bit converter.

3. How the Voltage Reference Affects ADC Performance: Design of a Voltage Reference System for 16-Bit Converters

By Bonnie Baker and Miro Oljaca

It's time to tackle the challenge of designing a voltage reference circuit that is appropriate for converters with 16+ bits. We will also examine methods to improve noise filtering and compensate for losses caused by the improved filters.

Basics of Reducing Voltage Reference Noise

As discussed in Part 2 of this series, the two sources of noise in a reference voltage are the internal output amplifier and the bandgap. Let's use the voltage reference circuit from Part 2 that was configured with an 8- to 14-bit analog-to-digital converter (ADC) as a starting point to continue the discussion.

The size of the least significant bit (LSB) of any converter in a 5V system is equal to 5V/2N, where N is the number of converter bits. The 8-bit LSB size in this environment is 19.5mV, and the 14-bit LSB size is 305µV. The target value for voltage reference noise should be less than these LSB values. Adding an external capacitor to the output to create a low-pass filter reduced the bandgap noise of the circuit from Part 2. Adding another capacitor as a passive low-pass filter can reduce this circuit's output noise even further.

Figure 1 shows an example of a design that uses a voltage reference from TI's REF5025 family. In this design, the 1µF capacitor, C1, provides a minimal 21dB noise reduction at the internal bandgap reference. C2, in combination with the open-loop output resistance, RO, of the voltage reference's internal amplifier, further reduces the output noise of the reference at the V_{REF_OUT} pin. In this case, the equivalent series resistance (ESR) of the 10µF ceramic capacitor, C2, is equal to 200mΩ.

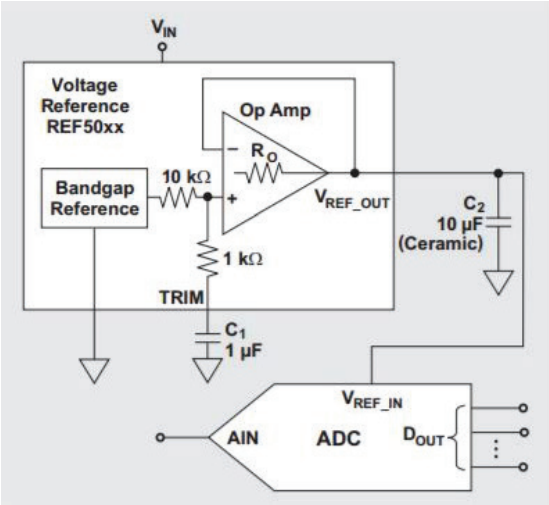


Figure 1: Voltage reference design appropriate for an 8- to 14-bit converter.

Figure 2 shows a fast Fourier transform (FFT) plot of the output signal of the circuit in **Figure 1**. The output-noise level peaks at around 9kHz because of the response of the circuit's internal amplifier to the capacitive load, C2. This peaking is the main contributor to the overall measured noise.

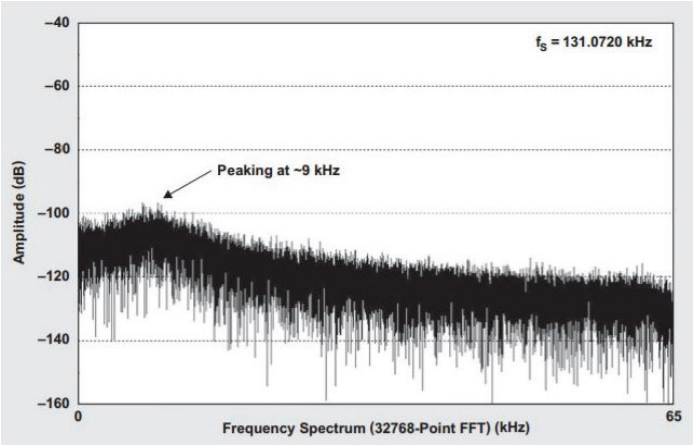


Figure 2: FFT plot of V_{REF_OUT} signal of the circuit shown in Figure 1.

The output noise, measured with an analog meter over a frequency range of up to 80kHz, is approximately 16.5µV_{RMS}. If you connected a voltage-reference circuit to the input of an ADC, the measured noise across a 65kHz frequency range would be 138µV_{PP}. This noise level makes the solution in **Figure 1** adequate for 8- to 14-bit converters.

Reducing Voltage Reference Noise for an ADC with 16+ Bits

Since the voltage reference circuit in **Figure 1** would introduce too much noise into a converter with 16+ bits, adding another low-pass filter can further reduce the voltage reference's output noise. This filter consists of a 10kΩ resistor, R1, and an additional capacitor, C3, as shown in **Figure 3**. The corner frequency of this added RC filter, 1.59Hz, will reduce broadband noise as well as noise at extremely low frequencies.

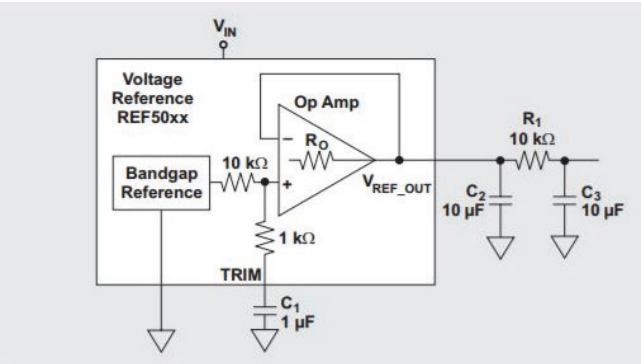


Figure 3: Voltage reference circuit with R1 and C3 added as filters.

Figure 4 shows that the addition of R1 and C3 has a significant effect on the output noise for this system. The 9kHz noise peak is gone. With this signal response, the output noise of the reference circuit in **Figure 3** becomes 2.2µV_{RMS} or 15µV_{PP}, a reduction of nearly 90 percent. This improvement brings the noise level so well under control that the voltage reference circuit is now appropriate for ADC resolutions of up to 20 bits.

While encouraging, pulling current through R1 from the ADC reference pin will corrupt the conversion by introducing a voltage drop equivalent to the average charge level from the reference pin of the ADC. Consequently, the output of this new circuit will not be able to adequately drive the ADC's voltage reference input. To accomplish this, you will need to add a buffer to the low-pass filters.

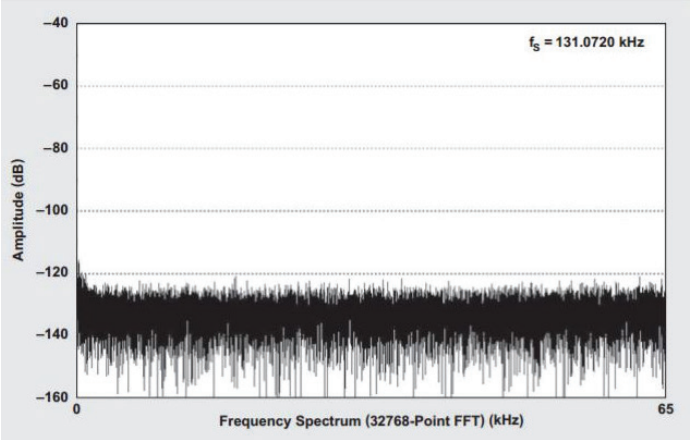


Figure 4: FFT plot of V_{REF_OUT} signal of the circuit with RC filter added.

Adding a Buffer to the Voltage Reference Circuit

Figure 5 shows an example of the fluctuations in ADC reference drive current that can occur during conversion. The signal was captured with a low-capacitance probe to show the voltage drop across the 10kΩ resistor, R1, between the input of the ADC voltage reference pin and V_{REF_OUT}. The top trace in **Figure 5** shows the trigger signal that the converter receives to initiate a new conversion. The ADC's voltage reference circuit demands different amounts of current (bottom trace) for the initiation of the conversion and for each code decision. Therefore, the voltage reference analog circuitry connected to the ADC must be able to accommodate these high-frequency fluctuations efficiently while maintaining a strong voltage reference for the converter.

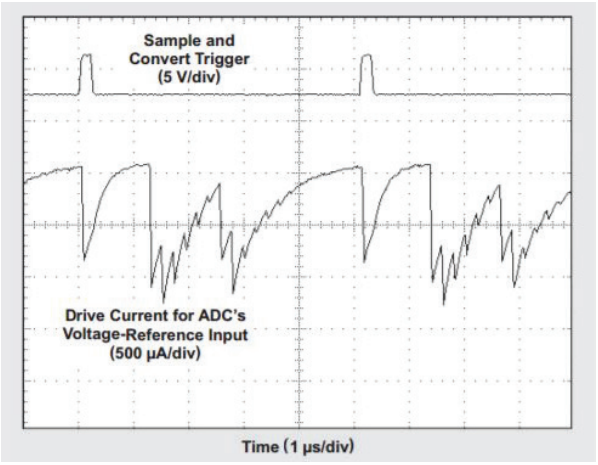


Figure 5: Drive current required by the ADC's reference input.

Figure 6 shows a voltage reference circuit that will adequately drive a high-resolution ADC. In this circuit, TI's OPA350 is placed as a buffer after the low-pass filter that was constructed with R1 and C3 for the circuit in **Figure 3.** The OPA350 drives a 10µF filter capacitor, C4, and the voltage reference input pin of the ADC. The noise measured at the output of the OPA350 in **Figure 6** is 4.5µVRMS or 42µVPP. The input bias current of the OPA350 is 10pA at 25°C. This current, in combination with the current through R1, generates a 100nV constant DC drop. This voltage drop does not change with the ADC's bit decisions. It is true that the input bias current of the OPA350 changes over temperature, but you can expect a maximum current that is no more than 10nA at 125°C. This value generates a change of 100µV over a temperature range of 100°C.

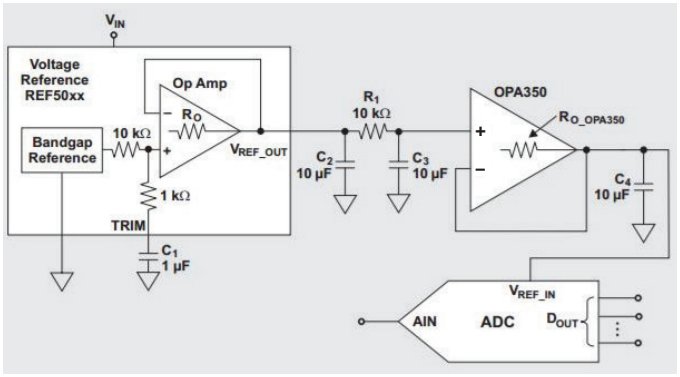


Figure 6: Voltage reference circuit with added buffer and output filter.

Let's put the voltage drop across R1 into perspective. This voltage drop is added to the errors contributed by the REF5025 and the OPA350. The initial error of the REF5025 output is ±0.05 percent, with an error over temperature of 3 ppm/°C. With a 4.096V reference (REF5040), the initial reference error is equal to 2.05mV at room temperature and an additional 1.23mV at 125°C. Therefore, the reference output error is significantly larger than the errors produced by R1 and variations in the OPA350's offset and input bias current.

Amplifier Stability

We have a final word of caution about the circuit in **Figure 6**. The stability of the OPA350 can be compromised if C4 and the OPA350's open-loop output resistance (RO_OPA350) modify the open-loop voltage-gain (AOL) curve to create a marginally stable state. To illustrate this phenomenon, **Figure 7** shows how the output capacitor, C4, with a 0.2W ESR and the OPA350's open-loop output resistance (43W), modifies the OPA350's AOL curve. You can use these curves to quickly determine the stability of the circuit.

A circuit with good stability would be one where the rate of closure of the operational amplifier's modified AOL curve and closed-loop voltage-gain (ACL) curve is 20dB/decade. The open-loop output resistance of the OPA350 is 43Ω, and the ESR of C4 (RESR_C4) is 200mΩ. The frequency locations of the pole and zero that are created by these values are:

$$\frac{I_{SINKN}}{I_{SINK1}} = \frac{V_{SN}/R_{SETN}}{V_{REF}/R_{SET1}} = \frac{V_{SN}}{V_{REF}} \cdot \frac{R_1}{R_N} = \frac{V_{SN}}{V_{REF}} \cdot M_{RN} = M$$

Per **Figure 7**, the circuit in **Figure 6** is stable.

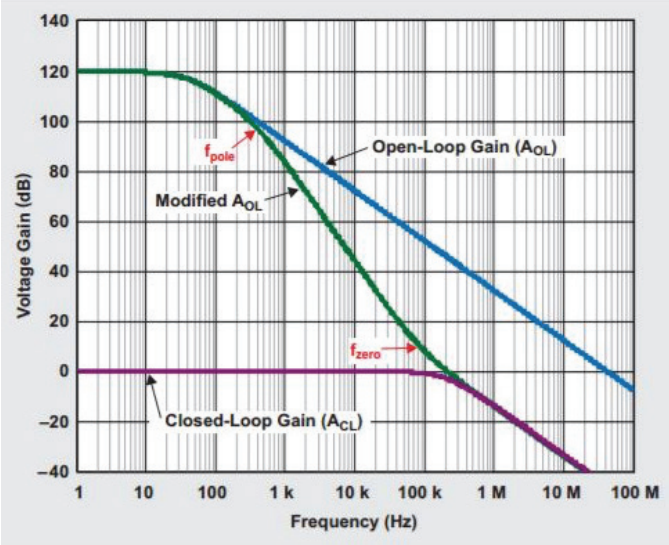


Figure 7: Frequency response of buffer with an RC load.

Unfortunately, the voltage reference designs in this article can degrade ADC performance by adding unwanted temperature drift and initial gain error. Higher-performance systems with 21+ bits may require a voltage reference design that addresses these issues.

4. SAR ADC PCB Layout: The Reference Path

By Luis Chioye

When designing a high-performance data-acquisition system, you probably carefully select a precision analog-to-digital converter (ADC) and the additional components you need for the analog front-end conditioning circuit. After spending weeks designing, performing simulations and optimizing the schematic, you quickly put a board layout together to meet a tight deadline. The first prototype board is tested a week later. To your surprise, the circuit does not perform as expected. Has this ever happened to you?

Optimal printed circuit board (PCB) layout is essential to obtain the performance you expect from your ADC. When designing circuits with mixed-signal devices, you should always start with a good grounding scheme and partition the design into analog, digital and power sections, using optimal component placement and signal routing.

The reference path is the most critical in ADC layout, because all conversions are a function of the reference voltage. With a traditional successive-approximation-register ADC (SAR ADC) architecture, the reference path is also the most sensitive, as the reference pin presents a dynamic load to the reference source.

Since the reference voltage is sampled several times during each conversion, high-current transients are present in the terminal where the ADC's internal capacitor array switches and charges as the bit decisions are made. The reference voltage must remain stable and settled to the required N-bit resolution during each conversion clock cycle, or linearity errors and missing code errors may occur.

Figure 1 shows the current transients during the conversion phase on the reference terminal for a classic 12-bit SAR ADC.

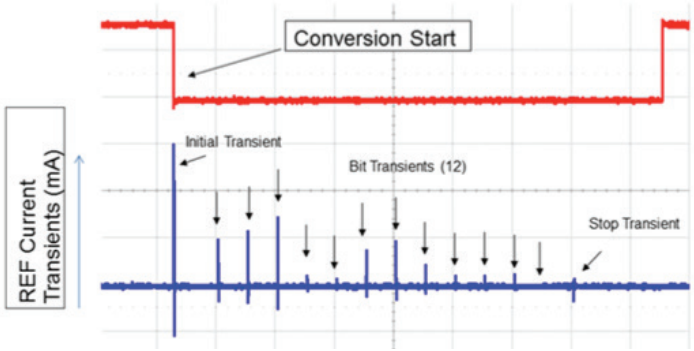


Figure 1: Current transients on the reference pin of a 12-bit SAR ADC.

Because of these dynamic currents, the reference pin requires good decoupling using a high-quality bypass capacitor, CREF. The bypass capacitor is used as a charge storage reservoir that can provide instantaneous charge during high-frequency transient currents. You should place the CREF as close as possible to the reference pin and connect them using short, low-inductance connections.

Figure 2 shows a board layout example for the ADS7851, a 14-bit dual ADC with two independent internal voltage references.

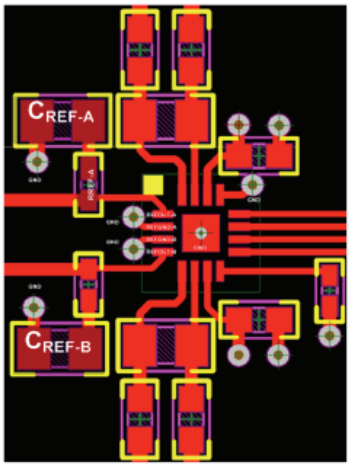


Figure 2: Layout example for a dual ADC with two independent internal references.

In this four-layer PCB example, using a solid ground plane right underneath the device partitions the board into analog and digital sections, keeping the sensitive inputs and reference signals away from noise sources. Bypassing the REFOUT-A and REFOUT-B reference outputs with 10µF, X7R-grade, 0805-size ceramic capacitors (CREF-x) optimizes performance. Connecting the capacitors to the device using small 0.1Ω series resistors keeps the overall impedance low and constant at high frequencies. Using wide traces reduces inductance.

I highly recommend placing CREF in the same layer as the ADC. You should also avoid placing vias (electrical interconnect holes that run through one or more adjacent layers in the PCB) between the reference pins and bypass capacitors. Each reference ground pin of the ADS7851 has an independent via connection to ground, and each bypass capacitor has its own low-inductance connection to the ground path.

If you're using an ADC that requires an external reference source, you should minimize the inductance in the reference signal path – starting from the reference buffer output to the bypass capacitor to the ADC's reference input.

Figure 3 shows a layout example for the ADS8881, an 18-bit SAR ADC using an external reference and buffer. Keep the inductance between the reference capacitor and the REF pin less than 2nH by placing the capacitor within 0.1 inches from the pin and connecting it with wide 20-mil traces and multiple 15-mil grounding vias. I recommend a single 10µF, X7R-grade, 0805-size ceramic capacitor with at least a 10V rating.

Keep the trace length from the reference buffer circuit to the REF pin as short as possible to ensure a fast settling response.

Proper decoupling of the REF pin is critical to achieving optimum performance. In addition, keeping low inductance connections in the reference path enables the reference driving circuit to remain stable and settled during the conversion phase, getting you one step closer to obtaining your desired results.

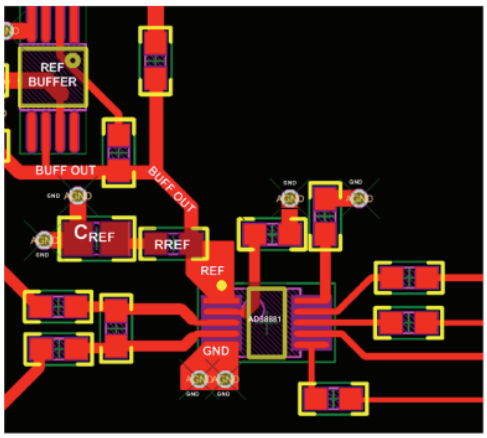


Figure 3. Layout example for an ADC with an external reference and buffer.

The layout guidelines in the ADS8881 and ADS7851 data sheets offer a deeper look into this topic.

5. Designing a Voltage Reference Circuit for an ADC

By Peggy Liska

High-precision data-acquisition systems are designed to minimize errors from various system components, like those introduced by switching transients on the reference input of a data converter. In the case of a successive-approximation-register analog-to-digital converter (SAR ADC), circuitry inside the data converter as it connects and disconnects different capacitive loads throughout the conversion cycle causes switching transients. Other data converters, such as delta-sigma ADCs and digital-to-analog converters (DACs), can also impose switching transients on the reference pin.

Figure 1 shows a simplified representation of the SAR ADC architecture. During operation, switches S1 and S2 inside the ADC control the acquisition and conversion cycles. When S1 closes and S2 opens, a transient condition occurs on the input because of an impedance change. There are detailed technical resources that discuss how to optimize the input circuitry to minimize the impact of the input transient, such as the user guide for the 16-bit 1MSPS Data Acquisition Reference Design for Single-Ended Multiplexed Applications. But here, I'd like to focus on the transients generated on the reference

voltage input pin (V_{REF}), since these transients and their effect on system performance are often overlooked in system-level design.

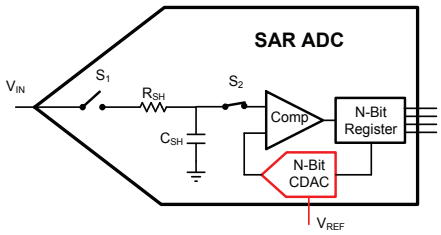


Figure 1: Simplified SAR ADC internal architecture.

The V_{REF} pin of a SAR ADC is internally connected to a capacitive DAC (CDAC), highlighted in red in **Figure 1**. **Figure 2** provides additional detail on a simplified CDAC structure. The CDAC is a binary weighted capacitor array that determines the digital value that best matches the input voltage in comparison to a reference voltage. The key point is that the reference input pin connects to the binary weighted capacitor array, which can cause variations in the reference voltage applied to the V_{REF} pin during a conversion cycle. The capacitors in the array will not be at the same potential as the reference, so there will be a large, fast spike of in-rush current when connecting the capacitors to the external reference.

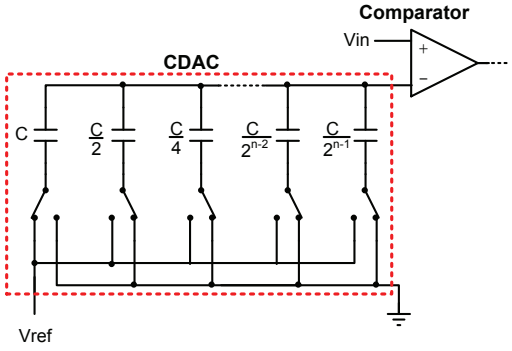


Figure 2: The internal CDAC architecture results in a switched capacitor load.

Figure 3 shows the spikes in reference input current that occur throughout the conversion cycle, which can be as large as 10mA and very short in duration (nanoseconds).

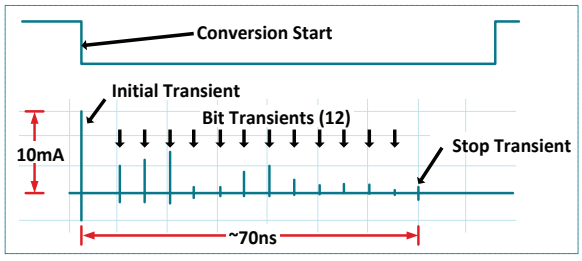


Figure 3: Switching transients on the VREF pin of a SAR ADC.

For optimal accuracy, the voltage reference connected to the SAR input needs to respond to the large, fast current spikes. These fast-switching current transients can cause a voltage drop across the high output impedance of the voltage reference. This voltage drop directly affects the output voltage of the reference and therefore the input voltage to the V_{REF} pin of the ADC, resulting in erroneous conversion of the input signal by the ADC.

To minimize the error introduced by these switching transients, the voltage reference should resettle to the desired output voltage between each current spike. A stand-alone voltage reference is designed to deliver a very accurate and stable voltage, given that the load is very light and slow-moving. Since these current spikes are very short in duration and large in magnitude, the reference is often buffered with a high-speed operational amplifier (op amp) (see **Figure 4)**. In addition, placing a capacitor at the pin can provide the total instantaneous current needed.

Although high-speed op amps are good from a transient perspective, they generally are not optimized for DC accuracy, such as offset voltage, linearity and drift. Thus, it can be challenging to find a buffer that meets the DC accuracy requirement but also has good transient behavior. In some cases, an amplifier topology containing two amplifiers will achieve this challenging objective. The user guide for that data-acquisition reference design I mentioned earlier explains this topology in more detail and covers the selection of the voltage reference, buffer amplifiers and associated filter components.

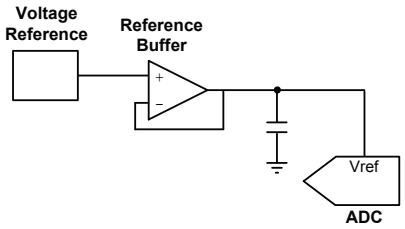


Figure 4: Voltage reference circuit using a high-speed amplifier.

In order to simplify the system-level design efforts required to minimize the effects of switching transients on the reference pin, TI's REF6000 voltage reference family integrates the reference buffer with the voltage reference. **Figure 5** shows this integration in a simplified data-acquisition system. The optimized internal buffer responds well to the types of transients generated on the reference pin of a data converter. The internal buffer is also optimized for DC performance. This combination of integrated voltage reference and reference buffer reduces circuit board area.

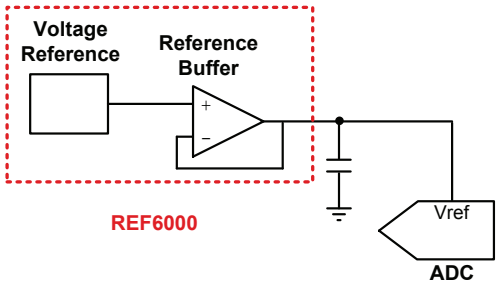


Figure 5: Voltage reference circuit using an integrated voltage reference and reference buffer.

With this integrated approach, the performance of the ADC improves by providing a high-bandwidth, low-output impedance, DC-optimized solution for the input to the V_{REF} pin.

Table 1 compares the noise and distortion performance of an ideal ADC to ADCs with different voltage reference circuit configurations. You can see that the case without a reference driving buffer has degraded performance. Comparing the integrated reference buffer to the external buffer, the reference with the integrated buffer performs best.

CONFIGURATION	Ideal ADC (no V_{REF} fluctuation)	REF6045 with integrated buffer	REF5045 with external buffer	REF5045 without buffer
Average reference pin voltage (V)	4.5	4.501	4.502	4.502
Peak-to-peak variation in V_{REF} (µV)	0	76.8	153.6	472.5
Signal-to-noise ratio (SNR) (dB)	109.7	109.8	109.6	109.7
Total harmonic distortion (THD) (dB)	-133.4	-123.7	-118.8	-92.5
Spurious-free dynamic range (SFDR) (dB)	128	124.5	119	92.5
Signal-to-noise and distortion ratio (SINAD) (d	109.7	109.6	109.2	92.4
Reference circuit quiescent current (mA)	N/A	0.8	1.925	1

Table 1: ADC performance of various buffer configurations with an 18-bit ADC sampling at 1MSPS and 10kHz input frequency.

Chapter 3: Voltage References as Flexible Low-Drift DC Voltage or Current Sources

1. Dual-Output Voltage References

By Ying Zhou

Developing a low-drift system can be very difficult, especially with a bipolar input signal. Applications such as bidirectional current sensing (shown in **Figure 1**) require the use of two well-matched, low-drift reference voltages. The first voltage, V_{REF}, defines the full-scale range of the analog-to-digital converter (ADC). A bias voltage, V_{BIAS}, is necessary in order to level-shift the bipolar signal. It is desirable to have $V_{BIAS} = V_{REF}/2$ so that there are equal positive and negative swings for the ADC. I'll discuss three topologies for generating two reference voltages here.

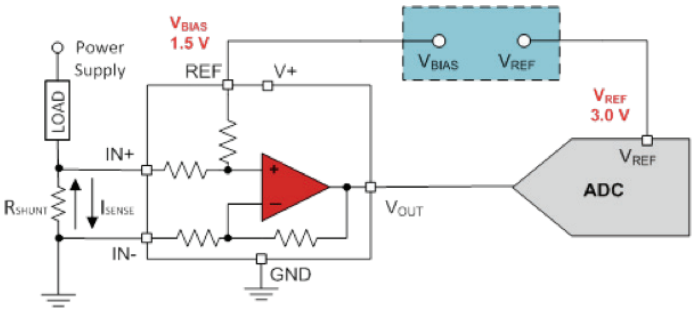


Figure 1: Low-drift bidirectional single-supply low-side current-sensing system.

Figure 2 demonstrates a straightforward approach using two separate voltage references.

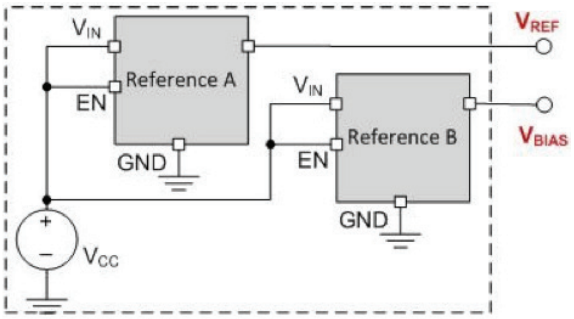


Figure 2: Solution No. 1 shows two separate references.

For the application in **Figure 1**, V_{REF} and V_{BIAS} are 3.0V and 1.5V, respectively. **Table 1** lists a couple of low-drift references. Considering drift, accuracy and cost, the REF5030A is a good option for the 3V reference voltage. Unfortunately, a low-drift, fixed 1.5V reference is not readily available. In that case, you might select a 1.25V reference such as the LM4140B, although this unbalances the positive and negative ranges.

Voltage (V)	Reference voltage	Drift (typ), ppm/ºC	Drift (max), ppm/ºC	Initial accuracy (%)
3	REF5030	2.25	3	0.05
	REF5030A	3	8	0.10
1.25	LM4140A-1.25	-	3	0.10
	LM4140B-1.25	-	6	0.10

Table 1: Drift and accuracy comparison of low-drift voltage reference options.

A secondary solution is possible given a 3V voltage reference using the voltage divider, as shown in **Figure 3**.

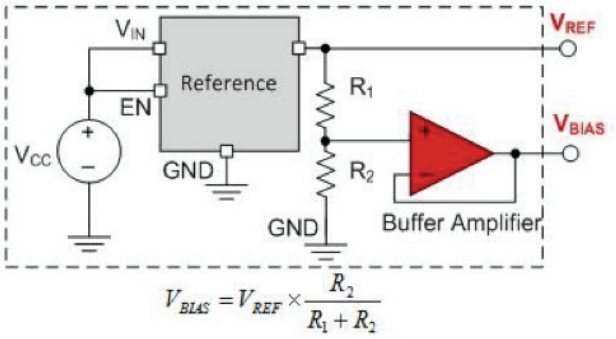


Figure 3: Solution No. 2 shows a reference + voltage divider + buffer.

Here, the drift of V_{BIAS}, as shown in **Equation 1**, comes from the drifts of the reference, δ_{REF}, resistor divider network, δ_{RDIV}, and buffer amplifier, δ_{BUF}:

$$\delta_{V_{BIAS}} = \sqrt{\delta_{REF}^{\ 2} + \delta_{RDIV}^{\ 2} + \delta_{BUF}^{\ 2}} \quad (1)$$

For a comparable low-drift solution, select resistors with 0.1 percent tolerance and 5 parts per million (ppm)/°C temperature drift. Considering that the full-scale range for the amplifier is 1.5V, the offset of the buffer amplifier is not significant. Targeting 0.1 percent error due to input offset voltage and 1ppm/°C drift error, the amplifier should have less than 1.5mV offset voltage and 1.5µV/°C drift.

Table 2 shows the devices selected for this solution. For more detail on component selection, see the Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design in the TI Designs reference designs library.

Voltage (V)	Device	Part number	Performance
3	Reference voltage	REF5030A	Initial accuracy: 0.1% Drift: 8 ppm/ºC (max)
1.25	Resistor	PCF0603-13-4K99BT1	Tolerance: 0.1% Drift: 5 ppm/ºC Resistance: 4.99 kΩ
	Amplifier	LMV831	Vos: 1.0 mV (max) Drift: 1.5 µV/ºC (max)

Table 2: Components for solution No. 2 (reference + voltage divider + buffer).

Take a quick look at the two solutions proposed here:

- Solution No. 1 is a straightforward approach, but restricted to fixed reference outputs. V_{BIAS} is not necessarily $V_{REF}/2$.
- Solution No. 2 uses only one reference, so the drift of V_{BIAS} will track with the drift of V_{REF}. Since the resistor can adjust accordingly, this solution has great value when $V_{BIAS} \neq V_{REF}/2$. On the downside, this solution requires more components.

Figure 4 shows a third solution that uses a dual-output voltage reference (REF2030) to offer both the V_{REF} and V_{BIAS} from one chip. Two independent buffers generate the V_{REF} and V_{BIAS} from the bandgap voltage. The internal resistors are sized such that $V_{BIAS} = V_{REF}/2$. **Table 3** lists the main specifications of the REF2030.

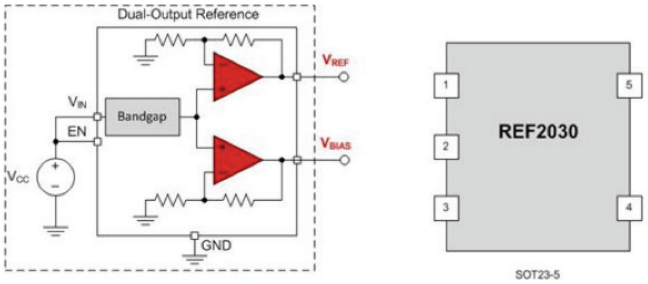


Figure 4: Solution No. 3 (REF2030 dual-output reference voltage).

Voltage (V)	Device	Performance
3, 1.25	REF2030	Initial accuracy: 0.05% Drift: 8 ppm/ºC (max) Drift: 3 ppm/ºC (typ) Drift tracking: 7 ppm/ºC (max) over –40ºC to 125ºC

Table 3: REF2030 specifications.

Now that you've seen three topologies to generate two reference voltages, let's now compare the performance of these solutions from three perspectives: total error, drift tracking and matching between outputs.

Total Error

Equation 2 converts specifications given as a percentage to parts per million:

$$ppm = 10000x\% \quad (2)$$

The total error performance metric of each voltage output depends on its initial accuracy and drift over the operating temperature range, as given by **Equation 3**:

$$E_{Total\_error} = \sqrt{E_{Initial\_accuracy}^{2} + E_{temp\_drift}^{2}} \quad (3)$$

In solution No. 1, as the LM4140B data sheet gives no typical drift, I used the maximum drift specification over a 70°C temperature range for calculation. In solution No. 2, the REF5030A, resistor network and a buffer generate the V_{BIAS}. Therefore, the initial accuracy and drift can be expressed as the root sum square (RSS) of these three error sources, as given in **Equation 1**. Since the REF2030 and REF5030A use the box method to determine drift, the temperature range for calculations is the entire operating range, or 165°C.

Table 4 shows that while the performance of V_{REF} in solution No. 1 is the same as solution No. 2, its V_{BIAS} output has considerably more error. The error for V_{BIAS} in solution No. 2 includes the error from V_{REF}. With high initial accuracy and low temperature drift on both outputs, solution No. 3 has the lowest error of the three solutions.

Solution	Voltage (V)		Error source	Initial accuracy error (ppm)		Temperature drift error (ppm)		Total error (ppm)
1	V_{REF}	3	REF5030A	1000		495		1116
	V_{BIAS}	1.25	LM4140B-1.250	1000		560		1146
2	V_{REF}	3	REF5030A	1000		495		1116
	V_{BIAS}	1.5	REF5030A	1000	1424	495	704	1589
			LMV831	167		33		
			PCF0603-13-4K99BT1	1000		500		
3	V_{REF}	3	REF2030	500		495		704
	V_{BIAS}	1.25						

Table 4: Comparison of error contributions for each output voltage.

Drift Tracking and Matching

Another important specification for this dual output system is drift tracking, which describes the accuracy matching between two voltages over a particular temperature range, as given by **Equation 4**. **Figure 5** shows the typical drift-tracking performance of the REF2030.

$$Drift\ Tracking = \left(\frac{V_{DIFF(MAX)} - V_{DIFF(MIN)}}{V_{REF} x TempRange} \right) x10^{6} (ppm) \quad (4)$$

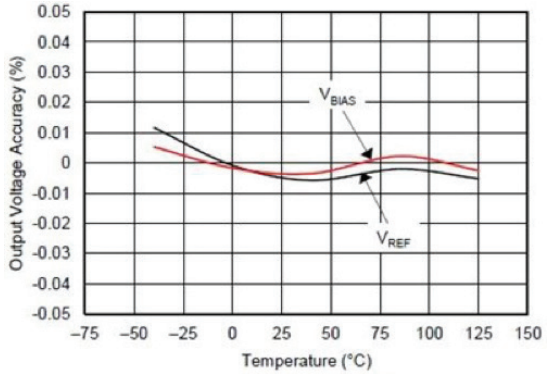


Figure 5: V_{REF} and V_{BIAS} tracking vs. temperature.

Since solution No. 1 applies two independent voltage references, theoretically the two references may not directly track each other, so the tracking is the RSS value of their maximum temperature drifts (11 ppm/°C). As the LM4140B is only specified from 0°C to 70°C, this drift tracking only applies for this temperature range.

In solution No. 2, since error in V_{REF} is common to both outputs, the drift tracking, $\delta_{Tracking}$, between V_{REF} and V_{BIAS} only depends on drift from resistor network, δ_{RES}, and buffer, δ_{BUF}), as given by **Equation 5**:

$$\delta_{Tracking} = \sqrt{\delta_{RES}^{\ 2} + \delta_{BUF}^{\ 2}} \quad (5)$$

Given the initial accuracy error, you can also calculate the matching (at 25°C) of the outputs in terms of RSS, as shown in **Equation 6**:

$$Output\_Matching = \sqrt{E_{V_{REF}\_Initial\_accuracy}^{\ 2} + E_{V_{MAX}\_Initial\_accuracy}^{\ 2}} \quad (6)$$

Table 5 is a comparison summary. The drift tracking and output matching in solution No. 2 heavily depend on the precision of the resistors. While the tracking of the two outputs in solution No. 2 is slightly better, the matching of the outputs is much worse than that in solution No. 3. Actually, solution No. 3 is about 900ppm better. This means that with only a 2ppm/°C difference in drift, it will take a 450°C temperature shift before solution No. 2 becomes the more accurate solution.

Solution	Error sources	Output matching (at 25°C, ppm)	Drift tracking (ppm/°C)
1	REF5030A LM4140B-1.250	1414	11
2	LMV831 PCF0603-13-4K99BT1	1014	5
3	REF2030	100	7

Table 5: Comparison of output matching and drift tracking.

From this comparison, you can see that solution No. 3 has the best overall performance in most cases. In reality, however, you have to consider more than performance. So let's take a look at how these three approaches stack up side by side with respect to space consumption and cost.

Space Consumption and Cost

Apart from system performance, printed circuit board (PCB) real estate requirements can be crucial in high-density applications. **Figure 6** offers a glance at the total PCB space (not considering decoupling capacitors) for each solution.

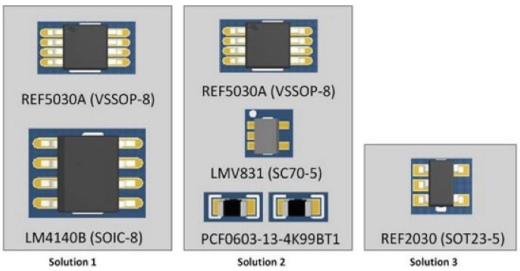


Figure 6: Total printed circuit board space for the three solutions.

Table 6 shows a brief calculation of the space needed (only considering body dimension). By offering dual outputs from one integrated solution with a package size of 4.64mm2, the REF2030 reduces total space by 83 percent and 67 percent relative to that occupied by solution Nos. 1 and 2, respectively. From the cost point of view, the REF2030 is 52 percent lower than solution No. 1 and 30 percent lower than solution No. 2.

Solution	Device	Package	Body size (mm x mm)	Total size (mm^2)	Cost (USD)
1	REF5030A	VSSOP-8	3 x 3	28.11	1.35
	LM4140B-1.250	SOIC-8	2.9 x 4.9		1.55
2	REF5030A	VSSOP-8	3 x 3	14.06	1.35
	LMV831	SC70-5	1.25 X 2		0.40
	2 x PFC0603-13-4K99BT	0603 (1608 metric)	1.6 X 0.8 (each)		0.48
3	REF2030	DDC-5	1.6 x 2.9	4.64	1.4

Table 6: Space consumption and cost of all three solutions.

Summary

Table 7 compares all three solutions.

Built by two independent voltage references, solution No. 1 is quite straightforward and easy to implement. However, the drawback is also obvious: it has limited availability in voltage

Solution	Voltage (V)	Device	Initial accuracy error (ppm)	Temperature drift error (ppm)	Total error (ppm)	Matching (at 25°C, ppm)	Drift tracking (ppm/°C	Body size (mm^2)
1	V_{REF} = 3	REF5030A	1000	495	116	1414	16	28.11
	V_{BIAS} = 1.25	LM4140B-1/25		560	1146			
2	V_{REF} = 3	REF5030A	1000	495	1116	1014	5	14.06
	V_{BIAS} = 1.25	LMV831	167	33	1589			
		PCF0603-13-4K99BT1	1000	500				
3	V_{REF} = 3 V_{REF} = 1.25	REF2030	500	495	704	100	7	4.64

Table 7: Final comparison of all three solutions.

options and no direct drift tracking between outputs. Besides, using two low-drift high-precision references is quite pricey.

While consuming more components and board space, solution No. 2 costs less and has better drift tracking than solution No. 1. However, the accuracy of V_{BIAS} in solution No. 2 is worse than solution No. 1 because it depends on the drift of V_{REF}, voltage divider and buffer amplifier. On the plus side, solution No. 2 is flexible in designing different bias voltages, where $V_{BIAS} \neq V_{REF}/2$.

The most notable difference with solution No. 3 is that it is a one-chip solution. This design has the best initial accuracy, along with lower cost and smaller PCB space usage.
In fact, solution No. 3 has 90 percent better output matching, consumes 67 percent smaller space and costs 30 percent less than solution No. 2. In another words, if you are targeting a low-drift system and don't want to pay high price for precision performance, solution No. 3 (REF2030) could be a good option.

2. Precision, Single-Output Current References

By Zachary Richards

Current sources and sinks are essential components of analog design, from the simple biasing of active analog circuitry to current-capacitor integrator reset and oscillator architectures. A convenient topology for implementing current sources and sinks uses a field-effect transistor (FET) driven by an operational amplifier to produce a current from the feedback of a small series resistance. **Figure 1** depicts this topology.

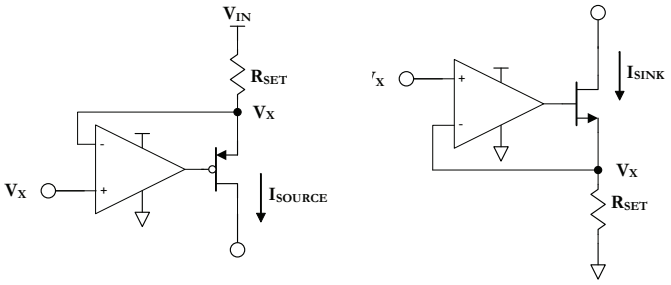


Figure 1: Feedback-generated current source and sink circuits.

As **Figure 1** illustrates, both circuits use negative feedback to force a voltage across the R_{SET} resistor, which generates the following source and sink currents (**Equations 1** and **2**):

$$I_{SOURCE} = \frac{(V_{IN} - V_X)}{R_{SET}} \quad (1)$$

$$I_{SINK} = \frac{V_X}{R_{SET}} \quad (2)$$

For these currents to be available as DC, the numerator in **Equations 1** and **2** must be constant. The simplest way to achieve this is to use a shunt voltage reference, as shown in **Figure 2**.

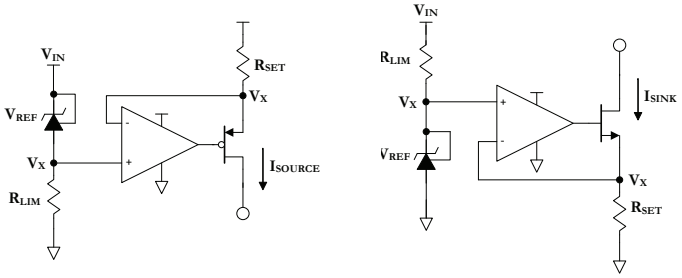


Figure 2: Feedback-generated current source and sink circuits from voltage references.

Note that in **Figure 2**, the R_{LIM} resistor drops excessive input voltage and limits current through the voltage reference. Further, a cathode-reference-tied adjustable voltage reference (such as the LMV431) forces the feedback voltage to its minimum value – this offers an important advantage that I'll explore later. Rewriting **Equations 1** and **2** as **Equations 3** and **4**:

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$$I_{SOURCE} = \frac{(V_{IN} - V_X)}{R_{SET}} = \frac{(V_{IN} - (V_{IN} - V_{REF}))}{R_{SET}} = \frac{V_{REF}}{R_{SET}} \quad (3)$$

$$I_{SINK} = \frac{V_X}{R_{SET}} = \frac{V_{REF}}{R_{SET}} \quad (4)$$

Combining **Equations 3** and **4** – since they are identical – into **Equation 5**, you can solve for the value of R_{SET} required to produce an arbitrary source or sink current, I_{SET}:

$$R_{SET} = \frac{V_{REF}}{I_{SET}} \quad (5)$$

The headroom that you must maintain across the FET and R_{SET} resistor limits the output voltage range of this topology. Minimizing the forced feedback voltage maximizes the valid output voltage range. **Equations 6** and **7** describe the current

source and sink behavior inside and outside the valid output voltage region, respectively:

$$I_{SOURCE} = \begin{cases} \frac{V_{REF}}{R_{SET}}, & V_{SOURCE} < V_{IN} - V_{REF} \\ \frac{V_{IN} - V_{SOURCE}}{R_{SET}}, & V_{SOURCE} \geq V_{IN} - V_{REF} \end{cases} \quad (6)$$

$$I_{SINK} = \begin{cases} \frac{V_{REF}}{R_{SET}}, & V_{SINK} > V_{REF} \\ \frac{V_{SINK}}{R_{SET}}, & V_{SINK} \leq V_{REF} \end{cases} \quad (7)$$

The internal V_{REF} of any adjustable voltage reference is roughly 1.24V. Generated via bandgap reference, this specific voltage will ultimately define the limits of this topology overall. To demonstrate, **Figure 3** is an example current sink characterization (including the linear current dropout) for an R_{SET} value of 124Ω.

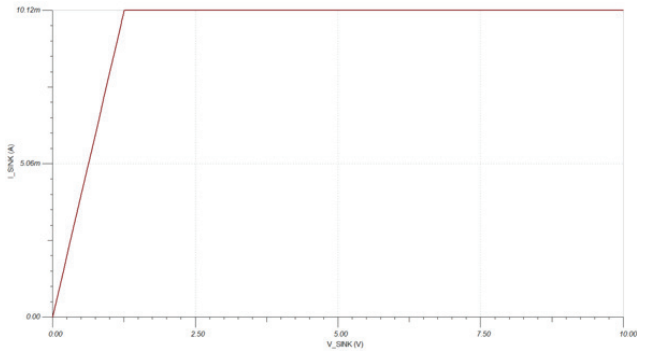

Figure 3: Sink current vs. output voltage characterization.

Substituting a bipolar junction transistor (BJT) for the FET in this topology may result in a marginally higher headroom requirement, although ultimately this substitution should behave almost identically.

The ideal current source is a fundamental element in circuit theory. While any physical implementation will always fall short of the ideal, it is valuable to understand the mechanisms behind these shortcomings in order to mitigate or avoid them. In the case of this topology, you have seen how the output voltage range impacts the output current and the important role that voltage reference selection plays in minimizing this.

3. Single Feedback Device Current Reference Networks

By Zachary Richards

Generating DC currents of arbitrary magnitude is a simple and straightforward process using operational amplifier feedback and a voltage reference. However, suppose it was necessary to generate some arbitrary number (N, for example) of current sinks (or sources), each with its own arbitrary magnitude, perhaps to bias the various stages of some complex analog circuitry. While the reference voltage generation requires only a single implementation, repetition of the entire feedback portion of the sink could become cost- and design area-intensive. So a question emerges: Is it possible to implement such a bias network using a single feedback source? The answer is yes – although it gets somewhat complicated and you must meet certain conditions. **Figure 1** shows such a network (sink only for this analysis).

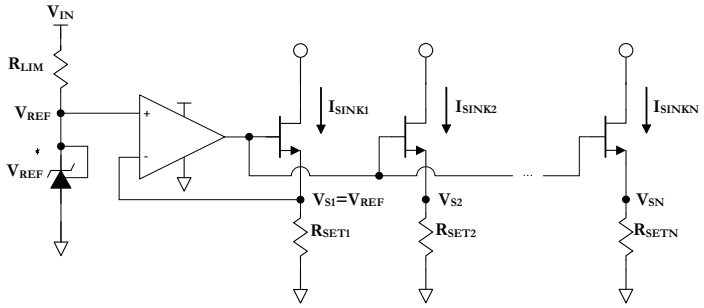

Figure 1: Current sink network.

The source voltage of the metal-oxide semiconductor field-effect transistor (MOSFET), V_S and R_{SET} resistor determine the sink current in each leg; by removing the feedback from the outer sink legs (that is, for all N>1), you lose direct control of V_{SN}. Thus, you must carefully select R_{SETN} to generate the desired, arbitrary Nth leg sink current, I_{SINKN}.

Examining **Figure 1, Equation 1** defines the ratio of current in the Nth leg of the bias network to that of the first:

$$\frac{SINKN}{SINK1} = \frac{V_{SN}/R_{SETN}}{V_{REF}/R_{SET1}} = \frac{V_{SN}}{V_{REF}} \cdot \frac{R_1}{R_N} = \frac{V_{SN}}{V_{REF}} \cdot M_{RN} = M_{IN} \quad (1)$$

Rearranging **Equation 1** in order to solve for the R_1 to R_N resistor ratio, M_{RN}, yields **Equation 2**:

$$M_{RN} = \frac{V_{REF}}{V_{SN}} \cdot M_{IN} \quad (2)$$

So what is the MOSFET source voltage in the Nth leg of the bias network, V_{SN}? Consider the drain current equation for an N-channel metal-oxide semiconductor (NMOS) operating in the saturation region (**Equation 3**):

$$I_{Dn} = \frac{1}{2} \cdot K_n \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad (3)$$

You can largely ignore the effects of channel-width modulation here because any increase in drain current from an increasing

drain voltage would drop across the R_{SET} resistor and result in an increased source voltage. In order for the MOSFET to maintain any current whatsoever, the gate voltage must be larger than the source and threshold voltages combined. That is, for a fixed gate voltage, the source voltage is ultimately clamped to at least a threshold voltage drop below it, and no amount of drain voltage increase will increase the drain current. Therefore, establishing the operating condition that R_{SET} must be sufficiently large to ensure this clamping allows me to make the following assumption. See **Equation 4**:

$$(1 + \lambda \cdot V_{DSN}) \approx 1 \tag{4}$$

Based on **Equations 3** and **4**, the ratio expressed in **Equation 1** can now be rewritten as **Equation 5**:

$$M_{IN} = \frac{I_{SINKN}}{I_{SINK1}} = \frac{\frac{1}{2} \cdot K_n \cdot (V_{GSN} - V_T)^2}{\frac{1}{2} \cdot K_n \cdot (V_{GS1} - V_T)^2} = \frac{(V_G - V_{SN} - V_T)^2}{(V_G - V_{REF} - V_T)^2} = \left(\frac{V_G - V_{SN} - V_T}{V_G - V_{REF} - V_T}\right)^2 \tag{5}$$

In order to simplify **Equation 5**, define the following term as **Equation 6**:

$$V_{GT} = V_G - V_T \tag{6}$$

After making this substitution and rearranging the terms in **Equation 5**, you can derive an equation for V_{SN} (**Equations 7** and **8**):

$$V_{GT} - V_{SN} = \sqrt{M_{IN}} \cdot (V_{GT} - V_{REF}) \tag{7}$$

$$V_{SN} = \left(1 - \sqrt{M_{IN}}\right) \cdot V_{GT} + \sqrt{M_{IN}} \cdot V_{REF} \tag{8}$$

Substituting **Equation 8** into **Equation 2** yields **Equations 9** and **10:**

$$M_{RN} = \frac{V_{REF}}{V_{SN}} \cdot M_{IN} = \left(\frac{V_{SN}}{V_{REF}}\right)^{-1} \cdot M_{IN} = \left[\frac{\left(1 - \sqrt{M_{IN}}\right) \cdot V_{GT} + \sqrt{M_{IN}} \cdot V_{REF}}{V_{REF}}\right]^{-1} \cdot M_{IN} \tag{9}$$

$$M_{RN} = \left[\left(1 - \sqrt{M_{IN}}\right) \cdot \frac{V_{GT}}{V_{REF}} + \sqrt{M_{IN}}\right]^{-1} \cdot M_{IN} \tag{10}$$

So what is the gate drive to threshold voltage difference, V_{GT}? It is ultimately determined by the feedback in the first leg of the bias network; it is essentially the voltage required to maintain the desired I_{SINK1} current, expressed by **Equation 11**:

$$I_{SINK1} = \frac{1}{2} \cdot K_n \cdot (V_{GT} - V_{REF})^2 = \frac{V_{REF}}{R_{SET1}} \tag{11}$$

After rearranging terms in **Equation 11**, you can determine an equation for V_{GT} (**Equations 12** and **13**):

$$\frac{2 \cdot V_{REF}}{K_n \cdot R_{SET1}} = (V_{GT} - V_{REF})^2 \tag{12}$$

$$V_{GT} = V_{REF} + \sqrt{\frac{2 \cdot V_{REF}}{K_n \cdot R_{SET1}}} \tag{13}$$

Substituting **Equation 13** into **Equation 10** yields **Equation 14**:

$$M_{RN} = M_{IN} \cdot \left[\left(1 - \sqrt{M_{IN}}\right) \cdot \left(\frac{V_{REF} + \sqrt{\frac{2 \cdot V_{REF}}{K_n \cdot R_{SET1}}}}{V_{REF}}\right) + \sqrt{M_{IN}}\right]^{-1} C \tag{14}$$

Finally, you can write the resistor ratio, M_{RN}, as solely a function of M_{IN} (along with some physical constants of the bias network devices) as **Equation 15**:

$$M_{RN} = M_{IN} \cdot \left[\left(1 - \sqrt{M_{IN}}\right) \cdot \left(1 + \sqrt{\frac{2}{K_n \cdot R_{SET1} \cdot V_{REF}}}\right) + \sqrt{M_{IN}}\right]^{-1} \tag{15}$$

So, what can you say about **Equation 15**? First of all, for an M_{IN} ratio of 1, the corresponding M_{RN} ratio will also be 1, as expected. Second, for values of M_{IN} greater than 1, notice that the two terms of the denominator of **Equation 15** take on different signs. This means that depending on certain physical quantities involved (Kn, R_{SET1}, V_{REF}), M_{RN} can become arbitrarily large. Thus, you should avoid this region, instead favoring the $M_{IN} \leq 1$ region by ensuring that I_{SINKN} is less than or equal to I_{SINK1} for all N.

Allowing the denominator of the root term in **Equation 15** (the Kn, R_{SET1}, V_{REF} product) to become large results in a 1-to-1 linear relationship between M_{RN} and M_{IN} in the limit. Ultimately, the range of usable values that V_{REF} and R_{SET1} can take on to increase this product will be limited by the headroom required for the sink, although it is worth noting that for a fixed I_{SINK1} value, increasing V_{REF} requires an increase in R_{SET1} as well. The final variable in the product, K_n, is the process transconductance of the MOSFET and can be maximized through device selection. **Figure 2** illustrates the effect of K_n on the linearity of the M_{RN}, M_{IN} relationship (across five decades of K_n values).

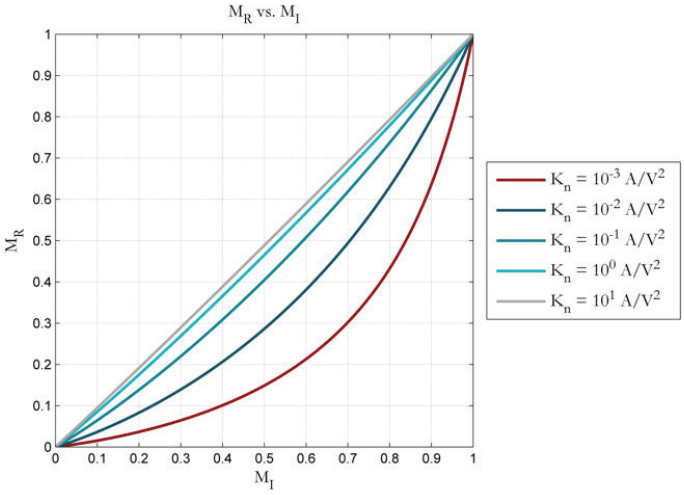

Figure 2: Resistor ratio vs. current ratio across process transconductance.

The process transconductance is so named due to its dependence on carrier mobility, oxide permittivity and oxide thickness (μ, εox, tox) – all material and process properties. See **Equation 16**:

$$K_n = k_n' \cdot \frac{W}{L} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} = \mu_n \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot \frac{W}{L} \quad (16)$$

However, the process transconductance is also dependent on the width-to-length ratio of the device, so in general, larger devices will result in the increasingly linear behavior in **Equation 15**. While most data sheets will not include K_n, you can calculate it from a common data sheet parameter, the forward transconductance, often listed as g_m or g_{FS}:

$$g_m = g_{FS} = \frac{\partial I_{Dn}}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left(\frac{1}{2} \cdot K_n \cdot (V_{GS} - V_T)^2\right) = K_n \cdot (V_{GS} - V_T) \quad (17)$$

Recall that the drain current equation for an NMOS operating in the saturation region is:

$$I_{Dn} = \frac{1}{2} \cdot K_n \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad (18)$$

Neglecting channel-length modulation and rewriting the terms of **Equation 18** to get **Equation 19**:

$$V_{GS} - V_T = \sqrt{\frac{2 \cdot I_D}{K_n}} \quad (19)$$

Substituting the result into **Equation 17** and ultimately solving for K_n using **Equations 20** and **21**:

$$g_m = K_n \cdot \sqrt{\frac{2 \cdot I_D}{K_n}} = \sqrt{2 \cdot I_D \cdot K_n} \quad (20)$$

$$K_n = \frac{{g_m}^2}{2 \cdot I_D} \quad (21)$$

Using **Equation 21**, it is possible to select the best MOSFET devices for the bias network. Further, having obtained this value, you can use it in **Equation 15** to calculate (more accurately) the required R_{SETN} resistor values to produce the desired I_{SINKN} currents.

Equation 15 tends to overestimate the R_{SETN} resistance in the $M_{IN} \leq 1$ region; that is, it results in currents that are lower than the desired value. However, the ideal transistor case ($M_{IN} = M_{RN}$) will always underestimate the R_{SETN} resistance in this region. Thus, calculating these two values will ultimately bound the exact value required.

Consider two randomly chosen N-channel field-effect transistors (NFETs): the N-channel MOSFET A and N-channel MOSFET B, which have listed g_{FS} values of 5.5A/V2 (at ID = 9A) and 15A/V2 (at ID = 31A), respectively. Suppose you use these NFETs to implement an M_{IN} ratio of one-fourth; **Table 1** shows the corrected $R_{SETN}$and M_{RN} ratios calculated using **Equation 15** (along with some straightforward design values).

	g_{FS} (S)	I_D (A)	K_N (A/V^2)	V_{REF} (V)	I_{SINK1} (A)	I_{SINKN} (A)	M_{IN}	R_{SET1} (Ω)	R_{SETN} (Ω)	M_{RN}
N-channel MOSFET A	5.5	9	1.68	1.25	1.0	0.25	0.25	1.25	7.18	0.174
N-channel MOSFET B	15	31	3.63	1.25	1.0	0.25	0.25	1.25	6.48	0.193

Table 1: Circuit parameters and calculated RSETN and MRN for MIN = one-fourth.

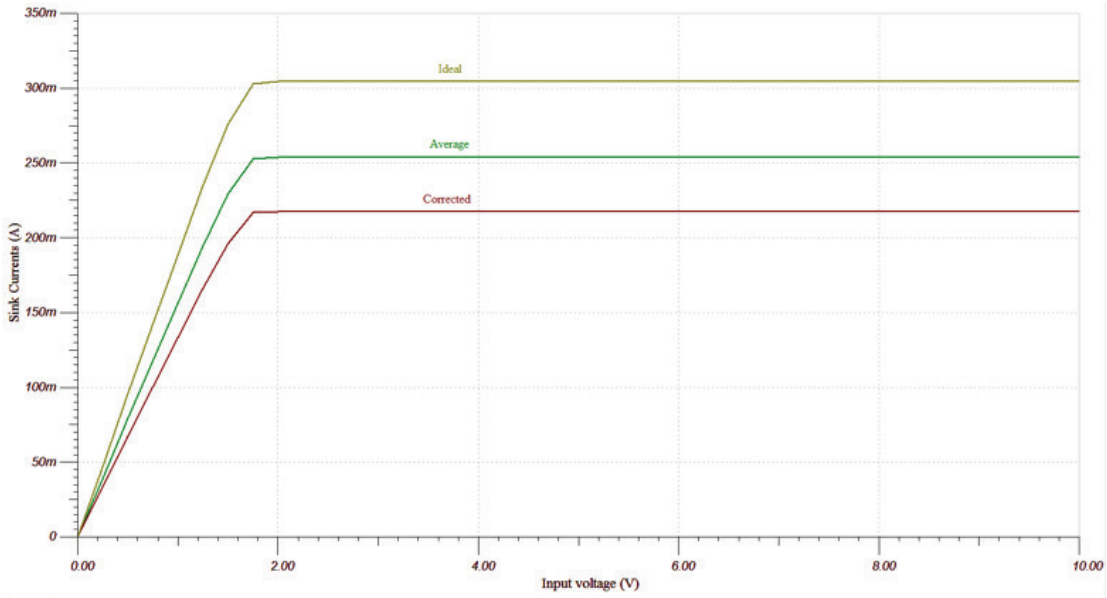

Figure 3: Sink current vs. drain voltage for ideal, corrected and average R_{SETN} values.

	Ideal			Corrected			Average		
	R_{SETN} (Ω)	I_{SINKN} (A)	Error (%)	R_{SETN} (Ω)	I_{SINKN} (A)	Error (%)	R_{SETN} (Ω)	I_{SINKN} (A)	Error (%)
N-channel MOSFET A	5.0	0.304	21.6	7.2	0.218	-12.8	6.1	0.254	1.5
N-channel MOSFET B	5.0	0.283	13.2	6.5	0.221	-11.6	5.7	0.248	-0.8

Table 2: R_{SETN} calculation methods and resulting accuracy.

Using the conditions listed in **Table 1** for the N-channel MOSFET B transistor, **Figure 3** displays the results of a TINA-TI™ software simulation of the circuit in **Figure 1** implemented with R_{SETN} values calculated from the ideal case (5Ω under these conditions), the corrected case (**Equation 15**) and the average of the two.

Table 2 summarizes the results of simulations using both the N-channel MOSFET A and N-channel MOSFET B with the three R_{SETN} values (as described above), along with their corresponding percent error calculations.

Ultimately, you can use a single feedback device to derive a bias network of arbitrary values as long as you meet certain conditions: that the current in the primary feedback-driven leg is the largest in the network and that proper headroom is maintained in each leg. Thus, a bias network is established from a single voltage reference.

4. Simple, Precision Current Sink Architecture

By Zachary Richards

Generating DC currents of arbitrary magnitude is a simple and straightforward process using operational amplifier feedback and a voltage reference. Several external operational amplifier (op amp) architectures exist for realizing individual or networks of current sources and sinks.

Let's address an architecture that uses feedback from within the voltage reference itself. Consider the voltage reference's symbol and its actual functional block diagram, as shown in **Figure 1**.

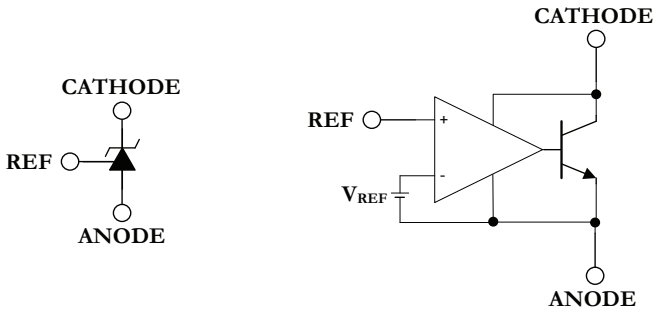

Figure 1: Voltage reference and its functional block diagram.

I borrowed the symbol for the Zener diode because that's essentially how the voltage reference behaves; however, this behavior is possible through clever design rather than simple device physics alone. Consider the self-referenced (cathode-reference-tied) configuration shown in **Figure 2**.

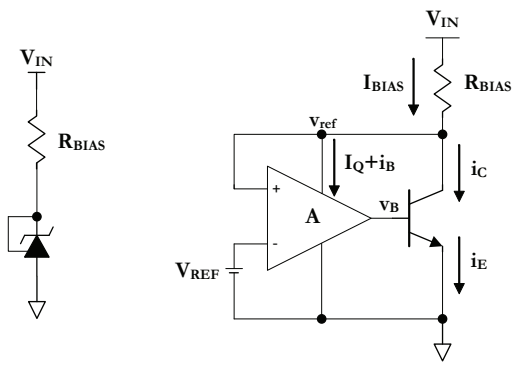

Figure 2: Voltage reference typical operation.

What can you say about this setup? First of all, you can greatly simplify and define the situation with all of the currents in **Figure 2**, as shown in **Equation 1**:

$$\boldsymbol{I_{BIAS} = I_Q + i_B + i_C = I_Q + i_E} \quad (1)$$

I_{BIAS} is the summation of the op amp quiescent current, I_Q, and the emitter current, i_E, of the bipolar junction transistor (BJT). **Equation 2** further simplifies this by acknowledging that the op amp quiescent current will be negligible compared to the emitter current during normal operation:

$$\boldsymbol{I_{BIAS} \approx i_E} \quad (2)$$

Equations 3 and **4** define the emitter current, beginning with the diode equation for the base-emitter junction and assuming forward bias operation with nominal ideality factor:

$$\boldsymbol{i_E = I_S \cdot (e^{\frac{v_{BE}}{n \cdot V_T}} - 1) \approx I_S \cdot e^{\frac{v_{BE}}{V_T}}} \quad (3)$$

$$\boldsymbol{I_{BIAS} \approx I_S \cdot e^{\frac{v_{BE}}{V_T}}} \quad (4)$$

As indicated by **Equation 4**, there must be some base-emitter voltage present to maintain I_{BIAS}. This implies that there is a non-zero difference between v_{ref} and V_{REF} in **Figure 2**; let's account for this by defining v_{ref} in **Equation 5** in terms of V_{REF} and a small perturbation voltage, ε_v:

$$\boldsymbol{v_{ref} = V_{REF} + \varepsilon_v} \quad (5)$$

You can now define ε_v in terms of the base-emitter voltage and op amp gain, as shown in **Equations 6** and **7**:

$$\boldsymbol{v_{BE} = A \cdot (V_{REF} + \varepsilon_v - V_{REF}) = A \cdot \varepsilon_v} \quad (6)$$

$$\boldsymbol{\varepsilon_v = \frac{v_{BE}}{A}} \quad (7)$$

Clearly ε_v drops to zero in the ideal op amp case; however, let's consider some very conservative values. **Equation 8** solves **Equation 7** assuming that the v_{BE} required to maintain I_{BIAS} is 0.5V and the gain of the op amp is a mediocre 104:

$$\boldsymbol{\varepsilon_v = \frac{0.5V}{10^4} = 50\mu V} \quad (8)$$

For a 1.25V voltage reference, this represents an error of some four thousandths of a percent or 40ppm – that is, you can safely regard such an error as negligible.

Now consider what happens to ε_v when you increase the input voltage, and therefore I_{BIAS}; specifically doubling I_{BIAS} from some arbitrary operating point, as illustrated by **Equations 9** and **10**:

$$\boldsymbol{I_{BIAS1} = I_S \cdot e^{\frac{v_{BE1}}{V_T}}} \quad (9)$$

$$\boldsymbol{I_{BIAS2} = I_S \cdot e^{\frac{v_{BE2}}{V_T}} = 2 \cdot I_{BIAS1}} \quad (10)$$

You can now derive the change in V_{BE} required to support doubling I_{BIAS} by dividing **Equation 10** by **Equation 9** and simplifying terms, as shown in **Equations 11** through **13**:

$$\boldsymbol{\frac{I_{BIAS2}}{I_{BIAS1}} = \frac{I_S \cdot e^{\frac{v_{BE2}}{V_T}}}{I_S \cdot e^{\frac{v_{BE1}}{V_T}}} = \frac{e^{\frac{v_{BE2}}{V_T}}}{e^{\frac{v_{BE1}}{V_T}}} = 2} \quad (11)$$

$$\boldsymbol{\frac{v_{BE2}}{V_T} - \frac{v_{BE1}}{V_T} = \ln(2)} \quad (12)$$

$$\boldsymbol{V_{GT} = V_{REF} + \sqrt{\frac{2 \cdot V_{REF}}{K_n \cdot R_{SET1}}}} \quad (13)$$

Finally, you can derive an equation for the change in ε_v required to support doubling I_{BIAS}, as shown in **Equations 14** and **15**:

$$\boldsymbol{\Delta v_{BE} = A \cdot \varepsilon_{v2} - A \cdot \varepsilon_{v1} = A \cdot \Delta\varepsilon_v} \quad (14)$$

$$\boldsymbol{\Delta\varepsilon_v = \frac{\Delta v_{BE}}{A} = \frac{V_T \cdot \ln(2)}{A}} \quad (15)$$

Substituting in the room-temperature value of the thermal voltage, V_T, and assuming (again) the mediocre op amp gain of 10^4, you can solve **Equation 15** for a conservative value of $\Delta\varepsilon_v$ required for doubling I_{BIAS}, resulting in **Equation 16**:

$$\boldsymbol{\Delta\varepsilon_v = \frac{V_T \cdot ln(2)}{A} = \frac{17.92mV}{10^4} = 1.792\mu V} \quad (16)$$

In this case, every time I_{BIAS} doubles, the voltage at v_{ref} increases by only 1.792µV. It is this multiplication of op amp gain with the exponential IV characteristic of the base-emitter diode that mimics Zener breakdown behavior.

Connecting the voltage reference differently, you can leverage its internal op amp to generate a simple current sink, as shown in **Figure 3**:

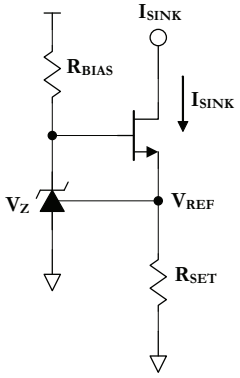

Figure 3: Simple voltage reference-derived current sink.

To visualize what's going on here, consider the functional diagram inserted in place of the symbol, as shown in **Figure 4**.

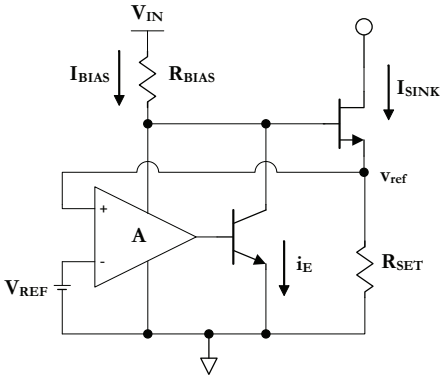

Figure 4: Simple current sink functional diagram.

The V_{IN}, R_{BIAS} and the BJT circuit essentially act as an inverting output stage for the op amp. Therefore, you can collapse the total combination into a new op amp symbol with a new gain, AT, and reversed input polarity, as shown in **Figure 5**.

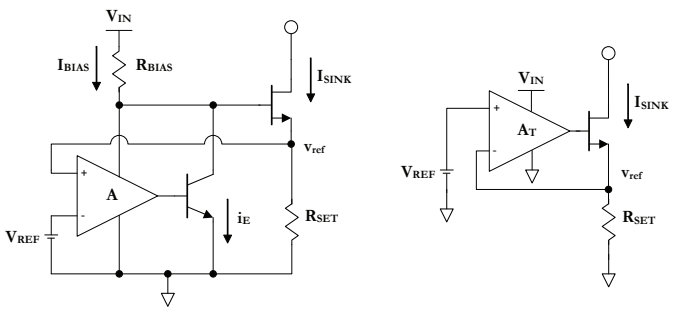

Figure 5: Simple current sink functional diagram and equivalent circuit.

5. Designing for Isolated DC/DC Converter Shunt Safety

By Ron Michallick

Did you know that your shunt regulator is in danger? No? Don't worry – the fix is free. Free is good.

A very common feedback circuit used in isolated DC-to-DC converter applications uses a shunt regulator such as the ATL431 and an optical isolator to feed back the output voltage to the pulse-width-modulator (PWM) controller. This circuit is effective and easy to use. However, you may not be aware of the hidden electrostatic discharge (ESD)/electrical overstress (EOS) danger.

At first glance, the shunt regulator in **Figure 1** seems immune to EOS. An overvoltage on V_{OUT} will cause the cathode voltage to drop and the reference pin will not rise due to the internal diode from the reference pin to the cathode pin. The series resistors will protect the shunt by limiting the current on both the reference and cathode pins. A negative voltage V_{OUT} will not hurt the shunt due to the rectifier clamping the voltage and the series resistors limiting current to the shunt.

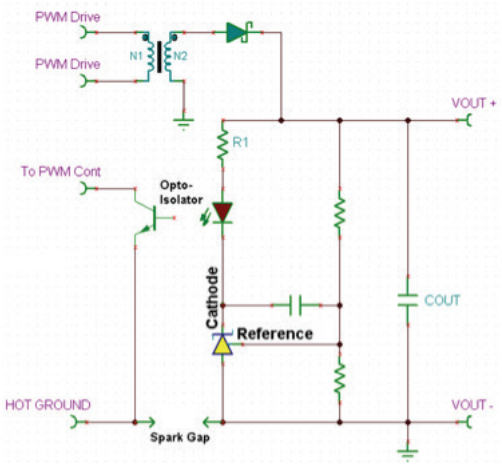

Figure 1: Error amplifier circuit for isolated DC/DC converter.

However, the shunt regulator can be damaged if the voltage across the isolation becomes too high during an ESD event. The weakest point in the isolation is usually the optical-isolator leads.

Once the optical-isolator gap is breached, the easiest path for ESD discharge will be though the shunt regulator, as shown by red line in **Figure 2**.

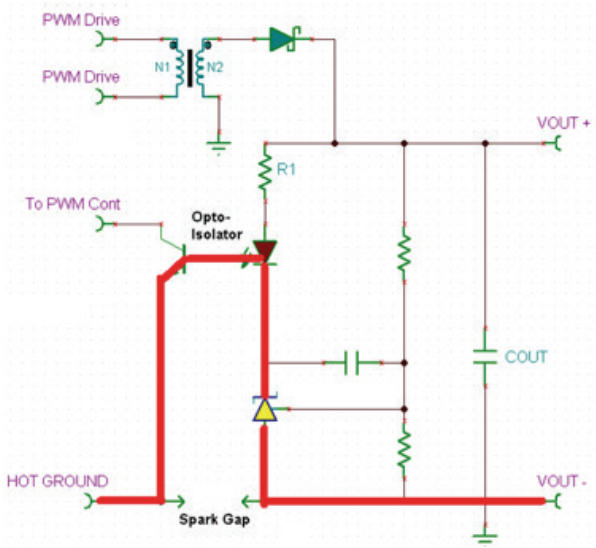

Figure 2: The red line is the ESD path, with an electric arc across optical-isolator leads.

Moving the resistor, R1, from the anode of the optical isolator to the cathode side will protect the shunt during an isolation breach. Moving the resistor has no impact on performance or stability. It works because the optical-isolator breach will now prefer the output capacitor as a path to ground. The red line in **Figure 3** shows the new ESD path.

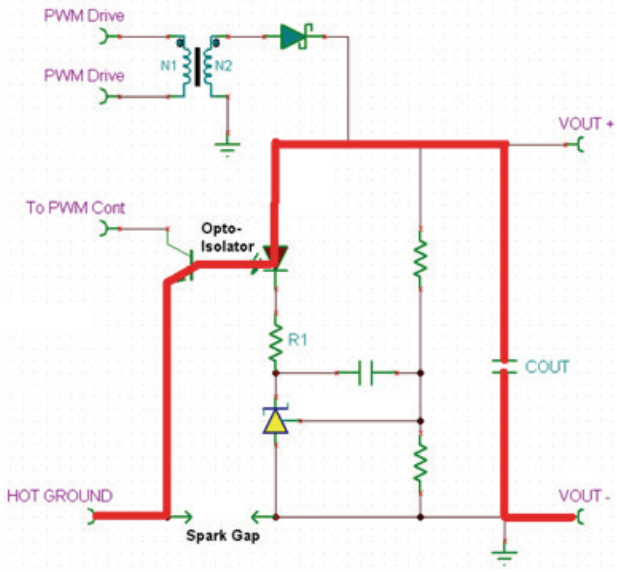

Figure 3: The red line shows the new ESD path, with an electric arc across optical-isolator leads.

Now that the shunt regulator is no longer in the primary ESD path, it will survive. The capacitor takes the current, but it will tolerate much higher ESD energies than the shunt regulator can survive. Depending on which pins on the optical isolator pass the electric arc, there will still be significant danger to the PWM controller and some danger to the optical isolator itself.

Another danger can occur in space-constrained designs. If you were to place the shunt or its node traces too close to the isolated (hot ground) traces, there's a chance that an electric arc can occur directly to the shunt or to its circuit traces, as shown in **Figure 4**. In this case, moving resistor R1 will not protect the shunt. The solution here is to rotate the shunt so that the anode (ground) is the closest node to the traces on the other side of the isolation gap.

Figure 4: Effects of electric arcs (red line) on shunt references.

For additional protection, you can add an intentional spark gap to cause an ESD event to arc from the ground of one side to the ground of the other side. The spark gap will need a substantially lower breakdown to ensure that the arc does not choose an alternate place to cross. It is clear from Figure 5 that an arc across a spark gap will not stress the components.

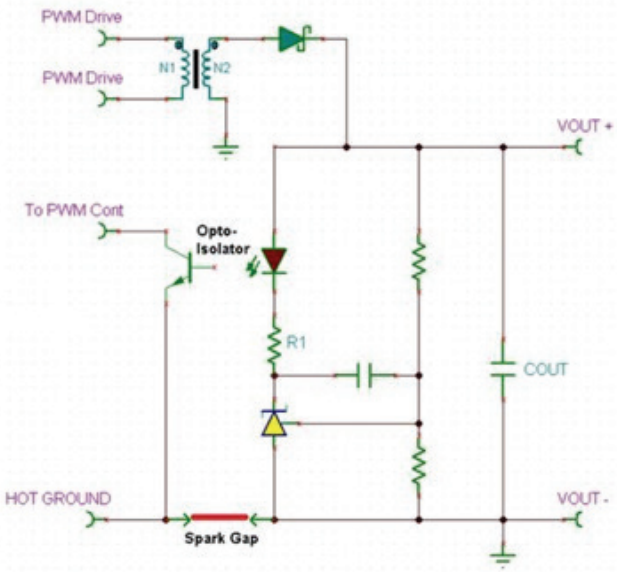

Figure 5: Spark gap protection components; the red line represents an electric arc.

As you can see, simple changes can greatly improve ESD performance – and as promised, these changes are free. You can apply the feedback safety circuit discussed here to all common-anode adjustable-shunt regulators, including TI's ATL431/2, TL431/2 and TLVH431.

Resources

- Texas Instruments Voltage Reference Landing page: **www.ti.com/vref**
- Shunt voltage reference external resistor quick start calculator: **www.ti.com/tool/shunt_voltage_reference_resistor_calculator**
- Technical articles on voltage references: **https://e2e.ti.com/blogs/tags/vref**
- How to select a voltage reference topology article: **http://embedded-computing.com/articles/shunt-versus-series-how-to-select-a-voltage-reference-topology/#**

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