Design review of a 2-kW parallelable power-supply module

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From defining specifications to selecting components, learn how to design a power system with a modular power-factor-corrected microcontroller.

Modular-built power supplies could bring additional value to applications in the industrial space though an increased number of possible solutions, flexibility and performance, as well as lower cost. For example, you could increase the output power of the converter by paralleling two or more power-supply unit (PSU) outputs on the secondary side, or by moving from a single alternating current (AC)-input source to a three-phase AC input source without changing any component in the system. If you parallel PSUs on the secondary side, the master PSU will communicate via a digital share bus to the slaves. The master defines what output voltage and current level should be delivered by all paralleled modules and directs the slaves to supply a part of this current for automatic current sharing.

You could also modify the software of the modular power-factor-corrected (PFC) microcontroller-controlled battery charger platform to address the needs of applications that may require a different charging profile, a constant voltage, a constant current or a constant output power on the secondary side, as well as keeping the input AC current constant (derating with the input-current capability). This opens up the use of this approach further, such as in telecommunications applications, by paralleling several rectifiers and adding redundancy for reliability purposes.

Based on achievable power levels, in this paper I describe the selection of the main power stages, including a continuous conduction mode (CCM) power-factor-correction circuit. Also included is a peak current mode-controlled isolated DC/DC resonant phase-shifted full-bridge converter with synchronous rectification.

Introduction

A power supply can be a simple switcher like a buck converter, or a complex system made up of several stages to create a PSU (with input inrush protection, an electromagnetic interference [EMI] filter, AC/DC, DC/DC, reverse-polarity protections, and so on). Connecting several of these PSUs in parallel forms a system capable of providing modular power during periods of high-current demand. For instance, in telecommunications applications, a percentage of nominal power offers redundancy in case one module fails (increasing reliability) or provides more current to charge the battery quicker.

Other applications requiring modularity, scalable solutions or increasing power demand, include battery chargers for forklifts and tow tractors. In these cases, you can translate modularity into redundancy with proper design (**Figure 1**).

Figure 1. *A modular telecommunications power system.*

You can implement modularity in several different ways, choosing either:

1. A fully functional module that "stands alone" and supplies the voltage/current according to its own characteristics. You can connect several of these modules in parallel through the backplane, which collects currents and information from each one.
2. A single enclosure containing modular boards that collect current on connectors and therefore increase the nominal output power. A single control board sets signals and parameters for the whole module. You can connect several of these modules in parallel.
3. A single system containing single boards hosting different patterns of passive and active components, and/or paralleling active components to increase the output power. Here the flexibility is only in the factory, during PSU assembly and validation.

This paper focuses on the first option and explains how to properly design such a module.

Main characteristics

Customer specifications drove the module design described in this paper, which is a battery-charging application in the industrial segment (for example, a charging system for forklifts). Even though the power supply must work in the entire universal input-voltage range, it is not necessary to deliver full power at low line; the customer accepted a root mean square (RMS) input-current limit of 10 A. Thus, I could select smaller and lower-cost components for the boost PFC converter. **Table 1** shows a list of the main parameters of the power module.

Design specification	Value
Nominal input AC voltage	230 VAC
Working AC voltage	90 VAC … 265 VAC
Output voltage	20V … 32V at 62.5 A
Harmonic limits	EN61000-3-2 Class A
Output power	2 kW at 230 VAC
Input current limit	10 A
Minimum plug-to-plug efficiency	90% (design to cost)
User interface	Liquid crystal display (LCD), four pushbuttons
Modularity	Parallel with master/slave architecture
Parallel function	Analog or digital, controller area network (CAN) communications bus
Settable parameters	Output voltage and current levels, input AC undervoltage lockout (UVLO) and overvoltage protection (OVP), reverse output-voltage protection, output short, overtemperature, master/slave configuration (up to one master and nine slaves)

Table 1. *Specifications of a power module.*

Table 2 compares three existing power modules from different vendors with the Texas Instruments (TI) module prototype.

Model	Power	VIN range	Efficiency	Power density	Cooling	Human interface
A	720 W at T_{AMB} <40ºC	Universal and extended	>85%	106 W/cm^3	Temperature-controlled fan	Status light-emitting diode (LED)
B	1 kW	High line (184 VAC ... 275 VAC)	96% peak	78.7 W/cm^3	Natural convection	Charging status indication (LED)
C	3 kW	High line (184 VAC ... 275 VAC)	94% peak	116 W/cm^3	Forced convection	Charging status indication (LED)
TI prototype	2 kW at T_{AMB} <80ºC	Universal with derating	>91% 93.5% peak	86.8 W/cm^3	Variable-speed fan	LCD pushbuttons

Table 2. *Three power modules/chargers from different vendors available today.*

Even though the TI module is not a commercial one and is only a prototype, the power density is comparable to the modules listed in **Table 2**. Module A has a derating characteristic of T_{AMB} >40ºC, with the higher-power (1 kW and 3 kW) modules working only in the high line input-voltage range. The TI prototype is designed to work in the entire universal mains range by derating the input current below 10 A.

I added a small LCD and four pushbuttons in order to set the main parameters and see them on a display: this way the input and output characteristics, alarms and warnings were under control. At the same time, the module can work in stand-alone mode, as a master or even as a slave. I describe this functionality in more detail later.

Figure 2 is a block diagram of the entire module.

The module's main components are:

- The EMI filter is a natural interface to the mains. It filters differential and common-mode ripple voltage present at the PFC converter. It also protects the whole module against surge and provides inrush current reduction.
- The PFC power stage which rectifies the input AC voltage and simulates a resistive load. It absorbs sinusoidal input current and maximizes the "power factor." See Equation 1:

$$PF = \frac{cos\varphi}{\sqrt{1+THDi^2}} = \frac{I_1(RMS)}{I(RMS)} \quad (1)$$

The displacement factor (cos**φ**) at nominal power is ~1, so the main contribution to power factor is total harmonic distortion (THD).

- The DC/DC converter processes and isolates the output of the PFC boost converter (400 V), supplying 0… 32 V at 62.5 A. The phase-shifted topology provides the highest efficiency possible for a low-cost DC/DC converter, while at the same time improving EMI thanks to zero voltage switching (ZVS). Due to the high output current, synchronous rectification is necessary to reduce the thermal interface and enhance efficiency. A single controller, the UCC28950, drives all field-effect transistors (FETs) on the primary and secondary side. This controller processes the information coming from the output voltage and current, closes the loop (taking into account the references provided by the microcontroller), and generates driving pulses for all six FETs.

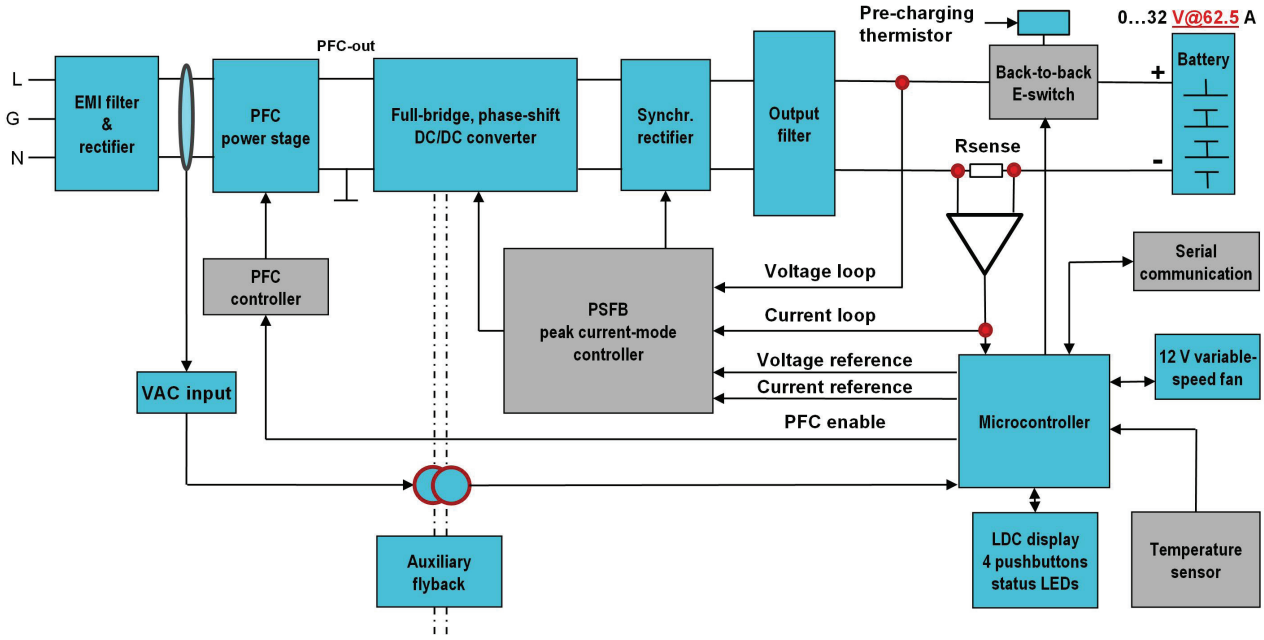


Figure 2. *This power supply module contains the main power stages and control functions.*

- Several back-to-back FETs are connected in series to the output filter in order to disconnect the load, taking into account both directions: inrush during load connection and reverse-voltage protection.
- The microcontroller is the heart of the system, generating output voltage and current references as well as reading temperatures, controlling the fan, and interfacing with the LCD and pushbuttons.
- The serial communication allows digital data exchange between modules through a CAN hardware interface. The software protocol is proprietary, and developed for minimum data traffic and maximum speed. Several modules, connected in a slave configuration, exchange commands and acquire warnings to and from the master, forming a whole system able to behave as a single power supply.
- The auxiliary power supply provides bias power both to the primary and secondary side.
- The VAC input function reads input RMS voltage with ±5 percent precision. This information is necessary in order to perform UVLO and OVP and allows the microcontroller to calculate the maximum input current, limiting its value to 10 A according to Equation 2:

$$I_{OUT(max)} = \frac{\eta . V_{IN} . 10A}{V_{OUT}} \quad (2)$$

- I_{OUT_MAX} is the maximum set point of output current, which also depends on V_{OUT}. Since this limitation is used only to avoid overheating, I considered a fixed value of $\eta = 0.92$.

PFC CCM boost converter: interleaved or single phase?

Interleaving clearly benefits input and output ripple-current cancellation, as shown in **Figure 3**. Further benefits come from a better thermal interface (heat spreading thanks to doubling the active components). On the output, the 100-Hz/120-Hz ripple is inherent to PFC converters and does not change substantially by interleaving.

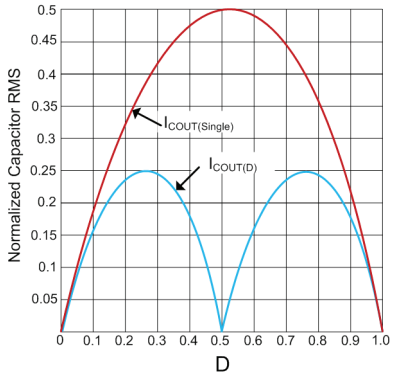


Figure 3. Ripple reduction due to interleaving.

Other advantages of interleaving include easy scalability to higher powers and a low profile. Conversely, a single-phase PFC converter (**Figure 4**) takes advantage of the simplicity and employs a low-cost controller. The PFC converter does not have to balance two-phase currents and you can employ a single current-sense resistor instead of two current-sense transformers.

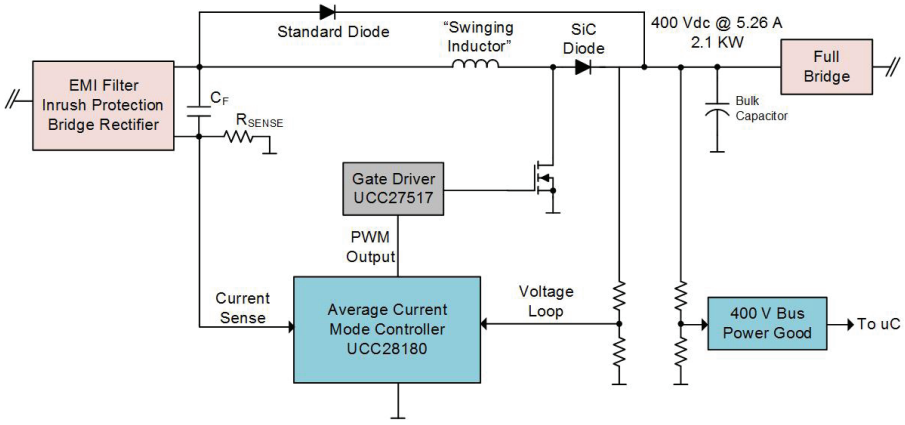


Figure 4. PFC boost converter block diagram.

DC/DC topology selection

The selection of a second-stage topology depends on how strong the stresses on each active component are, and you should leverage the magnetics as much as possible. I evaluated three main topologies for this paper: 1) resonant LLC half bridge (inductor-inductor-capacitor [LLC]), 2) hard switched half-bridge and 3) phase-shifted, full-bridge.

1. Resonant LLC

Figure 5 shows a simplified schematic of a resonant LLC converter. It is out of the scope of this paper to discuss these topologies in detail. **See references [1, 2 and 3]** for more information. In this case, the main characteristic of LLC converters is that they run at a 50 percent (minus dead time) duty cycle for switches Qa and Qb.

Varying the switching frequency below or above the resonant frequency regulates the output voltage, given by Equations 3-6 (knowing that L_M = T1 magnetizing inductance):

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L_1 \cdot (C_a + C_b)}} \quad (3)$$

$$M = \frac{V_{OUT}}{V_{IN}/2} \quad (4)$$

$$M = \frac{V_{OUT}}{V_{IN}/2} \quad (5)$$

$$L_n = \frac{L_M}{L_R} \quad (6)$$

Most waveforms at this resonance are sinusoidal (except the magnetizing current, which is triangular) – even the ripple voltage (considering the output capacitor's main impedance is equivalent series resistance [ESR]). **Figure 6** (right) shows that primary- and secondary-side currents are sinusoidal, allowing main FETs, Qa and Qb, as well as synchronous FETs, Qe and Qf, to work in a "zero current switching" condition. This condition leads to high efficiency (no switching losses) and reduced EMI generation.

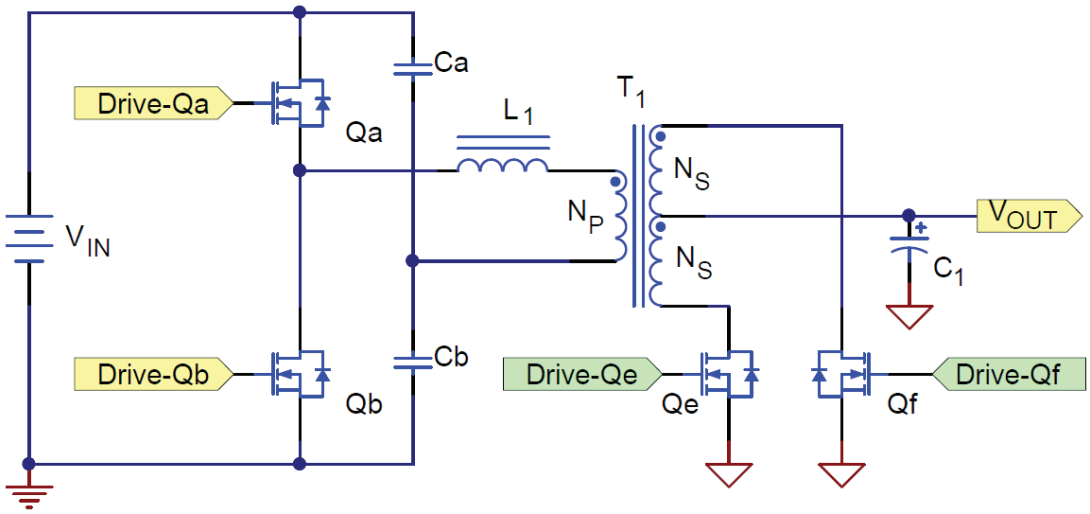


Figure 5. A resonant LLC converter.

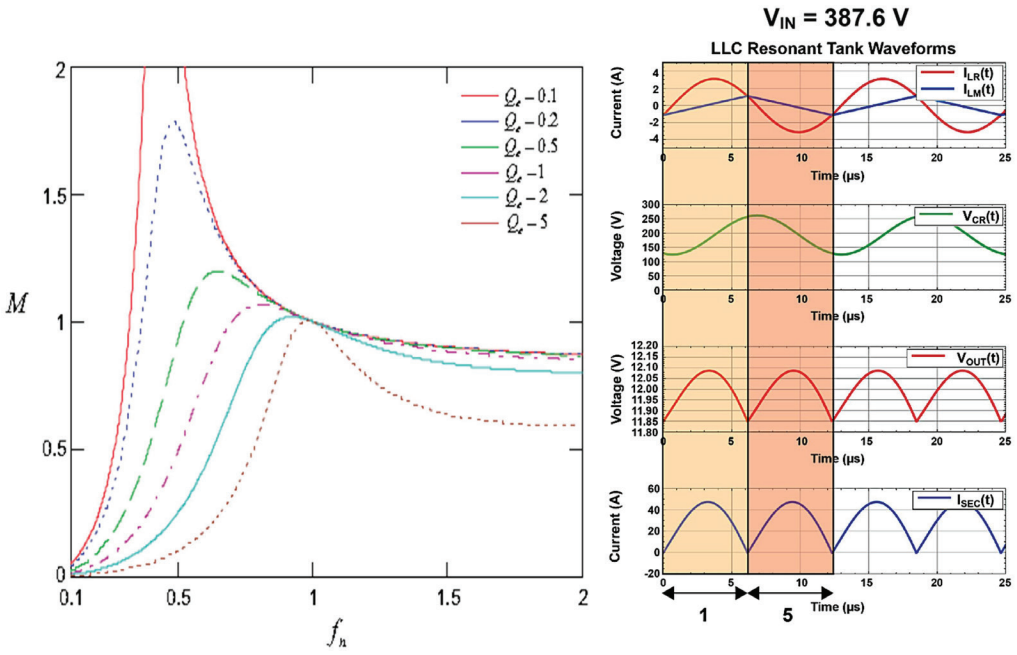


Figure 6. Gain curves and typical waveforms for the LLC.

To reduce the output voltage significantly, as shown in the graph of M(f) (**Figure 6 left**) the frequency needs to shift infinitely higher to get very low gain. An infinite shifting frequency increases switching losses (the converter now works far away from resonance and, therefore, the waveforms are no longer sinusoidal) and the parasitics will have much more of an impact in the calculation of copper and core losses. If the converter runs at a very low output voltage (heavy overload or short circuit), the controller reaches its maximum switching frequency and can no longer regulate the output (**Figure 6 left**).

2. Hard-switched, half-bridge

The main difference between a hard-switching, half-bridge topology and an LLC is that the half-bridge works in pulse-width modulation (PWM) mode by modulating the duty cycle instead of the frequency. **Figure 7** is a simplified schematic of a hard-switching, half-bridge topology.

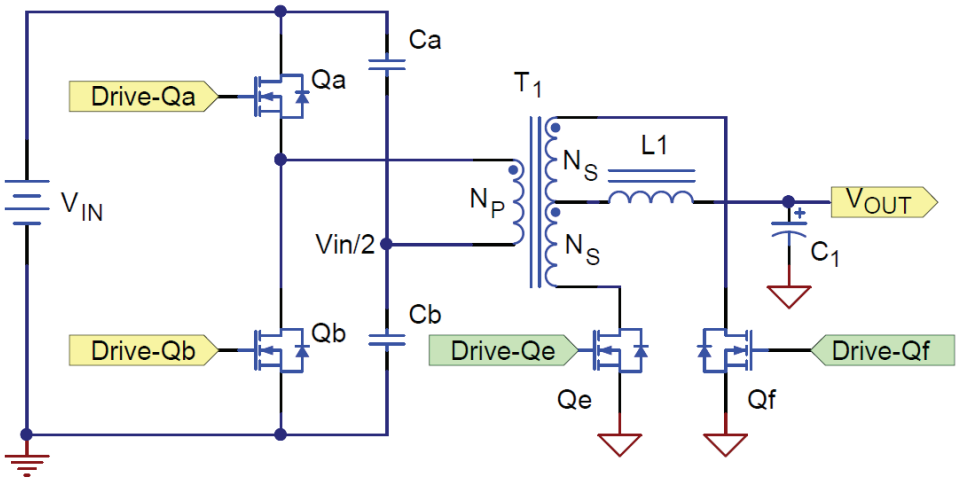


Figure 7. Simplified schematic of a hard-switched half bridge.

Equation 7 expresses the control law between V_{IN} and V_{OUT} as:

$$\frac{V_{OUT}}{V_{IN}} = D \cdot \frac{N_S}{N_P},\ D=0 \ldots 50\% \quad (7)$$

Just to compare with the next topology (phase-shifted, full-bridge), I calculated the stress for a 2-kW half-bridge converter with an estimated efficiency of 94 percent.

The switch current (IQa, IQb) in **Figure 8** has these values:

$I_{PEAK(min)}$ = 11.4 A
$I_{PEAK(max)}$ = 13 A
I_{INPUT} = 5.49 A = average input current

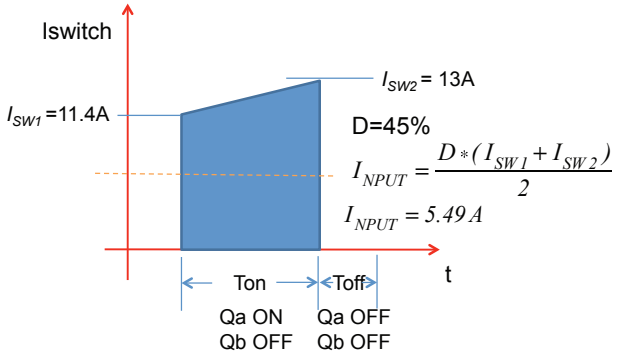


Figure 8. Current stress in a 2-kW hard-switched, half-bridge.

The switch current in the phase-shifted, full-bridge topology results in the waveform shown in **Figure 9**.

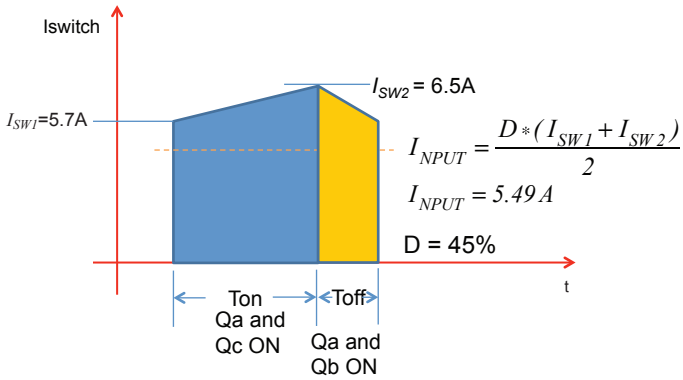


Figure 9. Current stress in a 2-kW phase-shifted full bridge.

The I_{INPUT} is identical – 5.49 A – but the peak current of the phase-shifted, full-bridge is exactly half of the hard-switched, half-bridge topology.

3. Phase-shifted, full-bridge

Figure 10 is a simplified schematic for a phase-shifted, full-bridge topology.

Still comparing the phase-shifted, full-bridge to the hard-switched, half-bridge, the main difference concerning switch current is the yellow shaded area shown in **Figure 9**. In the hard-switched topology, all FETs are off during the off-time, while in the phase-shifted, full-bridge mode, two FETs (Qa and Qc, or Qb and Qd) are on. During this short circuit, primary current is flowing in both FETs, increasing RMS current compared to hard switching.

Nevertheless, the phase-shifted, full-bridge topology

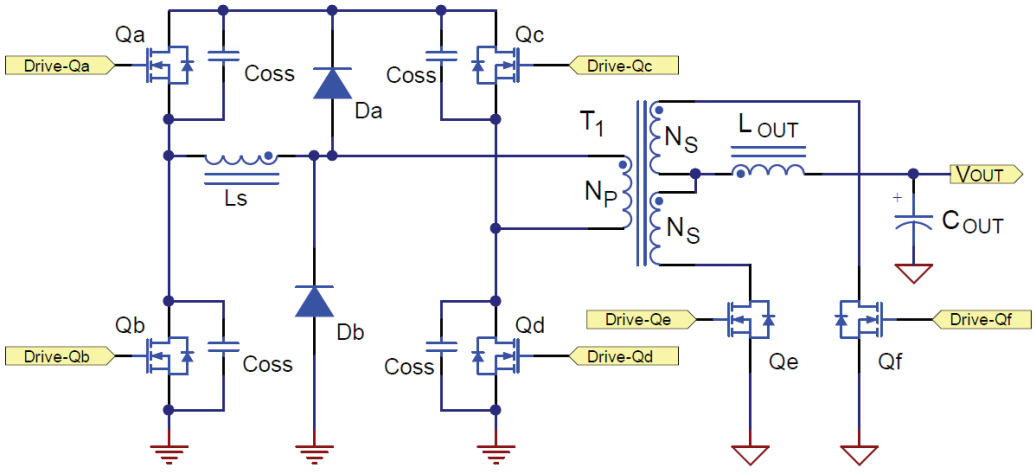


Figure 10. Simplified schematic for a phase-shifted, full-bridge topology.

Modulation Type	Good Standby Power	Low Cost	Opto-less	Overload Protection	Good Eff.	Good Vout Regulation	Good Transient Response	EMI
Quasi Resonant w/PSR	√	√	√	√	√	~	~	√
Quasi Resonant w/ Optocoupler & Depl.Mode FET	√	~	X	√	√	√	√	√
Constant Switching Frequency + Optocoupler	~	~	X	X	~	√	√	~
√ = Yes, X = No, ~ = average performance				Chose Quasi Resonant w/Optocoupler for best regulation, efficiency and stand-by performance				

Table 3. *Comparison of modulation schemes for an auxiliary power supply.*

has more pros than cons, with the main advantage being ZVS and a huge improvement regarding switching losses and EMI. Normally, you can achieve ZVS by leveraging the leakage inductance of T1. The amount of this inductance will define the minimum load where you still have ZVS, according to Equation 8:

$$L_{LK} = \frac{2 \cdot Coss \cdot (V_{IN}(nom))^2}{\left[I_{OUT}(min) \cdot \left(I_{PP} - \frac{dILout}{\frac{N_S}{N_P}}\right)\right]^2} \quad (8)$$

If you need ZVS at a lighter load (for example in telecommunications power, thanks to redundancies), you could add an external "shim" inductance (L_S). Achieving ZVS at a lighter load increases the efficiency but some duty cycle is lost; therefore, full-load losses increase. Da and Db clamp the voltage on the primary side of the transformer and allow a spike reduction on the secondary side as well. This way, you can achieve lower voltage ratings for Qe and Qf.

Auxiliary power-supply alternatives

The auxiliary power supply usually requires the least design effort on high-power modules, but since it supplies power to the whole converter, it deserves some extra effort! Select one of the modulation schemes shown in **Table 3** corresponding to the performance you need.

Quasi-resonant flyback converters with primary-side regulation (PSR) have excellent performance in most aspects, sacrificing some output-voltage regulation accuracy, but gaining in simplicity and cost. Since cost is not the main parameter here (and the impact is small on the module's total cost anyway), I selected a quasi-resonant topology plus an optocoupler. That way I could still obtain the best output-voltage regulation and take advantage of quasi-resonant mode.

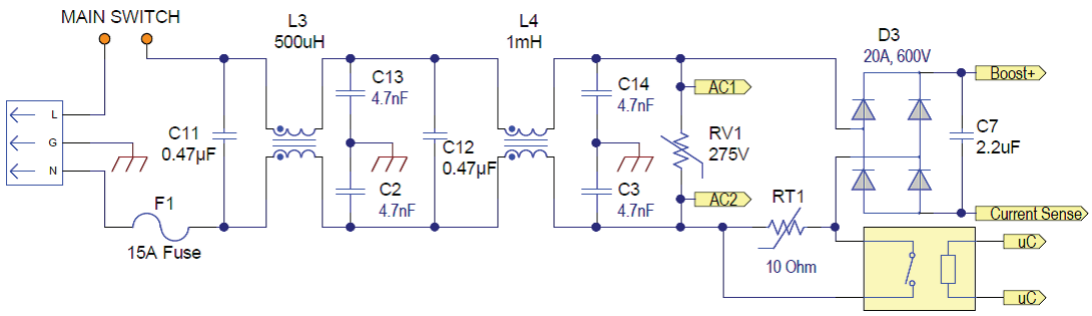


Figure 11. *Schematic of an EMI filter.*

Block designs

EMI filter

Figure 11 shows a schematic of the EMI filter.

Because the design specification limited the input AC current to 10-A RMS, I selected all components to support this maximum current. Two chokes (L3 and L4) reduce common-mode noise as well as class-Y capacitors C2, C3, C13 and C14; their values are heavily dependent on the instantaneous voltage rate of change of switch nodes and the associated capacitance to ground, which are difficult to predict. This paper covers only differential-mode noise, defined by C7, L4 and C12/C11.

L3 provides some differential-mode filtering but should take care of the high-frequency range; if the converter fulfills EMI limits with L4 alone, it will also fulfill EMI limits with L3.

Arbitrarily I selected L4 = 1 mH. L3 must have the same current capability as L4 but a different resonance frequency (one-half to one-fourth of L4) to avoid peaking and a higher-frequency range.

RT1 must support charging of the PFC electrolytic capacitors (C_{OUT}(pfc)) and be capable of withstanding the equivalent I^2T, which is a function of C_{OUT}(pfc). **Table 4** shows each RT1 possible value. For example, the NTC (negative temperature coefficient) can support a maximum of 100 µF at 230 V_{AC} and 400 µF at 110 V_{AC}.

R_{25} Ω	I_{max} (0...65 °C) A	C_{test} [1] 230 V AC µF	C_{test} [1] 110 V AC µF	R_{min} (@ I_{max}, 25 °C) Ω
4.7	3.0	100	400	0.154
8	2.2	100	400	0.279
10	2.0	100	400	0.340
15	1.8	100	400	0.430
16	1.7	100	400	0.473
20	1.6	100	400	0.528
33	1.3	100	400	0.832

Table 4. *Negative temperature coefficient parameters.*

The values of R_{MIN} and I_{MAX} are not important here because a microcontroller-driven relay will short the NTC resistor.

EMI filter, differential mode

Equation 9 gives a result of C7 = 1.54 µF by selecting 30 percent inductor ripple current (I_{PP}) and 1 percent ripple voltage on C7. Choose the standard value closest to 2.2 µF. Since the converter works in CCM, the highest ripple current is a triangle at a 50 percent duty cycle and is Ir = 4.58 Apk-pk. The Fourier analysis on a 1-Vpk square wave and triangular waveform shows that in both cases, you can use the third harmonic to select the filter; see **Figure 12**.

$$C7 = \frac{8}{\pi^2} \frac{Ir}{2 \cdot \pi \cdot Fsw \cdot Vr} \quad (9)$$

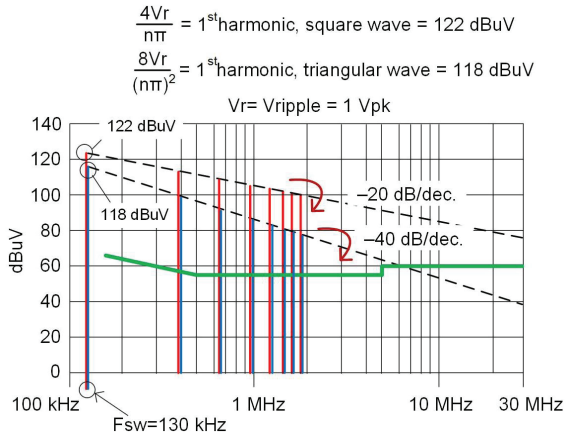


Figure 12. *Fourier analysis of square and triangle waveforms.*

Next, before I selected a switching frequency just below 150 kHz, which is the initial limit of Comité International Spécial des Perturbations Radioélectriques (CISPR) 22 quasi-peak, which starts at 66 dB and rolls down at –20 dB/decade. (The square-wave spectrum rolls at –20 dB/decade, while the triangular waveform rolls at –40 dB/decade.) Considering only the third harmonic of the triangular waveform, I filtered the ripple so that this harmonic was below the limit. As a result, all higher harmonics were below the green line.

Equation 10 expresses the equivalent third-harmonic ripple current coming from a peak-to-peak current equal to 4.58 A as:

$$I_{3H} = \frac{8 \cdot (\frac{Ipp}{2})}{9 \cdot \pi^2} = 0.206\ A \quad (10)$$

This ripple current flowing through C7 yields Equation 11:

$$V_{C7} = I_{3H} \cdot \frac{1}{2 \cdot \pi \cdot (3 \cdot F_{SW}) \cdot C7} = 38\ mV \quad (11)$$

Figure 13 shows the line impedance stabilization network (LISN) and equivalent circuit.

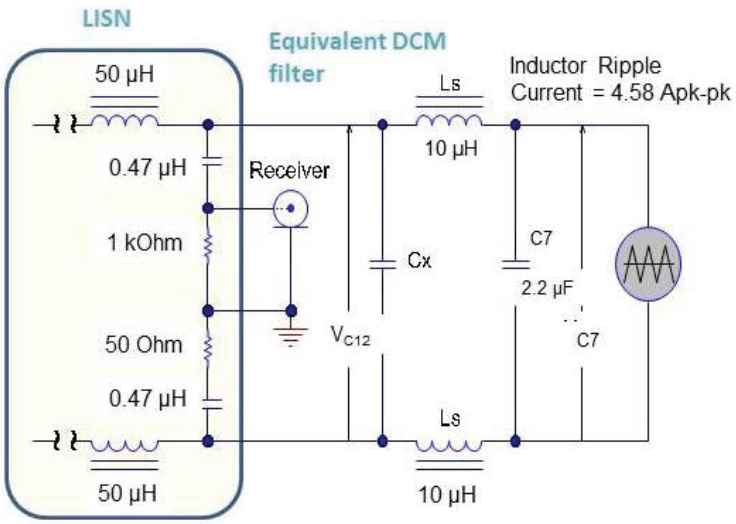


Figure 13. *Schematic of filter, including LISN.*

After the filter, which comprises two Ls and one Cx, I obtained the voltage (Vc12) and divided by two since the LISN is a balanced system. Equation 12 calculates the necessary attenuation:

$$Att = V_{C7}(dB) - Limit(QP) + Margin = 36.6\ dB \quad (12)$$

where margin = 3 dB and Limit(QP) = the quasi-peak CISPR22 limit at 390 kHz = 58 dBµV.

Ls and Cx define the corner frequency.

Fc = 47.4 kHz, which yields:

$$F_C = 10^{\frac{-Att}{40}} \cdot F_{3H} \quad (13)$$

$$C_X = \frac{1}{8 \cdot \pi^2 \cdot L_S \cdot (F_C)^2} = 563\ nF \quad (14)$$

Paralleling C11 and C12 defines CX, which is calculated by Equation 14; therefore, I selected C11 = C12 = 470 nF for further margin.

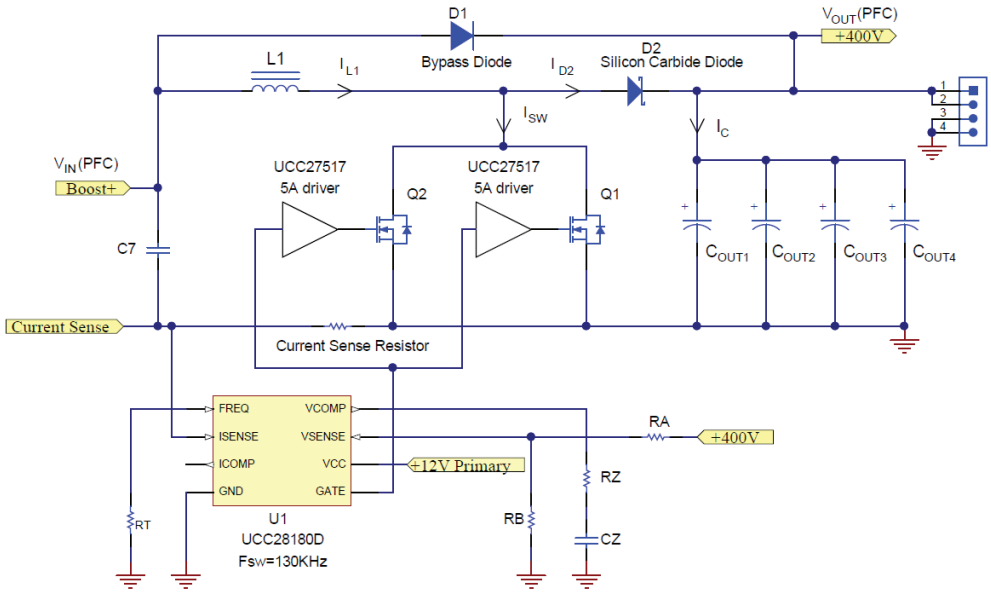


Figure 14. Schematic of PFC boost converter

PFC boost converter

Figure 14 is a simplified schematic of PFC boost converter.

Here, you can set important design constraints:

- A silicon carbide diode (D2) because of hard switching and CCM.
- A bypass diode (D1) to avoid high surge currents through the silicon carbide (SiC) diode.
- Two FETs instead of one to spread the heat and enable the use of cheaper components.
- Four output capacitors to keep 100-Hz/120-Hz ripple and transient response under control.

I selected the UCC28180 controller because of its simplicity. It improves performance compared to its predecessor controllers by reducing the current-sense working voltage level, thus reducing losses. I removed the resistor divider connected to "Boost+" and used the free pin to set the switching frequency.

PFC inductor value

As introduced in the filter design, I recommend choosing an inductor with 30 percent ripple current at a worst-case 50 percent duty cycle (V_{IN}(pfc) = V_{OUT}(pfc)/2) that supports 16 A (peak) and 10 A (RMS). Equation 15 is the resulting calculation:

$$L1 = \frac{V_{OUT}(pfc) \cdot (1 - D) \cdot D}{\Delta I \cdot F_{SW}} = 168\ \mu H \qquad (15)$$

Drawing the inductor current at full load, CCM mode gives you **Figure 15**.

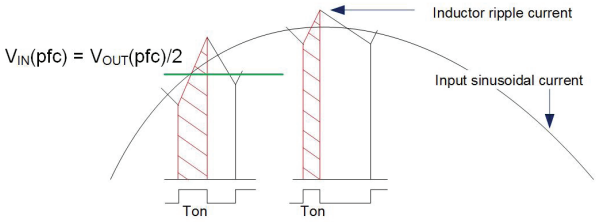


Figure 15. PFC inductor current.

The current flows through the FETs (red shaded area), while during T_{OFF} the diode is conducting. Defining K1, K2 and K3 in Equations 16-18, Equations 19-21 are the RMS currents in the PFC FET (I_{SW}), PFC diode (ID2) and PFC output capacitor (I_C):

$$K_1 = \frac{P_{OUT}(pfc)}{\eta \cdot V_{IN}(pfc,min)} \qquad (16)$$

$$K_2 = \frac{8 \cdot \sqrt{2}}{3 \cdot \pi} \qquad (17)$$

$$K_3 = \frac{V_{IN}(pfc,min)}{V_{OUT}(pfc)} \qquad (18)$$

$$I_{SW} = K_1 \cdot \sqrt{1 - K_2 \cdot K_3} = 6.9\ A \quad (19)$$

$$I_{D2} = K_1 \cdot \sqrt{K_2 \cdot K_3} = 8.3\ A \quad (20)$$

$$I_C = \frac{P_{OUT}(pfc)}{V_{OUT}(pfc)} \cdot \sqrt{\frac{K_2}{K_3} - 1} = 6.1\ A \quad (21)$$

The capacitor current includes the high-frequency content plus twice the line-frequency ripple current. I calculated these values at V_{IN}(pfc,min) = 195 VAC and η = 96 percent.

Component stress analysis

Keeping in mind the currents calculated above, I then selected each component according to these best practices:

- Employing an iron powder toroidal core, leveraging the capability of this material to show high inductance at a low magnetizing field and a progressive reduction in effective magnetic permeability (μe) value, which reduces the inductance but never saturates. These are called "swinging" inductors. You still have useful inductance value at light load (thus reducing THD), but acceptable ripple at full load. I considered the 168-μH value at full load and minimum high-line voltage.
- Allowing 0.2 percent conduction losses on the equivalent switch (with equivalent RDSON(EQ)) and 0.3 percent switching losses. This results in Equation 22:

$$RDS_{ON}(EQ) = \frac{2}{1000}\frac{P_{OUT}(pfc)}{\eta \cdot (I_{SW})^2} = 0.087\ \Omega \longrightarrow$$

$$P_{COND}(EQ) = \frac{RDS_{ON}(EQ)}{2}(I_{SW})^2 = 3.02\ W \quad (22)$$

- I selected two 650-V-rated FETs with RDS_{ON} = 125 mΩ ≤· 2·RDS_{ON}(EQ). This FET has rise and fall times of 15 ns and 8 ns and Coss equal to 53 pF.
- Equations 23 and 24 calculate switching (P_{SW}) and Coss (P_{COSS}) losses:

$$P_{SW}(EQ) = \frac{1}{2} \cdot V_{OUT}(pfc) \cdot I_{SW} \cdot (T_R + T_F) \cdot F_{SW} = 4.16\ W \quad (23)$$

$$P_{COSS}(EQ) = \frac{1}{2} \cdot (2 \cdot COSS) \cdot (V_{OUT}(pfc))^2 \cdot F_{SW} = 1.1\ W \quad (24)$$

- Equation 25 calculates the total losses for the equivalent switch as:

$$P(EQ) = P_{COND}(EQ) + P_{COSS}(EQ) + P_{SW}(EQ) = 8.28\ W \quad (25)$$

- Since two FETs will share the total FET losses, this results in 4.14 W per FET.
- Selecting a SiC diode to withstand peak and RMS current (ID2 = 8.3 ARMS). From the diode's characteristic, shown in **Figure 16**, the threshold voltage (VF) is around 1 V and the differential impedance (Zd) is around 0.05 Ω at 25ºC.

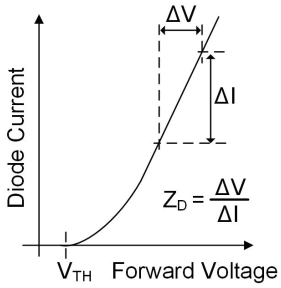


Figure 16. *SiC diode characteristics.*

Equation 26 gives the total diode loss as:

$$P_{D2} = V_{TH} \cdot I_{OUT}(pfc) + Z_D \cdot (I_{D2})^2 = 8.46\ W \quad (26)$$

Output bulk capacitor

The bulk capacitor present on the output of PFC converter:

- Holds the voltage in case of mains interruption (holdup time T_{HOLD}). T_{HOLD} is the most demanding parameter; it should be as small as possible and compatible with the application. For example, in a general power supply, T_{HOLD} is typically 10-20 ms, while in battery charging or telecommunications segments (like in the TI module prototype), it is 10 ms.

- Keeps the PFC V_{OUT} quite constant and reduces ripple. This enables the optimization of the next stage to work with the highest duty cycle, thus reducing peak currents. In this case, the difference V_{OUT}(pfc,nom) – V_{DROP} = V_{OUT}(pfc,min) plays a big role (where V_{DROP} is the drop on V_{OUT}(pfc) during mains interruption). Setting V_{DROP} = 50 V, V_{OUT}(pfc,min) = 350 V. Equation 27 calculates C_{OUT}(pfc):

$$C_{OUT}(pfc) = \frac{2 \cdot P_{OUT}(pfc) \cdot T_{HOLD}}{(V_{OUT}(pfc,nom))^2 - (V_{OUT}(pfc,nom) - V_{DROP})^2} = 1.08 \cdot 10^3\ \mu F \quad (27)$$

- Withstands ripple currents at both F_{SW} and at twice the line frequency. With four paralleled capacitors, each capacitor should support $I_{RMS} \geq 1.53\ A_{RMS}$ (6.11 A(RMS)/4).
- The controller can also limit the amount of allowable ripple voltage. In fact, if the peak-to-peak ripple is too high, the loop-response accelerator (enhanced dynamic response [EDR]) present in the UCC28180 controller will modify the loop gain and distort the input current.

  Figure 17 shows two thresholds set to a V_{REF} ±5 percent (4.75 V and 5.25 V). If V_{SENSE} goes beyond those limits, the EDR function will accelerate the gain loop in order to bring the output voltage back inside ±5 percent of the nominal voltage.

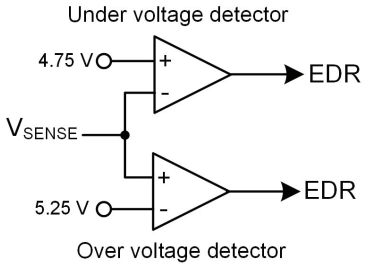


Figure 17. *EDR can limit the maximum allowable ripple.*

Using Equaiton 28, and accounting for all constraints, I got four capacitors, each with a value of 330 µF in parallel.

$$C_{OUT}(pfc) = 1080\ \mu F + 20\ percent\ (typical\ electrolytic\ capacitance\ tolerance) = \sim 1300\ \mu F \quad (28)$$

The peak-to-peak ripple voltage at full load and F_{LINE} = 47 Hz results in Equation 29, which is less than 2 percent.

$$V_{RIPPLE}(pfc) = \frac{I_{OUT}(pfc)}{2 \cdot \pi \cdot 2 \cdot F_{LINE} \cdot C_{OUT}(pfc)} = 7.9\ V \quad (29)$$

Auxiliary power supply

The controller employed for the auxiliary power supply is the LM5023, which works in quasi-resonant mode and performs valley switching at medium and full load. The main advantages of such modulation are reduced EMI signatures and lower switching losses. This controller drives a depletion-mode FET, which allows fast startup and zero standby losses. Thanks to current-mode modulation, you only need type II compensation (two poles and one zero).

Figure 18 is a schematic of the auxiliary power supply. It is important to analyze the total auxiliary power that the module needs. **Table 5** shows the main current consumption for each block or stage.

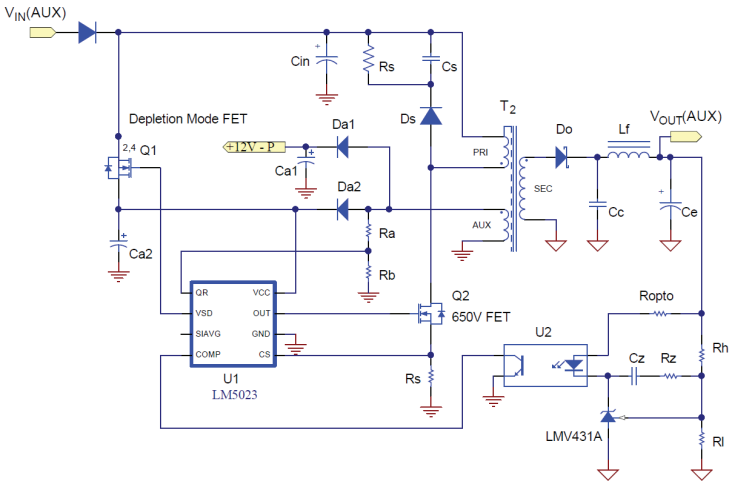


Figure 18. *Schematic of auxiliary power supply.*

Load	Type	Calculation	Power requirements
PFC boost converter	Relay	12V·330 mA	396 mW
	UCC28180	12V·8.75 mA	105 mW
Phase-shifted full bridge DC/DC converter	Gate drive	2·2V·(3 mA+40 nC·130 kHz)	197 mW
	UCC28950	12·10 mA	120 mW
	Gate drive full-bridge	12V·(2·3 mA+4·70 nC·200 kHz)	744 mW
	Gate drive synchronous rectification	12V·(2·3 mA+4·75 nC·100 kHz)	432 mW
Various	Analog + digital	Estimated 1 W	1 W
	Fan	Nominal RPM = 2.28 W	Worst case 4.92 W
	Display backlight	600 mW	600 mW
Total	Total power	Sum of all power consumptions	9.5 W

Table 5. *Summary of auxiliary power requirements.*

Regarding the power consumption of the phase-shifted, full-bridge gate driver, consider that a bipolar PWM drives the FETs, with peak voltage ±12 V. See the waveform in **Figure 19**.

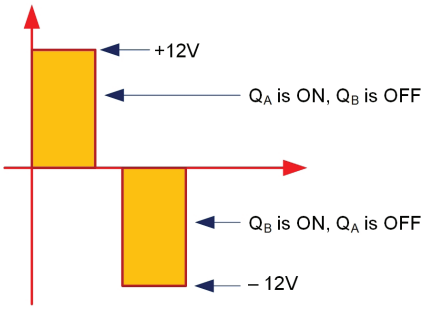


Figure 19. *Bipolar gate drive used for the phase-shifted full bridge.*

This means that the driver charges (and discharges) the gate two times per cycle, losing power in the gate driver.

Knowing the amount of auxiliary power needed, 10 W, you can properly design the auxiliary power supply. First define the minimum input voltage. When the auxiliary supply starts, the module does not deliver any power, so the minimum input voltage is V_{IN}(aux,min)*1.41 = 120 V. The maximum input voltage will be V_{PFC}(aux,max) = 400 V + overshoot ~ 420 V. In these conditions the fan is not rotating, and the worst-case power consumption will be ~8 W.

Choose the transformer ratio so that $V_{REFLECTED}$ ≤ V_{IN}(pfc,peak) (reduced by 20 percent), resulting in $V_{REFLECTED}$ = 100 V. Knowing that you need 12 V on secondary side and 12 V on the primary side, you can calculate N_{PS}(aux) (the primary to secondary turns ratio) and N_{PA}(aux) (primary to auxiliary) using Equation 30:

$$N_{PS}(\text{aux}) = N_{PA}(\text{aux}) \quad \frac{V_{REFLECTED}}{V_{OUT}(\text{aux})} = 8.33 \quad (30)$$
$$= \rightarrow \text{Select } N_{PS}(\text{aux}) = 8$$

By fixing the switching-frequency range between 70 kHz and 120 kHz, you can obtain LPmin = 2 mH with Equation 31:

$$L_P(\text{aux},\text{min}) = \frac{1}{2 \cdot Q_{Rfreq}(\text{min}) \cdot P_{OUT} \cdot \left[\frac{V_{IN}(\text{aux},\text{min}) + N_{PS}(\text{aux}) \cdot (V_{OUT}(\text{aux}) + V_F)}{\eta \cdot N_{PS}(\text{aux}) \cdot V_{IN}(\text{min})} \cdot (V_{OUT}(\text{aux}) + V_F)\right]^2} \quad (31)$$

where $V_{REFLECTED}$ = N_{PS}*(V_{OUT}(aux)+V_F), Q_{Rfreq}(min) = 70 kHz, V_F = 0.5 V, η = 80 percent and P_{OUT} = 10 W → L_P(aux,min) = 2 mH.

The maximum stress voltage on the FET (Q2) depends on the reflected voltage, input voltage, leakage inductance and snubber network. With no snubber, you will have Equation 32:

$$V_{PRIM}(max) = V_{IN}(aux,max) + N_{PS}(\text{aux}) \cdot (V_{OUT}(\text{aux}) + V_F) + I_{PK}(aux,min) \cdot \sqrt{\frac{L_{LEAKAGE}}{C_{OSS}}} = 743.4\,V \quad (32)$$

Without leakage inductance, Equation 33 expresses the primary voltage as:

$$V_{PRIM}(no\ leakage) = V_{DC}(max) + N_{PS} \cdot (V_{OUT} + V_F) = 473.4\,V \quad (33)$$

By defining $V_{CLAMP} = N_{PS}(aux)*(V_{OUT}(aux)+V_F)$, you cannot consider V_{PRIM}(no leakage) the maximum drain voltage because the clamping voltage (V_{CLAMP}) would be the same as the reflected voltage; thus, each switching cycle would lose some of the magnetizing energy. As a rule of thumb, I recommend choosing V_{CLAMP} as 150 percent of the reflected voltage; in this case V_{CLAMP} = 150 V. This way V_{PRIM}(max) = 420 V + 150 V = 570 V. Using snubbers to clamp the drain voltage enables the use of a 650-V FET. The snubber works by burning the energy stored in the leakage inductance ($L_{LEAKAGE}$) (Equation 34a):

$$E_{SNUBBER} = \frac{1}{2} L_{LEAKAGE} \cdot (I_{PK}(aux, max))^2 \text{ and} \quad (34a)$$

$$I_{RMS}(aux, max) = I_{PK}(aux, max) \cdot \sqrt{\frac{D_{MAX}}{3}} = 166mA \quad (34b)$$

Knowing the maximum RMS current flowing in the FET according to Equation 34-b, you can select the RDS_{ON}(aux); in this case, 1 Ω results in conduction losses of 166 mW.

AC voltage sensing

I evaluated three methods to sense the AC input voltage:

1. Using a secondary winding voltage (forward negative) of the auxiliary power supply.
2. Using the TI AMC1100 analog isolation amplifier plus an operational amplifier (op amp).
3. Using a current-driven 50-Hz transformer plus a full-wave precision rectifier.

A window comparator is normally sufficient to perform UVLO and OVP. Nevertheless, the TI module prototype needs to measure input VAC with a certain precision because it has to limit input current I_{IN}(pfc) to 10-A RMS to avoid overheating. For this purpose, ±5 percent accuracy will be enough, which I accomplished by measuring digitally output power, input voltage and by estimating efficiency.

The first method – using a secondary winding voltage – leverages the negative forward voltage of the secondary side of the auxiliary power supply according to the schematic section shown in **Figure 20**.

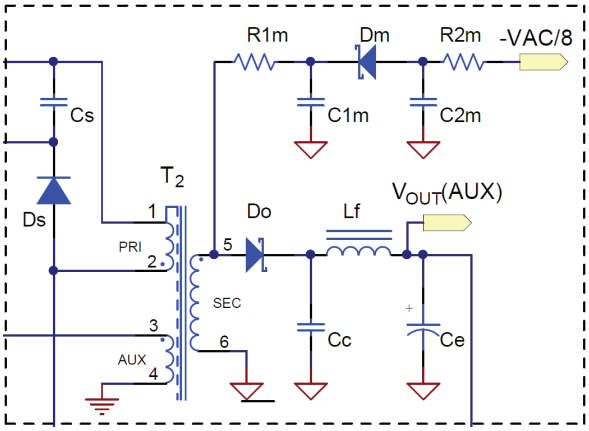


Figure 20. *Measuring AC input voltage by monitoring the auxiliary transformer winding.*

From pin 5 of T2, Do rectifies the flyback voltage, which supplies the whole module on the secondary side. The negative voltage present on pin 5 is proportional to $V_{IN}(aux)/N_{PS}(aux)$, and therefore is a function of VAC (true only if V_{IN}(aux) of the auxiliary supply comes from rectified AC voltage and not from PFC voltage). R1m and C1m remove the spike due to leakage inductance, while Dm and C2m rectify to peak.

This method provides good precision (±5 percent) at a constant load, but across all conditions of 0-100 percent load on both outputs, the precision is ±20 percent. This is also because of the auxiliary-supply bulk capacitor's 100-Hz/120-Hz ripple, as well as the AC voltage crest factor.

In order to get a more precise VAC reading, I tried the second method: using the AMC1100 analog isolation amplifier plus the LMV321 op amp. The op amp converts the AMC1100's differential output to a single output. The peak or RMS value of the sinusoidal VAC transfers to the secondary side. With the first method, you still have to consider the unpredictable crest factor; with the second method, you need a true RMS converter.

For the third method, I selected a small and inexpensive 50-Hz precision transformer with a virtual short circuit on the output to remove the magnetizing current contribution negatively affecting the measurement. The schematic in **Figure 21** shows a precision current-driven rectifier.

AC1 and AC2 are nets connected to mains after the main switch (see **Figure 11**). Since the secondary side of T3 is shorted (thanks to the virtual short circuit provided by the op amp), regarding the AC component, the voltage across T3 is ~ 0V. Therefore, there is no magnetizing current. The turns ratio is 1-to-1; see Equations 35 and 36:

$$I_1 = I_2 = I_{PEAK} = \frac{V_{AC1} - V_{AC2}}{4Rl} \quad (35)$$

and

$$V_{PEAK} = I_{PEAK} \cdot Rb \quad (36)$$

where $V_{PEAK} = V_{PIN7}$.

The double low-pass filter Rf1, Cf7 and Rf2, Cf8 converts the RMS-rectified voltage on pin 7 to an average value fed into the microcontroller, V_{OUT}(µC) = $V_{AVERAGE}$ (full scale = 300 VAC) = 2V. A few calculations results in Equation 37.

$$Vaverage = 2 \cdot \frac{V_{AC1} - V_{AC2}}{4Rl} \frac{Rb}{\pi} \quad (37)$$

By fixing Rl = 250 kΩ, Rb = 7.404 K Cf4 and Cf6 provide some high-frequency filtering (set to 10 kHz), while Cblk removes the error due to the op amp's inverting input-bias current. Rdmp damps the oscillation due to the magnetizing inductance of T3 and Cblk.

This measurement circuit works at full scale with 300-µA current (300-V (RMS) / 4Rl) therefore, it is sensitive to stray fields generated by high 50-/60-Hz current flowing in the EMI filter. Carefully route the I1 current-loop traces (best if routed in pairs).

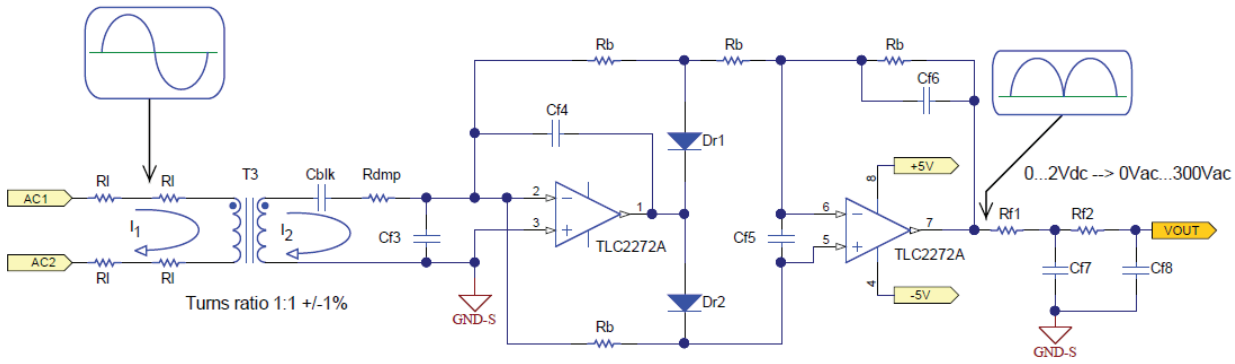


Figure 21. *Schematic of voltage sensing using a 50-Hz transformer.*

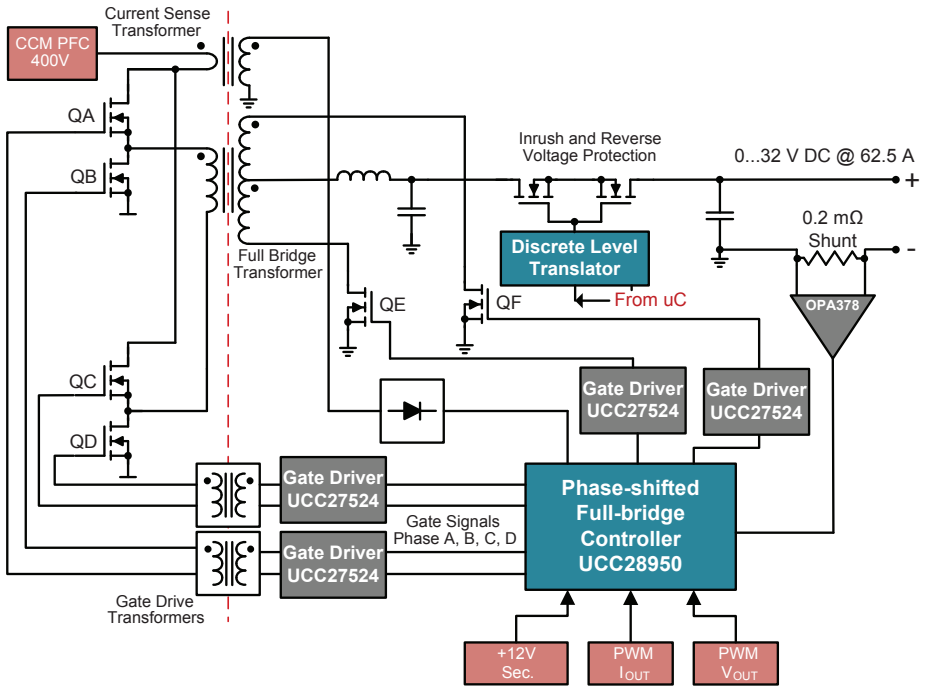


Figure 22. *Phase-shifted, full-bridge converter block diagram.*

Phase-shifted, full-bridge converter

Figure 22 shows the phase-shifted, full-bridge converter block diagram.

It is out of the scope of this paper to provide a deeper analysis of the phase-shifted full bridge, and several papers analyze this topology well [4, 5, 6, 7]. I will focus only on some key aspects. The core of this converter is the UCC28950 controller, which generates all PWM signals to the primary side, driving Qa through Qd as well as synchronous-rectification FETs Qe and Qf. Since the duty cycle on the primary side is almost 50 percent fixed, using UCC27524 gate drivers followed by transformers simplified the driving.

As long as the converter operates with ZVS, you do not need a very high gate current – because while the gate is transitioning from the off state to the on state, the FET body diode is conducting. If at light load you lose ZVS, driving the FET relatively slowly reduces EMI as well. The same driver drives the synchronous rectifiers, but you need enough gate current to avoid excessive switching losses.

A current-sense transformer allows the controller to run in peak-current mode, which balances the magnetizing current in the transformer and protects against any cross-conduction.

You do not need a series capacitance to balance the transformer. The controller compares the voltage and current references provided by the microcontroller to the values read by the voltage and current loop, which generates PWM pulses. Note that this is an analog controller (not digital) that is monitored and controlled by the microcontroller.

The inrush and reverse-voltage protection circuit provides:

- Inrush protection during the module connection of the module to the load, when the load is a large charged capacitor, a battery or a telecommunications bus.
- Reverse-voltage protection during module installation if the bus or load accidentally presents a negative voltage.

The microcontroller checks the voltage at the output terminals and decides whether or not to close the back-to-back FETs.

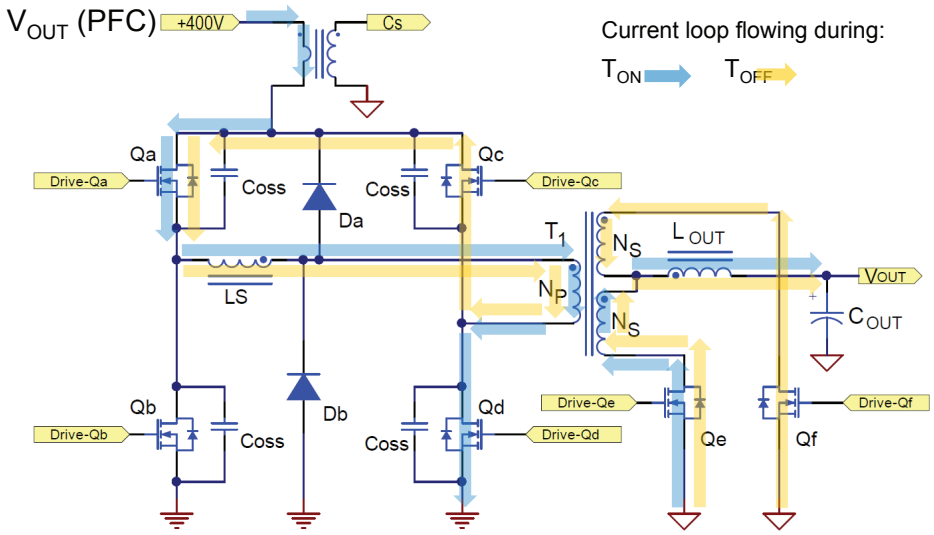


Figure 23. How currents flow in a phase-shifted full bridge topology.

Figure 23 illustrates how currents flow in a phase-shifted, full-bridge topology.

During the on-time of Qa and Qd (T_{ON}), current is flowing as indicated by the blue arrows. The secondary-side current (through L_{OUT}) divided by the turns ratio and added to the magnetizing current flows in the primary winding. The current-sense transformer senses this current and sends the information to the controller for comparison to the error amplifier output.

During T_{OFF}, Qa and Qc short the primary winding of T1 while the primary current is still flowing, thanks to resonant inductor L_S. On the secondary side, most of the current flows through QF, while only $\Delta IL_{OUT}/2$ flows through QE. Since this last current is small, I neglected its contribution and considered only the main parts shown in waveforms (**Figure 24**).

Even though the leading and lagging switches show different waveforms (but all have a 50 percent duty cycle), their relative RMS currents are almost identical. V_{OUT}(pfc) = V_{IN}(fb) where fb = full bridge. Considering V_{IN}(fb,nom) = 400 V and V_{OUT}(fb,nom) = 27 V, with Equation 38 you get:

$$L_{OUT} = \frac{V_{OUT}(fb,nom) \cdot \left(1 - D(fb,nom)\right)}{\Delta I_{Lout} \cdot F_{SW}} = 3.7\ \mu H \quad (38)$$

supporting I_{PEAK} = 60 A + 10 percent = 66 A.

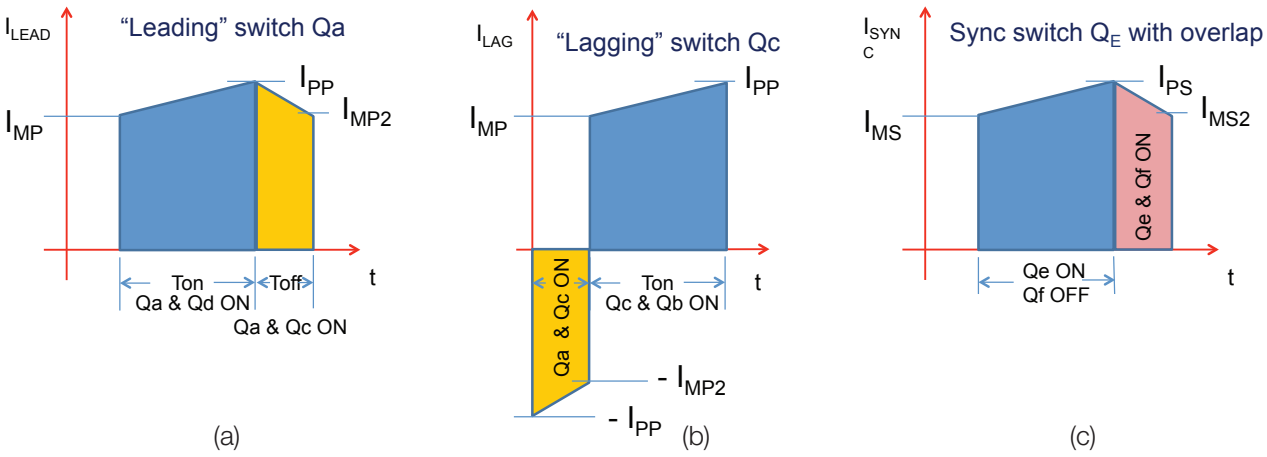


Figure 24. Idealized current waveforms in a phase-shifted, full-bridge topology where (a) is leading; (b) is lagging; and (c) is with overlap.

Equations 39-41 calculate peak currents on the secondary side:

$$I_{PS} = \frac{P_{OUT}(fb)}{V_{OUT}(fb)} + \frac{\Delta I_{Lout}}{2} = 66\ A \quad (39)$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{Lout}}{2} = 60\ A \quad (40)$$

$$I_{MS} = \frac{P_{OUT}(fb)}{V_{OUT}(fb)} - \frac{\Delta I_{Lout}}{2} = 54\ A \quad (41)$$

Then IQe(RMS) = 42.7 A.

Use Equation 42 to select the turns ratio (N_{PS}(fb)) of the transformer T1 according to V_{IN}(fb,min), V_{OUT}(fb,max) and D(fb,max):

$$N_{PS}(fb) \le \frac{D(fb,max)\cdot(V_{IN}(fb,min) - 2\cdot V_{RDSon})}{V_{OUT}(fb,max) + V_{RDSon}} = 9.665 \quad (42)$$

where V_{RDSon} = FET drop = 0.5 V, V_{IN}(fb,min) = 350 V and V_{OUT}(fb,max) = 32 V. Select N_{PS}(fb) = 9.5.

According to this turns ratio, Equations 43-45 calculate the primary currents I_{PP}, I_{MP} and I_{MP2} as:

$$I_{PP} = \left(\frac{POUT(fb,max)}{V_{OUT}(fb,max)\cdot\eta(fb)} + \frac{\Delta I_{Lout}}{2}\right)\cdot\frac{1}{N_{PS}(fb)} + \frac{\Delta I_{Lmag}}{2} = 7.526\ A \quad (43)$$

$$I_{MP} = \left(\frac{POUT(fb,max)}{V_{OUT}(fb,max)\cdot\eta(fb)} - \frac{\Delta I_{Lout}}{2}\right)\cdot\frac{1}{N_{PS}(fb)} - \frac{\Delta I_{Lmag}}{2} = 5.771\ A \quad (44)$$

$$I_{MP2} = I_{PP} - \frac{\Delta I_{Lmag}}{2}\cdot\frac{1}{N_{PS}(fb)} = 6.894\ A \quad (45)$$

The shaded areas in **Figure 25** show the RMS currents during the T_{ON} and T_{OFF} periods. These two RMS currents (I_{Qa1} and I_{Qa2}) are calculated, respectively, according to equations 46 and 47.

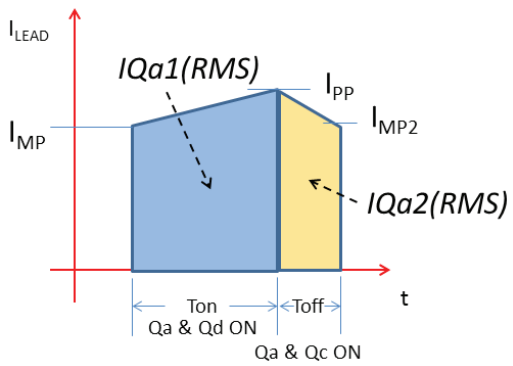


Figure 25. *RMS current comprises two periods.*

$$IQa1(RMS) = \sqrt{\frac{D(fb,max)}{2}\left[IPP\cdot IMP + \frac{(IPP-IMP)^2}{3}\right]} \quad (46)$$

$$IQa2(RMS) = \sqrt{\frac{(1-D(fb,max))}{2}\left[IPP\cdot IMP2 + \frac{(IPP-IMP2)^2}{3}\right]} \quad (47)$$

Equation 48 calculates the total Qa FET RMS current as:

$$I_{MP2} = I_{PP} - \frac{\Delta I_{Lmag}}{2}\cdot\frac{1}{N_{PS}(fb)} = 6.894\ A \quad (48)$$

Using the RMS currents in the primary side and synchronous-rectification FETs, I chose an equivalent RDS_{ON}(fb) (neglecting the switching losses thanks to ZVS). I budgeted a loss of 1 percent of P_{OUT}(fb) for Qa through Qd (Equation 49):

$$P_{Qa} = (0.25\%\ of\ 32\ V\cdot 60\ A) = 4.8\ W \quad (49)$$

$$P_{Qa} = \left(I_{Qa}(RMS)\right)^2\cdot RDS_{ON}(Qa) + 2\cdot Q_G(Qa)\cdot V_{GATE}\cdot\frac{F_{SW}(fb)}{2} \quad (50)$$

Not yet knowing which FET to select, I temporarily neglected the contribution from gate-charge loss . As result from Equation 50, we get an RDS_{ON}(Qa) ≤ 0.21 Ω. For Qa through Qd, I selected four FETs with RDS_{ON}= 0.19 Ω, 17 A, 650 V, which also incorporate ultra-fast body diodes to help

reduce current spikes when ZVS is lost at light load. According to Equation 51, the synchronous-rectification FETs QE and QF must withstand:

$$V_{DS}(Qe) = \frac{2 \cdot V_{IN}(fb,max)}{N_{PS}(fb)} \cdot 1.5 = 139\ V \quad (51)$$

where 1.5 is a 50 percent margin, N_{PS}(fb) is the transformer turns ratio = 9.5 and V_{IN}(fb,max) = 440 V.

You can select a 200-V FET because the spike (already calculated in the +50 percent) will be clamped. Considering the 1 percent loss budget from P_{OUT}(fb) on Qe and Qf, Equation 52 calculates the equivalent switch RDS_{ON}(EQ):

$$RDS_{ON}(EQ) \leq \frac{P_{BUDGET}(Qe)}{\left(I_{Qe(RMS)}\right)^2} = 5.5 \cdot 10^{-3}\Omega \quad (52)$$

You can then select four FETs with RDS_{ON} = 10.5 mΩ, 84 A, 200 V, connected two in parallel per equivalent switch (for example, Qe).

Equation 53 calculates the total equivalent-switch QE losses as:

$$P_{Qe} = \left(I_{Qe}(RMS)\right)^2 \cdot RDS_{ON}(Qe) + \frac{P_{OUT}(fb)}{V_{OUT}(fb,nom)} \cdot V_{DS}(Qe) \cdot T_F \cdot \frac{F_{SW}(fb)}{2} + 2 \cdot COSS(Qe,avg) \cdot \left(V_{DS}(Qe)\right)^2 \cdot \frac{F_{SW}(fb)}{2} + 2 \cdot Q_G(Qe) \cdot V_{GATE} \cdot F_{SW}(fb) = 25.2\ W \quad (53)$$

Resonant inductor calculation

The energy stored in the resonant (shim) inductor will charge and discharge the C_{OSS} of one leg (two FETs) of the phase-shifted full bridge. To reduce this energy down to 15 percent of full load, you need L_S (Equation 54):

$$LS \geq 2 \cdot C_{OSS}(Qa,avg) \cdot \frac{(V_{IN}(fb,nom))^2}{\left[\text{LOAD(min)} \cdot \left(I_{PP} - \frac{\Delta I_{Lout}}{N_{PS}(fb)}\right)\right]^2} - L_{LK} = 1.13 \cdot 10^{-5} H \quad (54)$$

where L_{LK} = 3.5 µH (0.1 percent of the magnetizing inductance).

If the result is negative, no shim inductor is necessary and the leakage inductance of the transformer will be sufficient to keep ZVS active down to a 15 percent load. In our case needed to add approximately 11.3 µH, so I selected a 10-µH shim inductor. Keep in mind that primary-transformer current is very close to shim-inductor current (by neglecting the small spike current flowing through clamping diodes Da, Db). **Figure 26** shows its waveform.

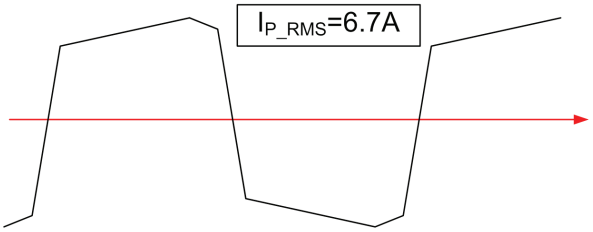


Figure 26. *Waveform of the transformer primary current.*

This waveform has only an AC component. You must take care when designing the inductor to support the peak-to-peak flux swing. Without getting into too much detail about the inductor design, I selected a PQ20/20 platform and obtained the following data:

- 10 turns of Litz wire (160 by 0.1 mm).
- Δ PEAK = 118 mT.
- N97 EPCOS core, gap = 0.77 mm, µe = 57.

This results in copper loss (Pcu) = 0.63 W and core loss (Pcore) = 0.57 W.

Full-bridge FET driving

Since the nominal duty cycle is always 50 percent (minus dead time) and you do not need extremely fast driving (thanks to ZVS and the lack of a Miller-capacitance issue), you can employ a simple driving scheme like the one shown in **Figure 27**.

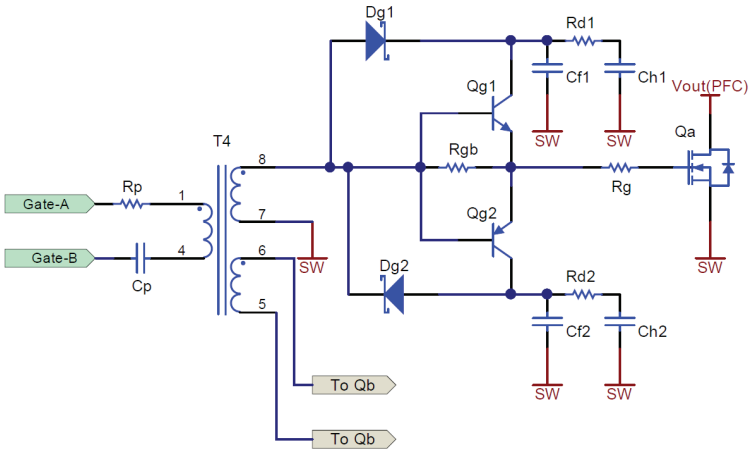


Figure 27. *Phase-shifted full bridge gate drive.*

The driving signals GATE-A and GATE-B combine, with the difference (minus any unwanted DC component) applied to transformer T4. The resistor R_P damps any oscillation due to the resonant circuit generated by L_P (the magnetizing inductance of T4) and C_P. To damp the oscillation on the secondary side of T4, first I chose the turns ratio. A drive voltage of 12 V was sufficient. Since the Vcc driver voltage is 12 V, N_P/N_S = 1-to-1.

Pin 8, referred to SW-node, has a ±12-V_{PEAK} square wave. Dg1 and Dg2 will rectify these two voltages to Cf1/Ch1 and Cf2/Ch2, respectively, generating V_{DD} and V_{EE}. Qg1 and Qg2 amplify the driving current into the FET's gate and keep the driving circuit as close as possible to FET Qa. The absence of Rd1, Ch1, Rd2 and Ch2 results in a low-frequency oscillation on VDD and VEE due to unwanted resonance. To avoid that, connect only small capacitors (Cf1 and Cf2) to provide the peak current needed to charge and discharge the FET's gate capacitance. Choose a Cf1 value 10 times the Ciss of FET Qa, which in this case is 1850 pF. That makes Cf2 = Cf1 ≥ 18.5 nF. Select 22 nF as closest standard value.

A snubber circuit (Rd1, Ch1 and Rd2, Ch2) in parallel to Cf1, Cfr2 is now necessary to stabilize the gate voltage and avoid bouncing.

Select a Ch1 value that is approximately four to five times the value of Cf1. Select Ch1 = 100 nF as the closest standard value. Next size Rd1 to damp the oscillation.

According to **Figure 28**, which shows a typical circulating current in a parallel LC resonant circuit, the best-value damping factor (ζ) is in the range of 0.4 to 1.

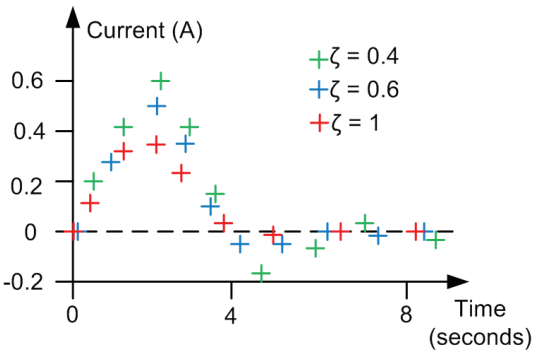


Figure 28. *Waveform comparison for different damping factors.*

If ζ = 0.5 (the minimum damping factor), Equation 55 calculates Rd1:

$$Rd1 = 2 \cdot \zeta \cdot \sqrt{\frac{L_M(T4)}{Ch1}} = 94.4\ \Omega \tag{55}$$

Finally I selected Rd1 = 100 Ω.

Phase-shifted, full-bridge voltage and current loop

Figure 29 shows how to interface the output voltage and current to the UCC28950 controller. The voltage information comes from a simple voltage divider ($R_{PARALLEL}$ + R_{HIGH}; R_{LOW}), while the current information comes from the shunt resistor and amplifier (**Figure 22**).

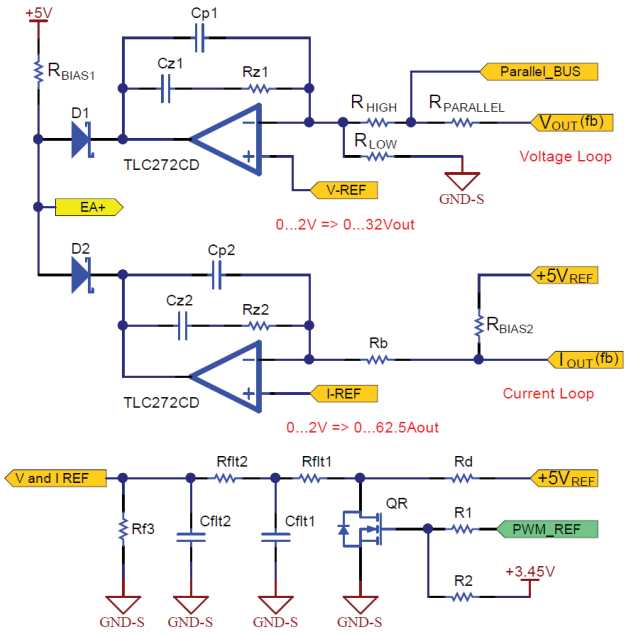


Figure 29. Voltage and current feedback to the controller.

A low-cost FET (Q_R) and a double RC filter, Rflt1, Cflt1 and Rflt2, Cflt2 generate the reference on each error amplifier. Using a square waveform PWM_REF as a reference from the microcontroller results in PWM with a peak voltage equal to +5 V_{REF} on the drain of Q_R (if the impedance of the filter is << Rd). Therefore, the average voltage out of the filter is a DC value in the range 0 to 5 V_{REF}. The PWM reference frequency typically falls in a range of 1 kHz to 10 kHz, so it is sufficient to keep the double-filter frequency Fco << F_{PWM}. I selected Fco = 16 Hz; therefore, Rflt1 = 100 K and Cflt1 = 100 nF. With these values (and for example at a 50 percent duty cycle and FPWM = 1 kHz), the triangular waveform on Cflt1 is 121 mVpp plus 2.5 V_{DC}. Place the second cell Rflt2, Cflt2 at the same frequency and choose the value close to Rf1, Cf1. I selected Rflt2 = ½ Rflt1 and Cflt2 = 2Cflt1. This results in 1.48 mVpp, plus 2.5 V_{DC} on Cflt2.

Other notes on the scope of other resistors in this circuit:

- R2 is useful if the microcontroller is in a reset condition. This resistor fixes the output-reference voltages to zero.
- R_{BIAS2} injects a small current into the error amplifier. The reference voltage, proportional to the output current, will start from zero and slowly reach the programmed value.

The COMP pin of the UCC28950 ORs the two outputs of the error amplifiers. **Figures 30 and 31** show the Bode plots for constant-current and constant-voltage regulation. The DC/DC converter works in peak-current mode, which translates into benefits for the compensation network. In fact, the power-stage transfer function is a single pole given by the output capacitance and load resistance. Remember that you are sensing the output current when running in constant-current mode, and the power stage shows a constant 90-degree phase shift. Therefore, a type I compensation network is sufficient.

Because I wanted to operate the TI module prototype as both a power supply and a battery charger, I did not know exactly what the load would look like. Therefore, I used a type II network for better flexibility. By properly selecting Rz1 and Rz2 so that the gain of the power stage at the crossover frequency equals the attenuation given by Rz2/Rb and Rz1/(R_{HIGH} +$R_{PARALLEL}$), you can obtain the compensation network center-band gain. Place a zero at low frequency, usually at the pole of the power stage. I selected the two zeros, respectively, at 23 Hz and 48 Hz for the voltage loop (VL) and current loop (CL). Place a pole at a higher frequency to provide some filtering at switching frequency. For me, the poles were at 1 kHz for VL and 1.9 kHz for CL.

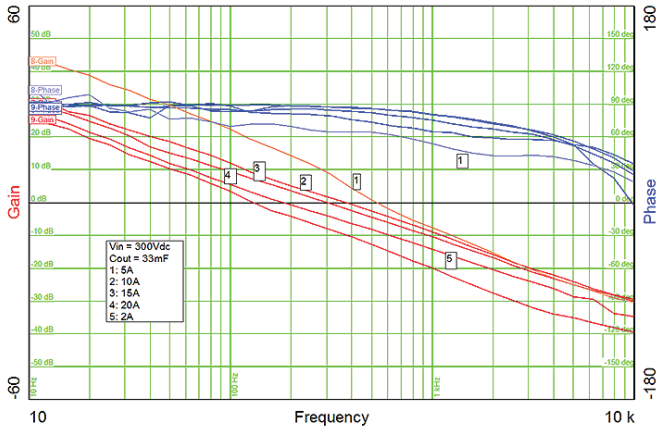


Figure 30. *Bode plots of the current loop at different load currents.*

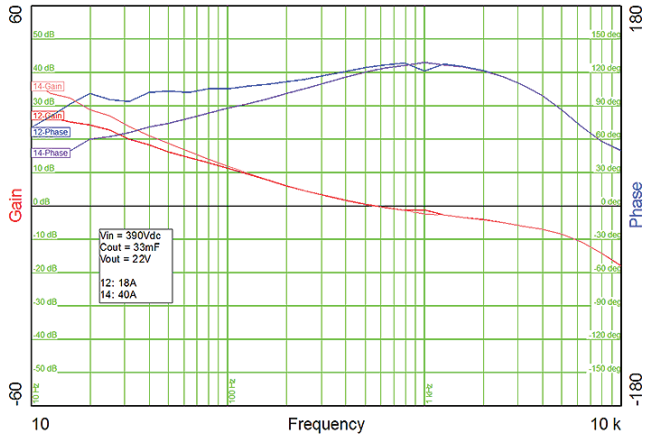


Figure 31. *Bode plots of the voltage loop at different load currents.*

Even though a high-loop bandwidth for battery chargers is not necessary, it is useful when using the module in parallel with others. Keep the parallel loop crossover frequency (F_{CO}(parallel)) slow (a few hertz of bandwidth). To avoid instability, each power supply must react quickly and have a crossover frequency greater than 10 to 20 times the F_{CO}(parallel).

Microcontroller characteristics

During the definition of a power module like the one described in this paper, you obviously must use a microcontroller, mainly because this module is not a simple power supply but has to be part of a system. It is best to leverage a microcontroller as much as possible. Keep in mind, however, that this is not a digital power supply. The microcontroller should only supervise the main functions, generate references, read values, and set parameters; the most demanding feature is the management of parallel modules. **Table 6** shows the main functions of a microcontroller.

Function	Description	Digital/analog
VAC, V_{IN}, I_{IN}, temp	Reads input VAC voltage, output voltage and current, and internal temperature	Analog
LCD management	Communicates with LCD display	Digital in/out
Backlight	Switches LCD display on/off backlight	Digital out
S1 … S4	Manages four pushbuttons	Digital in
V_{REF}, I_{REF}	Sets reference PWM for VOUT(fb) and IOUT(fb)	Digital out
RPM	Reads fan revolutions per minute (RPM)	Digital in
Fan PWM	Sets fan speed	Digital out
PFC power good	Acquires PFC power good (UVLO of DC/DC)	Digital in
Red/yellow/green LED	Drives three LEDs to visualize main status	Digital out
Rev_polarity	Recognizes reverse polarity on the output terminals	Digital in
Rx/Tx	Communicates between modules	Digital in/out

Table 6. *Main functions of a microcontroller.*

Managing all of the functions shown in **Table 6** would have been almost impossible without a microcontroller. With the help of an LCD and four pushbuttons, you can now set all necessary parameters.

First, I selected the right computational power for the microcontroller and its peripherals. According to **Table 6**, I needed four analog inputs; see **Table 7**.

Requirement	Variable or function	Hardware
4 analog inputs	V_{OUT}(fb), I_{OUT}, VAC(RMS) Tamb	4 ADCs
2 analog outputs	V_{OUT}(fb) and I_{OUT}(fb) PWM for reference generation	2 PWMs
General-purpose input/output (I/O)	Several inputs/ outputs	28 GPIOs
V_{OUT}(fb) and I_{OUT}(fb) reading	Output voltage and current, 100 Ksps, ±1%	10-bit ADC
V_{OUT}(fb) and I_{OUT}(fb) setting	Fclock = 16 kHz, compare fs = 16,000	PWM = 1 kHz

Table 7. *Microcontroller requirements.*

Considering the power level of the application, extremely low power consumption is not necessary. For the power module, I selected the MSP430F2252, which has 16 K + 256 bytes of flash memory and 512 bytes of RAM.

Microcontroller functionality

All high-speed functions (loop and protections) are performed in hardware; therefore you can delegate all “slow” tasks to the microcontroller. This way – no matter what happens – the module will never generate dangerous output voltages or lose control. On the PFC converter, for example, a loss of control might result in damage to passive and active components. I used states to develop the firmware of the module according to **Figure 32**.

The microcontroller increases a running software counter only if the module is enabled and there is no alarm. The counter decreases if there is either an active alarm, or the module is disabled. The system

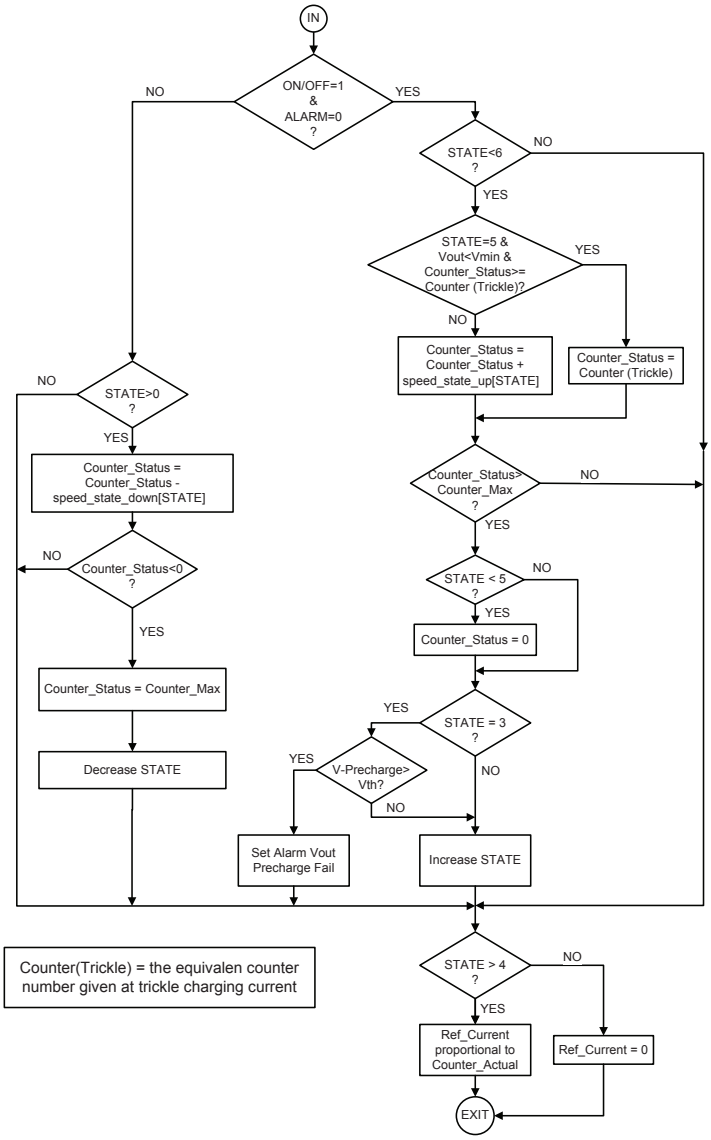


Figure 32. *Firmware flowchart.*

goes from state(N) to state(N+1) only if the counter is in overflow, or goes from state(N) to state(N-1) if the counter reaches zero.

For each state, the microcontroller sets the speed at which the counter increases or decreases. This simple method controls the timing between states.

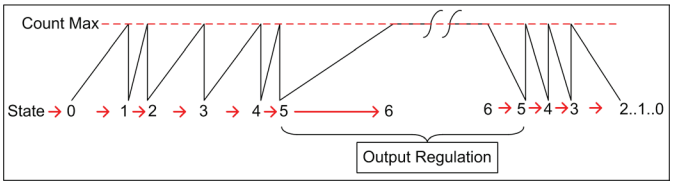


Figure 33. *Example of counter operation.*

The graph in **Figure 33** better explains the functionality, showing the counter number (Y axis, 0 … CountMax) and the state (and time) on the X axis. The system will switch faster when traveling from state(1) to state(2) compared to other states, according to the slope of the triangular waveform.

Table 8 describes each state number and state(N) function. All previous functions activate at each state number.

State number	Function	Description
0	All functions off	Standby
1	Boost relay on	AC inrush phase completed, relay on
2	Enable boost controller	Boost power stage starts regulation V_{PFC}
3	Reverse polarity	Check digital I/O if the output terminals have a negative voltage applied (reverse-polarity protection)
4	Enable full bridge	DC/DC converter starts delivering pulses
5	Enable hot-swap FETs and start current ramp	DC/DC converter starts delivering power and voltage/current is ramping up from zero
6	Regulation	DC/DC converter has reached the programmed output voltage/ current and is delivering power in a steady-state condition

Table 8. *Summary of different states. Each state identifies different working conditions of all power stages.*

The counter is also useful to ramp up and down the output voltage (or current). Between state(5) and state(6), the module delivers an output voltage (or current) proportional to the counter, which automatically generates soft-start and soft-stop functions. A proper setup on the display defines the regulated output characteristic (voltage or current) by specifying the module as a general power supply or battery charger. Setting the module as battery charger involves a more complex architecture, already described in **Figure 2**, entailing the addition of a further block in order to perform output hot swap, inrush current reduction and reverse-polarity protection.

Paralleling modules: using UART with the CAN bus interface

Specify the parallel between several modules as either a general power supply or a battery charger. A general power supply involves particular hardware that the UCC29002 manages by setting an analog parallel bus. But I would prefer to describe the digital parallel in more detail when using the module as a battery charger.

There are several ways to perform module paralleling and managing; for the example power module, I selected the master/slave architecture. I set one module as a master during parameter setup, entered via a human interface (pushbuttons and display), and set all other modules as slaves. Since the whole architecture is a “slow” system (because a battery charger reacts slowly to voltage and current variations), a serial bus can pass parameters such as alarms, warnings and working conditions between modules. As **Figure 34** illustrates, a full-duplex universal synchronous receiver/transmitter (UART) included in the microcontroller uses the SN65HVD256 as a CAN bus interface.

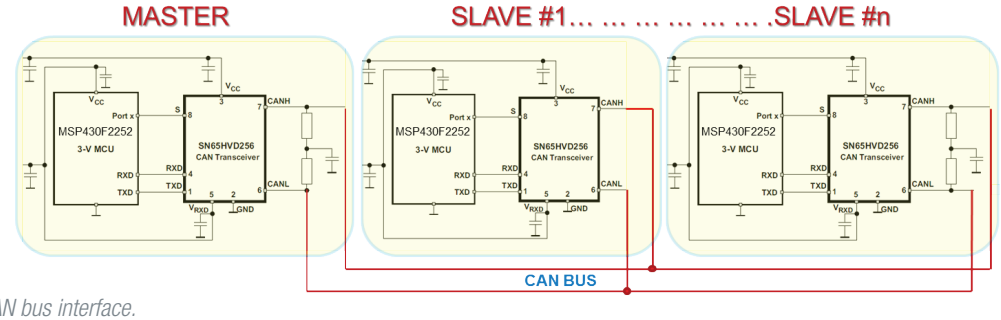


Figure 34. *CAN bus interface.*

UART full-duplex, 9600Bd, 8 bit, 1 stop, no parity

The master polls all slaves and sends commands every 50msec

The slaves respond within 10msec

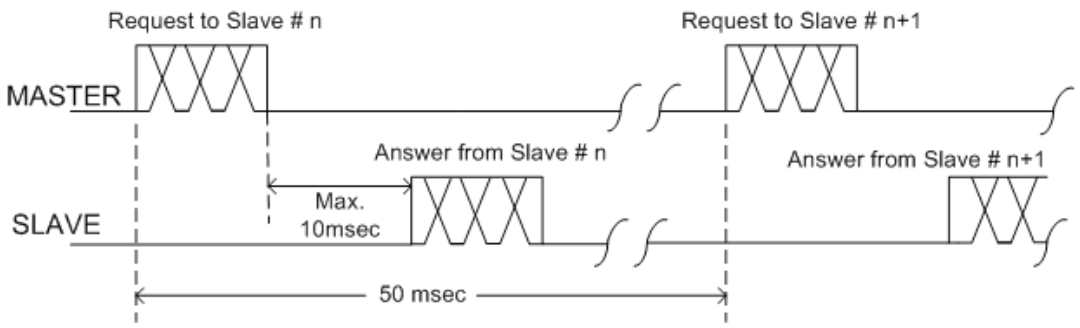


Figure 35. *Master/slave communication.*

Now the idea is to define a master module, which sets all important parameters of the charging process. The master also communicates with slaves and tells them whether to stay in standby or deliver power. Each slave receives commands from the master and sets its own current limit to the required level coming from the master, while the slave's own voltage set point shifts to the maximum value. In other words, the master decides the voltage and current on the output of the system, while the slave just delivers a current level set by the master. In this way, all slaves act as current amplifiers.

There is only one loop, closed on the master. If the master fails, such a methodology might show poor reliability – but you can develop software that manages automatic master generation. The UART communication is pretty standard: full-duplex, 9,600 baud, 8 bit, one stop and no parity.

Figure 35 shows that the master polls all slaves and sends commands every 50 ms, while the slaves respond within 10 ms.

Table 9 shows what parameters the modules exchange.

Start Char	Master Slave	Slave #	Command / Parameter #1	Parameter #2	Parameter #3	Description (Slave #n = "Sn")
#	M	n	S	*	*	Request of status to Sn
#	M	n	E / D	*	*	Enable or Disable Sn
#	M	n	W / A	*	*	Request of active warnings and alarms Sn
#	M	n	C	*	*	Request of supplied current from Sn
#	M	n	L	X_2	X_3	Set Sn current limit to X_2*10+X_3 (Ampere)

(a) Commands sent by master

Start Char	Master Slave	Slave #	Command / Parameter #1	Parameter #2	Parameter #3	Description (Slave #n = "Sn")
#	S	n	X_1	X_2	X_3	Readout of Sn output current → X_1*10 + X_2 + X_3 /10(Ampere)
#	S	n	E / D	*	*	Status of Sn, Enabled or Disabled
#	S	n	W	HN	LN	Content of **Warning** Byte Status (into 2 nibbles, 16 ASCII codes)
#	S	n	A	HN	LN	Content of **Alarm** Byte Status (into 2 nibbles, 16 ASCII codes)

(b) Slave's acquired values sent to master

Table 9. *Details of parameter exchange between (a) the master and (b) slave modules.*

#	Alarm Description
0	Mains too low
1	Mains overvoltage
2	Output overvoltage
3	Output shorted
4	Reverse polarity
5	Over temperature
6	Fan failure
7	DC/DC failure

MODULE OFF

#	Warning Description
0	Output current limit
1	Output power limit
2	Input current limit
3	Low battery voltage
4	not used
5	not used
6	not used
7	not used

Yellow LED ON

Figure 36. *Summary of alarms and warnings.*

Both the master and slaves transmit and receive a six ASCII-character string. The first character of the string must be the "#" character for synchronization. When a parameter is not necessary, the "*" character can be any character except the sync, or "#" character. A set timeout skips a truncated string. Since the sync character "#" is always expected by both master and slaves, the module will discard any incoming string not starting with the sync.

As I explained in the state description, each module, regardless of its own function as master or slave, will switch off in the event of an active alarm. Warnings only show up on the display and switch the yellow LED on. **Figure 36** lists the warnings and alarms.

The module display presents all alarms and warnings under the menu item "alarms/warnings." Some alarms are latched and resettable while others are non-latching, such as the mains UVLO, or OVP and overtemperature.

Fan speed is proportional to the output current; and the microcontroller measures and compares the RPM to the curve provided by the manufacturer. An RPM not in line with the data sheet generates a non-latching alarm.

Module hot swap plus reverse-polarity protection

Now that you have a module specified as a battery charger, you need to limit the output current when a module (or a system comprising several modules) connects to a battery. You also need to add reverse-polarity protection. The circuit shown in **Figure 37** accomplishes both functions.

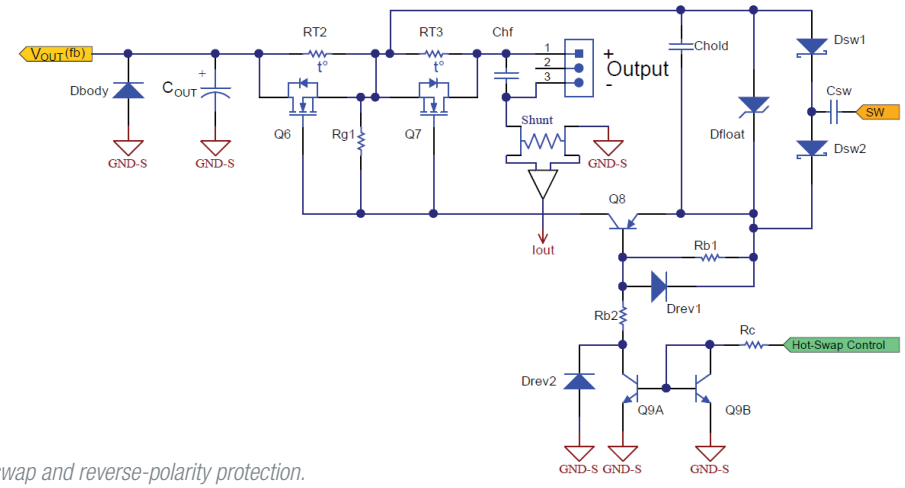


Figure 37. *Hot-swap and reverse-polarity protection.*

The V_{OUT}(fb) net connects to the output of the DC/DC converter; Dbody represents the total body diode of the synchronous-rectification FETs. The section comprising Q9A and Q9B, Drev1 and Drev2, Q8, Dfloat and Dsw1 and Dsw2 forms a floating driver, enabling back-to-back FETs Q6, Q7. These FETs must both be on before enabling the DC/DC converter.

The positive temperature coefficient (PTC) resistor RT2 limits the output current during inrush, while RT3 protects against high negative circulating currents if a negative voltage is accidentally applied to output terminals 1 and 3. I selected a PTC for RT3 to avoid high dissipation. The "SW" net connects to the switch node of a buck converter, which supplies power to the whole digital section and LCD backlight. Dsw1 and Dsw2 define a charge-pump system that builds 12 V on Chold. The current flows from the SW switch node through Dsw2, Chold and back to RT2, RT3. The Zener Dfloat avoids overvoltage on Chold due to spikes on the switch node.

If the hot-swap control net is zero, the current mirror Q9A-B is not conducting. Therefore, no current flows through Rb2 and the base of Q8. As a result, Q6 and Q7 are off.

In this condition, if a voltage (battery, for example) is present on output terminals, a charging current will flow from the battery through the PTC resistor RT3, the body diode of Q6, and the output capacitor C_{OUT}, therefore charging the output capacitance. After the inrush time expires, the microcontroller can switch Q6 and Q7 on by setting the hot-swap control net to 3.3 V through an I/O from the microcontroller.

The current mirror will pull down the base of Q8, which will drive FETs Q6 and Q7. In the event of a negative voltage, current will flow from this negative source through the body diode of Q7, RT2 and the body diode of the synchronous FETs (Dbody). It is not possible to disconnect this circuit and RT2 will present a higher impedance in this steady-state condition. Drev2, Drev1 and Dfloat protect Q8 and Q9 against reverse voltage and the currents are limited by Rb1, Rb2.

Of course, it is important that the microcontroller does not enable Q6 and Q7 if a negative voltage is applied to the output. Disabling Q6 and Q7 is done by reading the output voltage, clamping it to zero, and supplying this information to the microcontroller (**Figure 38**).

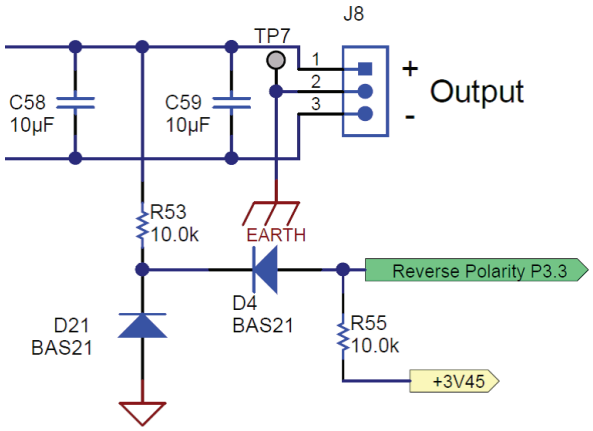


Figure 38. *The interface to the microcontroller detects output negative voltage (reverse polarity protection).*

The power lost in Q6 and Q7 should be as low as possible, but of course the lower the loss, the higher the cost. A good compromise is to accept 0.2 percent of P_{OUT}(nom), or 4 W (Equation 56):

$$RDS_{ON}(Q6+Q7) = \frac{0.2\% \cdot P_{OUT}(NOM)}{(I_{OUT}(NOM))^2} = 1.02\ m\Omega \qquad (56)$$

These FETs must withstand a V_{OUT}(max) of at least 32 V. Because 40 V is too close, I selected 60-V FETs – 10 CSD18532Q5B NexFET™ power MOSFETs connected back to back (five by five). Each one has an RDS_{ON} = 2.5 mΩ, so the total resistance will be 1 mΩ.

You can use a small-signal dual NPN transistor for Q9A and Q9B. I selected a low-cost 160-VCE0 MMDT5551.

Drev1 and Drev2 are standard 200-V diodes; Q8 is a standard 60-V PNP bipolar junction transistor (BJT).

Since Q6 and Q7 do not need high-speed switching, the off time can be constant and equal to a few milliseconds. For example, if Rg1 = 100 K (therefore minimizing current consumption in steady state) and the equivalent CISS of Q6 and Q7 = 10·5070 pF ~ 50 nF, the TOFF time is 5 ms.

Select Rb2 so that during a negative voltage on the output, the Q8 base current does not exceed the maximum absolute value of 32 mA. (Equation 57)

$$Rb2 \geq \frac{V_{OUT}(max)}{32mA} = \frac{32V}{32mA} = 1\ K\Omega \quad (57)$$

Set Rb1 to keep Q8 off in all other conditions.

The other components have the following values: Chold = 220 nF, Csw = Chold/10 and Dfloat = 13-V Zener diode.

Final block diagram

Figure 39 is the complete block diagram, including all controllers. The red blocks show which integrated circuit (IC) is in charge of which function. The blue blocks represent the passive main functions.

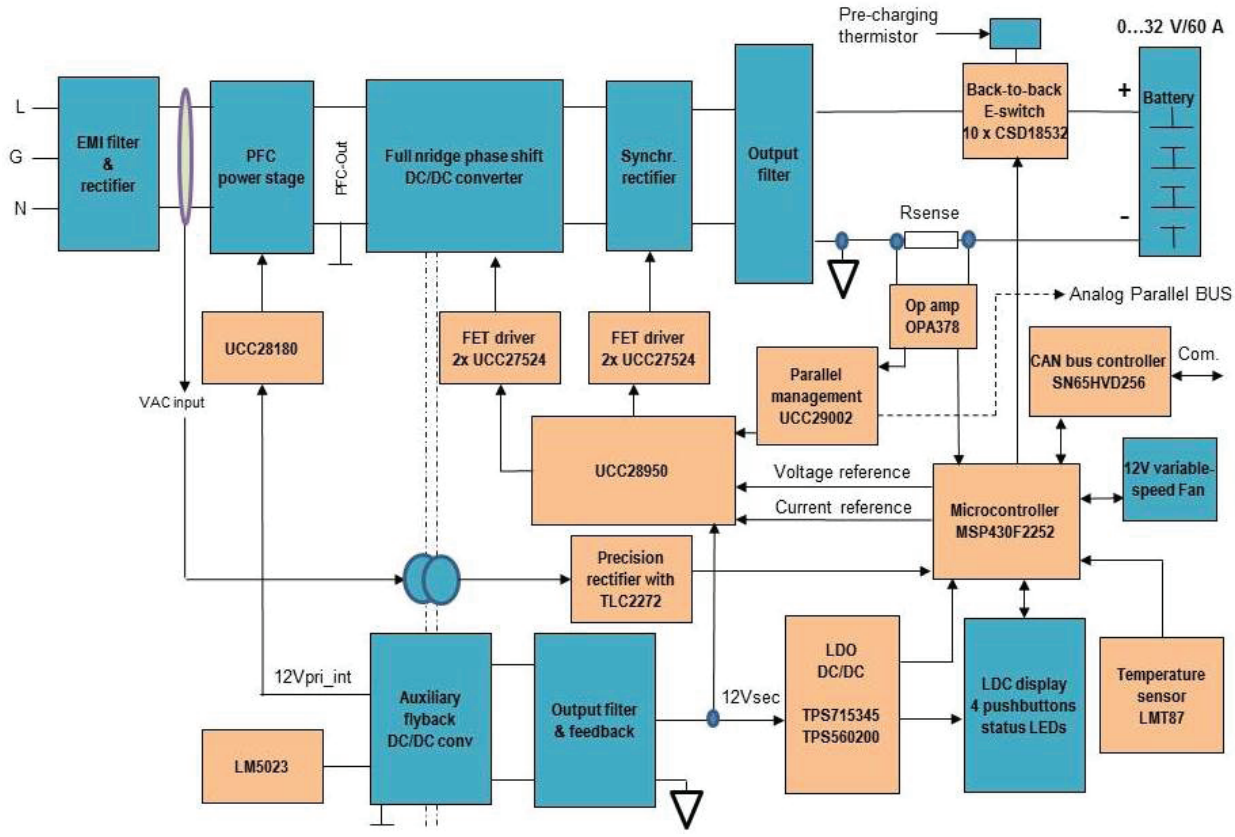
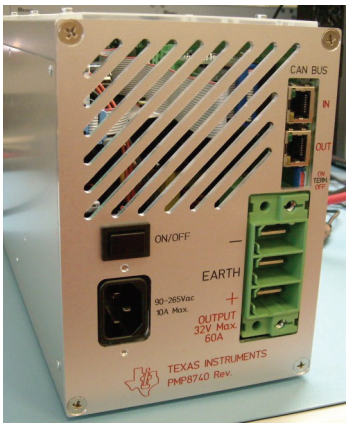


Figure 39. *Final block diagram.*

I built a complete module by employing a standard housing customized by the manufacturer to host all boards. I used special software provided by the company that produces the housing to design both the front and back panels. **Figure 40** shows the prototype.



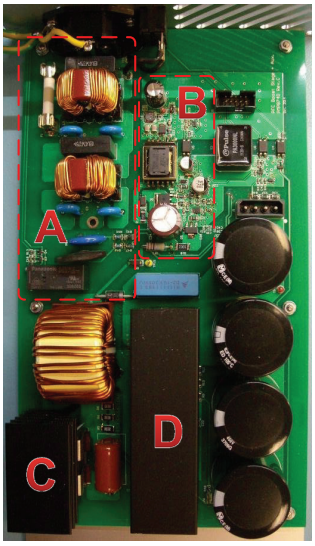
(a) Rear panel

(b) Front panel

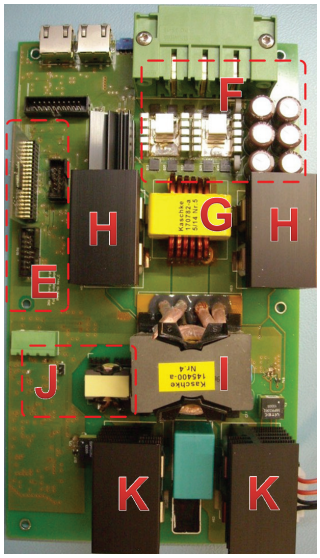
Figure 40. *Rear (a) and front (b) photos of the module.*

The dimensions of the module are 125 mm by 170 mm by 290 mm (width by height by depth). The human interface is on the front panel. Four pushbuttons are placed under the LCD display. Corresponding to the pushbuttons the menu page changes, according to the information needed. For example, in the main menu shown in **Figure 40b**, SET = set main parameters, READ = show readings (VAC, fan RPM, state of the module), ALM = alarm/ warning and ON = module status, which can be on or off. The pushbutton underneath the menu activates the related action. Figure 40a shows the module's rear panel with the output connector, input AC plug, main switch and CAN bus connectors

The back of the module has input and output connectors, a main switch, and CAN bus connectors for connecting several modules in a daisy chain. The termination impedance must switch on at the first and last module by means of a small switch. **Figure 41** shows the main boost and DC/DC boards.



PFC boost converter



DC/DC converter

Figure 41. *Pictures of the main boards.*

Where:

- A = EMI filter and inrush current limit
- B = Auxiliary power supply
- C = Bridge rectifier on heat sink
- D = Main FETs plus SiC diode on heat sink
- E = Microcontroller on daughterboard
- F = Back-to-back FETs plus PTCs plus output capacitors
- G = Output inductor
- H = Synchronous-rectification FETs on heat sink
- I = Full-bridge transformer
- J = Resonant (shim) inductor
- K = Full-bridge FETs on heat sink

I tested the module on the bench at a 23ºC ambient temperature. Because the AC electronic source power limit was 1.6 kW, I tested the system plug to plug, as well as each converter separately. When input PFC and THD was not relevant, I connected the converter directly to mains and tested it at 230 VAC and full power. **Figures 42-45** show some waveforms taken at a 1.6-kW load.

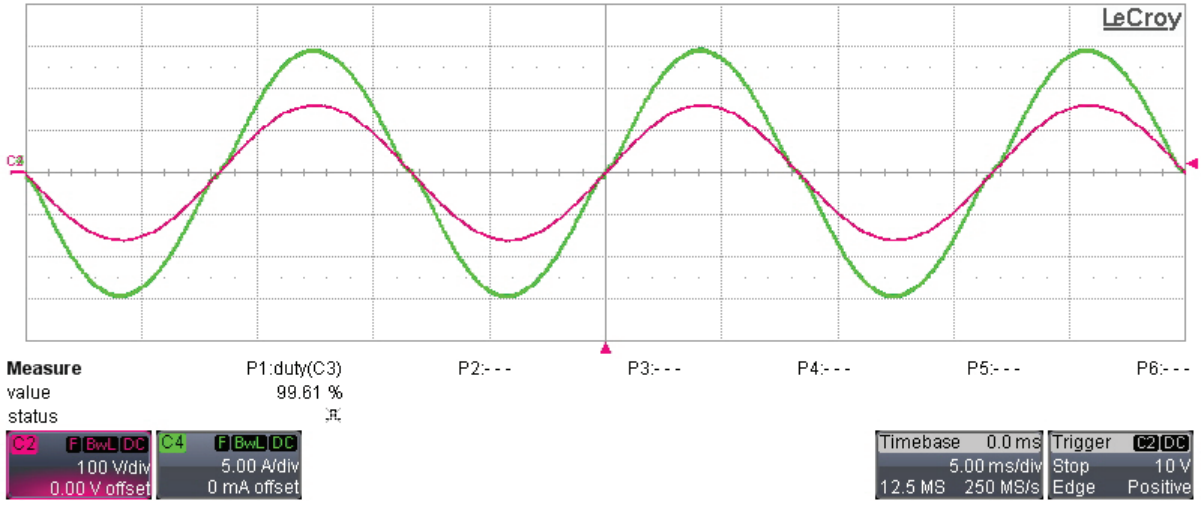


Figure 42. *Input voltage and current at 90 VAC.*

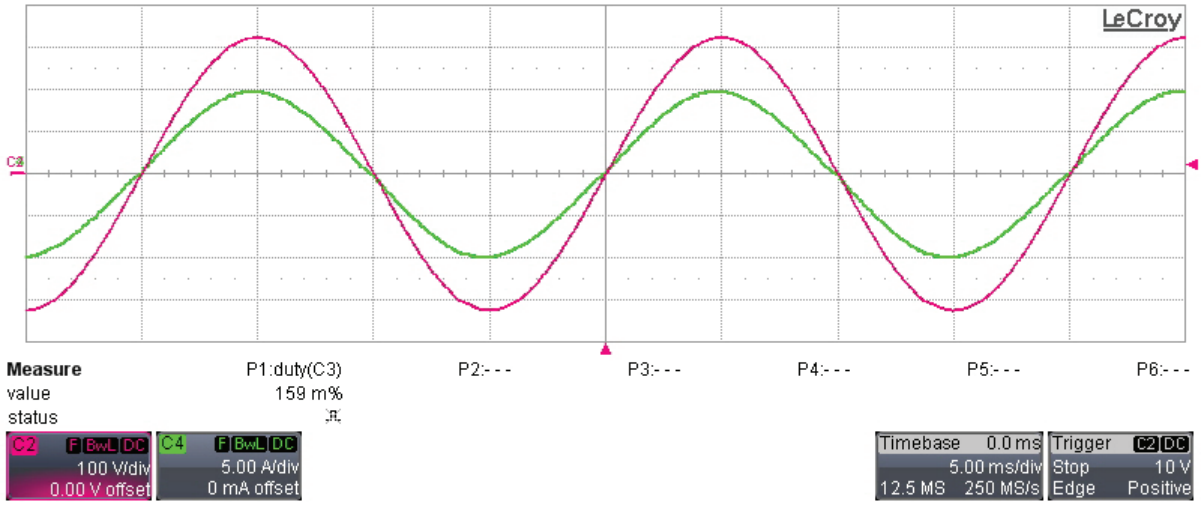


Figure 43. *Input voltage and current at 230 VAC.*

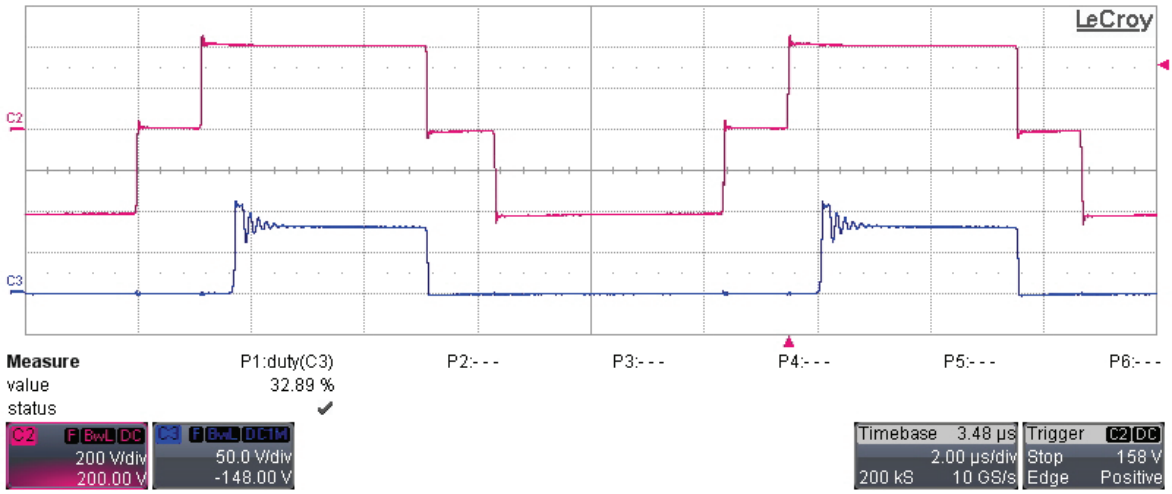


Figure 44. *Bridge voltage (C2) and synchronous-rectification drain voltage (C3).*

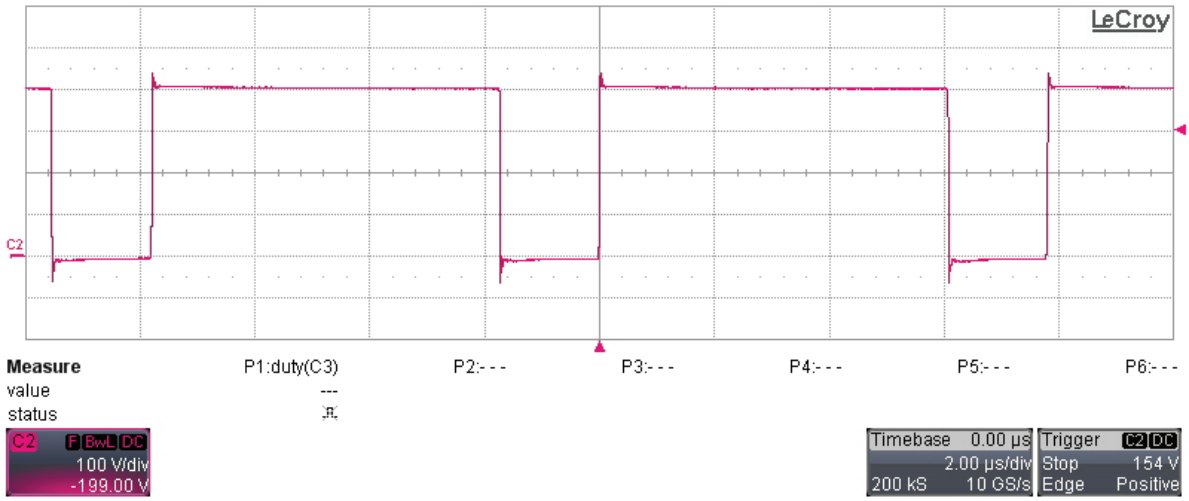


Figure 45. *PFC FET drain voltage.*

Figures 46 and **47** show the power-factor value and efficiency, respectively, of the PFC power converter versus VAC and load power. The first red line (10 ARMS) shows the input current limitation boundary, while the second red line (1.6 kW) shows the limit of the AC power source.

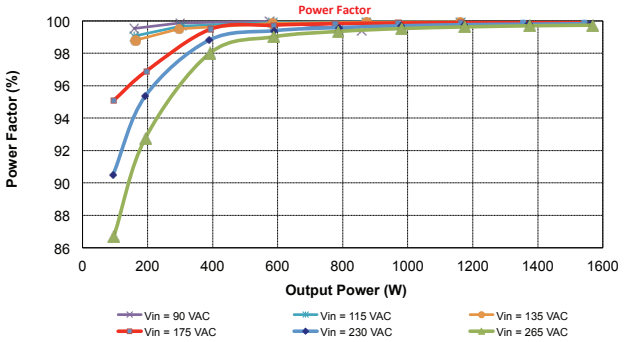


Figure 46. Power factor versus load and VAC.

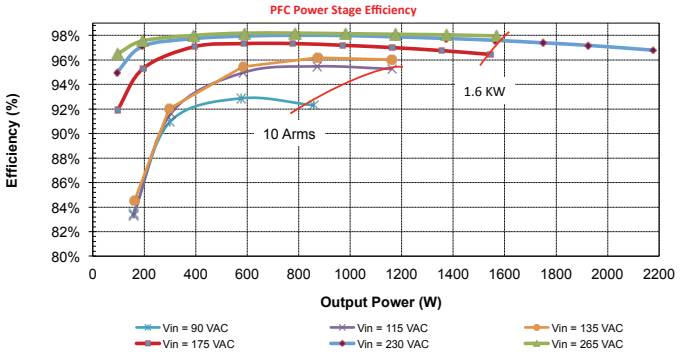


Figure 47. PFC power converter efficiency.

Figure 48 shows the DC/DC power converter efficiency at 230 VAC versus V_{OUT} and load power. The red line shows the TI module prototype's output current limitation (62.5 A).

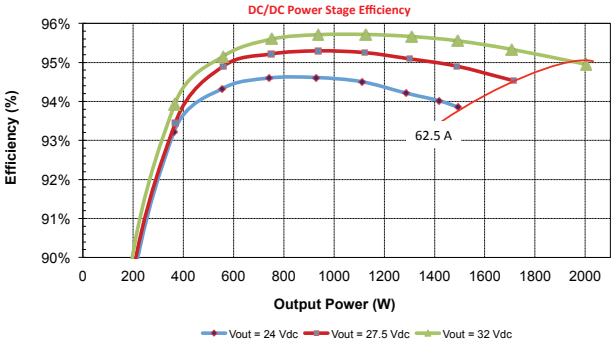


Figure 48. DC/DC power converter efficiency.

Figure 49 shows the total plug-to-plug efficiency at 230 VAC versus V_{OUT}.

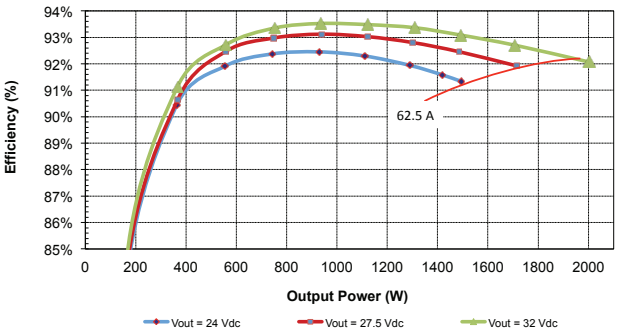


Figure 49. Total plug-to-plug efficiency at 230 VAC.

Summary

In this paper, I presented the complete design of a 2-kW TI module prototype. The module employs a master/slave parallel architecture suitable for lead-acid and Lithium-ion battery charging as well as redundant telecommunications applications. The typical master/slave configuration is one master and N-1 slaves, with the capability to work up to as many as 10 modules in parallel.

The firmware is also flexible to configure the system as a single module, with several master/slave boards sharing a single human interface or different modules, each one equipped with an LCD and pushbuttons.

Ultimately, I built and tested two modules, and the parallel structure was effective in showing an imbalance of ±1 percent maximum. This architecture has additional applications and is ideal for further development – for example, featuring automatic master/slave assignment if the master fails would improve reliability. A three-phase connection is also possible, but only if providing a neutral mains conductor.

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