16-Bit, 200-kSPS, Low-Power, Sampling ANALOG-TO-DIGITAL CONVERTER with Internal Reference and Parallel/Serial Interface

FEATURES

- 200-kHz Minimum Sampling Rate
- 4-V, 5-V, and ±10-V Input Ranges with High-Impedance Input
- ±1.5 LSB Max INL
- +1.5/–1 LSB Max/Min DNL, 16 Bits NMC
- ±2-mV Max BPZ, ±0.6 ppm/°C BPZ Drift
- ±2-mV Max UPZ, ±0.15 ppm/°C UPZ Drift
- 88.8-dB SINAD with 10-kHz Input
- SPI™-Compatible Serial Output With Daisy-Chain (TAG), SPI Master/Slave Feature
- Full Parallel Interface
- Binary Twos Complement or Straight Binary Output Code Formats
- Single 4.5-V to 5.5-V Analog Supply, 1.65-V to 5.5-V Interface Supply
- Uses Internal 2.5-V or External Reference
- No External Precision Resistors Required
- Low Power Dissipation (ADC+REF+BUF):
  - 47 mW Typ, 60 mW Max at 200 kSPS
- 50-µW Max Power-Down Mode
- Pin-Compatible with 16-Bit ADS7807 and ADS8507, and 12-Bit ADS7806 and ADS8506
- SO-28 and TSSOP-28 Packages

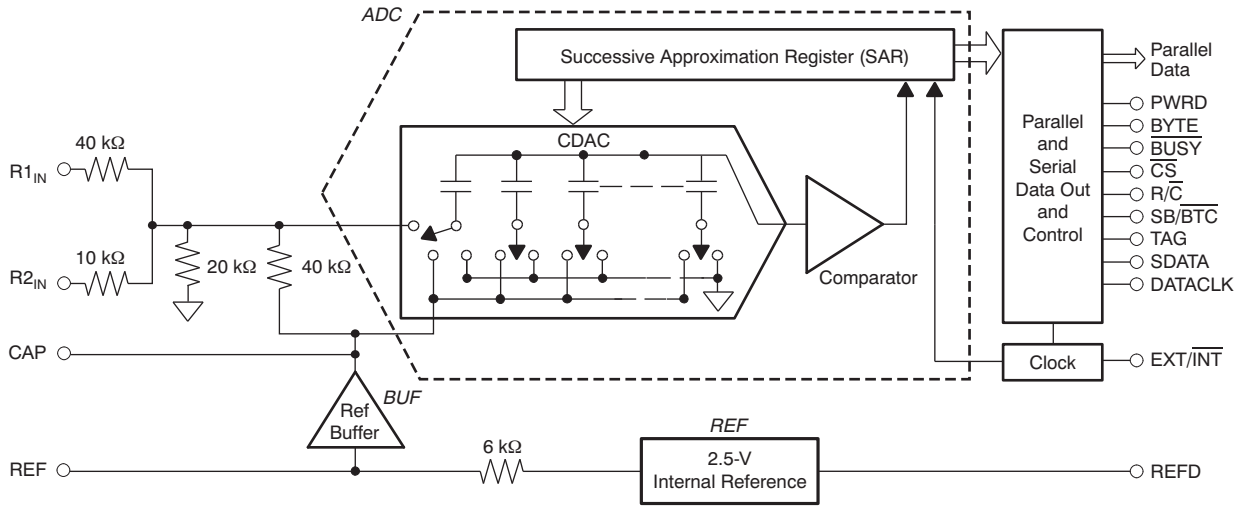
APPLICATIONS

- Portable Test Equipment
- USB Data Acquisition Module
- Medical Equipment
- Industrial Process Control
- Digital Signal Processing
- Instrumentation

DESCRIPTION

The ADS8517 is a complete low-power, single 5-V supply, 16-bit sampling analog-to-digital (A/D) converter. It contains a complete, 16-bit, capacitor-based, successive approximation register (SAR) A/D converter with sample-and-hold, clock, reference, and data interface. The converter can be configured for a variety of input ranges including ±10 V, 4 V, and 5 V. For most input ranges, the input voltage can swing to 25 V or –25 V without damage to the device.

An SPI-compatible serial interface allows data to be synchronized to an internal or external clock. A full parallel interface using the selectable BYTE pin is also provided to allow the maximum system design flexibility. The ADS8517 is specified at a 200-kHz sampling rate over the industrial –40°C to +85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	NO MISSING CODE	MINIMUM SINAD (dB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8517IB	±1.5	16	87	-40°C to +85°C	SO-28	DW	ADS8517IBDW	Tube, 20
							ADS8517IBDWR	Tape and Reel, 1000
					TSSOP-28	PW	ADS8517IBPW	Tube, 50
							ADS8517IBPWR	Tape and Reel, 2000
ADS8517I	±3	15	85	-40°C to +85°C	SO-28	DW	ADS8517IDW	Tube, 20
							ADS8517IDWR	Tape and Reel, 1000
					TSSOP-28	PW	ADS8517W	Tube, 50
							ADS8517IPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Over operating free-air temperature range (unless otherwise noted).

		UNIT
Analog inputs	$R1_{IN}$	±25 V
	$R2_{IN}$	±25 V
	REF	$+V_{ANA}$ + 0.3 V to AGND2 – 0.3 V
Ground voltage differences	DGND, AGND2	±0.3 V
	V_{ANA}	6 V
	V_{DIG} to V_{ANA}	0.3 V
	V_{DIG}	6 V
Digital inputs		-0.3 V to $+V_{DIG}$ + 0.3 V
Maximum junction temperature		+165°C
Storage temperature range		–65°C to +150°C
Internal power dissipation		700 mW

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = -40°C to +85°C, f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (see Figure 39), unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS8517I			ADS8517IB(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				16			16	Bits
ANALOG INPUT								
Voltage ranges	See Table 1	–10		10	–10		10	V
		0		5	0		5	
		0		4	0		4	
Impedance		See Table 1						
Capacitance			45			45		pF

(1) Shaded cells indicate different specifications for high-grade version of the device.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = -40°C to +85°C, f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (see Figure 39), unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8517I			ADS8517IB(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THROUGHPUT SPEED									
	Conversion time				2.5			2.5	µs
	Complete cycle	Acquire and convert			5			5	µs
	Throughput rate		200			200			kHz
DC ACCURACY									
INL	Integral linearity error		–3		3	–1.5		1.5	LSB(2)
DNL	Differential linearity error		–2		3	–1		1.5	LSB
	No missing codes		15			16			Bits
	Transition noise(3)			0.9			0.8		LSB
	Gain error			±0.2			±0.1		%
	Full-scale error(4)	Internal reference	–0.75		0.75	–0.75		0.75	%
		External 2.5-V reference	–0.75		0.75	–0.75		0.75	%
	Full-scale error drift	Internal reference		±9			±9		ppm/°C
		External 2.5-V reference		±1			±1		ppm/°C
BPZ	Bipolar zero error	±10 V range	–5	±1	5	–2	±1	2	mV
	Bipolar zero error drift	±10 V range		±0.6			±0.6		ppm/°C
UPZ	Unipolar zero error	0 V to 5 V, 0 V to 4 V ranges	–3	±0.1	3	–2	±0.1	2	mV
	Unipolar zero error drift	0 V to 5 V, 0 V to 4 V ranges		±0.15			±0.15		ppm/°C
	Recovery time to rated accuracy from power down(5)	2.2-µF capacitor to CAP		1			1		ms
	Power-supply sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75 V < V_{ANA} < +5.25 V	–8		+8	–6		+6	LSB
		+4.5 V < V_{ANA} < +5.5 V	–20		+20	–12		+12	
AC ACCURACY									
SFDR	Spurious-free dynamic range	f_{IN} = 10 kHz, ±10 V	92	100		96	101		dB(6)
THD	Total harmonic distortion	f_{IN} = 10 kHz, ±10 V		–97	–92		–98	–95	dB
SINAD	Signal-to-(noise+distortion)	f_{IN} = 10 kHz, ±10 V	85	88		87	88.5		dB
		–60 dB Input		29			29		
SNR	Signal-to-noise ratio	f_{IN} = 10 kHz, ±10 V	85	88		88	89		dB
	SNR usable bandwidth(7)	f_{IN} = 10 kHz, ±10 V		130			130		kHz
	SNR full-power bandwidth (–3 dB)	f_{IN} = 10 kHz, ±10 V		600			600		kHz
SAMPLING DYNAMICS									
	Aperture delay			40			40		ns
	Aperture jitter			20			20		ps
	Transient response	FS step			5			5	µs
	Overvoltage recovery(8)			750			750		ns

(2) LSB means Least Significant Bit. One LSB for the ±10 V input range is 305 µV.
(3) Typical rms noise at worst-case transitions.
(4) Full-scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) This is the time delay after the ADS8517 is brought out of Power-Down mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert command after this delay will yield accurate results.
(6) All specifications in dB are referred to a full-scale input.
(7) Usable bandwidth defined as full-scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60 dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = -40°C to +85°C, f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (see Figure 39), unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8517I			ADS8517IB(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE									
	Internal reference voltage	No load	2.48	2.5	2.52	2.48	2.5	2.52	V
	Internal reference source current (must use external buffer)			1			1		µA
	Internal reference drift			8			8		ppm/°C
	External reference voltage range for specified linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
	External reference current drain	External 2.5-V reference			100			100	µA
DIGITAL INPUTS									
V_{IL}	Low-level input voltage(9)	V_{DIG} = 1.65 V to 5.5 V	–0.3		0.6	–0.3		0.6	V
V_{IH}	High-level input voltage(9)	V_{DIG} = 1.65 V to 5.5 V	0.5 x V_{DIG}		V_{DIG} + 0.3	0.5 x V_{DIG}		V_{DIG} + 0.3	V
I_{IL}	Low-level input current	V_{IL} = 0 V			±10			±10	µA
I_{IH}	High-level input current	V_{IH} = 5 V			±10			±10	µA
DIGITAL OUTPUTS									
	Data format - Parallel 16-bits in 2-bytes, Serial								
	Data coding - Binary twos complement or straight binary								
V_{OL}	Low-level output voltage	I_{SINK} = 1.6mA, V_{DIG} = 1.65V to 5.5V			0.45			0.45	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500µA, V_{DIG} = 1.65V to 5.5V	V_{DIG} – 0.45			V_{DIG} – 0.45			V
	Leakage current	High-Z state, V_{OUT} = 0 V to V_{DIG}			±5			±5	µA
	Output capacitance	High-Z state			15			15	pF
DIGITAL TIMING									
	Bus access time	R_L = 3.3 kΩ, C_L = 50 pF			83			83	ns
	Bus relinquish time	R_L = 3.3 kΩ, C_L = 10 pF			83			83	ns
POWER SUPPLIES									
V_{DIG}	Interface voltage		1.65	1.8	5.5	1.65	1.8	5.5	V
V_{ANA}	ADC core voltage		4.5	5	5.5	4.5	5	5.5	V
I_{DIG}	Interface current	V_{DIG} = 5 V		0.3			0.3		mA
I_{ANA}	ADC core current	V_{ANA} = 5 V		9			9		mA
	Power dissipation	V_{ANA} = V_{DIG} = 5 V, f_S = 200 kHz		47	60		47	60	mW
		REFD high with BUF on		42			42		mW
		PWRD and REFD high		50			50		µW
TEMPERATURE RANGE									
	Specified performance		–40		+85	–40		+85	°C
	Derated performance		–55		+125	–55		+125	°C
	Storage temperature		–65		+150	–65		+150	°C
θ_{JA}	Thermal impedance	TSSOP		62			62		°C/W
		SO		46			46		

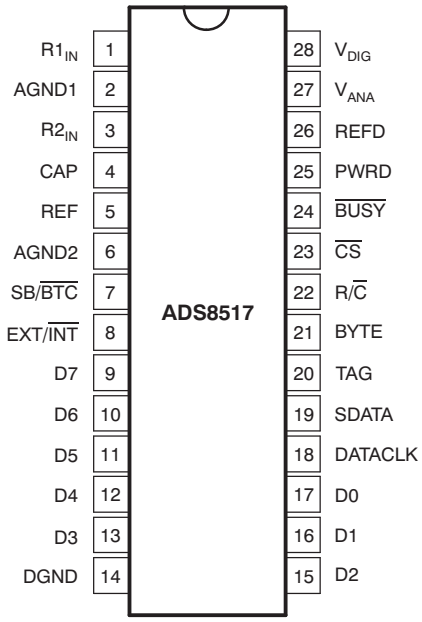
(9) TTL-compatible at 5V supply.

Table 1. Analog Input Range Connections (see Figure 38 and Figure 39)

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200 Ω TO	CONNECT $R2_{IN}$ VIA 100 Ω TO	IMPEDANCE
±10 V	V_{IN}	CAP	45.7 kΩ
0 V to 5 V	AGND	V_{IN}	20.0 kΩ
0 V to 4 V	V_{IN}	V_{IN}	21.4 kΩ

PIN CONFIGURATION

DW, PW PACKAGES
SO-28, TSSOP-28
(TOP VIEW)



PIN ASSIGNMENTS

PIN		DIGITAL I/O	DESCRIPTION
NAME	NO.		
$R1_{IN}$	1		Analog Input.
AGND1	2		Analog sense ground. Used internally as ground reference point. Minimal current flow
$R2_{IN}$	3		Analog Input.
CAP	4		Reference buffer output. 2.2-µF tantalum capacitor to ground.
REF	5		Reference input/output. Outputs internal 2.5-V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2-µF tantalum capacitor.
AGND2	6		Analog ground
SB/$\overline{BTC}$	7	I	Output mode select. Selects straight binary or binary twos complement for output data format. If high, data are output in a straight binary format. If low, data are output in a binary twos complement format.
EXT/$\overline{INT}$	8	I	External/internal data select. Selects external/internal data clock for transmitting data. If high, data is output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 16-clock pulses output on DATACLK.
D7	9	O	Data bit 7 if BYTE is high. Data bit 15 (MSB) if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low. Leave unconnected when using serial output.
D6	10	O	Data bit 6 if BYTE is high. Data bit 14 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
D5	11	O	Data bit 5 if BYTE is high. Data bit 13 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
D4	12	O	Data bit 4 if BYTE is high. Data bit 12 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
D3	13	O	Data bit 3 if BYTE is high. Data bit 11 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
DGND	14		Digital ground
D2	15	O	Data bit 2 if BYTE is high. Data bit 10 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
D1	16	O	Data bit 1 if BYTE is high. Data bit 9 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
D0	17	O	Data bit 0 (LSB) if BYTE is high. Data bit 8 if BYTE is low. High-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.

PIN ASSIGNMENTS (continued)

DATACLK	18	I/O	Data clock. Either an input or an output, depending on the EXT/$\overline{INT}$ level. Output data are synchronized to this clock. If EXT/$\overline{INT}$ is low, DATACLK transmits 16 pulses after each conversion, and then remains low between conversions.
SDATA	19	O	Serial data output. Data are synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16 bits of data, the ADC outputs the level input on TAG as long as $\overline{CS}$ is low and R/$\overline{C}$ is high. If EXT/$\overline{INT}$ is low, data are valid on both the rising and falling edges of DATACLK, and between conversions SDATA stays at the level of the TAG input when the conversion was started.
TAG	20	I	Tag input for use in the external clock mode. If EXT is high, digital data input from TAG is output on DATA with a delay that depends on the external clock mode.
BYTE	21	I	Byte select. Selects the eight most significant bits (low) or eight least significant bits (high) on parallel output pins.
R/$\overline{C}$	22	I	Read/convert input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold circuit into the hold state and starts a conversion. With EXT/$\overline{INT}$ is low, the transmission of the data results from the previous conversion is initiated.
$\overline{CS}$	23	I	Chip select. Internally ORed with R/$\overline{C}$. If R/$\overline{C}$ is low, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is low, this same falling edge will start the transmission of serial data results from the previous conversion.
$\overline{BUSY}$	24	O	Busy output. At the start of a conversion, $\overline{BUSY}$ goes low and stays low until the conversion is completed and the digital outputs have been updated.
PWRD	25	I	Power-down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
REFD	26	I	Reference disable. REFD high shuts down the internal reference. The external reference is required for conversions.
V_{ANA}	27		ADC core supply. Nominally +5 V. Decouple with 0.1-μF ceramic and 10-μF tantalum capacitors.
V_{DIG}	28		I/O supply. Nominally +1.8 V.

TYPICAL CHARACTERISTICS

At f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference (see Figure 39), unless otherwise specified.

POWER-SUPPLY CURRENT vs FREE-AIR TEMPERATURE

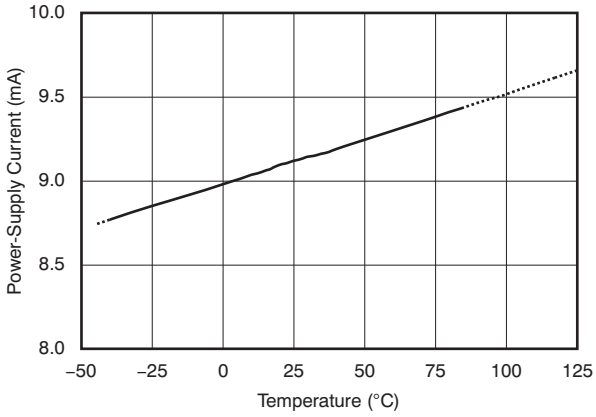


Figure 1.

INTERNAL REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

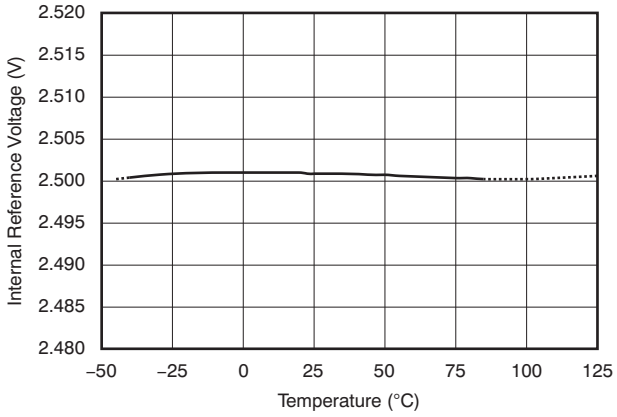


Figure 2.

POWER-SUPPLY CURRENT vs SAMPLING FREQUENCY

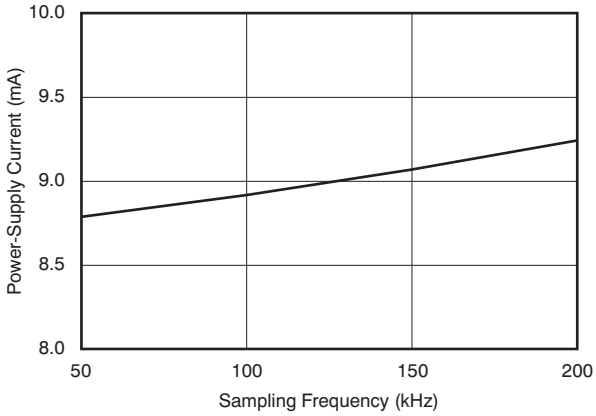


Figure 3.

BIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

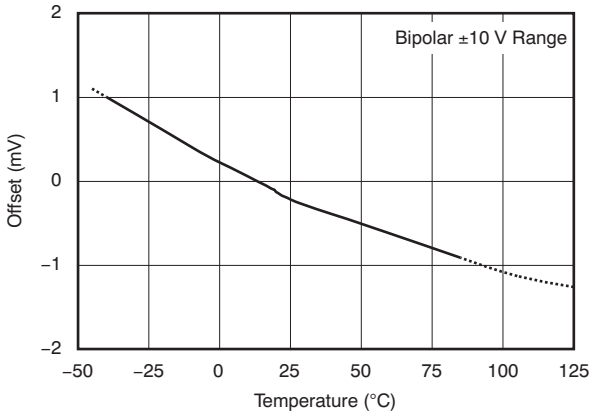


Figure 4.

BIPOLAR POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

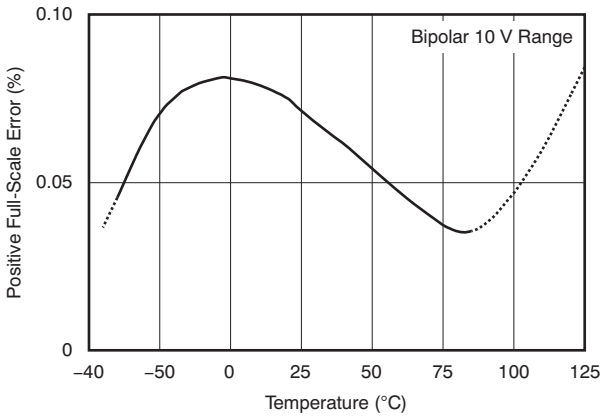


Figure 5.

BIPOLAR NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

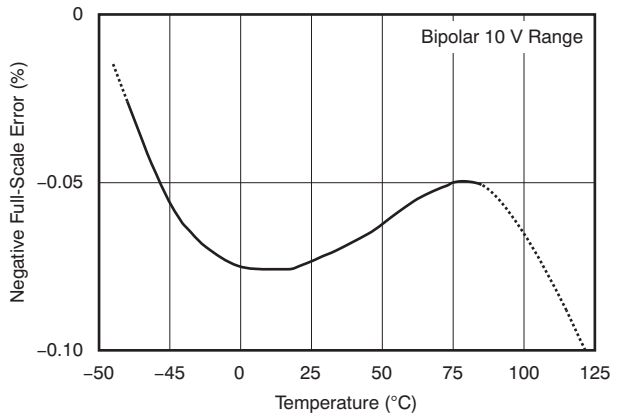


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference (see Figure 39), unless otherwise specified.

UNIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

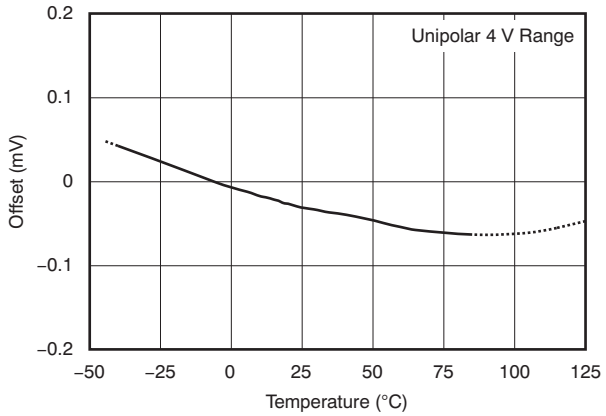


Figure 7.

UNIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

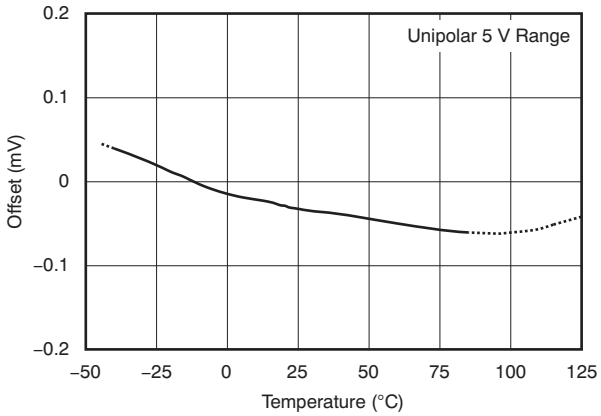


Figure 8.

UNIPOLAR FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

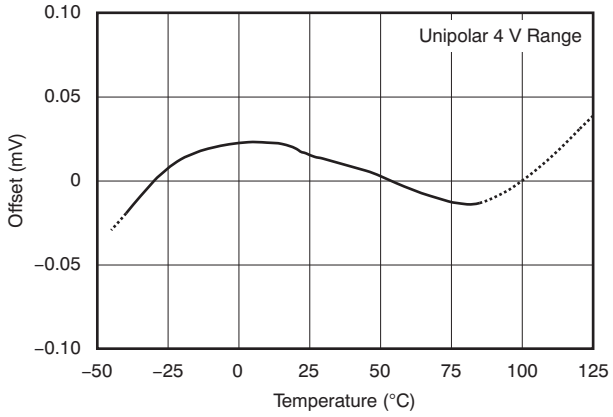


Figure 9.

UNIPOLAR FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

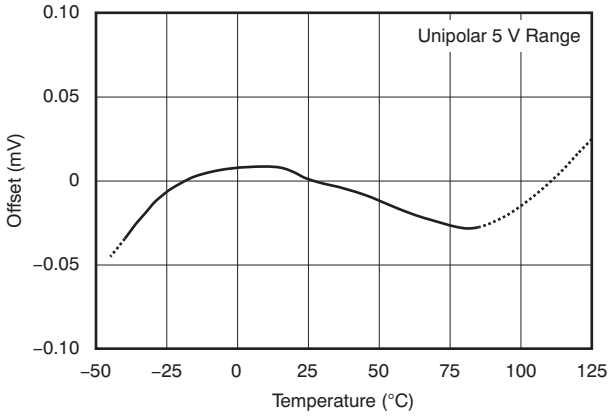


Figure 10.

AC PARAMETERS vs FREE-AIR TEMPERATURE

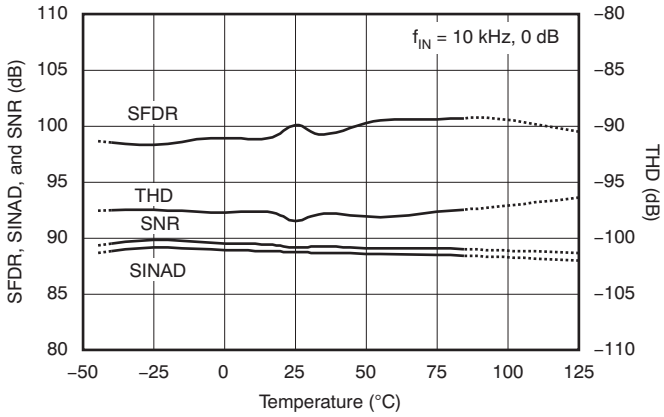


Figure 11.

SIGNAL-TO-(NOISE+DISTORTION) vs FREE-AIR TEMPERATURE

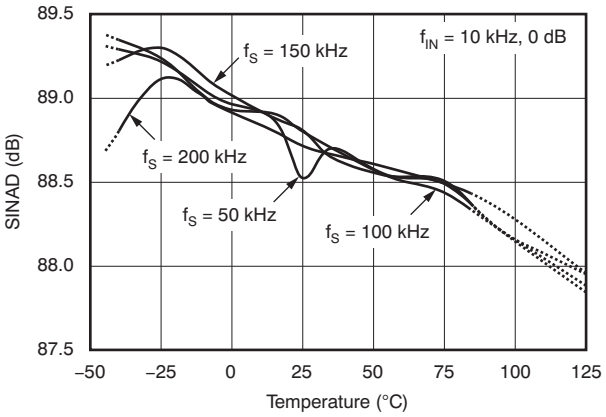


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference (see Figure 39), unless otherwise specified.

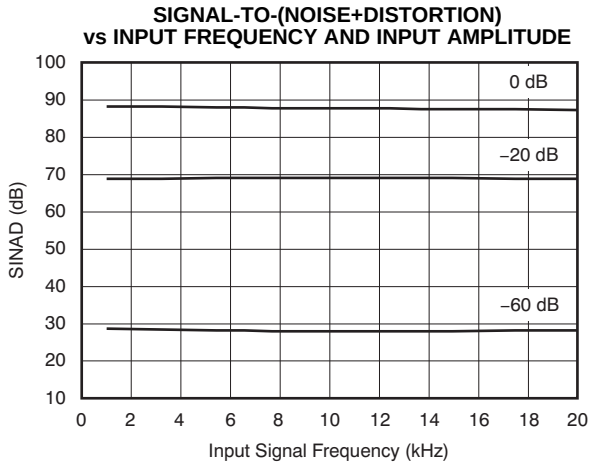


Figure 13.

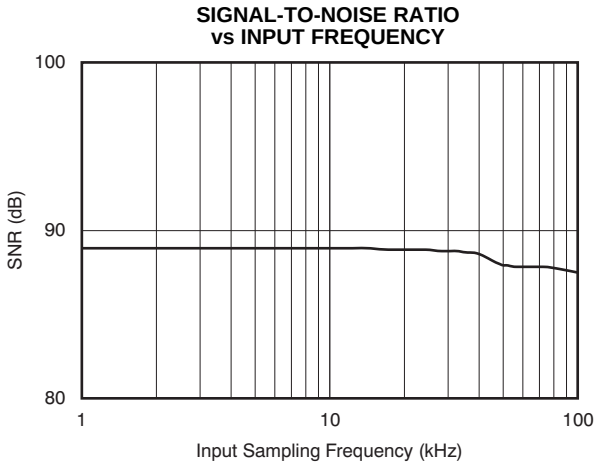


Figure 14.

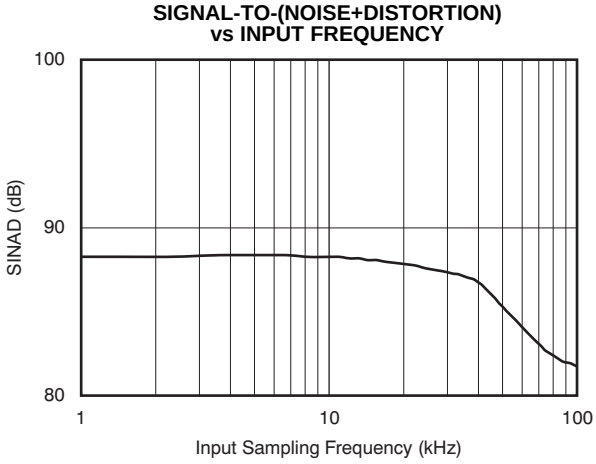


Figure 15.

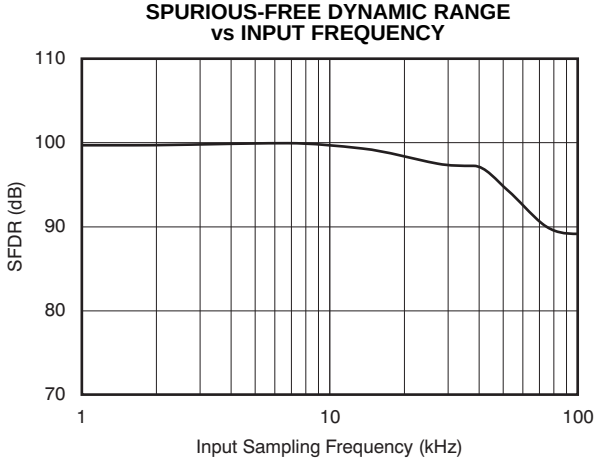


Figure 16.

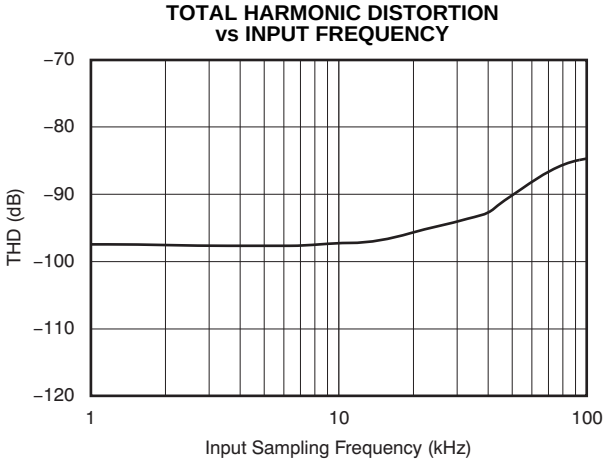


Figure 17.

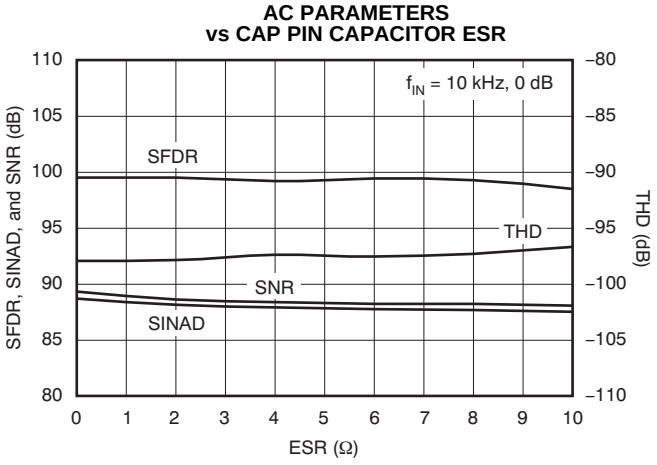


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference (see Figure 39), unless otherwise specified.

AC PARAMETERS vs POWER-SUPPLY VOLTAGE

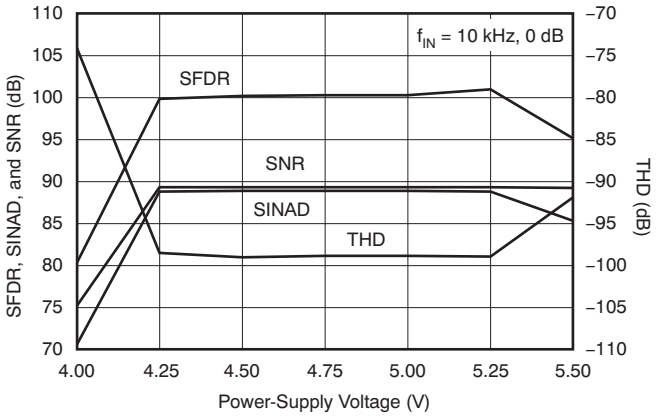


Figure 19.

OUTPUT REJECTION vs POWER-SUPPLY RIPPLE FREQUENCY

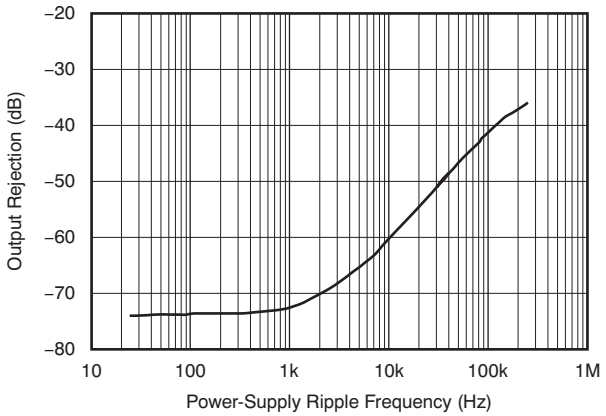


Figure 20.

CONVERSION TIME vs FREE-AIR TEMPERATURE

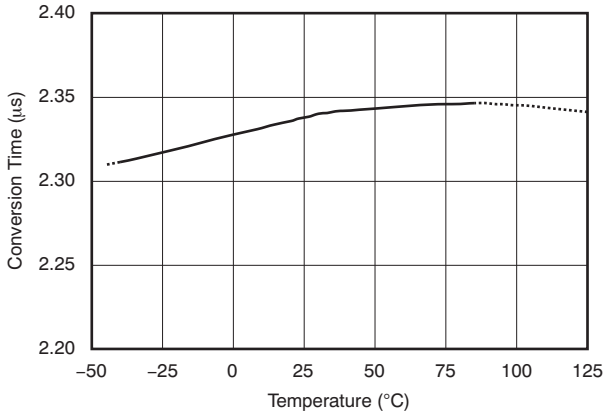


Figure 21.

INTEGRAL LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs POWER-SUPPLY VOLTAGE

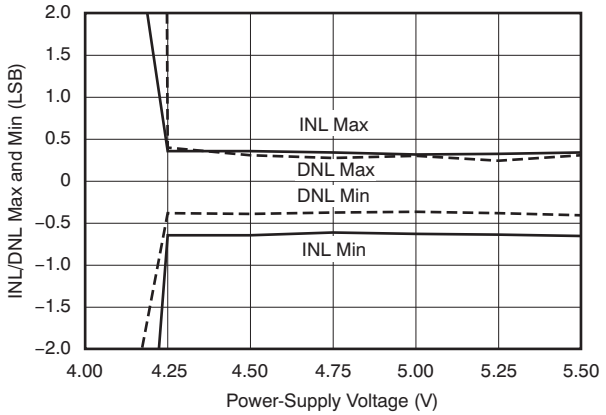


Figure 22.

INTEGRAL LINEARITY ERROR

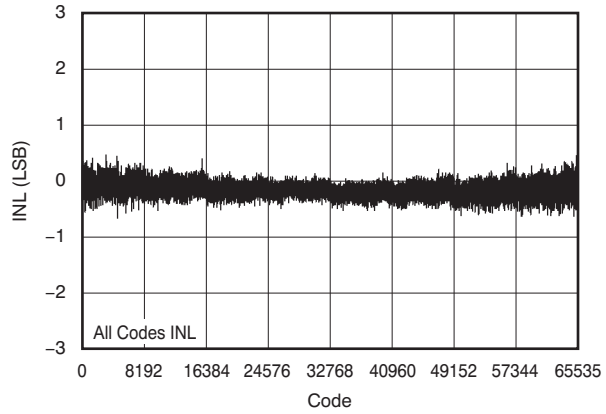


Figure 23.

DIFFERENTIAL LINEARITY ERROR

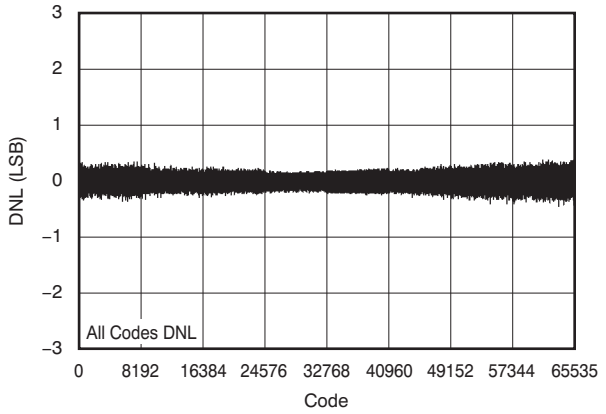


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At f_S = 200 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference (see Figure 39), unless otherwise specified.

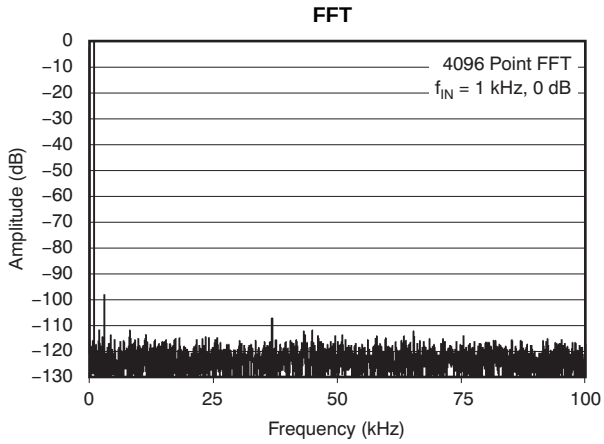


Figure 25.

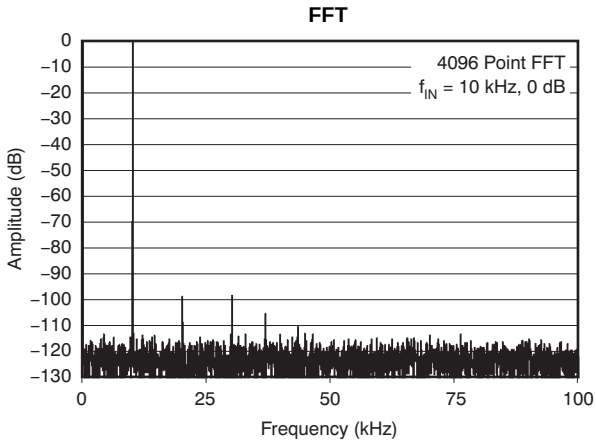


Figure 26.

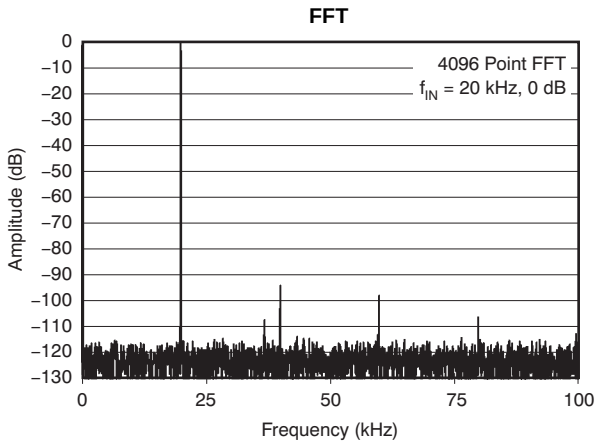


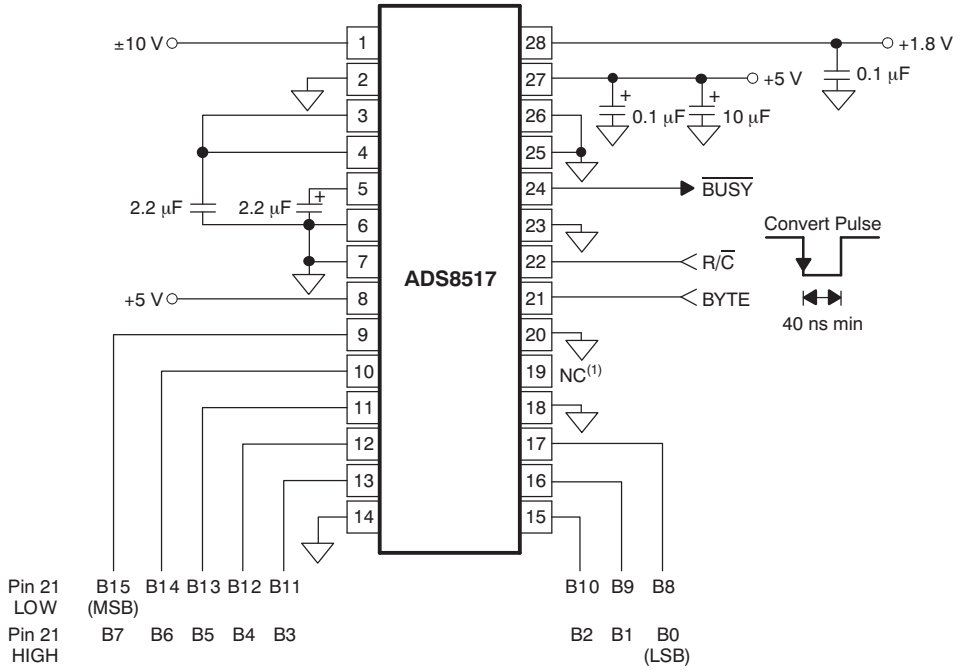
Figure 27.

BASIC OPERATION

PARALLEL OUTPUT

Figure 28 shows a basic circuit for operating the ADS8517 with a ±10-V input range and parallel output. Taking R/$\overline{C}$ (pin 22) low for a minimum of 40 ns (5 µs max) initiates a conversion. $\overline{BUSY}$ (pin 24) goes low and stays low until the conversion completes and the output register updates. If BYTE (pin 21) is low, the eight most significant bits (MSBs) will be valid when $\overline{BUSY}$ rises; if BYTE is high, the eight least significant bits (LSBs) will be valid when $\overline{BUSY}$ rises. Data are output in binary twos complement (BTC) format. $\overline{BUSY}$ going high can be used to latch the data. After the first byte has been read, BYTE can be toggled, allowing the remaining byte to be read. All convert commands are ignored while $\overline{BUSY}$ is low.

The ADS8517 begins tracking the input signal at the end of the conversion. Allowing 5 µs between convert commands assures accurate acquisition of a new signal.



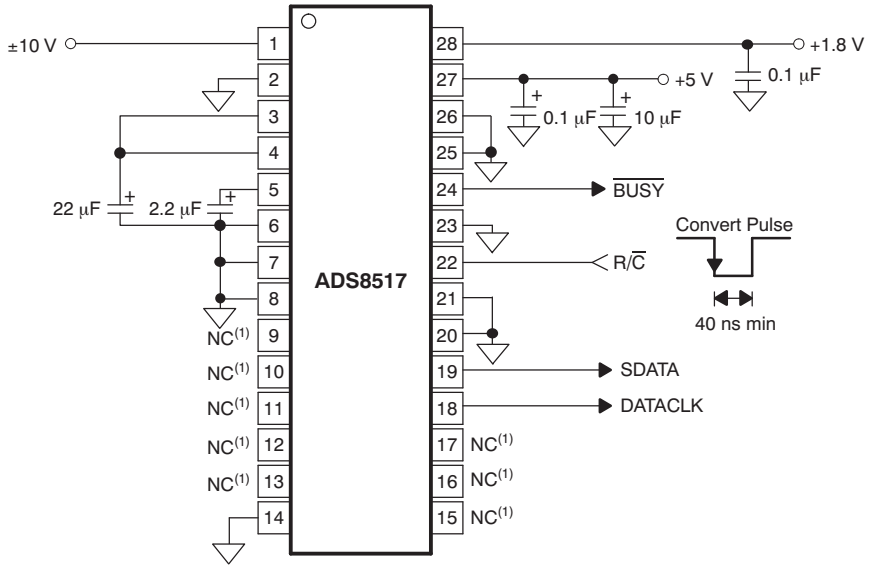
NOTE: (1) NC = not connected.

Figure 28. Basic ±10-V Operation, Both Parallel and Serial Output

SERIAL OUTPUT

Figure 29 shows a basic circuit to operate the ADS8517 with a ±10-V input range and serial output. Taking R/$\overline{C}$ (pin 22) low for 40 ns (5 μs max) initiates a conversion and outputs valid data from the previous conversion on SDATA (pin 19) synchronized to 16 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) goes low and stays low until the conversion completes and the serial data have been transmitted. Data are output in BTC format, MSB first, and are valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going high can be used to latch the data. All convert commands are ignored while $\overline{BUSY}$ is low.

The ADS8517 begins tracking the input signal at the end of the conversion. Allowing 5 μs between convert commands assures accurate acquisition of a new signal.



NOTE: (1) NC = not connected.

Figure 29. Basic ±10-V Operation with Serial Output

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) held low for a minimum of 40 ns puts the sample-and-hold of the ADS8517 in the hold state and starts conversion *N*. $\overline{BUSY}$ (pin 24) goes low and stays low until conversion *N* completes and the internal output register has been updated. All new convert commands received while $\overline{BUSY}$ is low are ignored.

The ADS8517 begins tracking the input signal at the end of the conversion. Allowing 5 µs between convert commands assures accurate acquisition of a new signal. Refer to Table 2 and Table 3 for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states, and Figure 30 through Figure 36 for timing diagrams.

Table 2. Control Functions When Using Parallel Output (DATACLK Tied Low, EXT/$\overline{INT}$ Tied High)

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Data bus is in High-Z state.
↓	0	1	Initiates conversion *N*. Data bus remains in High-Z state.
0	↓	1	Initiates conversion *N*. Data bus enters High-Z state.
0	1	↑	Conversion *N* completed. Valid data from conversion *N* on the data bus.
↓	1	1	Enables data bus with valid data from conversion *N*.
↓	1	0	Enables data bus with valid data from conversion *N–1*(1). Conversion *N* in progress.
0	↑	0	Enables data bus with valid data from conversion *N–1*(1). Conversion *N* in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data are invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be high when $\overline{BUSY}$ goes high.
X	X	0	New convert commands ignored. Conversion *N* in progress.

(1) See Figure 30 and Figure 31 for constraints on data valid from conversion N–1.

$\overline{CS}$ and R/$\overline{C}$ are internally ORed and level-triggered. It does not matter which input goes low first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion *N*, be sure the less critical input is low at least t_{su2} ≥ 10 ns before the initiating input. If EXT/$\overline{INT}$ (pin 8) is low when initiating conversion *N*, serial data from conversion *N–1* is output on SDATA (pin 19) following the start of conversion *N*. See *Internal Data Clock* in the Reading Data section for more information.

To reduce the number of control pins, $\overline{CS}$ can be tied low using R/$\overline{C}$ to control the read and convert modes. This configuration has no effect when using the internal data clock in the serial output mode. However, when using an active external data clock, the parallel and serial outputs are affected whenever R/$\overline{C}$ goes high; refer to the *Reading Data* section for more information. In the internal clock mode, data are clocked out every convert cycle regardless of the states of $\overline{CS}$ and R/$\overline{C}$. The conversion result is available as soon as BUSY returns to high. Therefore, data always represent the previously-completed conversion, even when read during a conversion.

READING DATA

The ADS8517 outputs serial or parallel data in straight binary (SB) or binary twos complement data output format. If SB/$\overline{BTC}$ (pin 7) is high, the output is in SB format; if it is low, the output is in BTC format. Refer to Table 4 for the ideal output codes. The first conversion immediately following a power-up does not produce a valid conversion result.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial port shifts the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port before reading the same data on the serial port, but data cannot be read through the serial port before reading the same data on the parallel port.

Table 3. Control Functions When Using Serial Output(1)

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion *N*. Valid data from conversion *N–1* clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion *N*. Valid data from conversion *N–1* clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion *N*. Internal clock still runs conversion process.
0	↓	1	1		Initiates conversion *N*. Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion *N* completed. Valid data from conversion *N* clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion *N–1* output on SDATA synchronized to external data clock. Conversion *N* in progress.
0	↑	0	1	Input	Valid data from conversion *N–1* output on SDATA synchronized to external data clock. Conversion *N* in progress.
0	0	↑	X	Input	New conversion initiated without acquisition of a new signal. Data are invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be high when $\overline{BUSY}$ goes high.
X	X	0	X	X	New convert commands ignored. Conversion *N* in progress..

(1) See Figure 34, Figure 35, and Figure 36 for constraints on data valid from conversion *N–1*.

Table 4. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWOS COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-scale range	±10	0 V to 5 V	0 V to 4 V				
Least significant bit (LSB)	305 µV	76 µV	61 µV	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full-scale (FS – 1LSB)	9.999695 V	4.999924 V	3.999939 V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0 V	2.5 V	2 V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
1 LSB below midscale	305 µV	2.499924 V	1.999939 V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full-scale	-10 V	0 V	0 V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

Parallel Output

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) high and DATACLK (pin 18) low. SDATA (pin 19) should be left unconnected. The parallel output is active when R/$\overline{C}$ (pin 22) is high and $\overline{CS}$ (pin 23) is low. Any other combination of $\overline{CS}$ and R/$\overline{C}$ 3-states the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17). When BYTE (pin 21) is low, the eight most significant bits are valid with the MSB on D7. When BYTE is high, the eight least significant bits are valid with the LSB on D0. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial device power-up, the parallel output contains indeterminate data.

Parallel Output (After a Conversion)

After conversion *N* is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) goes high. Valid data from conversion *N* are available on D7-D0 (pin 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table 5, Figure 30, and Figure 31 for timing specifications.

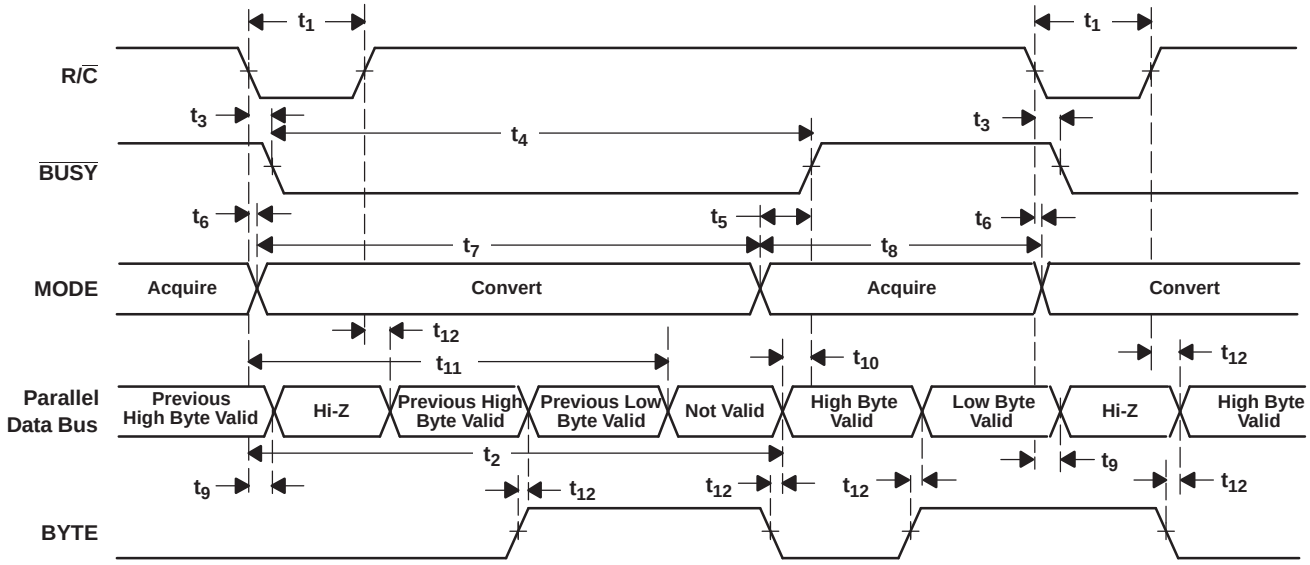


Figure 30. Conversion Timing With Parallel Output ($\overline{CS}$ and DATACLK Tied Low, EXT/INT Tied High)

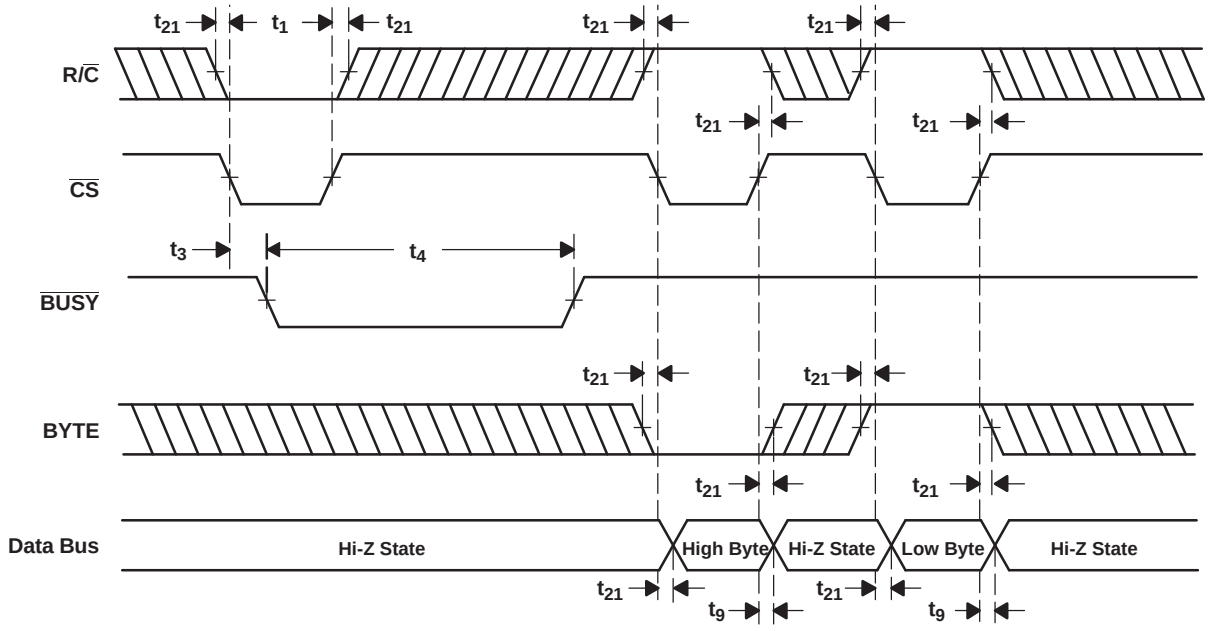


Figure 31. $\overline{CS}$ to Control Conversion and Read Timing With Parallel Outputs

Parallel Output (During a Conversion)

After conversion *N* has been initiated, valid data from conversion *N–1* can be read and are valid up to 2.2 µs after the start of conversion *N*. Do not attempt to read data beyond 2.2 µs after the start of conversion *N* until $\overline{BUSY}$ (pin 24) goes high; doing so may result in reading invalid data. Refer to Table 5, Figure 30, and Figure 31 for timing constraints.

Table 5. Conversion and Data Timing with Parallel Interface at T_A = –40°C to +85°C

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert pulse width	0.04		5	µs
t_2	Data valid delay after R/$\overline{C}$ low		2.3	2.5	µs
t_3	$\overline{BUSY}$ delay from start of conversion		20	85	ns
t_4	$\overline{BUSY}$ low		2.3	2.5	µs
t_5	$\overline{BUSY}$ delay after end of conversion		90		ns
t_6	Aperture delay		40		ns
t_7	Conversion time	1.8	2.2		µs
t_8	Acquisition time		2.7		µs
t_9	Bus relinquish time	10		83	ns
t_{10}	$\overline{BUSY}$ delay after data valid	20	60		ns
t_{11}	Previous data valid after start of conversion	1.8	2.2		µs
t_{21}	R/$\overline{C}$ to $\overline{CS}$ setup time	10			ns
$t_7 + t_8$	Throughput time			5	µs

Serial Output

Data can be clocked out with the internal data clock or an external data clock. When using the serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), because these pins come out of a High-Z state whenever $\overline{CS}$ (pin 23) is low and R/$\overline{C}$ (pin 22) is high. The serial output cannot be 3-stated and is always active. Refer to the *Applications Information* section for specific serial interfaces. If an external clock is used, the TAG input can be used to daisy-chain multiple ADS8517 data pins together.

Internal Data Clock (During a Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) low. The combination of R/$\overline{C}$ (pin 22) and $\overline{CS}$ (pin 23) low initiates conversion *N* and activates the internal data clock (typically, a 900-kHz clock rate). The ADS8517 outputs 16 bits of valid data, MSB first, from conversion *N–1* on SDATA (pin 19), synchronized to 16 clock pulses output on DATACLK (pin 18). The data are valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 16th clock pulse, DATACLK remains low until the next conversion is initiated, while SDATA returns to the state of the TAG pin input sensed at the start of transmission. Refer to Table 6 and Figure 33 for more information.

External Data Clock

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) high. The external data clock is not and cannot be synchronized with the internal conversion clock; care must be taken to avoid corrupting the data. To enable the output mode of the ADS8517, $\overline{CS}$ (pin 23) must be low and R/$\overline{C}$ (pin 22) must be high. DATACLK must be high for 20% to 70% of the total data clock period; the clock rate can be between dc and 10 MHz. Serial data from conversion *N* can be output on SDATA (pin 19) after conversion *N* completes or during conversion *N+1*.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ low and use R/$\overline{C}$ to initiate conversions.

While this configuration is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12 μs after the start of conversion *N* until $\overline{BUSY}$ rises, the internal logic shifts the results of conversion *N* into the output register. If $\overline{CS}$ is low, R/$\overline{C}$ high, and the external clock is high at this point, data are lost. Consequently, with $\overline{CS}$ low, either R/$\overline{C}$ and/or DATACLK must be low during this period to avoid losing valid data.

External Data Clock (After a Conversion)

After conversion *N* is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) goes high. With $\overline{CS}$ low and R/$\overline{C}$ high, valid data from conversion *N* are output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB is valid on the first falling edge and the second rising edge of the external data clock. The LSB is valid on the 16th falling edge and 17th rising edge of the data clock. TAG (pin 20) inputs a bit of data for every external clock pulse. The first bit input on TAG is valid on SDATA on the 17th falling edge and the 18th rising edge of DATACLK; the second input bit is valid on the 18th falling edge and the 19th rising edge, etc. With a continuous data clock, TAG data is output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table 6 and Figure 35 for more information.

External Data Clock (During a Conversion)

After conversion *N* has been initiated, valid data from conversion *N–1* can be read and are valid up to 2.2 μs after the start of conversion *N*. Do not attempt to clock out data from 2.2 μs after the start of conversion *N* until BUSY (pin 24) rises; doing so results in data loss.

NOTE:

For the best possible performance when using an external data clock, data should not be clocked out during a conversion.

The switching noise of the asynchronous data clock can cause digital feedthrough, degrading converter performance. Refer to Table 6 and Figure 36 for more information.

Table 6. Timing Requirements (T_A = –40°C to +85°C)

PARAMETER		MIN	TYP	MAX	UNIT
t_{w1}	Pulse duration, convert	0.04		5	µs
t_{d1}	Delay time, $\overline{BUSY}$ from R/$\overline{C}$ low		20	85	ns
t_{w2}	Pulse duration, $\overline{BUSY}$ low		2.3	2.5	µs
t_{d2}	Delay time, $\overline{BUSY}$, after end of conversion		90		ns
t_{d3}	Delay time, aperture		40		ns
t_{conv}	Conversion time	2.0	2.2	2.4	µs
t_{acq}	Acquisition time	2.6	2.7		µs
$t_{conv} + t_{acq}$	Cycle time			5	µs
t_{d4}	Delay time, R/$\overline{C}$ low to internal DATACLK output		171		ns
t_{c1}	Cycle time, internal DATACLK	92	96	98	ns
t_{d5}	Delay time, data valid to internal DATACLK high	2	3.5		ns
t_{d6}	Delay time, data valid after internal DATACLK low	41	43		ns
t_{c2}	Cycle time, external DATACLK	35			ns
t_{w3}	Pulse duration, external DATACLK high	15			ns
t_{w4}	Pulse duration, external DATACLK low	15			ns
t_{su1}	Setup time, R/$\overline{C}$ rise/fall to external DATACLK high	15			ns
t_{su2}	Setup time, R/$\overline{C}$ transition to $\overline{CS}$ transition	10			ns
t_{d8}	Delay time, data valid from external DATCLK high	2	25	40	ns
t_{d9}	Delay time, $\overline{CS}$ rising edge to external DATACLK rising edge	15			ns
t_{d10}	Delay time, previous data available after $\overline{CS}$, R/$\overline{C}$ low	1.8	2.2		µs
t_{su3}	Setup time, $\overline{BUSY}$ transition to first external DATACLK	5			ns
t_{d11}	Delay time, final external DATACLK to $\overline{BUSY}$ rising edge	825			ns
t_{su4}	Setup time, TAG valid before rising edge of DATACLK	2			ns
t_{h1}	Hold time, TAG valid after rising edge of DATACLK	2			ns

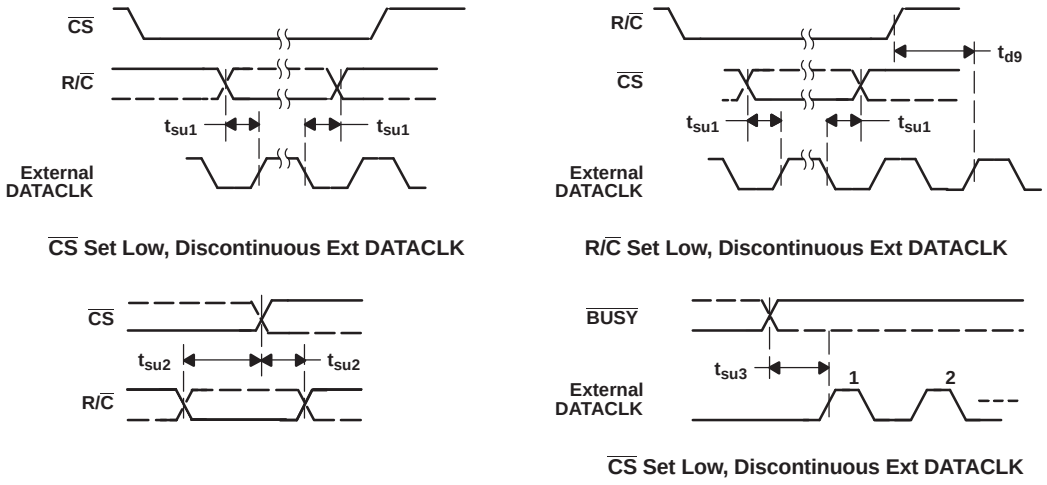


Figure 32. Critical Timing Parameters

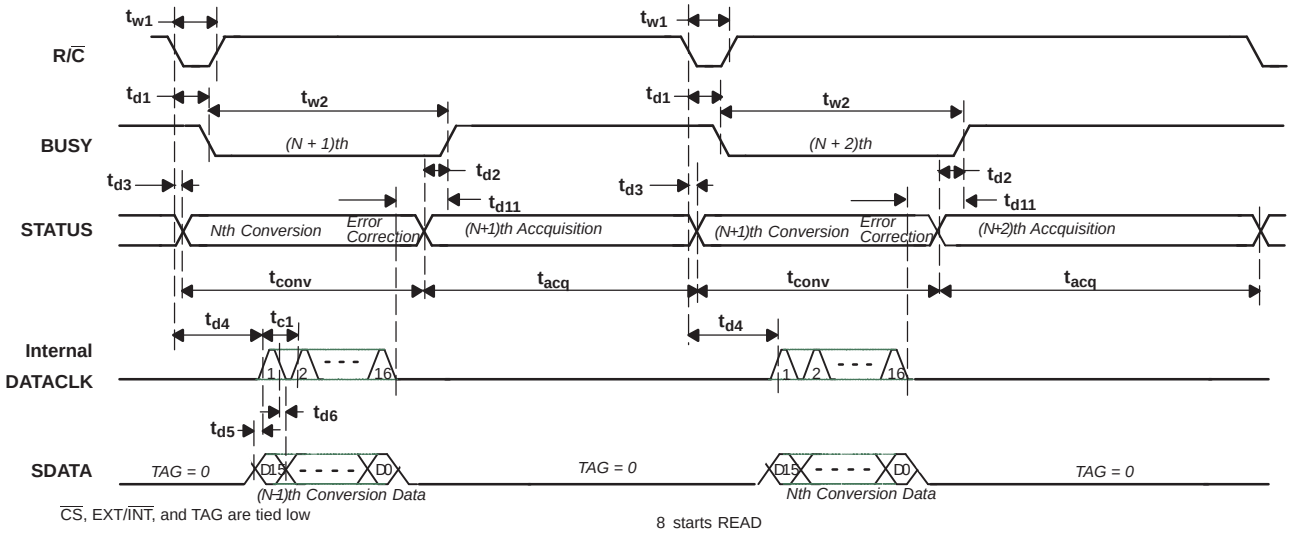


Figure 33. Basic Conversion Timing: Internal DATACLK (Read Previous Data During Conversion)

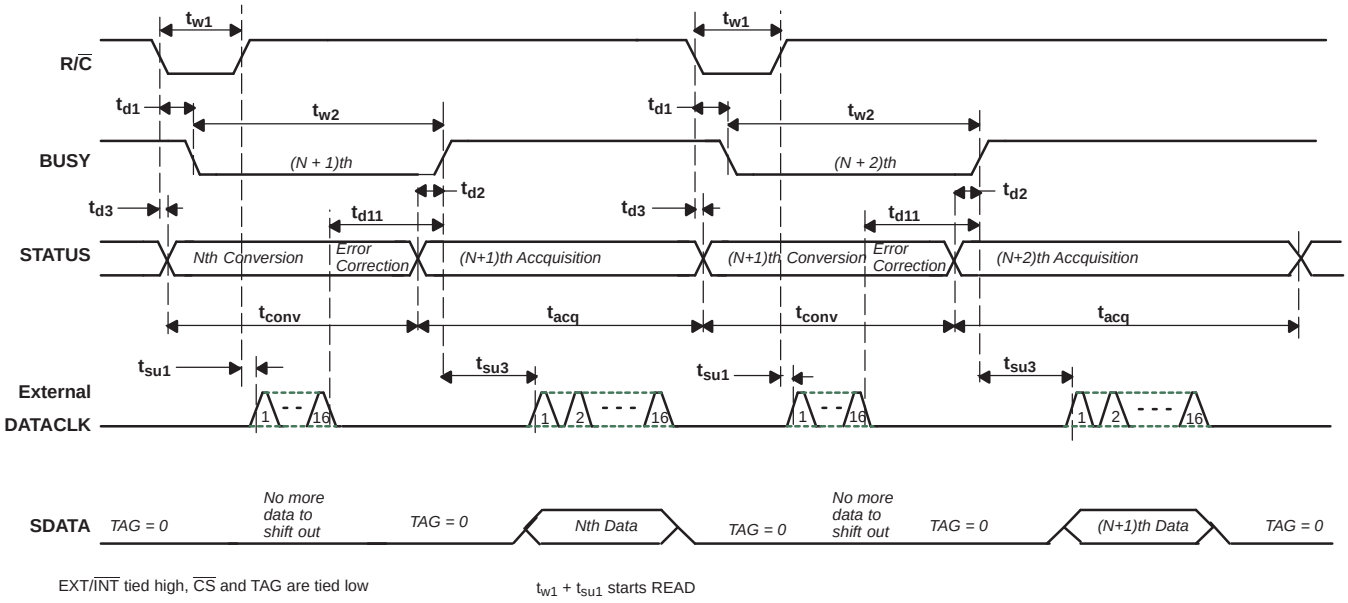


Figure 34. Basic Conversion Timing: External DATACLK

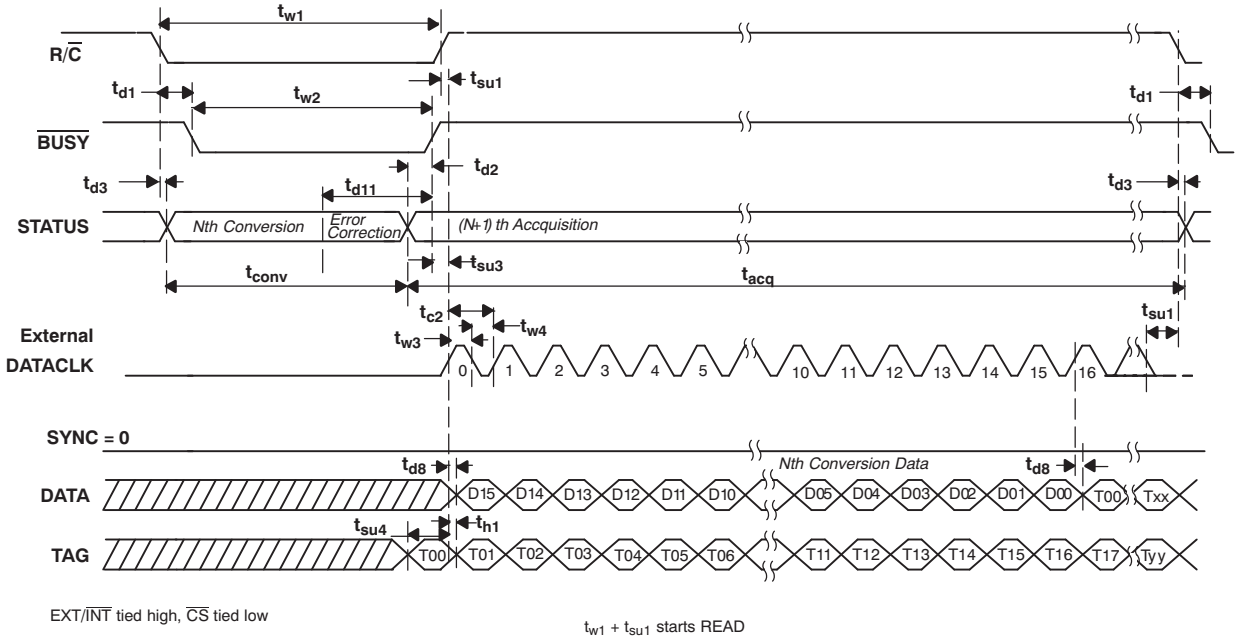


Figure 35. Read After Conversion (Discontinuous External DATACLK)

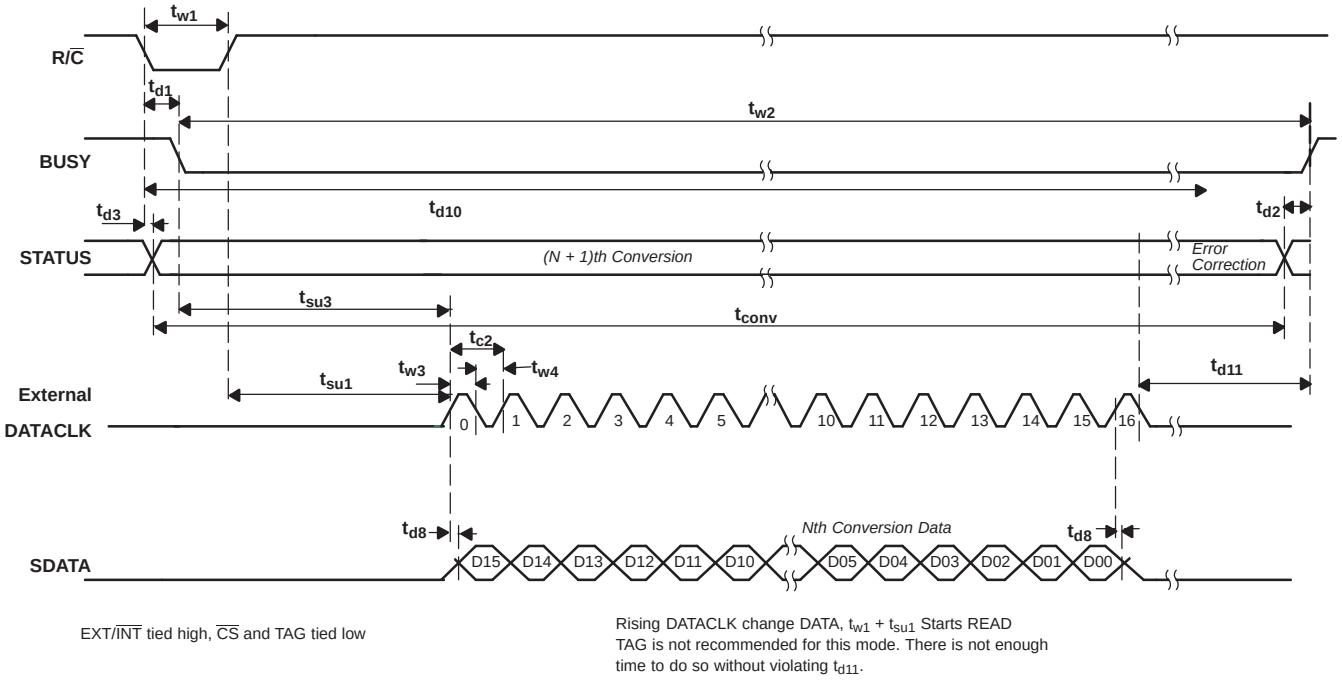


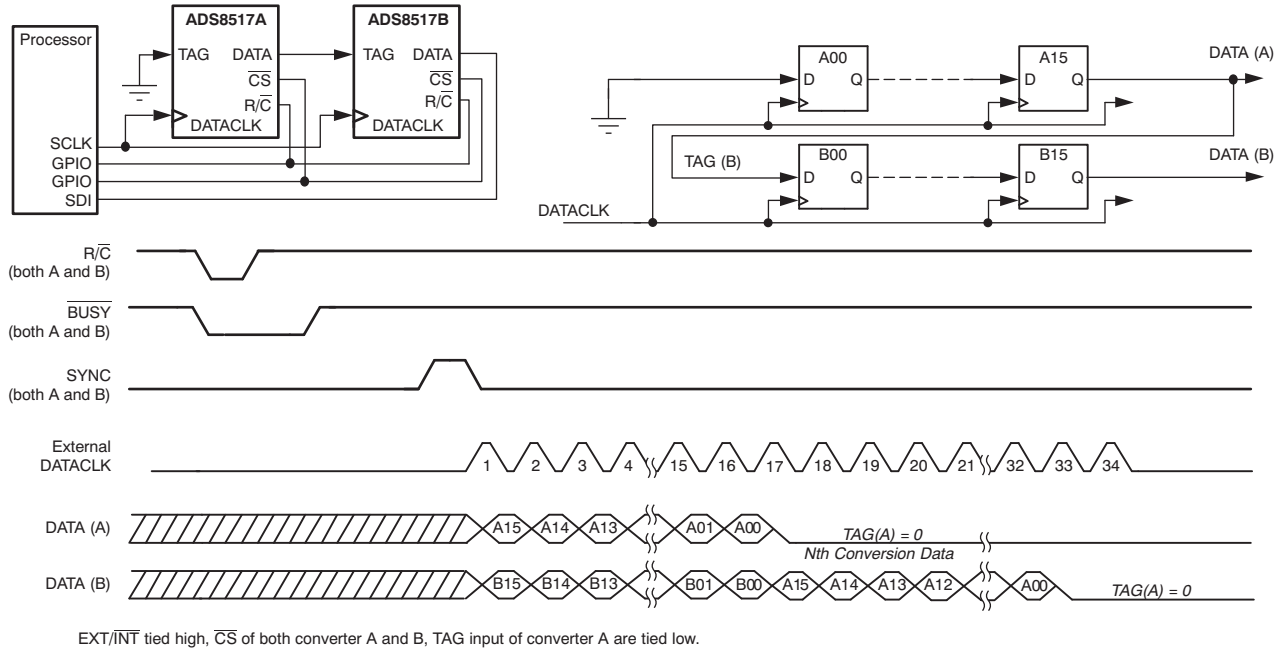
Figure 36. Read During Conversion (Discontinuous External DATACLK)

TAG FEATURE

The TAG feature allows data from multiple ADS8517 converters to be read on a single serial line. The converters are cascaded together using the DATA pins as outputs and the TAG pins as inputs, as illustrated in Figure 37. The DATA pin of the last converter drives the processor serial data input. Data are then shifted through each converter, synchronous to the externally supplied data clock, onto the serial data line. The internal clock cannot be used for this configuration.

The preferred timing uses the discontinuous, external data clock during the sampling period. Data must be read during the sampling period because there is not sufficient time to read data from multiple converters during a conversion period without violating the t_{d11} constraint (see the *External Data Clock* section). The sampling period must be sufficiently long enough to allow all data words to be read before starting a new conversion.

Note that in Figure 37, the state of the DATA pin at the end of a READ cycle reflects the state of the TAG pin at the start of the cycle for each converter. The ADS8517 works the same way when it is running in external or internal clock mode. That is, the state of the TAG pin is shown on the DATA pin at the 17th clock after all 16 bits have shifted out. However, it is only practical to use the TAG feature with the external clock mode when multiple ADS8517s are daisy-chained, so that they are running at the same clock speed. For example, when two converters (ADS8517A and ADS8517B) are cascaded together, the 17th external clock cycle brings the MSB data of ADS8517A onto the DATA pin of ADS8517B.



EXT/$\overline{INT}$ tied high, $\overline{CS}$ of both converter A and B, TAG input of converter A are tied low.

Figure 37. Timing of TAG Feature With Single Conversion (Using External DATACLK)

ANALOG INPUTS

The ADS8517 offers three analog input ranges, as shown in Table 1. The offset specification is factory-calibrated with internal resistors. The gain specification is factory-calibrated with 0.1%, 0.25-W external resistors, as shown in Figure 38 and Figure 39. The external resistors can be omitted if a larger gain error is acceptable or if using software calibration. The hardware trim circuitry shown in Figure 38 and Figure 39 can reduce the error to zero.

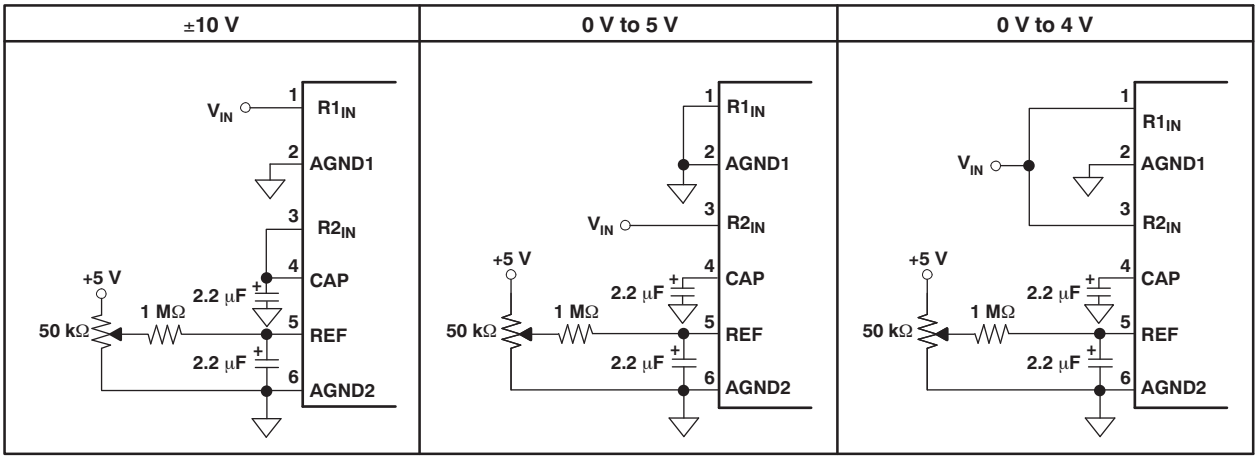


Figure 38. Circuit Diagrams (with Gain Adjust Trim)

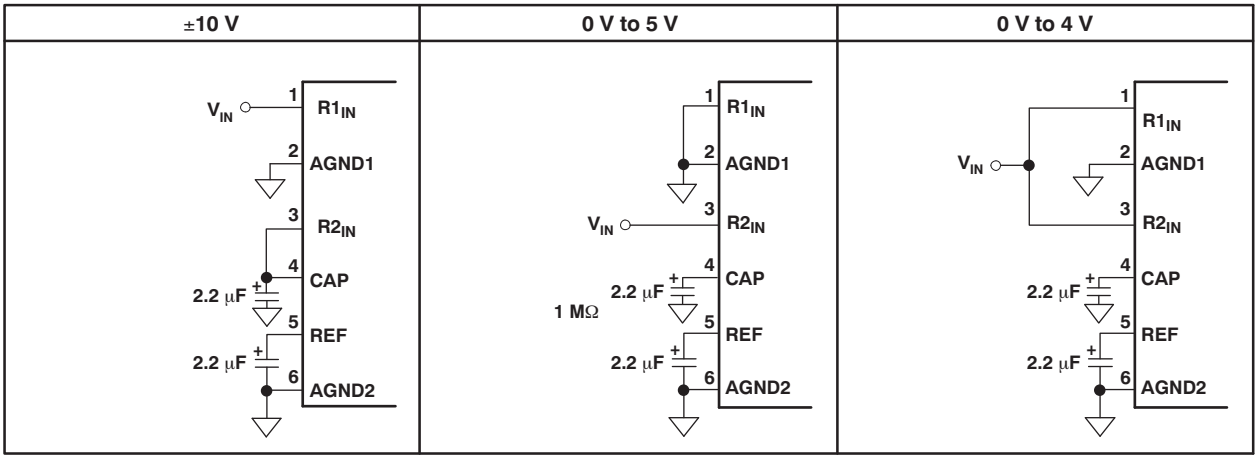


Figure 39. Circuit Diagrams (Without Gain Adjust Trim)

Analog input pins $R1_{IN}$ and $R2_{IN}$ have ±25-V overvoltage protection. The input signal must be referenced to AGND1. This referencing minimizes ground-loop problems typical to analog designs. The analog input should be driven by a low-impedance source. A typical driving circuit using the OPA627 or OPA132 is shown in Figure 40.

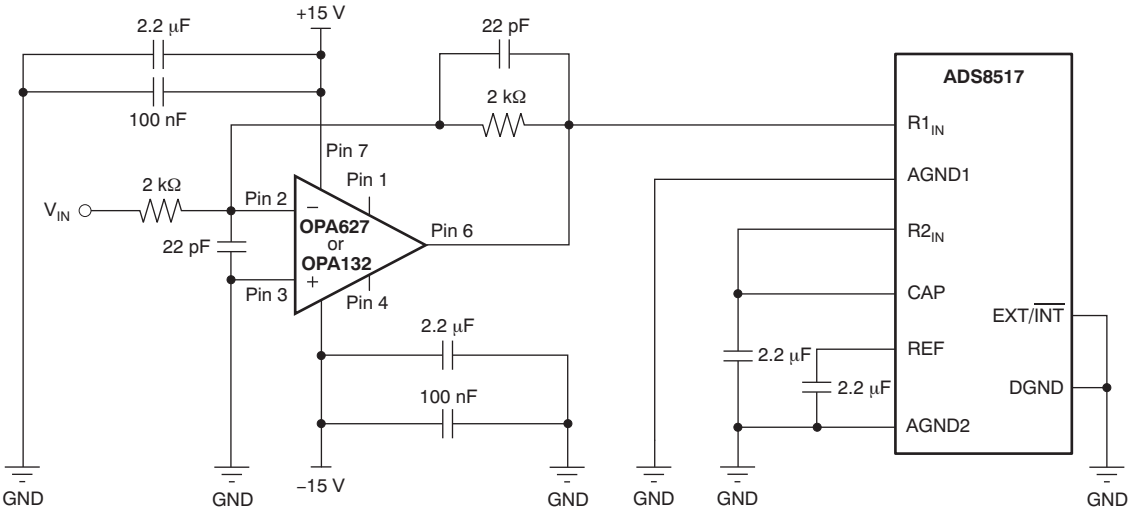
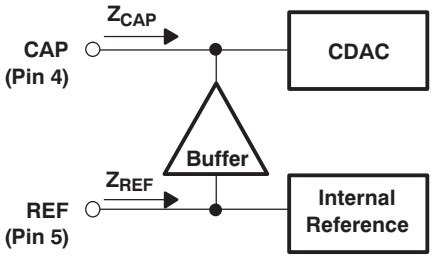


Figure 40. Typical Driving Circuit (±10 V, No Trim)

REFERENCE

The ADS8517 can operate with the internal 2.5 V reference or an external reference. An external reference connected to pin 5 (REF) bypasses the internal reference. The external reference must drive the 6-kΩ resistor that separates pin 5 from the internal reference (see the front page diagram). The load varies with the difference between the internal and external reference voltages. The internal reference is approximately 2.5 V (range is from 2.48 V to 2.52 V). The external reference voltage can vary from 2.3 V to 2.7 V. The reference, whether internal or external, is buffered internally with the output on pin 4 (CAP). Figure 41 shows characteristic impedances at the input and output of the buffer with all combinations of power-down and reference power-down. The reference voltage determines the size of the least significant bit (LSB). The larger reference voltages produce a larger LSB, which can improve SNR. Smaller reference voltages can degrade SNR.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} Ω	1	1	200	200
Z_{REF} Ω	6 k	1 M	6 k	1 M

Figure 41. Characteristic Impedances of the Internal Buffer

The ADS8517 is factory-tested with 2.2 µF capacitors connected to pin 4 (CAP) and pin 5 (REF). Each capacitor should be placed as close as possible to the pin. The capacitor on pin 5 band-limits the internal reference noise. A smaller capacitor can be used, but it may degrade SNR and SINAD. The capacitor on pin 4 stabilizes the reference buffer and provides switching charge to the CDAC during conversion. Capacitors smaller than 1 µF may cause the buffer to become unstable and not hold sufficient charge for the CDAC. The devices are tested to specifications with 2.2 µF, making larger capacitors unnecessary (Figure 42 shows how capacitor values larger than 2.2 µF have little effect on improving performance). The equivalent series resistance (ESR) of these compensation capacitors is also critical; keep the total ESR under 3 Ω. See the Typical Characteristics section concerning how ESR affects performance.

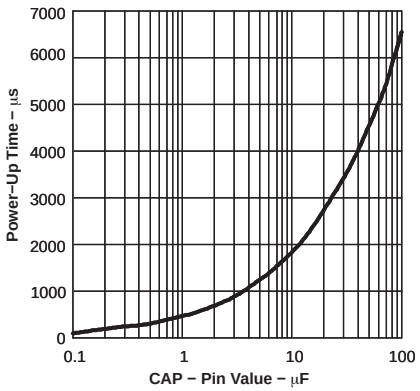


Figure 42. Power-Down to Power-Up Time versus Capacitor Value on CAP

Neither the internal reference nor the buffer should be used to drive an external load. Such loading can degrade performance, as shown in Figure 41. Any load on the internal reference causes a voltage drop across the 6-kΩ resistor and affects gain. The internal buffer is capable of driving ±2-mA loads, but any load can cause perturbations of the reference at the CDAC, thus degrading performance.

POWER-DOWN

The ADS8517 has analog power-down and reference power-down capabilities via PWRD (pin 25) and REFD (pin 26), respectively. PWRD and REFD high powers down all analog circuitry, maintaining data from the previous conversion in the internal registers, provided that the data have not already been shifted out through the serial port. Typical power consumption in this mode is 50 μW. Power recovery is typically 1 ms, using a 2.2-μF capacitor connected to CAP. Figure 42 shows power-down to power-up recovery time relative to the capacitor value on CAP. With +5 V applied to V_{DIG}, the digital circuitry of the ADS8517 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD high powers down all of the analog circuitry except for the reference. Data from the previous conversion are maintained in the internal registers and can still be read. With PWRD high, a convert command yields meaningless data.

REFD

REFD high powers down the internal 2.5-V reference. All other analog circuitry, including the reference buffer, is active. REFD should be high when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 41 for the characteristic impedance of the reference buffer input for both REFD high and low. The internal reference consumes approximately 5 mW.

LAYOUT

POWER

For host processors that are able to advantage of a lower interface supply voltage, the ADS8517 offers a wide range of voltages—from 5.5V to as low as 1.65V. The ADS8517 should be considered as an analog component because, as noted in the *Electrical Characteristics*, it uses 95% of its power for the analog circuitry. If the interface is at the same +5V as the analog supply, the two +5-V supplies should be separate. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance because of switching noise from the digital logic. For best performance, the +5-V supply should be produced from whichever analog supply is present for the rest of the analog signal conditioning. If a +12-V or +15-V suppy is present in the system, a simple +5-V regulator can be used. Although it is not suggested, if the digital supply in the system must be used to power the converter, be sure it is properly filtered.

POWER-ON SEQUENCE

Care must be taken with power sequencing when the interface and analog supplies are different. Refer to the *Absolute Maximum Ratings* for details. The analog supply should be powered on before the digital supply (used for the interface). It is important that the voltage difference between V_{DIG} and the digital inputs does not exceed the limit of –0.3V to V_{DIG} + 0.3V. All digital inputs should be kept inactive (logic low) until the digital (interface) supply is steady.

GROUNDING

Three ground pins are present on the ADS8517. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground to which all analog signals internal to the A/D converter are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

To achieve optimum performance, all the ground pins of the A/D converter should be tied to an analog ground plane, separated from the system digital logic ground. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This configuration helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The ADS8517 features high-impedance inputs as the result of the resistive input attenuation circuit. For ±10V, 0V to 5V, and 0V to 4V inputs, the equivalent input impedances are 45.7kΩ, 20kΩ and 21.4kΩ respectively. Lower cost op amps may be used to drive the ADC inputs because the driving requirement is not as high compared to other converters. This input circuit not only reduces the power consumption on the signal conditioning op amp, but it also works as a buffer to attenuate any charge injection resulting from the operation of the CDAC FET sample switches, even though the design of those FET switches is optimized to give minimal charge injection.

Another benefit provided by the ADS8517 high-impedance front-end is assured ±25V overvoltage protection. In most cases, this internal protection eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS8517 does have 3-state outputs for the parallel port, but intermediate latches should be used if the bus is active during conversion. If the bus is not active during conversion, the 3-state outputs can be used to isolate the A/D converter from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS8517 has an internal LSB size of 38 μV (with a 2.5-V internal reference). Transients from fast-switching signals on the parallel port, even when the A/D converter is 3-stated, can be coupled through the substrate to the analog circuitry, causing degradation of converter performance.

APPLICATION INFORMATION

TRANSITION NOISE

Apply a dc input to the ADS8517 and initiate 1000 conversions. The digital output of the converter varies in output codes because of the internal noise of the ADS8517. This variance is true for all 16-bit SAR converters. The transition noise specification found in the *Electrical Characteristics* section is a statistical figure that represents the one sigma limit or rms value of these output codes.

Using a histogram to plot the output codes, the distribution should appear bell-shaped, with the peak of the bell curve representing the nominal output code for the input voltage value. The ±1σ, ±2σ, and ±3σ distributions represent 68.3%, 95.5%, and 99.7%, respectively, of all codes. Multiplying the transition noise (TN) by 6 yields the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the five-code distribution when executing 1000 conversions. The ADS8517 has a TN of 0.8 LSBs, which yields five output codes for a ±3σ distribution. Figure 43 shows 16,384 conversion histogram results.

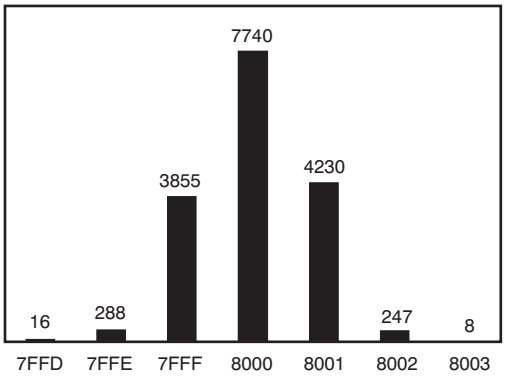


Figure 43. Histogram of 16,384 Conversions with V_{IN} = 0 V in ±10 V Bipolar Range

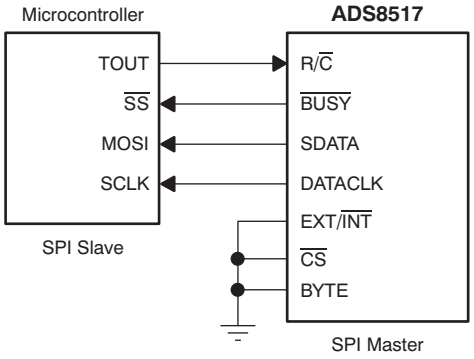
AVERAGING

The noise of the converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of $1/\sqrt{n}$ where *n* is the number of averages. For example, averaging four conversion results reduces the TN by 1/2 to 0.4 LSBs. Averaging should only be used for input signals with frequencies near dc.

For ac signals, a digital filter can be used to low-pass filter and decimate the output codes. This action works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio improves by 3 dB.

ADS8517 AS AN SPI MASTER DEVICE (INT/$\overline{\text{EXT}}$ TIED LOW)

Figure 44 shows a simple interface between the ADS8517 and an SPI-equipped microcontroller or TMS320 series digital signal processor (DSP) when using the internal serial data clock. This interface assumes that the microcontroller or DSP is configured as an SPI slave, is capable of receiving 16-bit transfers, and that the ADS8517 is the only serial peripheral on the SPI bus.



NOTE: CPOL = 0 (inactive SCLK is LOW)
CPHA = 0 or 1 (data valid on either SCLK edge)

Figure 44. ADS8517 as SPI Master

To maintain synchronization with the ADS8517, the microcontroller slave select ($\overline{\text{SS}}$) input should be connected to the $\overline{\text{BUSY}}$ output of the ADS8517. When a transition from high-to-low occurs on $\overline{\text{BUSY}}$ (indicating the current conversion is in process), the ADS8517 internal SCLK begins shifting the previous conversion data into the MOSI pin of the microcontroller. In this scenario, the $\overline{\text{CONV}}$ input to the ADS8517 can be controlled from an external trigger source, or a trigger generated by the microcontroller. The ADS8517 internal SCLK provides 2 ns (min) of setup time and 41 ns (min) of hold time on the SDATA output (see t_{d5} and t_{d6} in Table 6), allowing the microcontroller to sample data on either the rising or falling edge of SCLK.

ADS8517 AS AN SPI SLAVE DEVICE (INT/$\overline{EXT}$ TIED HIGH)

Figure 45 shows another interface between the ADS8517 and an SPI-equipped microcontroller or DSP in which the host processor acts as an SPI master device.

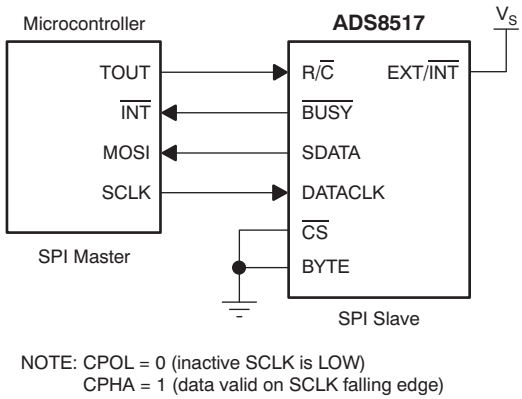


Figure 45. ADS8517 as SPI Slave

In this configuration, the data transfer from the ADS8517 is triggered by the rising edge of the serial data clock provided by the SPI master. The SPI interface should be configured to read valid SDATA on the falling edge of SCLK. When a minimum of 17 SCLKs are provided to the ADS8517, data can be strobed to the host processor on the rising SCLK edge providing a 2ns (min) hold time (see t_{d8} in Table 6).

When using an external interrupt to facilitate serial data transfers, as shown in Figure 45, there are two options for the configuration of the interrupt service routine (ISR): falling-edge-triggered or rising-edge-triggered.

A falling-edge-triggered transfer would initiate an SPI transfer after the falling edge of $\overline{BUSY}$, providing the host controller with the previous conversion results, while the current conversion cycle is underway. The timing for this type of interface is described in detail in Figure 36. Care must be taken to ensure the entire 16-bit conversion result is retrieved from the ADS8517 before $\overline{BUSY}$ returns high to avoid the potential corruption of the current conversion cycle.

A rising-edge-triggered transfer is the preferred method of obtaining the conversion results. This timing is depicted in Figure 35. This method of obtaining data ensures that SCLK is static during the conversion cycle and provides the host processor with current cycle conversion results.

8-BIT SPI INTERFACE

For microcontrollers that only support 8-bit SPI transfers, it is recommended to configure the ADS8517 for SPI slave operation, as depicted in Figure 45. With the microcontroller configured as the SPI master, two 8-bit transfers are required to obtain full 16-bit conversion results from the ADS8517. The eight MSBs of the conversion result are considered valid on the falling SCLK edges of the first transfer, with the remaining four LSBs being valid on the first four falling SCLK edges in the second transfer.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2008) to Revision A	Page
• Changed data sheet to reflect TSSOP-28 package availability	1
• Deleted lead temperature specification from Absolute Maximum Ratings	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8517IBDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8517I B	Samples
ADS8517IBPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS8517I B	Samples
ADS8517IBPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS8517I B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

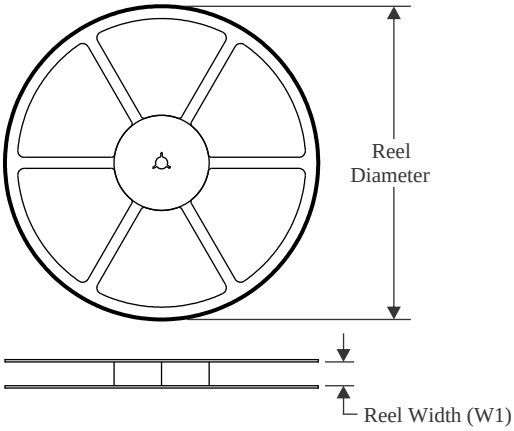
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

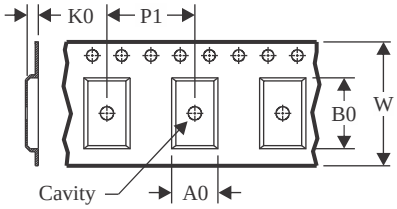
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

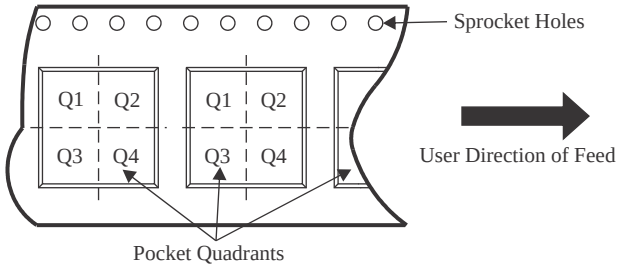


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

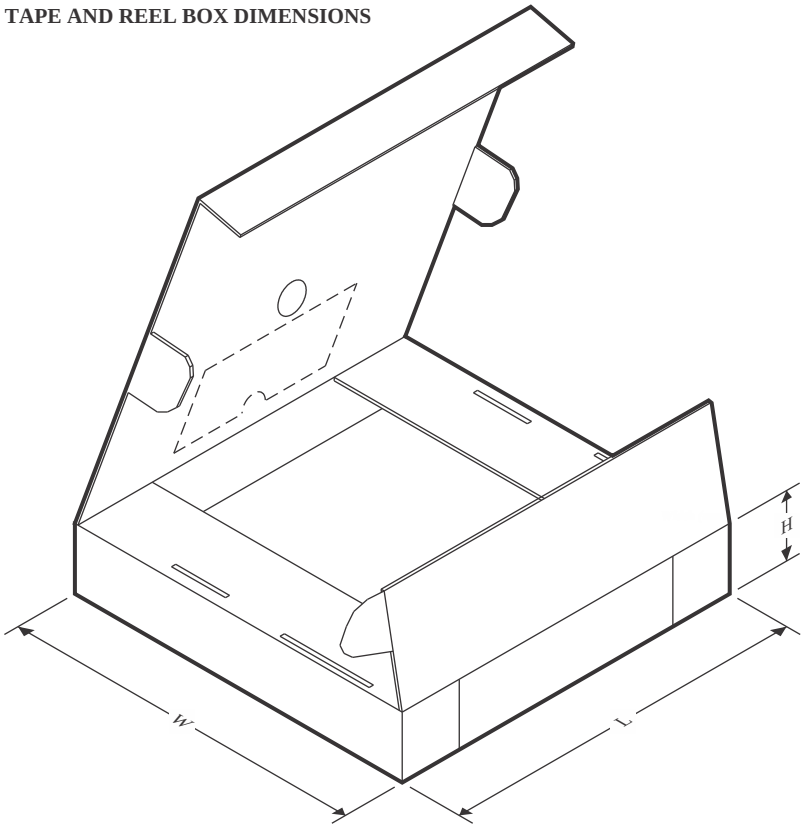
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8517IBPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

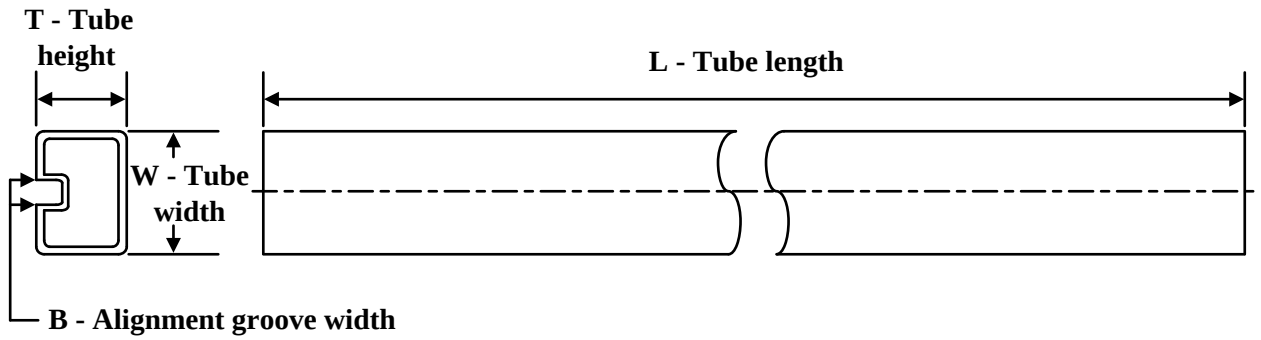
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8517IBPWR	TSSOP	PW	28	2000	350.0	350.0	43.0

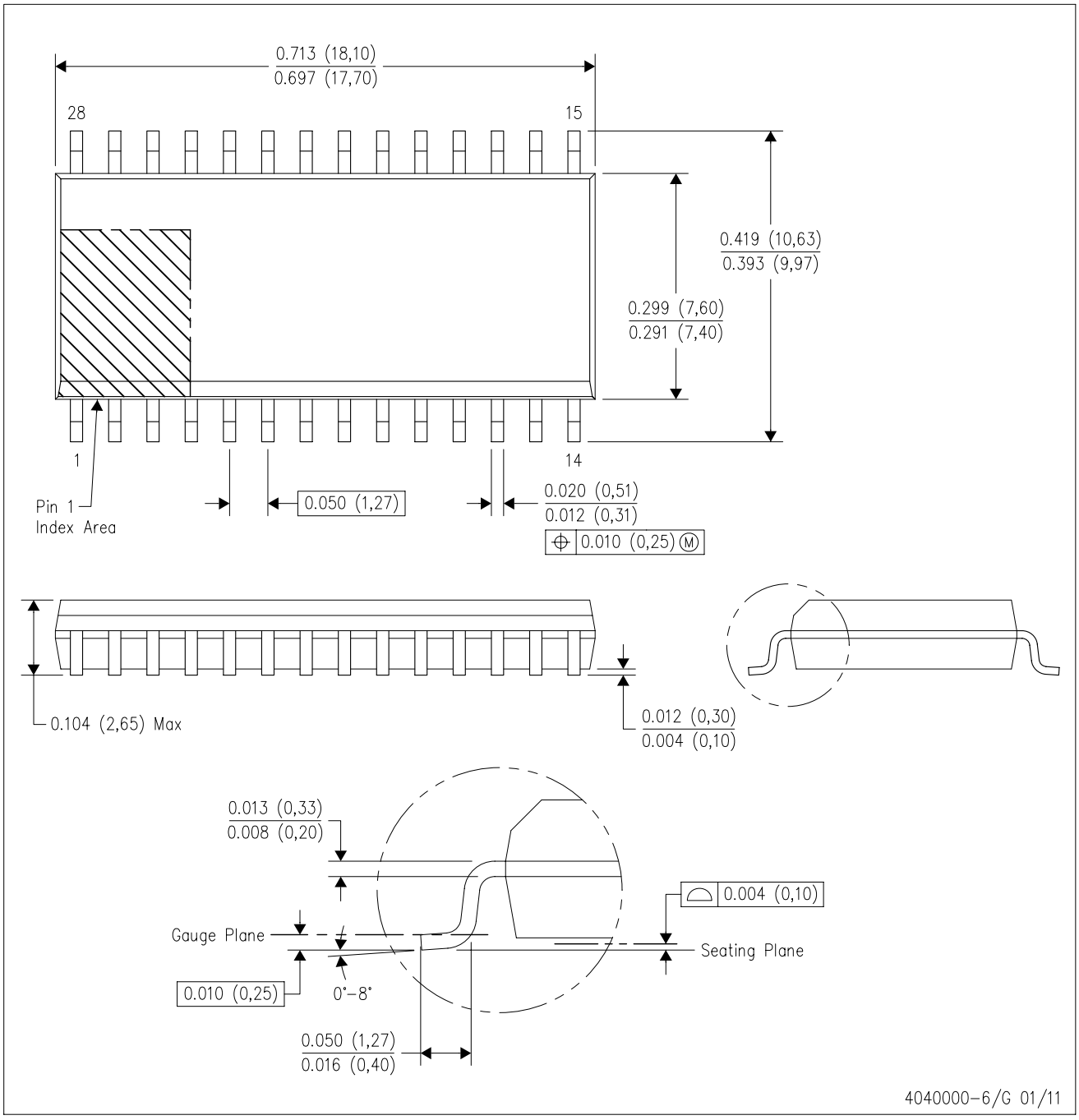
TUBE



*All dimensions are nominal

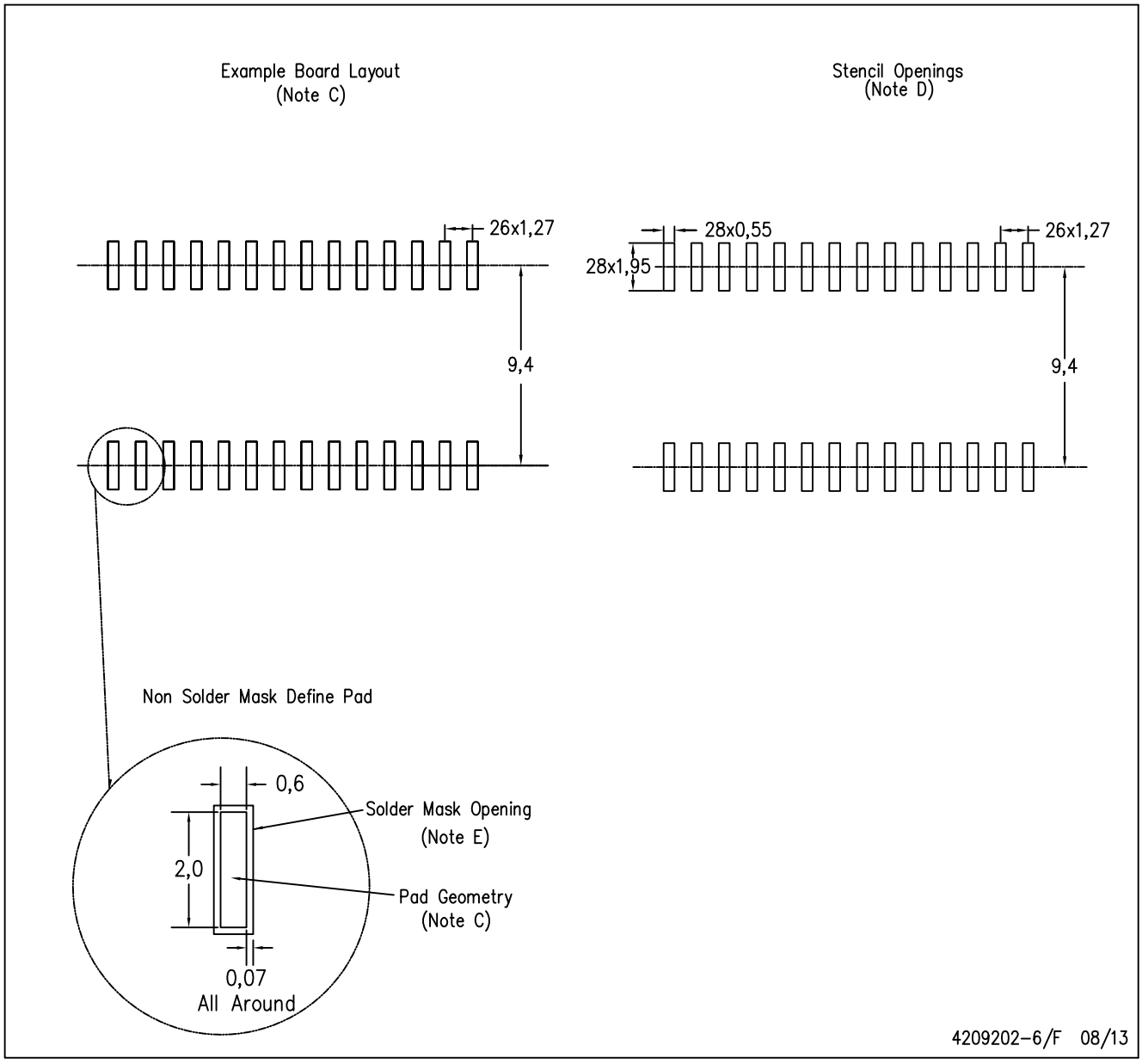
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS8517IBDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
ADS8517IBPW	PW	TSSOP	28	50	530	10.2	3600	3.5

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



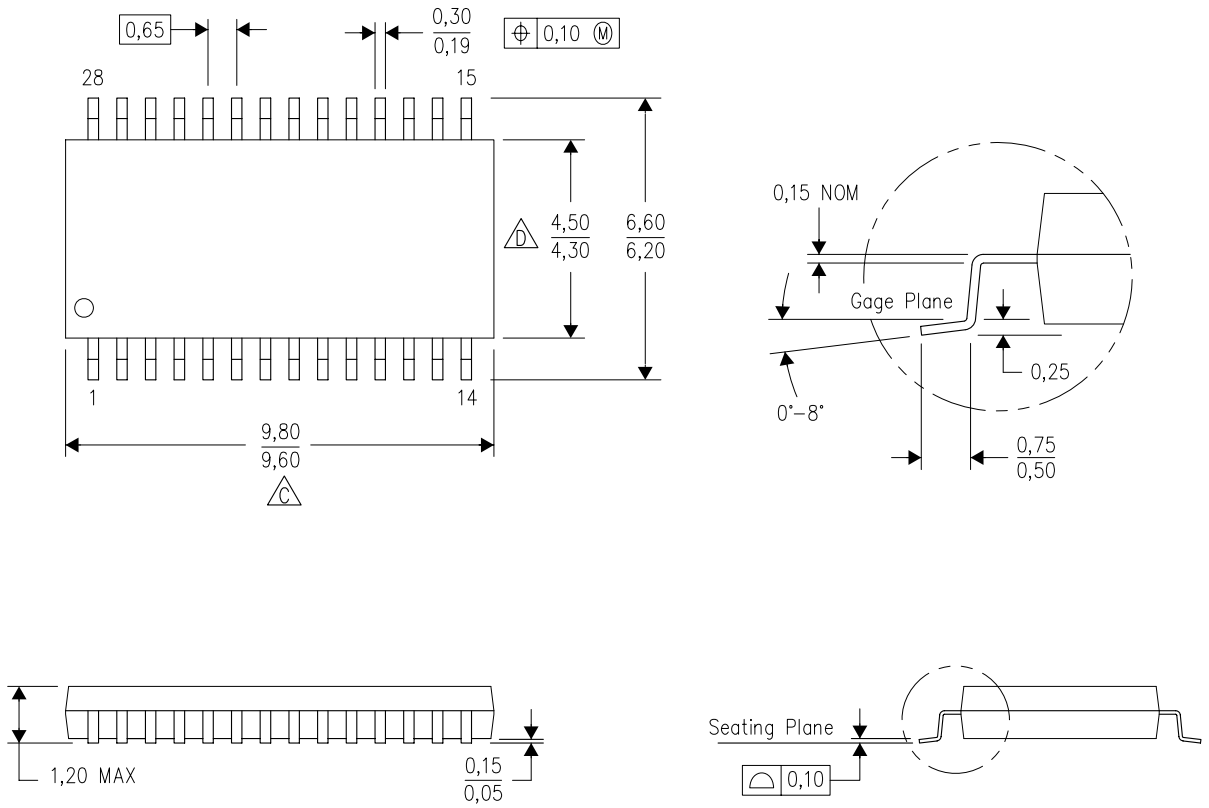
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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