

DLPC7530 High-Resolution Controller

1 Features

- DLPC7530 controller using the DLP472NE and DLP651NE digital micromirror device (DMD) supports
 - Up to 1080p at up to 240Hz (2D) and 120Hz (3D)
- Provides single V-by-One® HS video input port with one, two, four, or eight lanes
 - Up to 600MHz pixel clock support
 - Up to 3.0Gbps input transmission rate
- Two OpenLDI (FPD-Link™ I) video input ports with 6 lanes (five data) per port
- Input formats supported
 - RGB, YCbCr, and ICtCp
 - 4:4:4, 4:2:2, 4:2:0
- Internal Arm® Cortex® R4F processor with FPU
 - 88 configurable GPIOs
 - Programmable PWM generator
 - Programmable capture and delay timers
 - USB 2.0 high-speed OTG controller
 - SPI primary/secondary controllers
 - I²C primary/secondary controllers
 - UART and interrupt controllers
- Warping engine
 - Improved 1D, 2D, and 3D keystone correction
 - Warping (full warp map access 62 × 32 points)
 - Blending (full blending map access 63 × 32 points)
- Additional image processing
 - DynamicBlack
 - TI DLP® BrilliantColor™ Technology
 - HDR10 (PQ and HLG) support
 - Frame rate conversion
 - Color coordinate adjustment
 - White color temperature adjustment
 - Programmable degamma
 - Spatial-temporal multiplexing
 - Integrated support for 3-D display
- On-screen display (OSD)
- Splash screen display and capture
- Integrated 2G-bit frame memory eliminates the need for external high-speed memory
- External memory support
 - Parallel flash for μP and PWM sequences
 - Secondary flash for splash capture, warping
- System control
 - DMD power and reset driver control
 - DMD horizontal and vertical image flip
- JTAG boundary scan test support
- LED, RGB laser, and laser phosphor illuminations

2 Applications

- Enterprise projector
- Laser TV
- Smart projector
- Digital signage

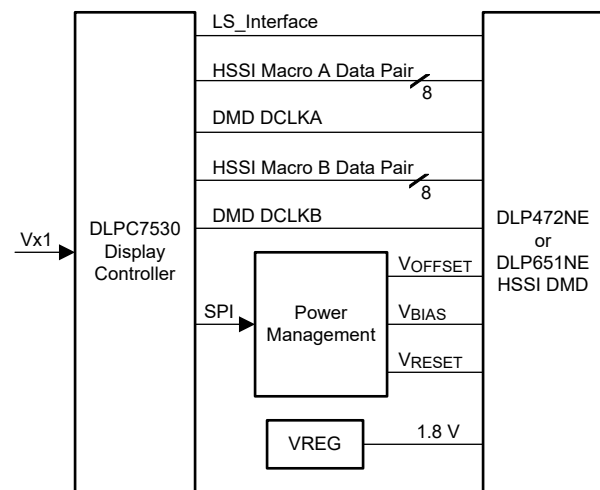
3 Description

The DLPC7530 is a digital display controller for the 1080p display chipsets, which comprises the DLPC7530 display controller, the DLP472NE and DLP651NE digital micromirror devices (DMD), and the DLPA100 power and motor driver. This solution targets display systems that require lower cost high resolution and high brightness in a small form factor. To ensure reliable operation, the DLPC7530 controller must always be used with the DLP472NE and DLP651NE DMDs and the DLPA100 power management integrated circuit in each application.

Device Information

PART NUMBER	PACKAGE ^{(1) (2)}	PACKAGE SIZE
DLPC7530ZDC	P-HBGA (676)	31.00mm × 31.00mm

- (1) See [Mechanical, Packaging, and Orderable Information](#).
 (2) Includes embedded heat slug



Typical Standalone System



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4 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A	●	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
B	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
C	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
D	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
E	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
F	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
G	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
H	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
J	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
K	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
L	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
M	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
P	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
R	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
T	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
U	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
V	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
W	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
Y	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AA	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AB	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AC	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AD	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AE	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AF	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AG	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AH	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AJ	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AK	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○

Figure 4-1. ZDC Package 676-Pin PBGA Top View

Table 4-1. Initialization, Board Level Test, and Debug

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
POSENSE	AE27	I ₈	Power-On Sense: Signal provided from external voltage monitoring circuit ('0' = All controller supply voltages not at valid level, '1' = All controller supply voltages have reached 90% specified minimum voltage) Drive this signal to inactive (low) after the falling edge of PWRGOOD as specified. See Section 5.13 for specific timing requirements as well as the required power up and power down sequence. This pin includes hysteresis.
PWRGOOD	AG30	I ₈	Power Good: Signal provided from external power supply of voltage monitor A high value indicates all power is within operating voltage specifications and the system is safe to exit its reset state. A transition from high to low indicates that the controller or DMD supply voltage drops below its rated minimum level. This transition must occur prior to the supply voltage dropping per the timing specified, as this is an early warning of an imminent power loss condition. This warning is required to enhance long term DMD reliability. When PWRGOOD goes low for the specified minimum time, a DMD park and full Controller reset are performed, protecting the DMD. Note that both controller and DMD supply voltages must be within operating voltage levels to successfully execute the DMD park. The minimum PWRGOOD deassertion time is used to protect the system input from glitches. When PWRGOOD is low, the Controller is held in its reset state. See Section 5.13 for specific timing requirements as well as the required power up and power down sequence. This pin includes hysteresis.
EXT_ARSTZ	AF29	O ₈	External Reset: General purpose reset output ('0' = Reset, '1' = Normal Operation) This output is asserted low immediately upon POSENSE being asserted low, and remains low while POSENSE remains low. This signal remains low after POSENSE is set high, until released by software. This signal is also asserted low approximately 5µs after the detection of PWRGOOD going low, or any internally generated reset. In all cases, this signal remains active low for a minimum of 2ms. Note: This signal can also be independently driven through the software register.
MTR_ARSTZ	AF27	O ₈	Color Wheel Motor Controller Reset: Color wheel motor controller reset output ('0' = Reset, '1' = Normal Operation) This output is asserted low immediately upon POSENSE being asserted low, and remains low while POSENSE remains low. This signal remains low after POSENSE is set high, until released by software. This signal is also asserted low approximately 5µs after the detection of PWRGOOD going low, or any internally generated reset. In all cases, this signal remains active low for a minimum of 2ms. Note: This signal can also be independently driven through the software register.
TCK	AK19	I ₈	JTAG, ARM-ICE, and CPU MBIST Serial Data Clock. This signal is shared between JTAG, ARM-ICE (TI test only), and CPU MBIST (Manufacturing test only) operation Includes a weak internal pulldown
TMS1	AH20	I ₈	JTAG Test Mode Select Includes a weak internal pullup
TMS2	AJ20	I ₈	ARM-ICE Test Mode Select For normal operation, this pin must be left open or unconnected. Includes a weak internal pullup
TMS3	AK20	I ₈	CPU MBIST Test Mode Select For normal operation this pin must be left open or unconnected. Includes a weak internal pullup

Table 4-1. Initialization, Board Level Test, and Debug (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
TRSTZ	AG21	I ₈	JTAG, ARM-ICE, and CPU MBIST Reset. This signal is shared between JTAG, ARM-ICE (TI test only), and CPU MBIST (Manufacturing test only) operation. <i>For normal operation, this pin must be pulled to ground through an external resistor with value 8kΩ or less. Failure to pull this pin low during normal operation causes start-up and initialization problems.</i> For JTAG Boundary Scan, ARM-ICE Debug operation, or CPU MBIST, this pin must be pulled-up or left disconnected. Includes a weak internal pullup and hysteresis
TDI	AG20	I ₈	JTAG, ARM-ICE, and CPU MBIST: Serial Data In Includes a weak internal pullup
TDO1	AG19	O ₈	JTAG Serial Data Out
TDO2	AH19	O ₈	ARM-ICE Serial Data Out For normal operation, this pin must be left open or unconnected.
TDO3	AJ19	O ₈	CPU MBIST Serial Data Out For normal operation, this pin must be left open or unconnected.
ETM_TRACECLK	C30	O ₈	TI internal use. Must be left unconnected (clock for trace debug)
ETM_TRACECTL	D30	O ₈	TI internal use. Must be left unconnected (control for trace debug)
ICTSEN	K26	I ₈	IC Tristate Enable (Active high) Asserting this signal transitions all outputs into tristate (except for the JTAG interface). Includes a weak internal pulldown, however, an external pulldown is recommended for added protection. Also includes hysteresis
ICTSE	M26	I ₈	TI internal use. Includes a weak internal pulldown, however, an external pulldown is recommended for added protection. Also includes hysteresis
TSTPT_0	E29	B ₈	Test pin 0 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10kΩ. Tristated while PWRGOOD is asserted low. It may be driven as an output for debug use as described in Section 6.3.9 .
TSTPT_1	E30	B ₈	Test pin 1 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10kΩ. Tristated while PWRGOOD is asserted low. It may be driven as an output for debug use as described in Section 6.3.9 .
TSTPT_2	F26	B ₈	Test pin 2 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10kΩ. Tristated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in Section 6.3.9 .
TSTPT_3	F27	B ₈	Test pin 3 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10kΩ. Tristated while PWRGOOD is asserted low. It may be driven as an output for debug use as described in Section 6.3.9 .
TSTPT_4	F28	B ₈	Test pin 4 This pin requires an external pulldown resistor (≤ 10kΩ). Tristated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in Section 6.3.9 .
TSTPT_5	F29	B ₈	Test pin 5 This pin requires an external pulldown resistor (≤ 10kΩ). Tristated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in Section 6.3.9 .
TSTPT_6	G26	B ₈	Test pin 6 This pin requires an external pulldown resistor (≤ 10kΩ). Tristated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in Section 6.3.9 .

Table 4-1. Initialization, Board Level Test, and Debug (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
TSTPT_7	G28	B ₈	Test pin 7 This pin requires an external pulldown resistor ($\leq 10k\Omega$). Tristated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in Section 6.3.9 .
HWTEST_EN	L26	I ₈	Manufacturing test enable signal. This signal must be connected directly to ground on the PCB for normal operation. Includes a weak internal pulldown and hysteresis

(1) See [Table 4-13](#) for more information on I/O definitions.

Table 4-2. Analog Front End

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
AFE_ARSTZ	K2	O ₈	External reset: Provided for analog front end ('0' = Reset, '1' = normal operation) This output is asserted low immediately upon POSENSE being asserted low, and remains low while POSENSE remains low. This signal remains low after POSENSE is set high, until released by software. This signal is also asserted low approximately 5 μ s after the detection of PWRGOOD going low, or any internally generated reset. In all cases, this signal remains active low for a minimum of 2ms. Note: This signal can also be independently driven through the software register.
AFE_CLK	K3	O ₈	External clock: Provides a fixed 5MHz clock for analog front end to support video decoder operation
AFE_IRQ	K4	I ₈	External interrupt: Provided to support analog front end ('0' = No Interrupt, '1' = Interrupt) Includes a weak internal pulldown and hysteresis
ALF_VSYNC	K5	I ₈	Dedicated VSYNC: Provided to support analog front end autolock functionality Includes a weak internal pulldown and hysteresis
ALF_HSYNC	J1	I ₈	Dedicated HSYNC: Provided to support analog front end autolock functionality Includes weak internal pulldown and hysteresis
ALF_CS SYNC	J2	I ₈	Dedicated composite sync (sync on green): Provided to support analog front end autolock functionality Includes weak internal pulldown and hysteresis.

(1) See [Table 4-13](#) for more information on I/O definitions.

Table 4-3. V-by-One® Interface Input Data and Control

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3)}
NAME	NO.		
VX1_DATA0_P	C18	I ₁	V-by-One® interface data lanes
VX1_DATA0_N	D18		
VX1_DATA1_P	A19		
VX1_DATA1_N	B19		
VX1_DATA2_P	C20		
VX1_DATA2_N	D20		
VX1_DATA3_P	A21		
VX1_DATA3_N	B21		
VX1_DATA4_P	C22		
VX1_DATA4_N	D22		
VX1_DATA5_P	A23		
VX1_DATA5_N	B23		
VX1_DATA6_P	C24		
VX1_DATA6_N	D24		
VX1_DATA7_P	A25		
VX1_DATA7_N	B25		

Table 4-3. V-by-One® Interface Input Data and Control (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3)}
NAME	NO.		
VX1_HTPDN	E17	O ₄	V-by-One interface hot plug detect (controller receiver pulls this signal low to indicate its presence to the transmitter) This signal is open drain at the controller output. A pullup resistor is required at the transmitter.
VX1_LOCKN	E19	O ₄	V-by-One interface clock detect lock (controller receiver pulls this signal low to indicate clock extraction lock to the transmitter) This signal is open drain at the controller output. A pullup resistor is required at the transmitter.
VX1_CM_CKREF0 VX1_CM_CKREF1 VX1_CM_CKREF2 VX1_CM_CKREF3	E20 E21 E23 E24	I ₁	V-by-One reserved: Tie these reserved pins to ground.
VX1_CM_AMOUT0 VX1_CM_AMOUT1 VX1_CM_AMOUT2 VX1_CM_AMOUT3	F19 F21 F22 F23	O ₁	V-by-One reserved: These pins are reserved and must remain unconnected.

- (1) See [Table 4-13](#) for more information on I/O definitions.
- (2) The system supports 1-lane, 2-lane, 4-lane, or 8-lane operation, based on the bandwidth requirement of the input source. The inputs for any unused data lanes must be left open.
- (3) The V-by-One port supports limited lane remapping to help optimize board layout. The details are described in [Section 6.3.5](#).

Table 4-4. OpenLDI (FPD-Link I) Ports Input Data and Control

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3)}
NAME	NO.		
FPDA_CLK_P FPDA_CLK_N	H3 H4	I ₅	FPD-Link Port A Clock Lane
FPDA_DATAA_P FPDA_DATAA_N FPDA_DATAB_P FPDA_DATAB_N FPDA_DATAC_P FPDA_DATAC_N FPDA_DATAD_P FPDA_DATAD_N FPDA_DATAE_P FPDA_DATAE_N	G1 G2 F3 F4 E1 E2 D3 D4 C1 C2	I ₅	FPD-Link Port A Data Lanes
FPDB_CLK_P FPDB_CLK_N	A4 B4	I ₅	FPD-Link Port B Clock Lane
FPDB_DATAA_P FPDB_DATAA_N FPDB_DATAB_P FPDB_DATAB_N FPDB_DATAC_P FPDB_DATAC_N FPDB_DATAD_P FPDB_DATAD_N FPDB_DATAE_P FPDB_DATAE_N	C5 D5 A6 B6 C7 D7 A8 B8 C9 D9	I ₅	FPD-Link Port B Data Lanes
FPDC_CLK_P FPDC_CLK_N	A10 B10	I ₅	FPD-Link Port C—Reserved for Parallel Port use only.

Table 4-4. OpenLDI (FPD-Link I) Ports Input Data and Control (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3)}
NAME	NO.		
FPDC_DATAA_P	C11	I ₅	FPD-Link Port C Data Lanes—Reserved for Parallel Port use only.
FPDC_DATAA_N	D11		
FPDC_DATAAB_P	A12		
FPDC_DATAAB_N	B12		
FPDC_DATAAC_P	C13		
FPDC_DATAAC_N	D13		
FPDC_DATAD_P	A14		
FPDC_DATAD_N	B14		
FPDC_DATAE_P	C15		
FPDC_DATAE_N	D15		

(1) See [Table 4-13](#) for more information on I/O definitions.

(2) Throughout this document the terms FPD and FPD-Link refer to OpenLDI (FPD-Link I).

(3) Tie the inputs for any unused port(s) to ground, or pull to ground through an external resistor.

Table 4-5. Parallel Port Input Data and Control

PIN		TYPE ⁽¹⁾	DESCRIPTION PARALLEL RGB MODE
NAME	NO.		
PCLK (<i>FPDB_DATAAB_N</i>)	B6	I ₆	Pixel clock
VSYNCR (<i>FPDA_DATAE_P</i>)	C1	I ₆	Vsync
HSYNCR (<i>FPDA_DATAE_N</i>)	C2	I ₆	Hsync
DATEN (<i>FPDB_DATAE_N</i>)	D9	I ₆	Data Valid ⁽²⁾
FIELD (<i>FPDC_DATAE_P</i>)	C15	I ₆	Field—This can be used as the 2-D field signal for interlaced sources as well as the 3-D TOPFIELD signal for decimated frame sequential 3-D sources.
3D_REF (<i>FPDC_DATAE_N</i>)	D15	I ₆	3D Left/Right Reference
(RGB 10,10,10)			
PDATA_A0 (<i>FPDA_CLK_P</i>)	H3	I ₆	Channel A Data (bit weight 0.25)
PDATA_A1 (<i>FPDA_CLK_N</i>)	H4		Channel A Data (bit weight 0.5)
PDATA_A2 (<i>FPDA_DATAA_P</i>)	G1		Channel A Data (bit weight 1)
PDATA_A3 (<i>FPDA_DATAA_N</i>)	G2		Channel A Data (bit weight 2)
PDATA_A4 (<i>FPDA_DATAAB_P</i>)	F3		Channel A Data (bit weight 4)
PDATA_A5 (<i>FPDA_DATAAB_N</i>)	F4		Channel A Data (bit weight 8)
PDATA_A6 (<i>FPDA_DATAAC_P</i>)	E1		Channel A Data (bit weight 16)
PDATA_A7 (<i>FPDA_DATAAC_N</i>)	E2		Channel A Data (bit weight 32)
PDATA_A8 (<i>FPDA_DATAD_P</i>)	D3		Channel A Data (bit weight 64)
PDATA_A9 (<i>FPDA_DATAD_N</i>)	D4		Channel A Data (bit weight 128)
(RGB 10,10,10)			
PDATA_B0 (<i>FPDB_CLK_P</i>)	A4	I ₆	Channel B Data (bit weight 0.25)
PDATA_B1 (<i>FPDB_CLK_N</i>)	B4		Channel B Data (bit weight 0.5)
PDATA_B2 (<i>FPDB_DATAA_P</i>)	C5		Channel B Data (bit weight 1)
PDATA_B3 (<i>FPDB_DATAA_N</i>)	D5		Channel B Data (bit weight 2)
PDATA_B4 (<i>FPDB_DATAAB_P</i>)	A6		Channel B Data (bit weight 4)
PDATA_B5 (<i>FPDB_DATAAC_P</i>)	C7		Channel B Data (bit weight 8)
PDATA_B6 (<i>FPDB_DATAAC_N</i>)	D7		Channel B Data (bit weight 16)
PDATA_B7 (<i>FPDB_DATAD_P</i>)	A8		Channel B Data (bit weight 32)
PDATA_B8 (<i>FPDB_DATAD_N</i>)	B8		Channel B Data (bit weight 64)
PDATA_B9 (<i>FPDB_DATAE_P</i>)	C9		Channel B Data (bit weight 128)
(RGB 10,10,10)			

Table 4-5. Parallel Port Input Data and Control (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION PARALLEL RGB MODE
NAME	NO.		
PDATA_C0 (FPDC_CLK_P)	A10	I ₆	Channel C Data (bit weight 0.25)
PDATA_C1 (FPDC_CLK_N)	B10		Channel C Data (bit weight 0.5)
PDATA_C2 (FPDC_DATAA_P)	C11		Channel C Data (bit weight 1)
PDATA_C3 (FPDC_DATAA_N)	D11		Channel C Data (bit weight 2)
PDATA_C4 (FPDC_DATAB_P)	A12		Channel C Data (bit weight 4)
PDATA_C5 (FPDC_DATAB_N)	B12		Channel C Data (bit weight 8)
PDATA_C6 (FPDC_DATAAC_P)	C13		Channel C Data (bit weight 16)
PDATA_C7 (FPDC_DATAAC_N)	D13		Channel C Data (bit weight 32)
PDATA_C8 (FPDC_DATAAD_P)	A14		Channel C Data (bit weight 64)
PDATA_C9 (FPDC_DATAAD_N)	B14		Channel C Data (bit weight 128)

- (1) See Table 4-13 for more information on I/O definitions.
(2) If the DATEN is not actively driven, then it must be pulled up to 3.3V with a weak pullup resistor (50kΩ max).

Table 4-6. DMD Reset and Low Speed Interfaces

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
DMD_LS0_CLK_P DMD_LS0_CLK_N	AH17 AG17	O ₂	DMD low speed differential interface, Port 0 Clock
DMD_LS0_WDATA_P DMD_LS0_WDATA_N	AK16 AJ16	O ₂	DMD low speed differential interface, Port 0 Write Data
DMD_LS1_CLK_P DMD_LS1_CLK_N	AH15 AG15	O ₂	DMD low speed differential interface, Port 1 Clock ⁽²⁾
DMD_LS1_WDATA_P DMD_LS1_WDATA_N	AK14 AJ14	O ₂	DMD low speed differential interface, Port 1 Write Data ⁽²⁾
DMD_LS0_RDATA	AH13	I ₃	DMD, low speed single ended serial interface, Port 0 Read Data ⁽³⁾
DMD_LS1_RDATA	AG13	I ₃	DMD, low speed single ended serial interface, Port 1 Read Data ^{(2) (3)} . If this port is not used, this signal requires an external pullup or pulldown to keep this input from floating.
DMD_DEN_ARSTZ	AK12	O ₃	DMD driver enable signal or Active Low Asynchronous Reset ('1' = Enabled, '0' = Reset) This signal is driven low after the DMD is parked and before power is removed from the DMD. If the 1.8V power to the DLPC7530 is independent of the 1.8V power to the DMD, then an external pulldown resistor must be used to hold the signal low in the event the DLPC7530 power is inactive while DMD power is applied.

- (1) See Table 4-13 for more information on I/O definitions.
(2) DMD LS1 port is reserved for single controller, two DMD applications.
(3) All control interface reads make use of the single ended low speed signals. The read data is clocked by the low speed differential write clock.

Table 4-7. DMD HSSI (High Speed Serial Interface)

PIN ⁽¹⁾		TYPE ⁽²⁾	DESCRIPTION
NAME	NO.		
DMD_HSSI0_CLK_P DMD_HSSI0_CLK_N	AK25 AJ25	O ₇	DMD high speed serial interface, Port 0 Clock Lane

Table 4-7. DMD HSSI (High Speed Serial Interface) (continued)

PIN ⁽¹⁾		TYPE ⁽²⁾	DESCRIPTION
NAME	NO.		
DMD_HSSI0_D0_P	AK29	O ₇	DMD high speed serial interface, Port 0 Data Lanes
DMD_HSSI0_D0_N	AJ29		
DMD_HSSI0_D1_P	AH28		
DMD_HSSI0_D1_N	AG28		
DMD_HSSI0_D2_P	AK27		
DMD_HSSI0_D2_N	AJ27		
DMD_HSSI0_D3_P	AH26		
DMD_HSSI0_D3_N	AG26		
DMD_HSSI0_D4_P	AH24		
DMD_HSSI0_D4_N	AG24		
DMD_HSSI0_D5_P	AK23		
DMD_HSSI0_D5_N	AJ23		
DMD_HSSI0_D6_P	AH22		
DMD_HSSI0_D6_N	AG22		
DMD_HSSI0_D7_P	AK21		
DMD_HSSI0_D7_N	AJ21		
DMD_HSSI1_CLK_P	AH7	O ₇	DMD high speed serial interface, Port 1 Clock Lane
DMD_HSSI1_CLK_N	AG7		
DMD_HSSI1_D0_P	AH11	O ₇	DMD high speed serial interface, Port 1 Data Lanes
DMD_HSSI1_D0_N	AG11		
DMD_HSSI1_D1_P	AK10		
DMD_HSSI1_D1_N	AJ10		
DMD_HSSI1_D2_P	AH9		
DMD_HSSI1_D2_N	AG9		
DMD_HSSI1_D3_P	AK8		
DMD_HSSI1_D3_N	AJ8		
DMD_HSSI1_D4_P	AK6		
DMD_HSSI1_D4_N	AJ6		
DMD_HSSI1_D5_P	AH5		
DMD_HSSI1_D5_N	AG5		
DMD_HSSI1_D6_P	AK4		
DMD_HSSI1_D6_N	AJ4		
DMD_HSSI1_D7_P	AK2		
DMD_HSSI1_D7_N	AJ2		
HSSI_ATETEST	AJ12	O ₇	Manufacturing Test use only—Must be left open (that is, unconnected)

- (1) A number of pin remapping options are available for the HSSI high speed channels to aid with optimizing board signal routing. See [Section 6.3.6](#) for information on these pin remapping options.
- (2) See [Table 4-13](#) for more information on I/O definitions.

Table 4-8. Program Memory (FLASH) Interface

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
PM_CSZ_0	T27	O ₈	Chip select: boot FLASH only (Boot FLASH must use this chip select.)
PM_CSZ_1	T28	O ₈	Chip select:
PM_CSZ_2	T29	O ₈	Chip select: additional peripheral device
PM_ADDR_0	T30	O ₈	Address bit (LSB)
PM_ADDR_1	U26	O ₈	Address bit
PM_ADDR_2	U27	O ₈	Address bit
PM_ADDR_3	U29	O ₈	Address bit
PM_ADDR_4	U30	O ₈	Address bit
PM_ADDR_5	V29	O ₈	Address bit
PM_ADDR_6	V28	O ₈	Address bit
PM_ADDR_7	V27	O ₈	Address bit
PM_ADDR_8	V26	O ₈	Address bit
PM_ADDR_9	W30	O ₈	Address bit

Table 4-8. Program Memory (FLASH) Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
PM_ADDR_10	W29	O ₈	Address bit
PM_ADDR_11	W28	O ₈	Address bit
PM_ADDR_12	W26	O ₈	Address bit
PM_ADDR_13	Y30	O ₈	Address bit
PM_ADDR_14	Y29	O ₈	Address bit
PM_ADDR_15	Y28	O ₈	Address bit
PM_ADDR_16	Y27	O ₈	Address bit
PM_ADDR_17	Y26	O ₈	Address bit
PM_ADDR_18	AA30	O ₈	Address bit
PM_ADDR_19	AA29	O ₈	Address bit
PM_ADDR_20	AA27	O ₈	Address bit
PM_ADDR_21	AA26	O ₈	Address bit
PM_ADDR_22	AB29	O ₈	Address bit
PM_ADDR_23 (GPIO_47)	AB28	B ₈	Address bit (MSB) ⁽²⁾
PM_WEZ	R28	O ₈	Write enable (active low)
PM_OEZ	R29	O ₈	Output enable (active low)
PM_BLSZ_0	R30	O ₈	Lower Byte (7:0) Enable (active low)—only applicable to devices using PM_CSZ_1 or PM_CSZ_2
PM_BLSZ_1	T26	O ₈	Upper Byte (15:8) Enable (active low)—only applicable to devices using PM_CSZ_1 or PM_CSZ_2
PM_Data_0	L29	B ₈	Data bit
PM_Data_1	L30	B ₈	Data bit
PM_Data_2	L28	B ₈	Data bit
PM_Data_3	M27	B ₈	Data bit
PM_Data_4	M28	B ₈	Data bit
PM_Data_5	M29	B ₈	Data bit
PM_Data_6	M30	B ₈	Data bit
PM_Data_7	N26	B ₈	Data bit
PM_Data_8	N27	B ₈	Data bit
PM_Data_9	N29	B ₈	Data bit
PM_Data_10	N30	B ₈	Data bit
PM_Data_11	P26	B ₈	Data bit
PM_Data_12	P27	B ₈	Data bit
PM_Data_13	P28	B ₈	Data bit
PM_Data_14	P29	B ₈	Data bit
PM_Data_15	R26	B ₈	Data bit

(1) See [Table 4-13](#) for more information on I/O definitions.

(2) The Program Memory address bus can be extended by one bit to 24 bits by making use of GPIO_47. Add an external pull-down resistor when this GPIO is configured for this purpose.

Table 4-9. Peripheral Interfaces

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IIC0_SCL	E27	B ₁₃	I ² C Port 0 (controller-target). Typically, target for host command and control to controller, SCL (bidirectional, open-drain): An external pullup is required. The minimum acceptable value for this pullup is 1KΩ.

Table 4-9. Peripheral Interfaces (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IIC0_SDA	D29	B ₁₃	I ² C Port 0 (controller-target). Typically, target for Host Command and Control to Controller, SDA. (bidirectional, open-drain): An external pullup is required. The minimum acceptable value for this pullup is 1K Ω .
SSP0_TXD	AD27	O ₈	SSP/SPI Port 0 Data Out (controller): transmit data pin
SSP0_RXD	AD29	I ₈	SSP/SPI Port 0 Data In (controller): receive data pin
SSP0_CLK	AD28	O ₈	SSP/SPI Port 0 clock (controller): clock pin
SSP0_CSZ_2	AC28	O ₈	SPI Port 0 chip select 2 (controller): chip select (active low) An external pullup resistor ($\leq 100k\Omega$) is suggested to avoid a floating chip select input to the external device.
SSP0_CSZ_1	AC26	O ₈	SPI Port 0 chip select 1 (controller): chip select (active low) An external pullup resistor ($\leq 100k\Omega$) is suggested to avoid a floating chip select input to the external device.
SSP0_CSZ_0	AB27	O ₈	SPI Port 0 chip select 0 (controller): chip select (active low) An external pullup resistor ($\leq 100k\Omega$) is suggested to avoid a floating chip select input to the external device.
UART0_TXD	P4	O ₈	UART Port 0 (peripheral): serial data transmit This UART port is reserved for TI debug. An external pullup resistor ($\leq 10k\Omega$) is required.
UART0_RXD	P5	I ₈	UART Port 0 (peripheral): serial data receive This UART port is reserved for TI debug. An external pullup resistor ($\leq 10k\Omega$) is required.
UART0_RTSZ	N2	O ₈	UART Port 0 (peripheral): ready to send (hardware flow control signal [active low]) This UART port is reserved for TI debug. An external pullup resistor ($\leq 10k\Omega$) is required.
UART0_CTSZ	N3	I ₈	UART Port 0 (peripheral): clear to send (hardware flow control signal [active low]) This UART port is reserved for TI debug. An external pullup resistor ($\leq 10k\Omega$) is required.
USB_DAT_P USB_DAT_N	B27 A27	B ₁₁	USB OTG Data Lane (controller-peripheral)
USB_VBUS	D26	B ₁₁	USB OTG 5V Power Supply Detection (controller-peripheral)
USB_ID	C27	I _{Other}	USB OTG Mini Receptacle Identification (controller-peripheral)
USB_TXRTUNE	C26	B _{GND}	USB OTG Reference Resistor An external reference resistor must be connected as shown in Section 9.1.7 .
USB_XI	A29	I _{GND}	USB OTG External Oscillator XI—Not used (clock provided internally) For normal operation this pin must be connected to GND.
USB_XO	B29	B _{GND}	USB OTG External Oscillator XO—Not used (clock provided internally) For normal operation this pin must be left open (unconnected).
USB_ANALOGTEST	C28	B _{Other}	USB OTG Manufacturing Test This pin must be left open (unconnected).
PMD_INTZ	AD26	I ₈	Interrupt from DLPA100 (active low) This signal requires an external pullup. It also has hysteresis.
CW_PWM	AE30	O ₈	Color wheel control PWM
CW_INDEX	AE29	I ₈	Color wheel index This pin has hysteresis.

(1) See [Table 4-13](#) for more information on I/O definitions.

Table 4-10. GPIO Peripheral Interface

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_87	K1	B ₈	General purpose I/O 87: Options: 1. Alt 0: Reserved 2. Alt 1: DAO_CLKIN (I) 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_86	L5	B ₈	General purpose I/O 86: Options: 1. Alt 0: Reserved 2. Alt 1: DAO_DI_1 (I) 3. Optional GPIO
GPIO_85	L4	B ₈	General purpose I/O 85: Options: 1. Alt 0: Reserved 2. Alt 1: DAO_DI_0 (I) 3. Optional GPIO
GPIO_84	L3	B ₈	General purpose I/O 84: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_CLKIN_2 (I) 3. Optional GPIO
GPIO_83	L2	B ₈	General purpose I/O 83: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_DI_2 (I) 3. Optional GPIO
GPIO_82	M5	B ₈	General purpose I/O 82: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_CLKIN_1 (I) 3. Optional GPIO
GPIO_81	M4	B ₈	General purpose I/O 81: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_DI_1 (I) 3. Optional GPIO
GPIO_80	M2	B ₈	General purpose I/O 80: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_CLKIN_0 (I) 3. Optional GPIO
GPIO_79	M1	B ₈	General purpose I/O 79: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_DI_0 (I) 3. Optional GPIO
GPIO_78	N5	B ₈	General purpose I/O 78: Options: 1. Alt 0: Reserved 2. Alt 1: SEQ_SYNC (B/ open drain) 3. Optional GPIO
GPIO_77	N4	B ₈	General purpose I/O 77: Options: 1. Alt 0: Reserved 2. Alt 1: EFSYNC (O)/ DASYNC (I) 3. Optional GPIO
GPIO_76	AD5	B ₈	General purpose I/O 76: Options: 1. Alt 0: AWC1_DACD_PWMB_1 (O) 2. Alt 1: N/A 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_75	AC1	B ₈	General purpose I/O 75: Options: 1. Alt 0: AWC1_DACS_PWMA_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_74	AC2	B ₈	General purpose I/O 74: Options: 1. Alt 0: AWC1_DACD_PWMB_0 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_73	AC4	B ₈	General purpose I/O 73: Options: 1. Alt 0: AWC1_DACS_PWMA_0 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_72	AC5	B ₈	General purpose I/O 72: Options: 1. Alt 0: AWC1_DACCLK_0_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_71	AD1	B ₈	General purpose I/O 71: Options: 1. Alt 0: AWC1_OUT_ENZ (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_70	AD2	B ₈	General purpose I/O 70: Options: 1. Alt 0: AWC0_DACD_PWMB_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_69	AD3	B ₈	General purpose I/O 69: Options: 1. Alt 0: AWC0_DACS_PWMA_1 (O) 2. Alt 1: MEMAUX_1 (O) (#2) 3. Optional GPIO
GPIO_68	AD4	B ₈	General purpose I/O 68: Options: 1. Alt 0: AWC0_DACD_PWMB_0 (O) 2. Alt 1: IIC2_SDA (B) (#3) 3. Optional GPIO
GPIO_67	AF4	B ₈	General purpose I/O 67: Options: 1. Alt 0: AWC0_DACS_PWMA_0 (O) 2. Alt 1: IIC2_SCL (B) (#3) 3. Optional GPIO
GPIO_66	AE2	B ₈	General purpose I/O 66: Options: 1. Alt 0: AWC0_DACCLK_0_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_65	AE3	B ₈	General purpose I/O 65: Options: 1. Alt 0: AWC0_OUT_ENZ (O) 2. Alt 1: N/A 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_64	AE4	B ₈	General purpose I/O 64: Options: 1. Alt 0: OCLKB (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_63	AG2	B ₈	General purpose I/O 63: Options: 1. Alt 0: PWM_OUT_UVLED (O) 2. Alt 1: OCLKD (O) (#2) 3. Optional GPIO
GPIO_62	AG3	B ₈	General purpose I/O 62: Options: 1. Alt 0: PWM_OUT_IRLED (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_61	AF1	B ₈	General purpose I/O 61: Options: 1. Alt 0: PWM_OUT_BLED (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_60	AF2	B ₈	General purpose I/O 60: Options: 1. Alt 0: PWM_OUT_GLED (O) 2. Alt 1: UART2_RXD (I) (#2) 3. Optional GPIO
GPIO_59	AG1	B ₈	General purpose I/O 59: Options: 1. Alt 0: PWM_OUT_RLED (O) 2. Alt 1: UART2_TXD (O) (#2) 3. Optional GPIO
GPIO_58	V1	B ₈	General purpose I/O 58: Options: 1. Alt 0: PWM_OUT_STD_2 (O) 2. Alt 1: ALF_COAST (O) 3. Optional GPIO
GPIO_57	V2	B ₈	General purpose I/O 57: Options: 1. Alt 0: PWM_OUT_STD_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_56	W2	B ₈	General purpose I/O 56: Options: 1. Alt 0: PWM_OUT_STD_0 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_55	K29	B ₈	General purpose I/O 55: Options: 1. Alt 0: PWM_OUT_CW2 (O) 2. Alt 1: 3. Optional GPIO
GPIO_54	K28	B ₈	General purpose I/O 54: Options: 1. Alt 0: PWM_OUT_CW1 (O) 2. Alt 1: N/A 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_53	W3	B ₈	General purpose I/O 53: Options: 1. Alt 0: Reserved 2. Alt 1: LED_DRIVER_ON (O) 3. Optional GPIO
GPIO_52	W4	B ₈	General purpose I/O 52: Options: 1. Alt 0: Reserved 2. Alt 1: N/A 3. Optional GPIO
GPIO_51	V5	B ₈	General purpose I/O 51: Options: 1. Alt 0: Reserved 2. Alt 1: DMD_PWR_EN (O) 3. Optional GPIO
GPIO_50	AC29	B ₈	General purpose I/O 50: Options: 1. Alt 0: SSP0_CSZ_3 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_49	AC30	B ₈	General purpose I/O 49: Options: 1. Alt 0: SSP0_CSZ_4 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_48	AB26	B ₈	General purpose I/O 48: Options: 1. Alt 0: USB_OTG_External_USB_Switch_Control (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_47	AB28	B ₈	General purpose I/O 47: Options: 1. Alt 0: PM_ADDR_23 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_46	K27	B ₈	General purpose I/O 46: Options: 1. Alt 0: CW_Index_2 (I) (#1) 2. Alt 1: SSP2_BC_CSZ (O-MST/I-SLV) 3. Optional GPIO
GPIO_45	J30	B ₈	General purpose I/O 45: Options: 1. Alt 0: CW_Index_1 (I) (#1) 2. Alt 1: SSP2_CSZ_2 (O-MST/I-SLV) 3. Optional GPIO
GPIO_44	J29	B ₈	General purpose I/O 44: Options: 1. Alt 0: OCLKC (O) (#1) 2. Alt 1: SSP2_CSZ_1 (O-MST/I-SLV) 3. Optional GPIO
GPIO_43	J27	B ₈	General purpose I/O 43: Options: 1. Alt 0: OCLKD (O) (#1) 2. Alt 1: SSP2_CSZ_0 (O-MST/I-SLV) 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_42	J26	B ₈	General purpose I/O 42: Options: 1. Alt 0: IIC2_SDA (B) (#1) 2. Alt 1: SSP2_DO (O) 3. Optional GPIO
GPIO_41	H30	B ₈	General purpose I/O 41: Options: 1. Alt 0: IIC2_SCL (B) (#1) 2. Alt 1: SSP2_DI (I) 3. Optional GPIO
GPIO_40	H29	B ₈	General purpose I/O 40: Options: 1. Alt 0: MEMAUX_1 (O) (#1) 2. Alt 1: SSP2_SCLK (O-MST/I-SLV) 3. Optional GPIO
GPIO_39	H28	B ₈	General purpose I/O 39: Options: 1. Alt 0: UART2_RXD (I) (#1) 2. Alt 1: HBT_CLKOUT (O) 3. Optional GPIO
GPIO_38	H27	B ₈	General purpose I/O 38: Options: 1. Alt 0: UART2_TXD (O) (#1) 2. Alt 1: HBT_DO (O) 3. Optional GPIO
GPIO_37	H26	B ₈	General purpose I/O 37: Options: 1. Alt 0: CW_Index_2 (I) (#2) 2. Alt 1: DAO_CLKOUT (O) 3. Optional GPIO
GPIO_36	G30	B ₈	General purpose I/O 36: Options: 1. Alt 0: CW_Index_1 (I) (#2) 2. Alt 1: DAO_DO_1 (O) 3. Optional GPIO
GPIO_35	G29	B ₈	General purpose I/O 35: Options: 1. Alt 0: OCLKC (O) (#2) 2. Alt 1: DAO_DO_0 (O) 3. Optional GPIO
GPIO_34	Y1	B ₈	General purpose I/O 34: Options: 1. Alt 0: WRP_CAMERA_TRIG (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_33	Y2	B ₈	General purpose I/O 33: Options: 1. Alt 0: PAUX11 (O) {CW Spoke} 2. Alt 1: IIC2_SDA (B) (#2) 3. Optional GPIO
GPIO_32	Y4	B ₈	General purpose I/O 32: Options: 1. Alt 0: PAUX10 (O) {CW Rev} 2. Alt 1: IIC2_SCL (B) (#2) 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_31	Y5	B ₈	General purpose I/O 31: Options: 1. Alt 0: PAUX9 (O) {XPR-Y} 2. Alt 1: PAUX_INT3 (O) 3. Optional GPIO
GPIO_30	AA1	B ₈	General purpose I/O 30: Options: 1. Alt 0: PAUX8 (O) {XPR-X} 2. Alt 1: PAUX_INT2 (O) 3. Optional GPIO
GPIO_29	AA2	B ₈	General purpose I/O 29: Options: 1. Alt 0: PAUX7 (O) {SSI Subframe} 2. Alt 1: N/A 3. Optional GPIO
GPIO_28	AA3	B ₈	General purpose I/O 28: Options: 1. Alt 0: PAUX6 (O) {UV_LED_EN} 2. Alt 1: LEDSEL_4 (O) 3. Optional GPIO
GPIO_27	AA4	B ₈	General purpose I/O 27: Options: 1. Alt 0: PAUX5 (O) {IR_LED_EN} 2. Alt 1: LEDSEL_3 (O) 3. Optional GPIO
GPIO_26	AA5	B ₈	General purpose I/O 26: Options: 1. Alt 0: PAUX4 (O) {B_LED_EN} 2. Alt 1: LEDSEL_2 (O) 3. Optional GPIO
GPIO_25	AB2	B ₈	General purpose I/O 25: Options: 1. Alt 0: PAUX3 (O) {G_LED_EN} 2. Alt 1: LEDSEL_1 (O) 3. Optional GPIO
GPIO_24	AB3	B ₈	General purpose I/O 24: Options: 1. Alt 0: PAUX2 (O) {R_LED_EN} 2. Alt 1: LEDSEL_0 (O) 3. Optional GPIO
GPIO_23	AB4	B ₈	General purpose I/O 23: Options: 1. Alt 0: PAUX1 (O) {SEQ Index} 2. Alt 1: PAUX_INT1 (O) 3. Optional GPIO
GPIO_22	AB5	B ₈	General purpose I/O 22: Options: 1. Alt 0: PAUX0 (O) {LED SENSE} 2. Alt 1: PAUX_INT0 (O) 3. Optional GPIO
GPIO_21	P3	B ₈	General purpose I/O 21: Options: 1. Alt 0: PWM-IN1 (I) 2. Alt 1: N/A 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_20	P2	B ₈	General purpose I/O 20: Options: 1. Alt 0: PWM-IN0 (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_19	P1	B ₈	General purpose I/O 19: Options: 1. Alt 0: IR1 (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_18	R5	B ₈	General purpose I/O 18: Options: 1. Alt 0: IR0 (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_17	R4	B ₈	General purpose I/O 17: Options: 1. Alt 0: N/A 2. Alt 1: N/A 3. Optional GPIO
GPIO_16	R2	B ₈	General purpose I/O 16: Options: 1. Alt 0: UART1_RTSZ (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_15	R1	B ₈	General purpose I/O 15: Options: 1. Alt 0: UART1_CTSZ (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_14	T3	B ₈	General purpose I/O 14: Options: 1. Alt 0: UART1_RXD (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_13	T4	B ₈	General purpose I/O 13: Options: 1. Alt 0: UART1_TXD (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_12	T5	B ₈	General purpose I/O 12: Options: 1. Alt 0: IIC1_SDA (B) 2. Alt 1: N/A 3. Optional GPIO
GPIO_11	T2	B ₈	General purpose I/O 11: Options: 1. Alt 0: IIC1_SCL (B) 2. Alt 1: N/A 3. Optional GPIO
GPIO_10	V3	B ₈	General purpose I/O 10: Options: 1. Alt 0: SAS_INTGTR_EN (O) 2. Alt 1: N/A 3. Optional GPIO

Table 4-10. GPIO Peripheral Interface (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION ^{(2) (3) (4)}
NAME	NO.		
GPIO_09	U1	B ₈	General purpose I/O 09: Options: 1. Alt 0: SAS_CSZ (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_08	U2	B ₈	General purpose I/O 08: Options: 1. Alt 0: SAS_DO (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_07	U4	B ₈	General purpose I/O 07: Options: 1. Alt 0: SAS_DI (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_06	V4	B ₈	General purpose I/O 06: Options: 1. Alt 0: SAS_CLK (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_05	A17	B ₈	General purpose I/O 05: Options: 1. Alt 0: SSP1_CSZ_2 (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO
GPIO_04	B17	B ₈	General purpose I/O 04: Options: 1. Alt 0: SSP1_CSZ_1 (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO
GPIO_03	B15	B ₈	General purpose I/O 03: Options: 1. Alt 0: SSP1_CSZ_0 (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO
GPIO_02	C16	B ₈	General purpose I/O 02: Options: 1. Alt 0: SSP1_DO (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_01	D16	B ₈	General purpose I/O 01: Options: 1. Alt 0: SSP1_DI (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_00	E16	B ₈	General purpose I/O 00: Options: 1. Alt 0: SSP1_SCLK (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO

(1) See [Table 4-13](#) for more information on I/O definitions.

(2) This table defines the GPIO capabilities of the DLPC7530. Please see [Section 6.3.8](#) for specific product configuration allocations of these GPIO.

(3) Most GPIO have at least one alternate hardware functional use in addition to being available as a general purpose I/O. Depending on the product configuration, GPIO may be reserved specifically for use as an alternate hardware function (and would therefore not be

available as a general purpose I/O). More information on GPIO allocations for specific product configurations can be found in [Section 6.3.8](#).

- (4) All GPIO that are available as a general purpose I/O must be configured as an input, a standard output, or an open-drain output. This is set in the flash configuration. Configure unused GPIO as a logic zero output and leave unconnected, otherwise an external pullup or pulldown resistor is required to avoid a floating input. The reset default for all GPIO is as an input signal. An external pullup resistor ($\leq 10k\Omega$) is required for each signal configured as open-drain output.

Table 4-11. Clock and Support

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
REFCLKA_I	AJ18	I ₉	Crystal A Input: Reference clock crystal input ^{(2) (3)}
REFCLKA_O	AK18	O ₁₀	Crystal A Output: Reference clock crystal output ⁽²⁾
REFCLKB_I	B16	I ₁₄	Crystal B Input: Reference clock crystal input ^{(2) (3)}
REFCLKB_O	A16	O ₁₅	Crystal B Output: Reference clock crystal output ⁽²⁾
OCLKA	AD30	O ₈	General Purpose Output Clock A ⁽⁴⁾ Targeted for driving Color Wheel motor controller. Frequency is software programmable, with a power-up default frequency of 0.77MHz. Note: The output frequency is not affected by non-power-up reset operations (that is, the system holds the last programmed value until system is power cycled).

- (1) See [Table 4-13](#) for more information on I/O definitions.
(2) For more information on this signal see [Section 5.12](#).
(3) For applications where an external oscillator is used in place of a crystal, use an oscillator to drive this pin.
(4) For more information on this signal see [Section 5.22](#).

Table 4-12. Power and Ground

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VDD115_PLLMA	AE18	PWR	1.15V digital power for MCG (Controller Clock Generator A) PLL
VDD115_PLLMB	F15	PWR	1.15V digital power for MCG (Controller Clock Generator B) PLL
VAD115_PLLS	F16	PWR	1.15V analog power for SCG doubler PLL
VAD18_PLLMA	AE19	PWR	1.8V analog power for MCG (Controller Clock Generator A) PLL
VAD18_PLLMB	F14	PWR	1.8V analog power for MCG (Controller Clock Generator B) PLL
VAD33_OSCA	Y18	PWR	3.3V analog power for Crystal-OSC
VAD33_OSCB	L17	PWR	3.3V analog power for Crystal-OSC
VAD115_FPD	F7,F9,F11,J6,L12	PWR	1.15V analog power for FPD
VDD33_FPD	E6,E8,E10,E12,E14,G6,L11,L13	PWR	3.3V digital power for FPD
VAD115_VX1	F24,L18	PWR	1.15V analog power for VX1
VAD18_VX1	E18,L19	PWR	1.8V analog power for VX1
VAD33_USB	D27,E26,F25	PWR	3.3V analog power for USB
VDD18_SCS	L16,R6,T25,AE16	PWR	1.8V digital power for SCS DRAM
VDD121_SCS	L15,N11,P20,U11,V20,Y16	PWR	1.21-V digital power for SCS SRAM
VAD115_HSSI	Y14,Y19,AF7,AF9,AF11,AF13AF21,A F23,AF25	PWR	1.15V analog power for HSSI interface
VAD115_HSSI0_PLL	AE22	PWR	1.15V analog power for HSSI-0 PLL
VAD115_HSSI1_PLL	AE10	PWR	1.15V analog power for HSSI-1 PLL
VDD33_HSSI	Y12,Y20,AE8,AE12,AE20,AE24	PWR	3.3V digital power for HSSI interface
VAD18_LSIF	Y15,AE13,AE14	PWR	1.8V analog power for DMD low-speed interface
LVDS_VREFTEST	AF16		Manufacturing test use only; must be left open-unconnected
VDD115	L14,L20,M11,N20,P11,R20,T11,U20, V11,W20,Y11,Y13,Y17	PWR	1.15V core power

Table 4-12. Power and Ground (continued)

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
		NO.		
VDD33	H25,K25,L6,M20,M25,N6,P25,R11,T20,U6,V25,W6,W11,Y25,AA6,AB25,AC6,AD25,AE6		PWR	3.3V digital power
VSS	A1,A2,A3,A5,A7,A9,A11,A13,A15,A18,A20,A22,A24,A26,A28,A30,B1,B2,B3,B5,B7,B9,B11,B13,B18,B20,B22,B24,B26,B28,B30,C3,C4,C6,C8,C10,C12,C14,C17,C19,C21,C23,C25,C29,D1,D2,D6,D8,D10,D12,D14,D17,D19,D21,D23,D25,D28,E3,E4,E5,E7,E9,E11,E13,E15,E22,E25,E28,F1,F2,F5,F6,F8,F10,F12,F13,F17,F18,F20,F30,G3,G4,G5,G27,H1,H2,H5,H6,J3,J4,J5,J25,J28,K6,K30,L1,L25,L27,M3,M6,(M12),(M13),(M14),(M15),(M16),(M17),(M18),(M19),N1,(N12),(N13),(N14),(N15),(N16),(N17),(N18),(N19),N25,N28,P6,(P12),(P13),(P14),(P15),(P16),(P17),(P18),(P19),P30,R3,(R12),(R13),(R14),(R15),(R16),(R17),(R18),(R19),R25,R27,T1,T6,(T12),(T13),(T14),(T15),(T16),(T17),(T18),(T19),U3,U5,(U12),(U13),(U14),(U15),(U16),(U17),(U18),(U19),U25,U28,V6,(V12),(V13),(V14),(V15),(V16),(V17),(V18),(V19),V30,W1,W5,(W12),(W13),(W14),(W15),(W16),(W17),(W18),(W19),W25,W27,Y3,Y6,AA25,AA28,AB1,AB6,AB30,AC3,AC25,AC27,AD6,AE1,AE5,AE7,AE9,AE11,AE15,AE17,AE21,AE23,AE25,AE26,AE28,AF3,AF5,AF6,AF8,AF10,AF12,AF14,AF15,AF17,AF18,AF19,AF20,AF22,AF24,AF26,AF28,AF30,AG4,AG6,AG8,AG10,AG12,AG14,AG16,AG18,AG23,AG25,AG27,AG29,AH1,AH2,AH3,AH4,AH6,AH8,AH10,AH12,AH14,AH16,AH18,AH21,AH23,AH25,AH27,AH29,AH30,AJ1,AJ3,AJ5,AJ7,AJ9,AJ11,AJ13,AJ15,AJ17,AJ22,AJ24,AJ26,AJ28,AJ30,AK1,AK3,AK5,AK7,AK9,AK11,AK13,AK15,AK17,AK22,AK24,AK26,AK28,AK30		RTN	GND for all power supplies. Ball numbers in parenthesis are also used as thermal balls and are located within the package center region.
VPGM	G25			Manufacturing use only (efuse); must be tied to ground

(1) See [Table 4-13](#) for more information on I/O definitions.

Table 4-13. I/O Type Subscript Definition

TYPE		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8V SERDES (VX1)	VAD18_VX1	ESD diode to supply rail and GND
2	1.8V LVDS (LS DMD)	VAD18_LSIF	ESD diode to supply rail and GND
3	1.8V LCMOS (LS DMD)	VAD18_LSIF	ESD diode to supply rail and GND
4	3.3V OpenDrain (VX1)	VDD33	ESD diode to supply rail and GND
5	3.3V LVDS (FPD)	VDD33_FPD	ESD diode to supply rail and GND
6	3.3V LVCMOS (PP)	VDD33_FPD	ESD diode to supply rail and GND
7	1.15V HSSI (HS DMD)	VAD115_HSSI	ESD diode to supply rail and GND
8	3.3V LVCMOS I/O (8ma output drive - GPIO, etc.)	VDD33	ESD diode to supply rail and GND
9	3.3V LVCMOS I/O (OSC)	VAD33_OSCA	ESD diode to GND
10	3.3V LVCMOS I/O (OSC)	VAD33_OSCA	ESD diode to supply rail and GND
11	3.3V USB (USB)	VAD33_USB	ESD diode and LBJT to GND
12	3.3V LVCMOS (USB)	VAD33_USB	ESD diode to supply rail and GND
13	3.3V OpenDrain (I2C)	VDD33	ESD diode to supply rail and GND
14	3.3V LVCMOS I/O (OSC)	VAD33_OSCB	ESD diode to GND
15	3.3V LVCMOS I/O (OSC)	VAD33_OSCB	ESD diode to supply rail and GND
TYPE			
I	Input		N/A
O	Output		
B	Bidirectional		
PWR	Power		
RTN	Ground return		

Table 4-14. Internal Pullup and Pulldown Characteristics

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS ⁽¹⁾	CONDITIONS	MIN	MAX	UNIT
Weak pullup resistance	V _{IN} = 0.8V, VDD33 = 3.3V	19	50	kΩ
	V _{IN} = 2.0V, VDD33 = 3.3V	12	39	kΩ

(1) An external 5.7kΩ or less pullup or pulldown resistor (if needed) is sufficient for any voltage condition to correctly override any associated internal pullup or pulldown resistance.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)⁽¹⁾

SUPPLY VOLTAGE ⁽²⁾	MIN	MAX	UNIT
V _(VDD115) (Core)	-0.3	1.6	V
V _(VDD115_PLLMA) (Core)	-0.3	1.6	V
V _(VDD115_PLLMB) (Core)	-0.3	1.6	V
V _(VDD115_PLLS) (Core)	-0.3	1.6	V
V _(VAD115_FPD) (Core)	-0.3	1.6	V
V _(VAD115_VX1) (Core)	-0.5	1.5	V
V _(VAD115_HSSI) (Core)	-0.3	1.6	V
V _(VAD115_HSSI0_PLL) (Core)	-0.3	1.6	V
V _(VAD115_HSSI1_PLL) (Core)	-0.3	1.6	V
V _(VDD121_SCS) (Core)	-0.4	1.6	V
V _(VAD18_PLLMA) (Core)	-0.3	2.5	V

Over operating free-air temperature (unless otherwise noted)⁽¹⁾

SUPPLY VOLTAGE ⁽²⁾		MIN	MAX	UNIT
$V_{(VAD18_PLLMB)}$ (Core)		-0.3	2.5	V
$V_{(VAD18_VX1)}$ (I/O)		-0.5	2.5	V
$V_{(VDD18_SCS)}$ (Core)		-0.4	2.3	V
$V_{(VDD18_LVDS)}$ (I/O)		-0.3	2.5	V
$V_{(VDD33)}$ (I/O)		-0.3	3.9	V
$V_{(VAD33_OSCA)}$ (I/O)		-0.3	3.9	V
$V_{(VAD33_OSCB)}$ (I/O)		-0.3	3.9	V
$V_{(VDD33_FPD)}$ (I/O)		-0.3	3.9	V
$V_{(VAD33_USB)}$ (I/O)		-0.3	3.9	V
$V_{(VDD33_HSSI)}$ (I/O)		-0.3	3.9	V
GENERAL				
T_J	Operating junction temperature	0	115	°C
T_C	Operating case temperature	0	108 ⁽³⁾	°C
I_{lat}	Latch-up	-100	100	mA
T_{stg}	Storage temperature range	-40	125	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to GND.
- (3) Value calculated using package parameters defined in [Section 5.4](#).

5.2 ESD Ratings

PARAMETER		VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI-ESDA-JEDEC JS-001 ⁽¹⁾	V	
		All pins (except Vx1_CM_CKREF0, 1, 2, 3)		±1000
		Vx1_CM_CKREF0, 1, 2, 3		±750
		Charged device model (CDM), per ANSI-ESDA-JEDEC JS-002 ⁽²⁾		±500
		All pins (except Vx1_CM_CKREF0, 1, 2, 3)	+500	
		Vx1_CM_CKREF0, 1, 2, 3	-200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TOLERANCE	MIN	NOM	MAX	UNIT
V _(VDD115) (Core)	1.15V Power	± 4.35% tolerance	1.10	1.15	1.20	V
V _(VDD115_PLLMA) (Core)	1.15V Digital Power - MCG-A PLL (Controller Clock Generator)	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
V _(VDD115_PLLMB) (Core)	1.15V Digital Power - MCG-B PLL (Controller Clock Generator)	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
V _(VDD115_PLLS) (Core)	1.15V Analog Power - SCG Doubler PLL	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
V _(VAD115_FPD) (Core)	1.15V Analog Power - FPD	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
V _(VAD115_VX1) (Core)	1.15V Analog Power - VX1	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
V _(VAD115_HSSI) (Core)	1.15V Analog Power - HSSI	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
ΔV _(VAD115_HSSI) (Core)	pk-pkVAD115_HSSI supply noise @ 10MHz (sine)				20	mV
V _(VAD115_HSSI0_PLL) (Core)	1.15V Analog Power - HSSI0 PLL	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
ΔV _(VAD115_HSSI0_PLL) (Core)	pk-pkVAD115_HSSI0_PLL supply noise @ 10MHz (sine)				20	mV
V _(VAD115_HSSI1_PLL) (Core)	1.15V Analog Power - HSSI1 PLL	+4.35/–9.13% tolerance	1.045	1.15	1.20	V
ΔV _(VAD115_HSSI1_PLL) (Core)	pk-pkVAD115_HSSI1_PLL supply noise @ 10MHz (sine)				20	mV
V _(VDD121_SCS) (Core)	1.21V Digital Power - SCS DRAM	+7.43/–4.95% tolerance	1.15	1.21	1.30	V
V _(VAD18_PLLMA) (Core)	1.8V Analog Power - MCG-A PLL (Controller Clock Generator)	±5.0% tolerance	1.71	1.80	1.89	V
V _(VAD18_PLLMB) (Core)	1.8V Analog Power - MCG-B PLL (Controller Clock Generator)	±5.0% tolerance	1.71	1.80	1.89	V
V _(VAD18_VX1) (I/O)	1.8V Analog Power - VX1 Interface	±5.0% tolerance	1.71	1.80	1.89	V
V _(VDD18_SCS) (Core)	1.8V Digital Power - SCS DRAM	±5.0% tolerance	1.71	1.80	1.89	V
V _(VDD18_LVDS) (I/O)	1.8V Analog Power - DMD LS Interface	±5.0% tolerance	1.71	1.80	1.89	V
V _(VDD33) (I/O)	3.3V Digital Power - (All 3.3V I/O without dedicated 3.3V supply - for example, GPIO)	±5.0% tolerance	3.135	3.3	3.465	V
V _(VAD33_OSCA) (I/O)	3.3V Analog Power - Crystal-OSCA Interface	±5.0% tolerance	3.135	3.3	3.465	V
V _(VAD33_OSCB) (I/O)	3.3V Analog Power - Crystal-OSCB Interface	±5.0% tolerance	3.135	3.3	3.465	V
V _(VDD33_FPD) (I/O)	3.3V Digital Power - FPD interface	±5.0% tolerance	3.135	3.3	3.465	V
V _(VAD33_USB) (I/O)	3.3V Analog Power - USB Interface	±5.0% tolerance	3.135	3.3	3.465	V
V _(VDD33_HSSI) (I/O)	3.3V Digital Power - DMD HSSI Interface	±5.0% tolerance	3.135	3.3	3.465	V

5.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TOLERANCE	MIN	NOM	MAX	UNIT
$\Delta V_{(VDD33_HSSI)} (I/O)$	pk-pkVDD33_HSSI supply noise @ 10MHz (sine)				60	mV
GENERAL						
T_J	Operating junction temperature		0		115	°C
T_C	Operating case temperature		0		108	°C
T_A	Operating ambient temperature (1) (2)		0		55	°C

(1) The operating ambient temperature range values were determined based on the board design parameters described in [Section 9.1.1](#), rather than using a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Ambient thermal conditions, which impact $R_{\theta JA}$, vary by application. Thus, maximum operating ambient temperature varies by application.

a. $T_{a_min} = T_{j_min} - (P_{d_min} \times R_{\theta JA}) = 0^\circ\text{C} - (\text{host_min_valueW} \times \text{host_value}^\circ\text{C/W}) = -\text{host_calculated_value}^\circ\text{C}$

b. $T_{a_max} = T_{j_max} - (P_{d_max} \times R_{\theta JA}) = +115^\circ\text{C} - (\text{host_max_valueW} \times \text{host_value}^\circ\text{C/W}) = +\text{host_calculated_value}^\circ\text{C}$

(2) Operating ambient temperature is dependent on system thermal design. Operating case temperature cannot exceed its specified range across ambient temperature conditions.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TEST CONDITIONS ⁽²⁾	ZDC	UNIT
			P-HBGA676	
			676 PINS (576 Populated)	
R _{θJA}	Junction-to-air thermal resistance ⁽³⁾	0m/s of forced airflow, without heatsink	7.4	°C/W
		1m/s of forced airflow, without heatsink	6.3	
		2m/s of forced airflow, without heatsink	6.0	
		1m/s of forced airflow, with heatsink, 7W	5.3	
		2m/s of forced airflow, with heatsink, 7W	4.8	
		1m/s of forced airflow, with heatsink, 15W	4.0	
		2m/s of forced airflow, with heatsink, 15W	3.5	
R _{JC}	Junction-to-case thermal resistance ⁽⁴⁾		2.7	°C/W
R _{JB}	Junction-to-board thermal resistance ⁽⁴⁾		3.5	°C/W
ψ _{JT} ⁽⁵⁾	Temperature variance from junction to package top center temperature, per unit power dissipation.	0m/s of forced airflow, without heatsink	0.6	°C/W
		1m/s of forced airflow, without heatsink	0.6	
		2 m/s of forced airflow, without heatsink	0.6	
P _{MAX}	Package - Maximum Power ^{(3) (6)}	0m/s of forced airflow, without heatsink	8.10	W
		1m/s of forced airflow, without heatsink	9.52	
		2m/s of forced airflow, without heatsink	10.00	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) These test conditions also included a PCB sized at 101.3mm x 152.4mm incorporating the recommended PCB thermal enhancements specified in [Section 9.1.1](#). In addition, airflow is parallel to the board surface directed at the device.
- (3) See [Table 5-1](#) for thermal parameters based on the example heatsinks listed below
 - a. Heatsink-7W: S1525-7W, Size = 25mm × 25 mm × 7mm, Pins = 7 × 7 = 49 (Vendor: Alpha, Type S Series)
 - b. Heatsink-15W: S1530-15W, Size = 30mm × 3 0mm x 15mm, Pins = 8 × 8 = 64 (Vendor: Alpha, Type S Series)
- (4) Due to the complex internal construction of the DLPC7530 controller, the R_{JC} and R_{JB} thermal coefficients do not always produce an accurate junction temperature estimate. A limited set of comparison scenario data shows that the R_{JC} and R_{JB} modeled junction temperature can have a +9% to -2% error vs the actual temperature. The amount of this error varies with the use and size of an external heat sink as well as the amount of external air flow. Validate all thermal estimates based on R_{JC} and R_{JB} with an actual temperature measurement at the top-center of the package plus the delta-temp defined by ψ_{JT}.
- (5) Example: Using the power we expect of 11.31W
 $11.31W \times 0.6 \text{ } ^\circ\text{C/W} = 6.786 \text{ } ^\circ\text{C} \Rightarrow T_{C\text{-max}} = 115 \text{ } ^\circ\text{C} - \sim 7^\circ\text{C} = 108^\circ\text{C}$
- (6) $P_{MAX} = (T_{J\text{-max}} - T_{A\text{-max}}) / R_{\theta JA}$

Table 5-1. Thermal Examples using Two Different Heatsinks

THERMAL METRIC ⁽¹⁾		TEST CONDITIONS	ZDC	UNIT
			P-HBGA676	
			676 PINS (576 Populated)	
R _{θJA}	Junction-to-air thermal resistance	1m/s of forced airflow, with heatsink, 7W	5.3	°C/W
		2m/s of forced airflow, with heatsink, 7W	4.8	
		1m/s of forced airflow, with heatsink, 15W	4.0	
		2m/s of forced airflow, with heatsink, 15W	3.5	
P _{MAX}	Package - Maximum Power	1m/s of forced airflow, with heatsink, 7W	11.32	W
		2m/s of forced airflow, with heatsink, 7W	12.50	
		1m/s of forced airflow, with heatsink, 15W	15.00	
		2m/s of forced airflow, with heatsink, 15W	17.14	

- (1) This table show examples of what is achievable based on the two example heatsinks.

5.5 Power Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX ⁽¹⁾	UNIT
V _(VDD115)	1.15V Power	Maximum current at VDD115 = 1.2V			5640	mA
V _(VDD115_PLLMA) (Core)	1.15V Digital Power MCG-A PLL (Controller Clock Generator)	Maximum current at VDD115_PLLMA = 1.2V			6	mA
V _(VDD115_PLLMB) (Core)	1.15V Digital Power MCG-B PLL (Controller Clock Generator)	Maximum current at VDD115_PLLMB = 1.2V			6	mA
V _(VDD115_PLLS) (Core)	1.15V Analog Power SCG Doubler PLL	Maximum current at VDD115_PLLS = 1.2V			3	mA
V _(VAD115_FPD) (Core) ⁽²⁾	1.15V Analog Power FPD	Maximum current at VAD115_FPD = 1.2V Ports A and B Active, Port C inactive			99	mA
V _(VAD115_VX1) (Core) ⁽²⁾	1.15V Analog Power VX1	Maximum current at VAD115_VX1 = 1.2V 8 Lanes, with total BW = 3.0Gbps)			400	mA
V _(VAD115_HSSI) (Core)	1.15V Digital Power HSSI	Maximum current at VDD115_HSSI = 1.2V Both ports active			462	mA
V _(VAD115_HSSI0_PLL) (Core)	1.15V Digital Power HSSI0 PLL	Maximum current at VDD115_HSSI0_PLL = 1.2V Both ports active			1	mA
V _(VAD115_HSSI1_PLL) (Core)	1.15V Digital Power HSSI1 PLL	Maximum current at VDD115_HSSI1_PLL = 1.2V Both ports active			1	mA
V _(VDD121_SCS) (Core)	1.21V Digital Power SCS DRAM	Maximum current at VDD121_SCS = 1.30V			334	mA
V _(VAD18_PLLMA) (Core)	1.8V Analog Power MCG-A PLL (Controller Clock Generator)	Maximum current at VAD18_PLLMA = 1.89V			10	mA
V _(VAD18_PLLMB) (Core)	1.8V Analog Power MCG-B PLL (Controller Clock Generator)	Maximum current at VAD18_PLLMB = 1.89V			10	mA
V _(VAD18_VX1) (I/O) ⁽²⁾	1.8V Analog Power VX1 Interface	Maximum current at VAD18_VX1 = 1.89V 8 Lanes, with total BW = 3.0Gbps			41	mA
V _(VDD18_SCS) (Core)	1.8V Digital Power SCS DRAM	Maximum current at VDD18_SCS = 1.89V			327	mA
V _(VDD18_LVDS) (I/O)	1.8V Analog Power DMD LS Interface	Maximum current at VDD18_LVDS = 1.89V			31	mA
V _(VDD33) (I/O)	3.3V Digital Power - (All 3.3V I/O without dedicated 3.3V supply - for example, GPIO)	Maximum current at VDD33 = 3.3456V			28	mA
V _(VAD33_OSCA) (I/O)	3.3V Analog Power Crystal/OSCA Interface	Maximum current at VDD33_OSCA = 3.3456V			5	mA
V _(VAD33_OSCB) (I/O)	3.3V Analog Power Crystal-OSCB Interface	Maximum current at VDD33_OSCB =3.3456V			5	mA
V _(VDD33_FPD) (I/O) ⁽²⁾	3.3V Digital Power FPD interface	Maximum current at VDD33_FPD = 3.3456V Ports A and B Active, Port C inactive			102	mA

5.5 Power Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX ⁽¹⁾	UNIT
$V_{(VAD33_USB)}$ (I/O)	3.3V Analog Power USB Interface	Maximum current at VDD33_USB = 3.3456V			78	mA
$V_{(VDD33_HSSI)}$ (I/O)	3.3V Digital Power DMD HSSI Interface	Maximum current at VDD33_HSSI = 3.3456V Both ports active, with total BW = 3.0Gbps			194	mA

- (1) Vendor estimate for worst case power PVT condition = corner process, high voltage, high temperature (115°C junction).
 (2) The V-by-One® interface and FPD-Link™ receivers are never intended to be simultaneously enabled. Always disable one of these interfaces.

5.6 Pin Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	1.8V LVCMOS (I/O type 3 - LS DMD)	1.05			V
		3.3V OpenDrain (I/O type 4 - VX1)	N/A			
		3.3V LVCMOS (I/O type 6 - FPD)	$0.8 \times V_{DD33_FPD}$			
		3.3V LVCMOS (I/O type 6 - PP)	2.0			
		3.3V LVCMOS (I/O type 8 - GPIO)	2.0			
		3.3V LVCMOS (I/O type 9 - OSCA)	2.0			
		3.3V LVCMOS (I/O type 10 - OSCB)	2.0			
		3.3V OpenDrain (I/O type 13 - I2C)	$0.7 \times V_{DD33}$			
V_{IL}	Low-level input threshold voltage	1.8V LVCMOS (I/O type 3 - LS DMD)			0.6	V
		3.3V OpenDrain (I/O type 4 - VX1)			N/A	
		3.3V LVCMOS (I/O type 6 - FPD)			$0.2 \times V_{DD33_FPD}$	
		3.3V LVCMOS (I/O type 6 - PP)			0.8	
		3.3V LVCMOS (I/O type 8 - GPIO)			0.8	
		3.3V LVCMOS (I/O type 9 - OSCA)			0.8	
		3.3V LVCMOS (I/O type 10 - OSCB)			0.8	
		3.3V OpenDrain (I/O type 13 - I2C)			$0.3 \times V_{DD33}$	

5.6 Pin Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IH}	High-level input current	1.8 V LVCMOS (I/O type 3 - LS DMD)	V _{IN} = VAD18_LSIF	-10		10	μA
		3.3V OpenDrain (I/O type 4 - VX1)		N/A		N/A	
		3.3V LVCMOS (I/O type 6 - PP)		-10		10	
		3.3V LVCMOS (I/O type 8 - GPIO)	V _{IN} = VDD33	-10		10	
		3.3V LVCMOS (I/O type 9 - OSCA)	V _{IN} = VDD33	-10		10	
		3.3V LVCMOS (I/O type 10 - OSCB)	V _{IN} = VDD33	-10		10	
		3.3V OpenDrain (I/O type 13 - I2C)		-10		10	
I _{IL}	Low-level input current	1.8 V LVCMOS (I/O type 3 - LS DMD)	V _{IN} = VSS	-10		10	μA
		3.3V OpenDrain (I/O type 4 - VX1)		N/A		N/A	
		3.3V LVCMOS (I/O type 6 - PP)		-10		10	
		3.3V LVCMOS (I/O type 8 - GPIO)	V _{IN} = VSS	-10		10	
		3.3V LVCMOS (I/O type 9 - OSCA)	V _{IN} = VSS	-10		10	
		3.3V LVCMOS (I/O type 10 - OSCB)	V _{IN} = VSS	-10		10	
		3.3V OpenDrain (I/O type 13 - I2C)		-10		10	
V _{OH}	High-level output voltage	1.8 V LVCMOS (I/O type 3 - LS DMD)		VDD18 – 0.6			V
		3.3V OpenDrain (I/O type 4 - VX1)		N/A			
		3.3V LVCMOS (I/O type 6 - PP)		N/A			
		3.3V LVCMOS (I/O type 8 - GPIO)	I _{OH} = 8mA	VDD33 - 0.6			
		3.3V LVCMOS (I/O type 9 - OSCA)		N/A			
		3.3V LVCMOS (I/O type 10 - OSCB)		N/A			
		3.3V OpenDrain (I/O type 13 - I2C)		N/A			

5.6 Pin Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	1.8 V LVCMOS (I/O type 3 - LS DMD)			0.4	V
		3.3V OpenDrain (I/O type 4 - VX1)	I _{OL} = 8mA		0.4	
		3.3V LVCMOS (I/O type 6 - PP)			N/A	
		3.3V LVCMOS (I/O type 8 - GPIO)	I _{OL} = 8mA		0.4	
		3.3V LVCMOS (I/O type 9 - OSCA)			N/A	
		3.3V LVCMOS (I/O type 10 - OSCB)			N/A	
		3.3V OpenDrain (I/O type 13 - I2C)	3mA sink		0.4	
I _{OH}	High-level output current	1.8 V LVCMOS (I/O type 3 - LS DMD)		N/A		mA
		3.3V OpenDrain (I/O type 4 - VX1)		N/A		
		3.3V LVCMOS (I/O type 6 - PP)		N/A		
		3.3V LVCMOS (I/O type 8 - GPIO)	V _{OH} = VDD33 – 0.6V	8		
		3.3V LVCMOS (I/O type 9 - OSCA)		N/A	N/A	
		3.3V LVCMOS (I/O type 10 - OSCB)		N/A	N/A	
		3.3V OpenDrain (I/O type 13 - I2C)		N/A		
I _{OL}	Low-level output current	1.8 V LVCMOS (I/O type 3 - LS DMD)		N/A		mA
		3.3V OpenDrain (I/O type 4 - VX1)	V _{OL} = 0.4V	8		
		3.3V LVCMOS (I/O type 6 - PP)			N/A	
		3.3V LVCMOS (I/O type 8 - GPIO)	V _{OL} = 0.4V	8		
		3.3V LVCMOS (I/O type 9 - OSCA)		N/A	N/A	
		3.3V LVCMOS (I/O type 10 - OSCB)		N/A	N/A	
		3.3V OpenDrain (I/O type 13 - I2C)	V _{OL} = 0.6V	6	-	

5.6 Pin Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _{oz}	High-impedance leakage current	1.8 V LVCMOS (I/O type 3 - LS DMD)	N/A			μA	
		3.3V OpenDrain (I/O type 4 - VX1)	-10		10		
		3.3V LVCMOS (I/O type 6 - PP)	-10		10		
		3.3V LVCMOS (I/O type 8 - GPIO)	V _{OUT} = V _{DD33}	-10			10
		3.3V LVCMOS (I/O type 9 - OSCA)		N/A			N/A
		3.3V LVCMOS (I/O type 10 - OSCB)		N/A			N/A
		3.3V OpenDrain (I/O type 13 - I2C)		N/A			N/A

(1) The number inside each parenthesis for the I/O refers to the type defined in Table 4-13.

5.7 DMD HSSI Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V _{DIFF}	Output Peak-to-Peak Differential ⁽¹⁾ (into floating load R _{LOAD} = 100Ω)	Data	400		1000	mVppd
		Clock	590		1000	mVppd
V _{CM}	Output common mode (into floating load R _{LOAD} = 100Ω)		200		700	mV
V _{OD}	Output differential voltage ⁽¹⁾ (into floating load R _{LOAD} = 100Ω)	Data	200		500	mV
		Clock	295		500	mV
R _{DIFF}	Differential termination resistance		80	100	120	Ω
R _{TERM}	Single-ended termination resistance		40	50	60	Ω
SDD22	Differential output return loss (100MHz to 0.75 × baud)				-8	dB
SCC22	Common mode return loss (100MHz to 0.75 × baud)				-6	dB
N _{CM}	Transmitter common mode noise				(7.5% × V _{DIFF}) + 25 mV	mVppd
DJ _{DATA}	Deterministic jitter data (non-DCD)				0.20	UI pp
DJ _{CLOCK}	Deterministic jitter clock (non-DCD)				0.16	UI pp
DCD	Duty cycle distortion				0.05	UI pp
TJ	Total jitter (random + DJ)				0.30	UI pp

(1) $V_{DIFF-pp} = (V_p - V_n)_{cycle_N} - (V_p - V_n)_{cycle_N+1} = 2 \times |V_{OD}|$
See Figure 5-1.

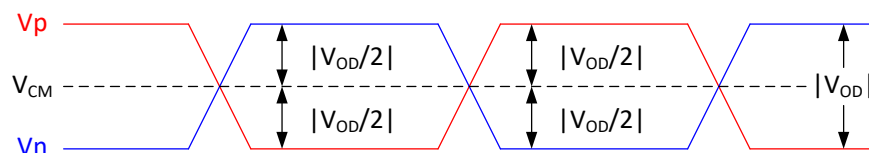


Figure 5-1. HSSI Differential Voltage Parameters

5.8 DMD Low-Speed LVDS Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{DIFF}	Output peak-to-peak differential (into $R_{LOAD} = 100\Omega$)	VAD18_LSIF (I/O type 2)	340		600	mVppd
V_{CM}	Steady-state common mode voltage	VAD18_LSIF (I/O type 2)	1100	1200	1300	mV
$ V_{OD} ^{(1)}$	Differential output voltage (into $R_{LOAD} = 100\Omega$)	VAD18_LSIF (I/O type 2)	170		300	mV
$ V_{OD}(\Delta) ^{(2)}$	V_{OD} change (between logic states)	VAD18_LSIF (I/O type 2)			25	mV
$V_{CM}(\Delta)$	V_{CM} change (between logic states)	VAD18_LSIF (I/O type 2)			25	mV
V_{OH}	Single-ended output voltage high ⁽³⁾	VAD18_LSIF (I/O type 2)			1450	mV
V_{OL}	Single-ended output voltage low ⁽³⁾	VAD18_LSIF (I/O type 2)	950			mV
TX_{term}	Internal differential termination		85	100	115	Ω

- (1) $V_{DIFF-pp} = (V_p - V_n)_{cycle_N} - (V_p - V_n)_{cycle_N+1} = 2 \times |V_{OD}|$
See Figure 5-2.
- (2) $|V_{OD}(\Delta)| = ||V_{OD}|_{cycle_N} - |V_{OD}|_{cycle_N+1}|$
- (3) $V_{OH} = 1300 + 300/2 = 1450$; $V_{OL} = 1100 - 300/2 = 950$

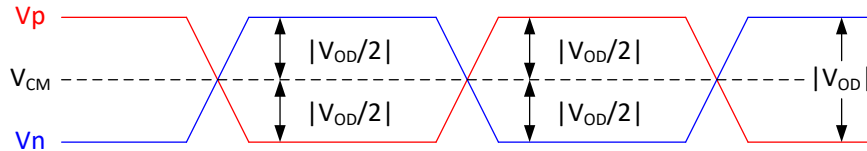


Figure 5-2. DMD Low-Speed Differential Voltage Parameters

5.9 V-by-One Interface Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER ⁽¹⁾			MIN	NOM	MAX	UNIT
V_{DIFF}	Input peak-to-peak differential	VAD18_VX1 (I/O type 1)	100			mVppd
$ V_{ID} $	Differential input voltage	VAD18_VX1 (I/O type 1)	50			mV
RX_{term}	Internal differential termination	VAD18_VX1 (I/O type 1)	80	100	120	Ω

- (1) See the [V-by-One interface standard](#) for more information.

5.10 FPD-Link LVDS Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER ⁽¹⁾			MIN	NOM	MAX	UNIT
V_{DIFF}	Input peak-to-peak differential	VDD33_FPD (I/O type 5)	200		1200	mVppd
$ V_{ID} $	Differential input voltage	VDD33_FPD (I/O type 5)	100		600	mV
V_{CM}	Steady-state common mode voltage ⁽²⁾	VDD33_FPD (I/O type 5)	0.25		2.4	V
RX_{term}	Internal differential termination	VDD33_FPD (I/O type 5)	90	110	132	Ω

- (1) See Figure 5-15.
- (2) If V_{CM} falls below $V_{CM(min)}$ at the inputs to the receiver, an open input detection circuit is automatically enabled. This detection circuit disables the receiver until the input V_{CM} rises above $V_{CM(min)}$.

5.11 USB Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER ^{(1) (2)}			MIN	NOM	MAX	UNIT
Low Speed and Full Speed (Input Level)						
V_{IH}	Single-ended input voltage high (driven)		2.0			V

5.11 USB Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER ⁽¹⁾ (2)			MIN	NOM	MAX	UNIT
V _{IHZ}	Single-ended input voltage high (floating)		2.7		3.6	V
V _{IL}	Single-ended input voltage low				0.8	V
V _{DI}	Differential input sensitivity	(DP) – (DM)	0.2			V
V _{CM}	Differential common mode voltage	Includes V _{DI} range	0.8		2.5	V
Low-Speed and Full Speed (Output Level)						
V _{OL}	Low-level output voltage	with 1.425K Ω pullup to 3.6V	0.0		0.3	V
V _{OH}	High-level output voltage	with 14.25K Ω pulldown	2.8		3.6	V
V _{CRS}	Output signal crossover voltage		1.3		2.0	V
High-Speed (Input Level)						
V _{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV
V _{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)		525		626	mV
V _{HSCM}	High-speed data signal common mode voltage		–50		500	mV
High-Speed (Output Level)						
V _{HDOI}	High-speed idle level		–10.0		10.0	mV
V _{HDOH}	High-speed data signal - high		360		440	mV
V _{HDOH}	High-speed data signal - low		–10.0		10.0	mV
V _{CHIRPJ}	High-speed chirp J level (differential voltage)		700		1100	mV
V _{CHIRPK}	High-speed chirp K level (differential voltage)		–900		–500	mV
Termination						
R _{PU}	Bus pullup resistor		1.425		1.575	K Ω
R _{PD}	Bus pulldown resistor		14.25		15.75	K Ω
Z _{HSDRV}	High-speed driver output impedance		40.5		49.5	Ω

(1) Referenced to VAD33_USB (I/O type 11)

(2) When used as a controller as part of USB OTG, the DLPC7530 requires an external USB switch to provide the USB 5V power. The example shown in [Figure 5-3](#) uses a TI TPS2500/2501 device. The example figure does not describe the required ancillary components (such as resistors and capacitors). For this information, refer to the USB switch logic data sheet for the selected device. The external USB switch is not required for product configurations that support USB peripheral mode only.

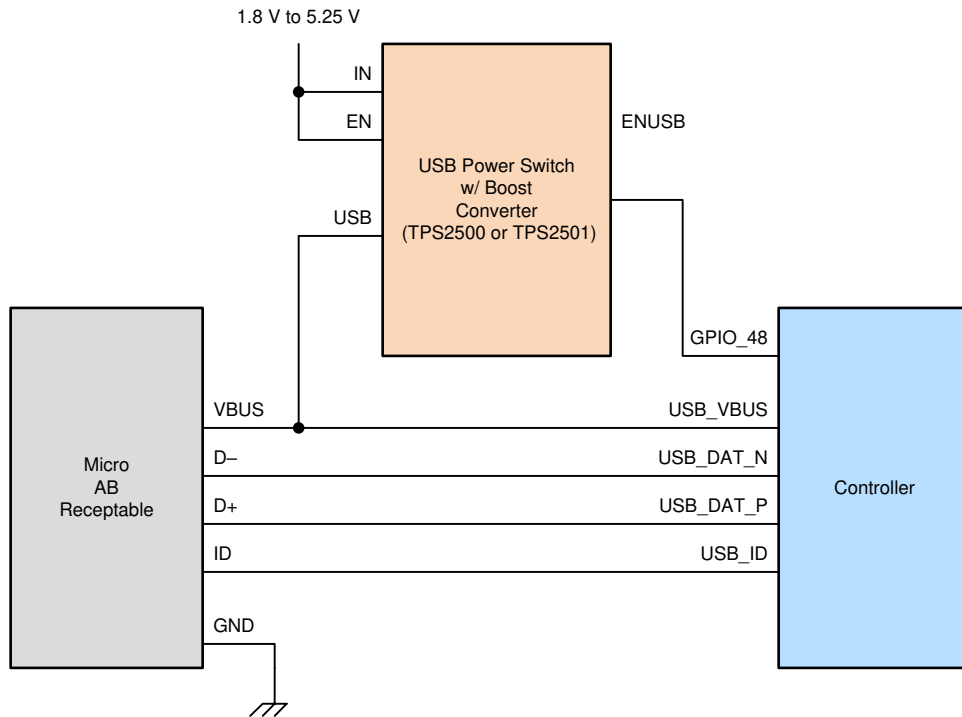


Figure 5-3. External USB Switch Example for DLPC7530 Controller as USB OTG Controller

5.12 System Oscillator Timing Requirements

PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, REFCLKA ^{(1) (2)}	PLLA: 40MHz	39.9960	40.000	40.0040	MHz
t_c	Cycle time, REFCLKA ⁽¹⁾	PLLA: 40MHz	24.9975	25.000	25.0025	ns
$t_{w(H)}$	Pulse duration ⁽³⁾ , REFCLKA, high	PLLA: 40MHz 50% to 50% reference points (signal)	11.25			ns
$t_{w(L)}$	Pulse duration ⁽³⁾ , REFCLKA, low	PLLA: 40MHz 50% to 50% reference points (signal)	11.25			ns
t_t	Transition time ⁽³⁾ , REFCLKA, $t_t = t_f / t_r$	PLLA: 40MHz 20% to 80% reference points (signal)			2.5	ns
t_{jP}	Long term periodic jitter ⁽³⁾ , REFCLKA (that is the deviation in period from ideal period due solely to high frequency jitter)	PLLA: 40MHz			18	ps
f_{clock}	Clock frequency, REFCLKB ⁽¹⁾	PLLB: 38MHz	37.9962	38.000	38.0038	MHz
t_c	Cycle time, REFCLKB ⁽¹⁾	PLLB: 38MHz	26.3132	26.3157	26.3184	ns
$t_{w(H)}$	Pulse duration ⁽³⁾ , REFCLKB, high	PLLB: 38MHz 50% to 50% reference points (signal)	11.84			ns
$t_{w(L)}$	Pulse duration ⁽³⁾ , REFCLKB, low	PLLB: 38MHz 50% to 50% reference points (signal)	11.84			ns
t_t	Transition time ⁽³⁾ , REFCLKB, $t_t = t_f / t_r$	PLLB: 38MHz 20% to 80% reference points (signal)			2.63	ns
t_{jP}	Long term periodic jitter ⁽³⁾ , REFCLKB (that is the deviation in period from ideal period due solely to high frequency jitter)	PLLB: 38MHz			18	ps

- (1) The REFCLK inputs do not support spread spectrum clock spreading.
- (2) Multi-controller systems require that a single oscillator be used to drive the REFCLKA input for all controllers in the system.
- (3) Applies only when driven through an external digital oscillator. This is a 1-sigma RMS value.

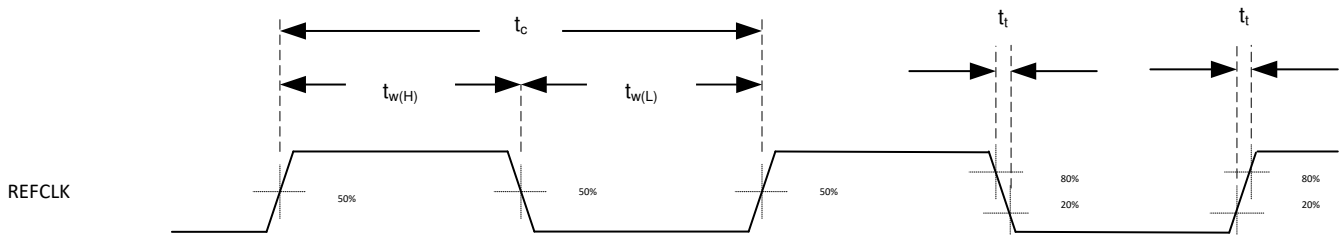


Figure 5-4. System Oscillators

5.13 Power Supply and Reset Timing Requirements

PARAMETER		MIN	MAX	UNIT
$t_{\text{RAMP-UP}}$	Power supply ramp-up time ⁽¹⁾ (Figure 5-5)	Power supply ramp for <i>each</i> supply Ramp-up time: TOV × 10% to TOV × 90% TOV = Typical Operational Voltage		ms
$t_{\text{RAMP-UP-TOTAL}}$	Total power supply ramp-up time ⁽¹⁾	Total time within which the 1.15V, 1.8V, 1.21V, and 3.3V supplies must complete their ramp-up from the start of the 1.15V ramp-up. Ramp-up time: TOV × 10% to TOV × 90% TOV = typical operational voltage		ms
$t_{\text{RAMP-DOWN}}$	Power supply ramp-down time ⁽¹⁾ (Figure 5-5, Figure 5-6)	Power supply ramp for <i>each</i> supply Ramp-down time: TOV × 90% to TOV × 10% TOV = typical operational voltage		ms
$t_{\text{RAMP-DOWN-TOTAL}}$	Total power supply ramp-down time ⁽¹⁾	Total time within which the 1.15V, 1.8V, 1.21V, and 3.3V supplies must complete their ramp-down from the start of the 3.3V ramp-up. Ramp-down time: TOV × 90% to TOV × 10% TOV = typical operational voltage		ms
t_{RUSD18}	1.8V supply ramp-up start delay ⁽²⁾ (Figure 5-6)	Delay from 1.15V supply ramp start to 1.8V supply ramp start		ms
t_{RUSD33}	3.3V supply ramp-up start delay ⁽²⁾ (Figure 5-6)	10	50	ms
t_{RUSD12}	1.21V supply ramp-up start delay, ⁽²⁾ (Figure 5-6)	Delay from 1.8V supply ramp start to 1.21V supply ramp start		ms
t_{RDSD18}	1.8V supply ramp-down start delay, ⁽²⁾ (Figure 5-6)	Delay from 1.21V supply ramp start to 1.8V supply ramp start		ms
t_{RDSD115}	1.15V supply ramp-down start delay, ⁽²⁾ (Figure 5-6)	Delay from 3.3V supply ramp start to 1.15V supply ramp start		ms
t_{EW}	Early warning time (Figure 5-8)	PWRGOOD goes inactive low (as an early warning) prior to any power supply voltage going below the controller specification		μs
t_{PH}	Power hold time (Figure 5-8)	POSENSE remains active after PWRGOOD is disabled.		μs
t_{w1}	Pulse duration, in-active low, PWRGOOD (Figure 5-7)	PWRGOOD inactive time while POSENSE is active 50% to 50% reference points (signal)		μs
t_{t1}	Transition time, PWRGOOD $t_{\text{t1}} = t_{\text{f1}}$ and t_{r1} (Figure 5-7)	Rise and Fall time for PWRGOOD 20% to 80% reference points (signal)		μs
t_{w2}	Pulse duration, in-active low, POSENSE (Figure 5-8)	POSENCE inactive time while PWRGOOD is inactive 50% to 50% reference points (signal)		ms
t_{t2}	Transition time, POSENSE $t_{\text{t1}} = t_{\text{f1}}$ and t_{r1} (Figure 5-8)	Rise and Fall time for POSENSE ⁽⁷⁾ 20% to 80% reference points (signal)		μs
t_{PSD}	PWRGOOD start delay (Figure 5-7)	51.5	60	ms
$t_{\text{PROJ_ON}}$	PROJ_ON fall time delay to PWRGOOD (Figure 5-8)	Fall Delay PROJ_ON 80% to PWRGOOD 80% fall time start		ms
t_{REFCLKA}	Time to stable REFCLKA (Figure 5-7)	Time to stable REFLCKA before POSENSE		ms

- (1) It is assumed that all 1.15V supplies come from the same source, although some can have additional filtering before entering the DLPC7530. As such, it is expected these supplies to ramp together (aside from differences caused by filtering). This same expectation is true for the 1.21V, 1.8V, and 3.3V supplies.
- (2) The DLPC7530 has specific power supply sequencing requirements, listed below, that include the timings specified in this table.
- Power Up Order:

- i. 1.15V (Core, Analog) » 1.8V (I/O, SCS) » 1.21V (SCS)
 - ii. 1.15V (Core, Analog) » 3.3V (I/O)
 - b. Power Down Order:
 - i. 3.3V (I/O) » 1.15V (Core, Analog)
 - ii. 1.21V (SCS) » 1.8V (I/O, SCS) » 1.15V (Core, Analog)
- (3) This delay requirement parameter is defined as the time between two events. The first event is the point where the 1.15V power supply ramp-up is started, and the second event is when the 1.15V supply ramp-up reaches 80% of TOV (at which point the 1.8V supply can start its ramp-up). Because the occurrence of the second event depends on the specific design of the 1.15V power supply, the designer must determine the specific delay time.
- (4) This delay requirement parameter is defined as the time between two events. The first event is the point where the 1.8V power supply ramp-up is started, and the second event is when the 1.8V supply ramp-up reaches 80% of TOV (at which point the 1.21V supply can start its ramp-up). Because the occurrence of the second event depends on the specific design of the 1.8V power supply, the designer must determine the specific delay time.
- (5) This delay requirement parameter is defined as the time between two events. The first event is the point where the 1.21V power supply ramp-down is started, and the second event is when the 1.21V supply ramp-down reaches 20% of TOV (at which point the 1.8V supply can start its ramp-down). Because the occurrence of the second event depends on the specific design of the 1.21V power supply, the designer must determine the specific delay time. The intent of this delay time is to determine that the voltage level of the 1.8V supply never falls lower than the voltage level of the 1.21V supply during the ramp-down until the 1.2V supply is below 300 mV.
- (6) This max value is only applicable if the 1.8V power remains ON while PWRGOOD is inactive. Otherwise, there is no maximum limit.
- (7) As long as noise on this signal is below the hysteresis threshold
- (8) This delay requirement parameter is defined as the time between two events. The first event is the point where the 3.3V power supply ramp-down is started, and the second event is when the 3.3V supply ramp-down and 1.8V supply ramp down reaches 10% of TOV (at which point the 1.15V supply can start its ramp-down). Because the occurrence of the second event depends on the specific design of the 3.3V and 1.8V power supply, the designer must determine the specific delay time.
- (9) If PROJ_ON is used for power down then Power Hold Time (t_{PH}) is not required.
- (10) This delay requirement parameter is defined by design of RECLKA oscillator. Stable clock must be provided before releasing POSENSE.

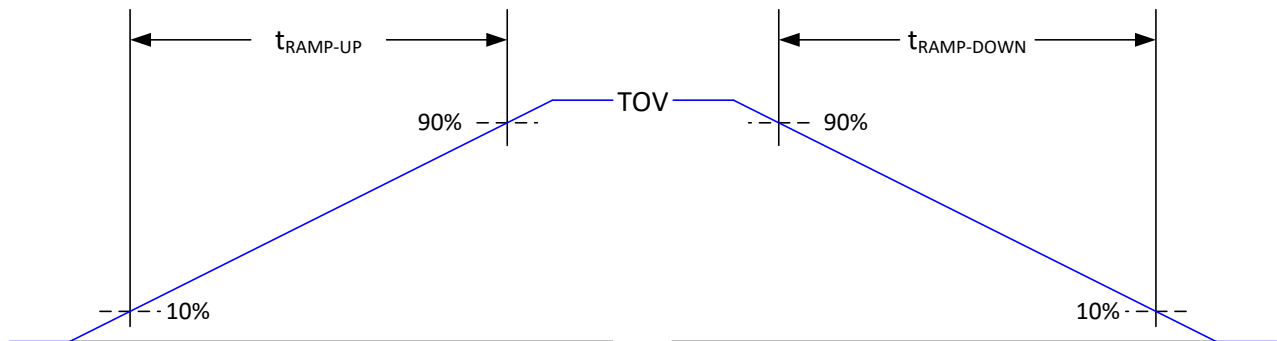
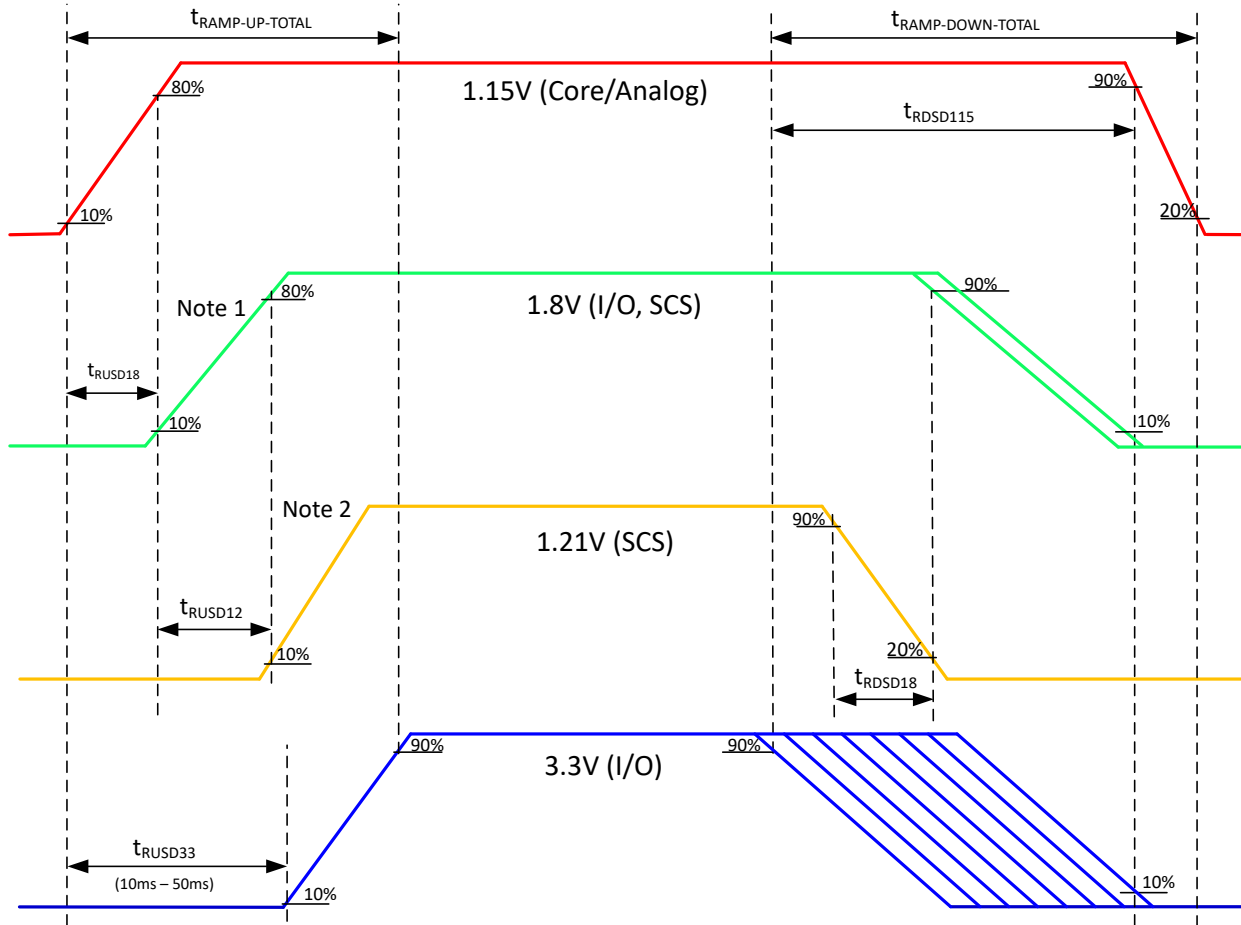


Figure 5-5. Power Supply Ramp Time



Note 1: No power up or power down timing dependency between 1.8V and 3.3V
 Note 2: No power up or power down timing dependency between 1.21V and 3.3V

Figure 5-6. Power Supply Ramp Sequencing Profiles

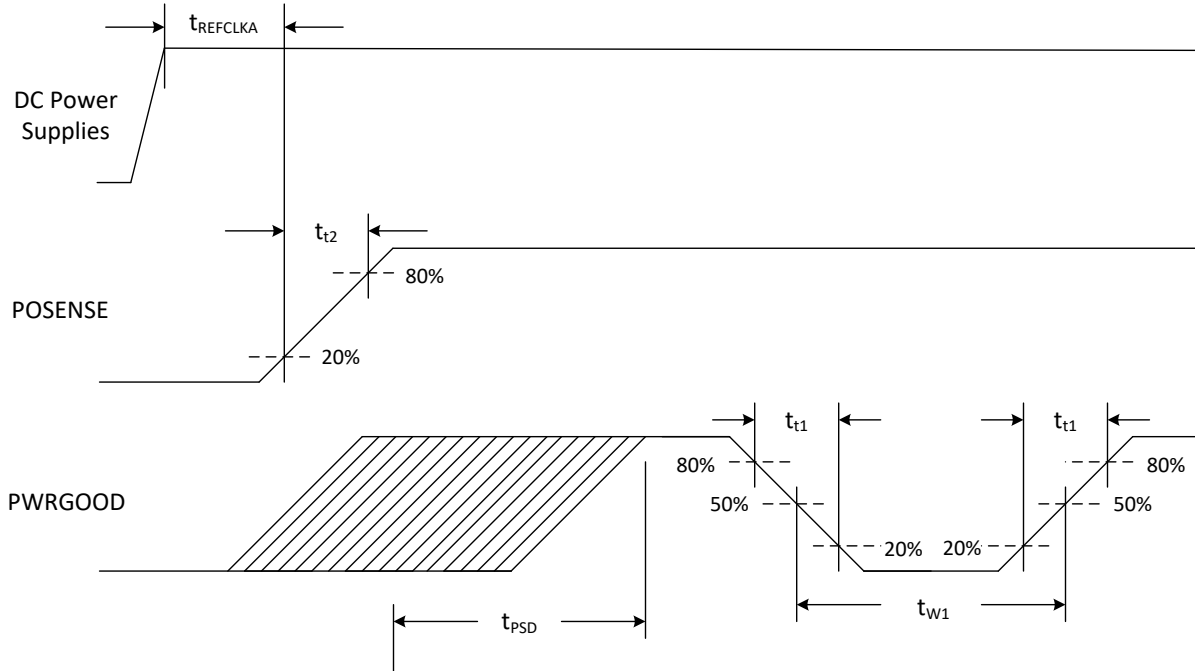


Figure 5-7. Power Up Timing

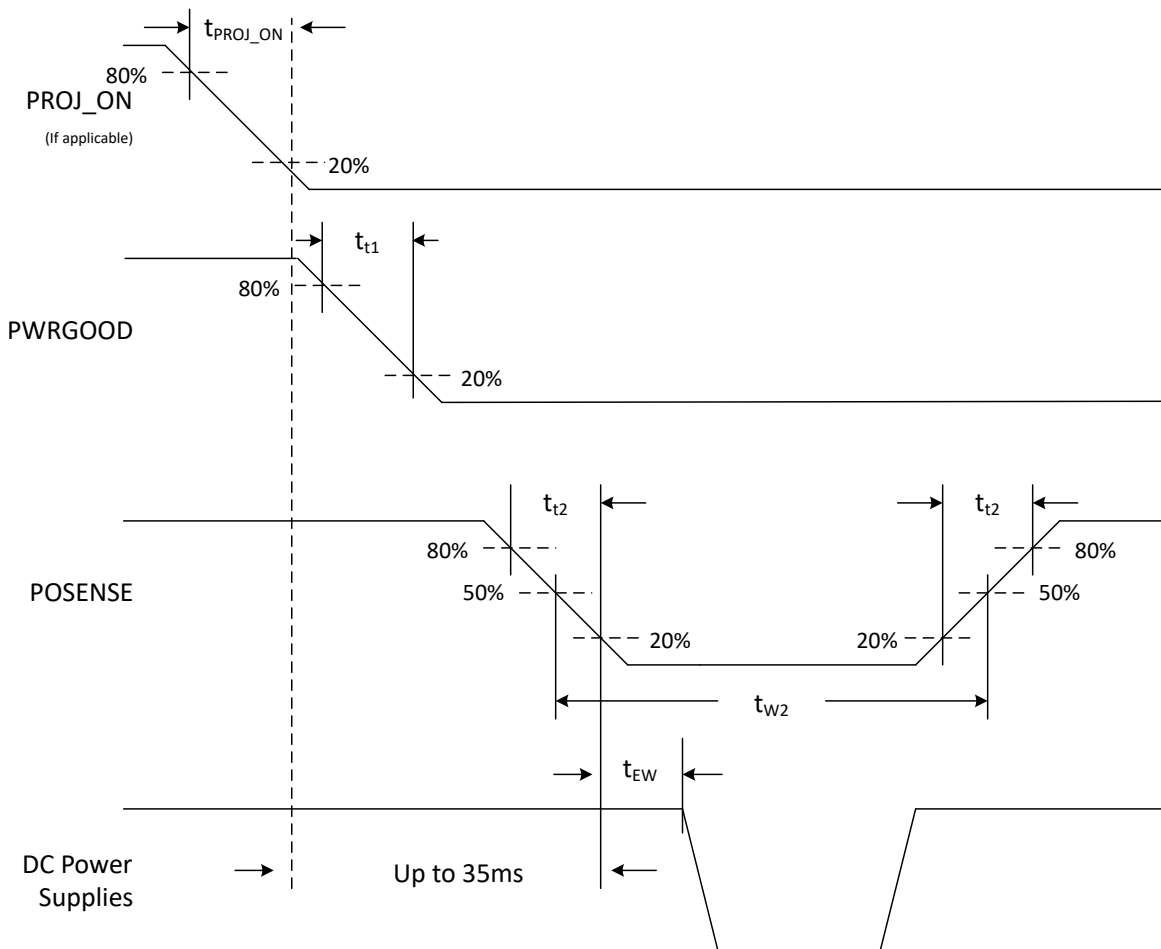


Figure 5-8. Power Down Timing—Normal

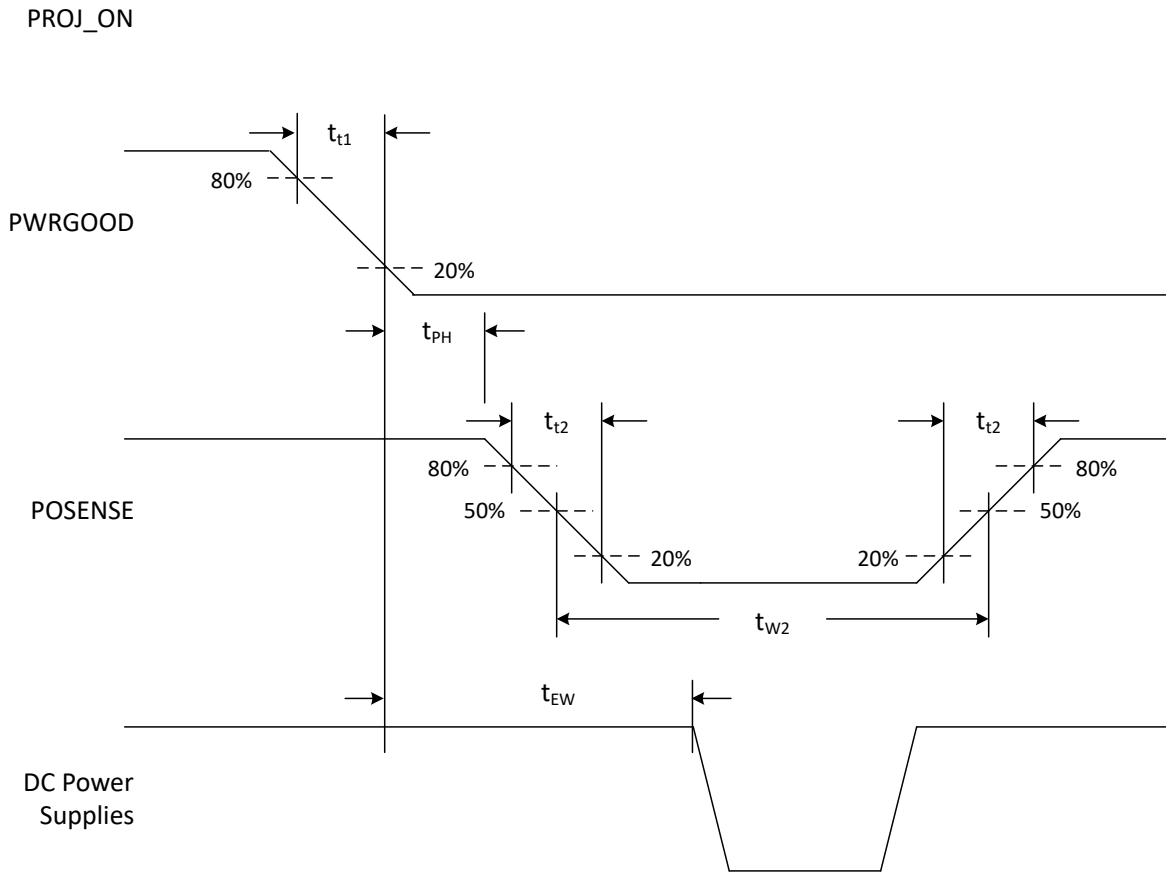


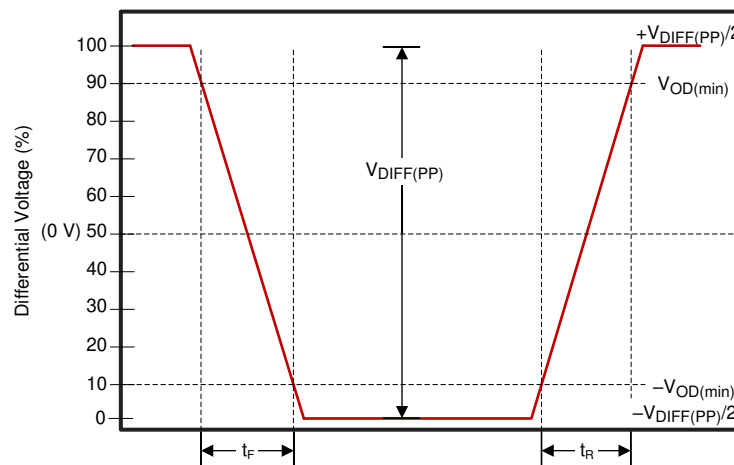
Figure 5-9. Power Down Timing—Fault

5.14 DMD HSSI Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
Baud	Baud rate		2.4		3.2	Gbps
UI	Unit interval, 1/baud		312.5		416.7	ps
t_R	Differential output rise time ⁽¹⁾ ⁽²⁾ (0% to 100% of minimum eye mask height)	Data	50		115	ps
		Clock	50		135	ps
t_F	Differential output fall time ⁽¹⁾ ⁽²⁾ (0% to 100% of minimum eye mask height)	Data	50		115	ps
		Clock	50		135	ps
t_{X1}	Maximum eye closure ⁽³⁾	at zero crossing			0.15	UI
t_{X2}	Maximum eye closure ⁽³⁾	at minimum eye height			0.375	UI
t_{EYE}	Differential data eye ⁽³⁾		0.7			UI
$t_{skIn2In}$	Lane to lane skew within a macro ⁽²⁾				200	ps
t_{skM2M}	Lane to lane skew macro to macro ⁽²⁾				4UI+200	ps
f_{SSCD}	Spread Spectrum (down spreading only) ⁽⁴⁾	When SSCD enabled			1	%
f_{MOD}	Modulation frequency ⁽⁴⁾	When SSCD enabled		78.125		KHz

- (1) Rise and fall times are associated with $V_{DIFF-pp}$, as shown in Figure 5-10.
- (2) Measured with an interconnect with an insertion loss of 3dB at 1.6GHz
- (3) See Figure 5-11.
- (4) When SSCD is enabled, the available modulation waveform is triangular.



V_{CM} is removed when signals are viewed differentially.

Figure 5-10. HSSI Differential Timing Parameters

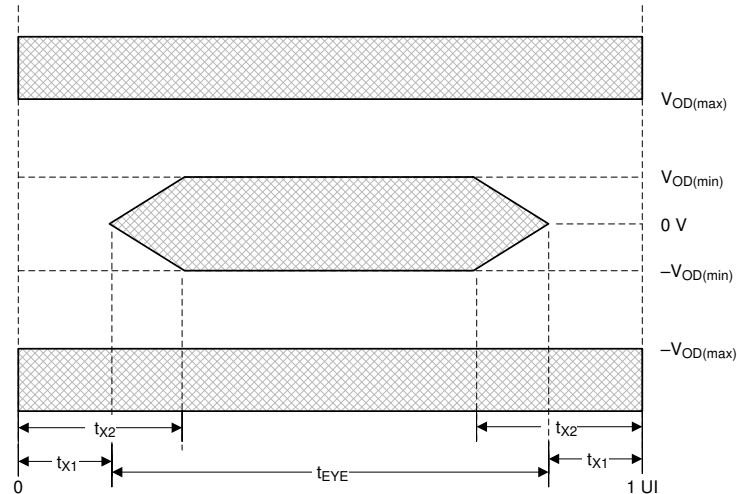


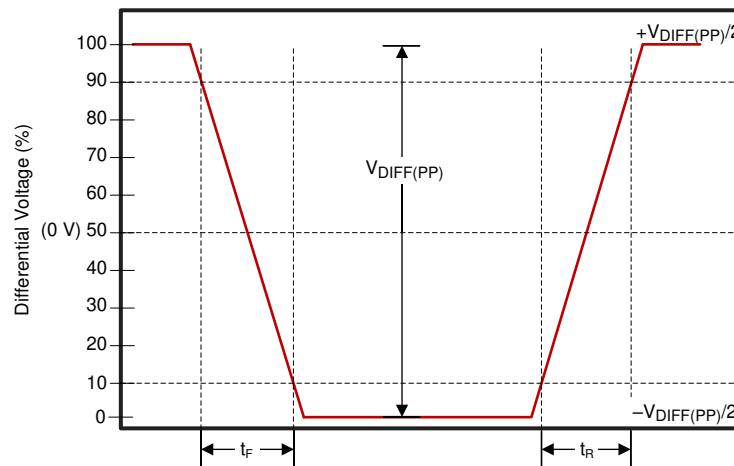
Figure 5-11. HSSI Eye Characteristics

5.15 DMD Low-Speed LVDS Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
f _{clock}		119.966	120	120.034	MHz
t _R (1)	Differential output rise time (10% to 90%)			250	ps
t _F (1)	Differential output fall time (10% to 90%)			250	ps
DCD	Duty cycle distortion	45%		55%	

(1) Rise and fall times are associated with $V_{DIFF-pp}$, as shown in Figure 5-12 .



V_{CM} is removed when signals are viewed differentially.

Figure 5-12. DMD Low-Speed Differential Timing Parameters

5.16 V-by-One Interface General Timing Requirements

PARAMETER ⁽¹⁾		MIN	MAX	UNIT
f _{clock}	Source clock frequency	40 (1 lane) 20 (1 lane with pixel repeat) ⁽²⁾	600 (8 lanes)	MHz

5.16 V-by-One Interface General Timing Requirements (continued)

PARAMETER ⁽¹⁾			MIN	MAX	UNIT
$f_{\text{link-ck}}$	Link clock frequency per lane ⁽³⁾	8 lanes	43	75	MHz
		4 lanes	43	85	
		2 lanes	43	85	
		1 lane	43 (21.5 with pixel repeat)	85	
f_{link}	Link transfer rate ⁽³⁾	3-byte mode	2	2.55	Gbps
		4-byte mode	2	3.0	
		5-byte mode	2.15	3.0	
t_{RBIT}	Unit interval	3-byte mode	392	500	ps
		4-byte mode	294	500	ps
		5-byte mode	294	500	ps
t_{A}	Jitter margin	0.25		UI	
t_{B}	Rise / fall time	0.05		UI	
t_{EYE}	Differential data eye	0.5		UI	
$t_{\text{skew_intra}}$	Allowable intra-pair skew		0.3	UI	
$t_{\text{skew_inter}}$	Allowable inter-pair skew		5	UI	
$f_{\text{oskew_inter}}$	Allowable inter-pair frequency offset	-300	300	ppm	
T_{J}	Total jitter	—	0.5	UI	
R_{J}	Random jitter	10^{12} UI	—	UI	
$D_{\text{J_ISI}}$	Deterministic jitter (ISI)	—	0.2	UI	
S_{J}	Sinusoidal jitter	—	0.1	UI	

- (1) V-by-One high-speed technology supports 1-, 2-, 4-, or 8-lane operation, in addition to 3-byte, 4-byte, and 5-byte transfer modes.
- (2) Pixel repeat is a method used to support slower clock rate sources, whereby, the source come at twice the original clock rate, with each data pixel being repeated once, and blanking being doubled as well. This method must operate external to DLPC7530. Once received, the DLPC7530 discards each duplicate data pixel and blanking clock. Pixel repeat is supported only during a 1-lane operation.
- (3) For V-by-One high-speed technology, both link clock rate and link transfer rate limits must be met for any source.

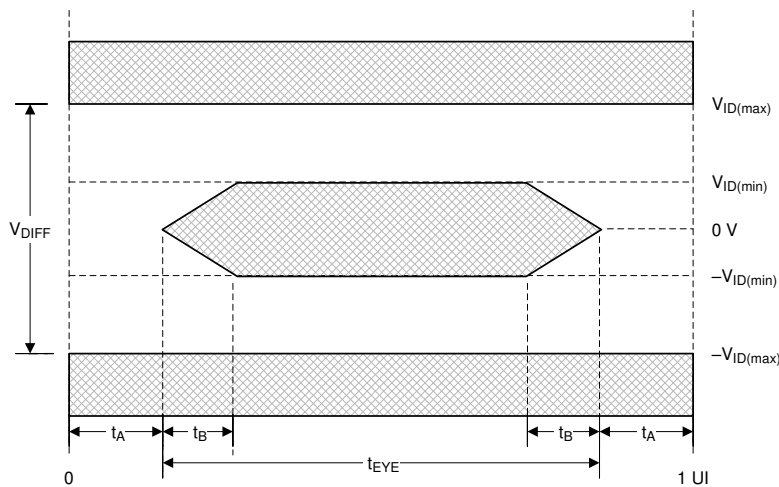


Figure 5-13. V-by-One Timing

5.17 FPD-Link Interface General Timing Requirements

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, FPDA_CLK_P/N, FPDB_CLK_P/N	20.0 (1 port) 10 (1 port with pixel repeat) ⁽¹⁾	330 (165 per port)	MHz
t_{clock}	Clock period, FPDA_CLK_P/N, FPDB_CLK_P/N	3.03 (6.06 per port)	50 (1 port) 100 (1 port with pixel repeat) ⁽¹⁾	ns
t_{RBIT}	Unit interval (Figure 5-14)	0.865 (per port)	7.143 (1 port)	ns
$t_{\text{skew_ports}}$	Clock to clock skew margin between ports on the same controller, and between ports on different controllers		1	clocks
t_{A}	Jitter margin and skew margin between clock and data (on the same port) (Figure 5-15)	$f_{\text{clock}} \leq 90$ MHz	0.25	UI
		$f_{\text{clock}} > 90$ MHz	0.23	UI
t_{B}	Rise/fall time (Figure 5-15)	$f_{\text{clock}} \leq 90$ MHz	333	ps
		$f_{\text{clock}} > 90$ MHz	200	ps
t_{EYE}	Differential data eye (Figure 5-15)	$f_{\text{clock}} \leq 90$ MHz	0.50	UI
		$f_{\text{clock}} > 90$ MHz	0.54	UI

(1) Pixel repeat is a method used to support slower clock rate sources, whereby, the source comes at twice the "original" clock rate, with each data pixel repeated once, and blanking is doubled. Both the pixel doubling and double blanking must be done external to DLPC7530. The DLPC7530 discards each duplicate data pixel and blanking clock. The device supports a pixel repeat only when using one port.

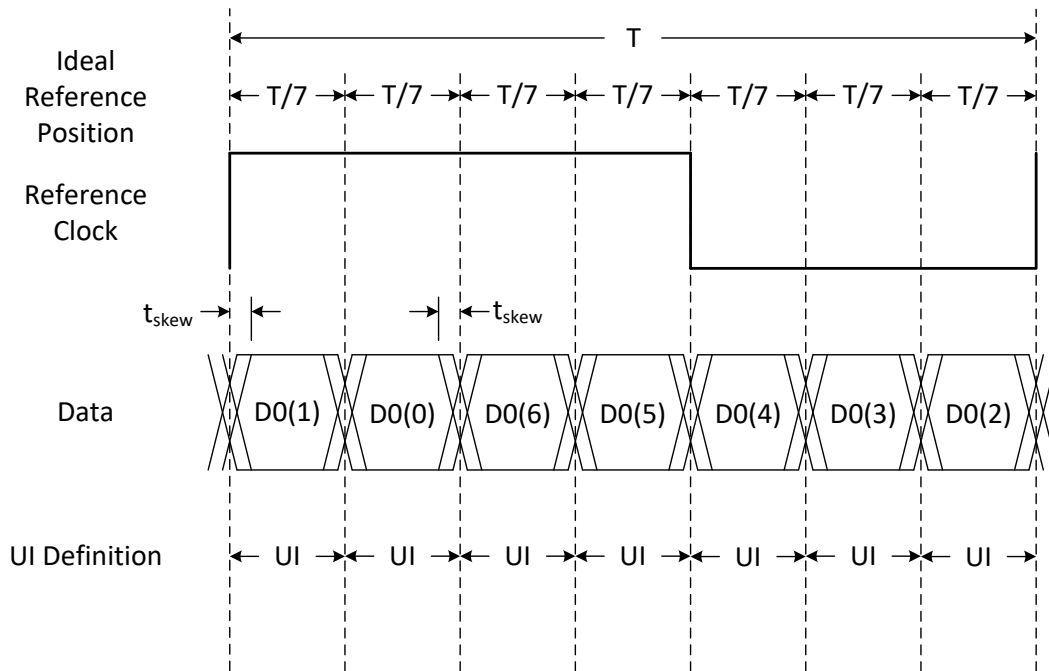


Figure 5-14. FPD-Link Data Skew

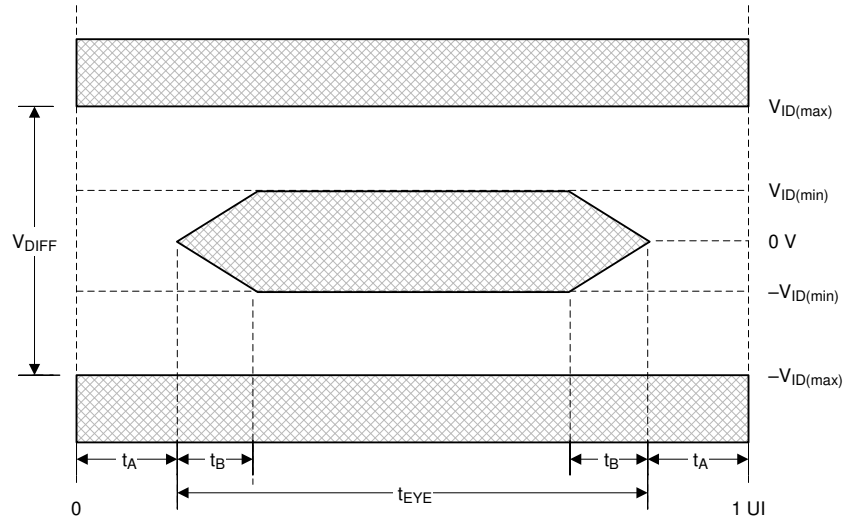


Figure 5-15. FPD-Link Timing

5.18 Parallel Interface General Timing Requirements

PARAMETER		MIN	MAX	UNIT	
f_{clock}	Clock frequency, PCLK	12 ⁽¹⁾	165	MHz	
t_{clock}	Clock period, PCLK	50% reference points	6.015	83.33 ⁽¹⁾	ns
$t_{\text{w(H)}}$	Pulse duration low, PCLK	50% reference points	2.3		ns
$t_{\text{w(L)}}$	Pulse duration high, PCLK	50% reference points	2.3		ns
t_{s}	Setup time – HSYNC, DATEN, PDATA_x valid before the active edge of PCLK ⁽²⁾	50% reference points	0.8		ns
t_{h}	Hold time – HSYNC, DATEN, PDATA_x valid after the active edge of PCLK ⁽²⁾	50% reference points	0.8		ns
t_{t}	Transition time (t_{r} and t_{f} – PCLK	20% to 80% reference points	0.6	2.0	ns
t_{t}	Transition time (t_{r} and t_{f} – all other signals on this port	20% to 80% reference points	0.6	3.0	ns
t_{t}	Transition time (t_{r} and t_{f} – ALF_HSYNC, ALF_VSYNC, ALF_CS _{SYNC} ⁽³⁾	20% to 80% reference points	0.6	3.0	ns
t_{clkjit}	Clock jitter, PCLK	At max f_{clock}	See ⁽⁴⁾ .		ps

- (1) It is expected that the minimum clock rate can go down to approximately 2.75MHz but this has not been tested. At these low rates especially, the minimum line rate must be considered (see [Section 5.19](#)).
- (2) The active edge of PCLK is software programmable. The spec to be applied to whichever edge is active (rising or falling).
- (3) ALF_HSYNC, ALF_VSYNC, and ALF_CS_{SYNC} are asynchronous signals
- (4) Maximum acceptable clock period jitter = $\pm (t_{\text{clock}} - 5715\text{ps})$

5.19 Source Frame Timing Requirements

See [Figure 5-16](#) .

PARAMETER ⁽¹⁾			MIN	MAX	UNIT
t_{p_vsw}	VSYNC active pulse width	50% reference points	1	127	lines
t_{p_vbp}	Vertical back porch (VBP) ⁽²⁾	50% reference points	2 ⁽³⁾		lines
t_{p_vfp}	Vertical front porch (VFP) ⁽²⁾	50% reference points	MAX[(TVB _{MIN} – 65), 1] ⁽³⁾		lines
t_{p_tvb}	Total vertical blanking (TVB) ⁽²⁾	50% reference points	See ⁽⁴⁾ .		lines
t_{p_hsw}	HSYNC active pulse width	50% reference points	16		PCLKs
t_{p_hbp}	Horizontal back porch (HBP) ⁽⁵⁾	50% reference points	5 (Digital Video Sources) 65 (Analog Video Sources)		PCLKs
t_{p_hfp}	Horizontal front porch (HFP) ⁽⁵⁾	50% reference points	2		PCLKs
t_{p_thb}	Total horizontal blanking (THB) ⁽⁵⁾	50% reference points	20 (Digital Video Sources) 80 (Analog Video Sources) ⁽⁶⁾		PCLKs
f_{line}	Horizontal line rate		37.354		K Hz
APPL	Active pixels per line		640	4096	Pixels
ALPF	Active lines per frame		480	2160 (normal)	Lines

(1) The requirements in the table apply to all external sources.

(2) Vertical Blanking Parameter Definitions:

- a. Vertical Back Porch: Time from the leading edge of VSYNC to the leading edge of HSYNC for the first active line, and includes the VSYNC pulse width t_{p_vsw} .
- b. Vertical Front Porch: Time from the leading edge of HSYNC following the last active line in a frame to the leading edge of VSYNC
- c. Total Vertical Blanking: The sum of VBP + VFP = TVB.

(3) The vertical blanking required (per TVB) can be allocated as desired as long as the VFP and VBP minimum values are met.

(4) The minimum TVB can be calculated using the following:

$TVB_{min} = 11 + \text{ROUNDUP}(\text{LLS_VFP_MIN} \times (\text{Source_ALPF}/\text{VPS_ALPF}))$, where:

- a. LLS_VFP_MIN (Normal Mode) = 22
- b. Source_ALPF = Active Lines Per Frame of the incoming source
- c. VPS_ALPF = 1080 (for 1920×1080 Native products and 3840×2160 4-way XPR products)
- d. Less TVBmin blanking can be required depending on the video processing being done. The configurations that drive the worst case minimum value are those configurations that combine the maximum (or near maximum) capabilities of functions such as scaling, warping, and keystone correction.
- e. This is applicable to all sources ([Section 6.4](#)). Other sources require directed testing in the end application.
- f. The minimum recommended TVB with CVT 1.2 sources is 23.

(5) Horizontal Blanking Parameter Definitions:

- a. Horizontal Back Porch: Time from the leading edge of HSYNC to the rising edge of DATEN, and includes the HSYNC pulse width t_{p_hsw} .
- b. Horizontal Front Porch: Time from the falling edge of DATEN to the leading edge of HSYNC.
- c. Total Horizontal Blanking: The sum of HBP + HFP = THB.

(6) The horizontal blanking required (per THB) can be allocated as desired as long as the HFP and HBP minimum values are met.

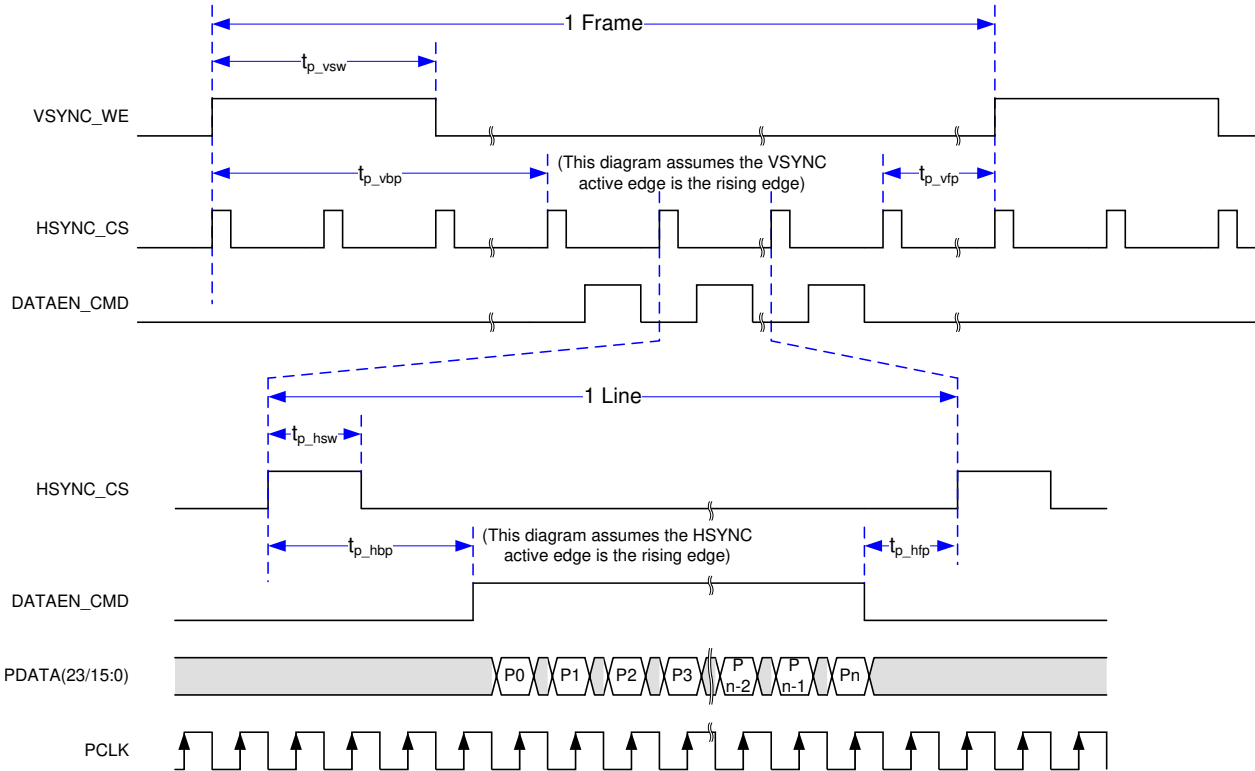


Figure 5-16. Source Frame Timing

5.20 Synchronous Serial Port Interface Timing Requirements

For SSP0, SSP1, and SSP2⁽¹⁾⁽²⁾

PARAMETER		MIN	MAX	UNIT	
SSP Controller					
f_{clock}	Clock frequency, SSPx_CLK	50% to 50% reference points	0.38	39.0	MHz
t_{clock}	Clock Period, SSPx_CLK	50% to 50% reference points	25.6	3632	ns
$t_{w(L)}$	Pulse duration low, SSPx_CLK	50% to 50% reference points	12.0		ns
$t_{w(H)}$	Pulse duration high, SSPx_CLK	50% to 50% reference points	12.0		ns
t_{delay}	Output Delay – SSPx_TXD (MOSI)		-2.5	2.5	ns
t_{su}	Setup time – SSPx_RXD (MISO)	50% to 50% reference points	15.0		ns
t_h	hold time – SSPx_RXD (MISO)	50% to 50% reference points	0		ns
t_t	Transition time (t_r and t_f SSPx_RXD)	20% to 80% reference points		1.5	ns
t_{clkjit}	Clock jitter, SSPx_CLK			300	ps
$t_{delay\Delta}$	Clock output delay $\Delta \{ t_{w(H)} - t_{w(L)} \}$			500	ps
SSP Peripheral					
t_{delay}	Output Delay – SSPx_TXD (MOSI)		0	15	ns
t_{su}	Setup time – SSPx_RXD (MISO)	50% to 50% reference points	2.5		ns
t_h	Hold time – SSPx_RXD (MISO)	50% to 50% reference points	2.5		ns

- (1) The DLPC7530 SPI interfaces support SPI Modes 0, 1, 2, and 3 (that is, both clock polarities and both clock phases) as shown in Table 5-2 and Figure 5-17. As such, each SPI interface configuration must be setup to match the SPI mode being used.
- (2) In most SPI applications, one clock edge is used by both controller and peripheral devices for transmitting data while the other edge is used by both for sampling received data. This is referred to as *Standard SPI Protocol*. To maximize the SPI_CLK frequency potential, SPI controllers can alternatively be designed to sample the data in (MISO) bit on the same clock edge used to transmit the next data out (MOSI) bit. This is referred to as *Enhanced SPI Protocol*. The DLPC7530 SPI controller implementation supports both protocols (part of SPI interface configuration), however, to be able to use the "Enhanced SPI Protocol," the peripheral device must meet the requirement shown in Figure 5-18.

Table 5-2. SPI Clocking Modes

SPI CLOCKING MODE	SPI CLOCK POLARITY	SPI CLOCK PHASE
0	0	0
1	0	1
2	1	0
3	1	1

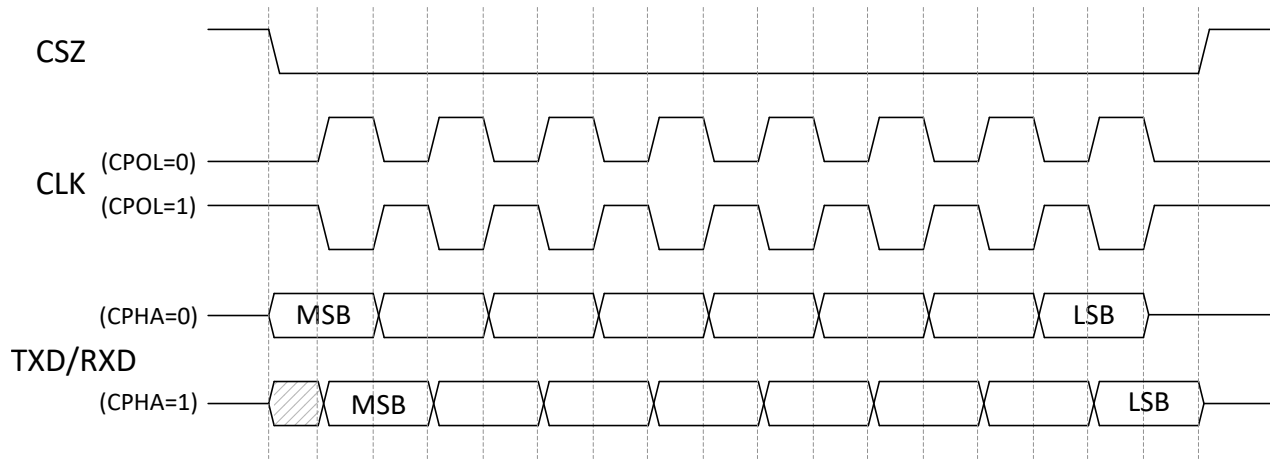


Figure 5-17. Timing Diagram for SPI Clocking Modes

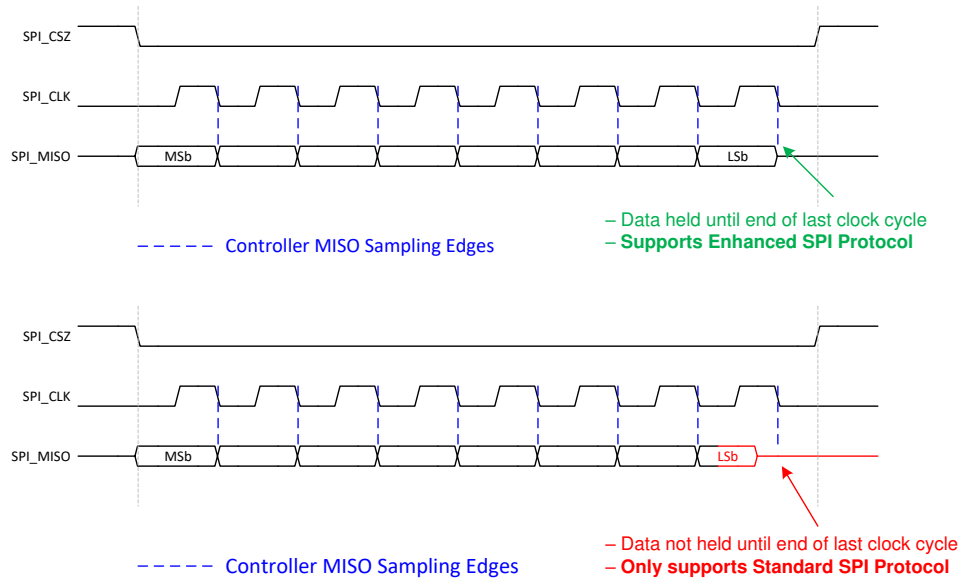


Figure 5-18. Requirement for Enhanced SPI Protocol

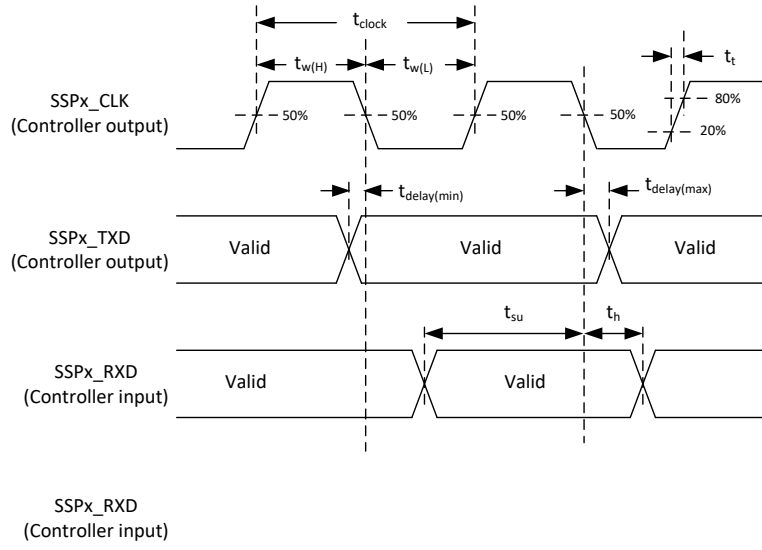


Figure 5-19. Timing Diagram for SSP Controller (Modes 0/3)

5.21 Controller and Target I²C Interface Timing Requirements

For IIC0, IIC1, and IIC2

PARAMETER ⁽¹⁾		MIN	MAX	UNIT
f _{clock}	Clock frequency, IICx_SCL ⁽²⁾ (50% reference points)	Full speed	400	kHz
		Standard mode	100	kHz
C _L	Capacitive load (for each bus line)		200	pF

- (1) Meets all I²C timing per the I²C bus specification (except for capacitive loading as specified). For reference, see Version 2.1 of the Phillips-NXP specification.
- (2) By definition, I²C transactions operate at the speed of the slowest device on the bus. Full-speed operation requires all other I²C devices on the bus support full-speed operation. The length of the line (due to its capacitance), as well as the value of the I²C pullup resistors, can reduce the obtainable clock rate.

5.22 Programmable Output Clock Timing Requirements

PARAMETER		MIN	MAX	UNIT
f _{clock}	Clock frequency, OCLKA ⁽¹⁾	0.19	48.75	MHz
t _{clock}	Clock period, OCLKA	20.52	5263.15	ns
t _{w(H)}	Pulse duration high, OCLKA (50% reference points)	(t _{clock} /2) - 2		ns
t _{w(L)}	Pulse duration low, OCLKA (50% reference points)	(t _{clock} /2) - 2		ns
t _{cclkjit}	Jitter, OCLKA		200	ps
f _{clock}	Clock frequency, OCLKB ⁽¹⁾	0.19	48.75	MHz
t _{clock}	Clock period, OCLKB	20.52	5263.15	ns
t _{w(H)}	Pulse duration high, OCLKB (50% reference points)	(t _{clock} /2) - 2		ns
t _{w(L)}	Pulse duration low, OCLKB (50% reference points)	(t _{clock} /2) - 2		ns
t _{cclkjit}	Jitter, OCLKB		200	ps
f _{clock}	Clock frequency, OCLKC ⁽¹⁾	0.19	48.75	MHz
t _{clock}	Clock period, OCLKC	20.52	5263.15	ns
t _{w(H)}	Pulse duration high, OCLKC (50% reference points)	(t _{clock} /2) - 2		ns

PARAMETER		MIN	MAX	UNIT
$t_{w(L)}$	Pulse duration low, OCLKC (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{cclkjit}$	Jitter, OCLKC		200	ps
f_{clock}	Clock frequency, OCLKD ⁽¹⁾	0.19	48.75	MHz
t_{clock}	Clock period, OCLKD	20.52	5263.15	ns
$t_{w(H)}$	Pulse duration high, OCLKD (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{w(L)}$	Pulse duration low, OCLKD (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{cclkjit}$	Jitter, OCLKD		200	ps

- (1) a. OCLKA is a dedicated pin, while OCLKB thru OCLKD are available via GPIO as alternate functions.
- b. The frequency of OCLKA thru OCLKD is programmable, with each having a power-up default frequency of 0.77 MHz. This default frequency is not that meaningful for OCLKB thru OCLKD since they must be configured to their alternate GPIO function before they can be used as a clock output.

5.23 JTAG Boundary Scan Interface Timing Requirements (Debug Only)

See [Figure 5-20](#)

PARAMETER		MIN	MAX	UNIT	
f_{clock}	Clock frequency, TCK		20	MHz	
t_{clock}	Clock period, TCK	50		ns	
$t_{w(H)}$	Pulse duration low, TCK	50% reference points	23	ns	
$t_{w(L)}$	Pulse duration high, TCK	50% reference points	27	ns	
t_s	Setup time – TDI valid before TCK↑	50% reference points	10	ns	
t_h	Hold time – TDI valid after TCK↑	50% reference points	10	ns	
t_s	Setup time – TMS1 valid before TCK↑	50% reference points	10	ns	
t_h	Hold time – TMS1 valid after TCK↑	50% reference points	10	ns	
t_t	Transition time (t_r and t_f)	20% to 80% reference points	3	ns	
t_{delay}	Output delay, TCK↓ to TDO1	60pF load	0	15	ns

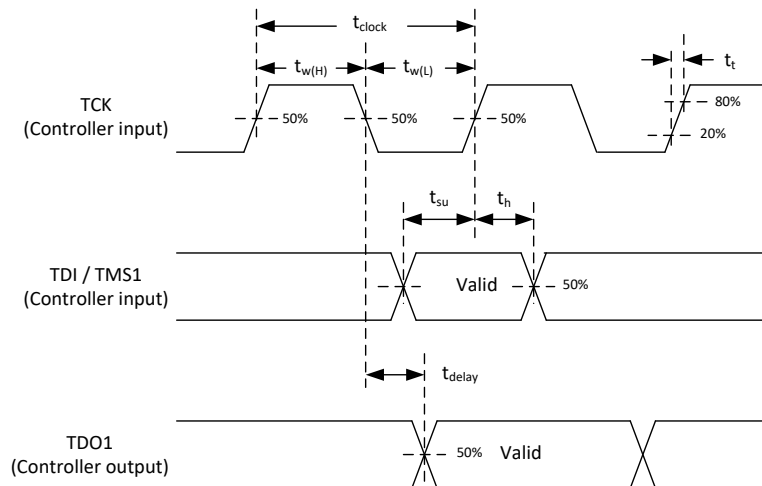


Figure 5-20. Timing Diagram for JTAG Boundary Scan

5.24 JTAG ARM Multi-Ice Interface Timing Requirements (Debug Only)

See [Figure 5-21](#) .

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK		8.33	MHz
t_{clock}	Clock period, TCK	120		ns
$t_{w(H)}$	Pulse duration low, TCK	50% reference points	50	ns
$t_{w(L)}$	Pulse duration high, TCK	50% reference points	50	ns
t_s	Setup time – TDI valid before TCK↑	50% reference points	15	ns
t_h	Hold time – TDI valid after TCK↑	50% reference points	15	ns
t_s	Setup time – TMS2 valid before TCK↑	50% reference points	15	ns
t_h	Hold time – TMS2 valid after TCK↑	50% reference points	15	ns
t_t	Transition time (t_r and t_f)	20% to 80% reference points	5	ns
t_{delay}	Output delay, TCK↓ to TDO2	0	15	ps

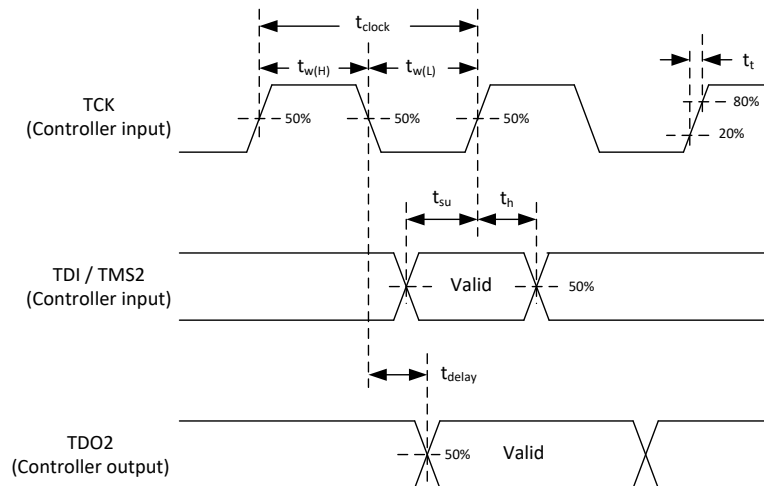


Figure 5-21. Timing Diagram for JTAG ARM Multi-Ice

5.25 Multi-Trace ETM Interface Timing Requirements

See Figure 5-22.

PARAMETER ⁽¹⁾		MIN	MAX	UNIT
f_{clock}	Clock frequency, ETM_TRACECLK		41.56	MHz
t_{clock}	Clock period, ETM_TRACECLK	24.1		ns
$t_{w(H)}$	Pulse duration low, ETM_TRACECLK	50% reference points	11.2	ns
$t_{w(L)}$	Pulse duration high, ETM_TRACECLK	50% reference points	11.2	ns
t_{delay}	Output delay, ETM_TRACECLK \uparrow to "ETM_OUTPUTS" ⁽²⁾	3.0	9.0	ps
t_{delay}	Output delay, ETM_TRACECLK \downarrow to "ETM_OUTPUTS" ⁽²⁾	3.0	9.0	ps

- (1) The trace interface is a source-synchronous DDR interface. TRACE_CLK has a programmable delay to provide for centering its edges in the center of the trace data to optimize performance.
- (2) "ETM_OUTPUTS" are TSTPT_(7:0) and ETM_TRACECTL.

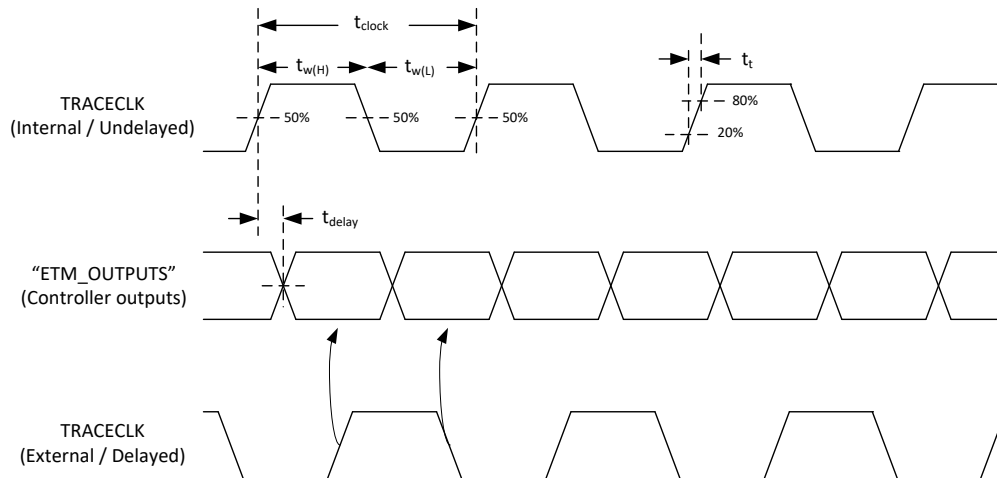


Figure 5-22. Timing Diagram for Multi-Trace ETM

6 Detailed Description

6.1 Overview

The DLPC7530 is a high-resolution digital micromirror device (DMD) controller. When coupled with the DLP472NE and DLP651NE DMDs and the DLPA100 power and motor controller, the DLPC7530 enables low cost, high brightness 1080p displays. The DLPC7530 supports 1080p video up to 240Hz and 3D at 120Hz. Input formats include RGB, YCbCr and ICtCp (HDR10). Advanced video and color processing include HDR10, improved linear light space processing, DynamicBlack, frame rate conversion, and a full parametric surface warping engine. It accepts 10-bit V-by-One®, FPD-Link™, and parallel data inputs. The DLPA100 has full illumination controls for LED, laser phosphor, RGB laser and hybrid illumination, and includes the memory bus for flash storage. Control interfaces include SPI, I²C, UART, JTAG, and USB2.0 OTG.

6.2 Functional Block Diagram

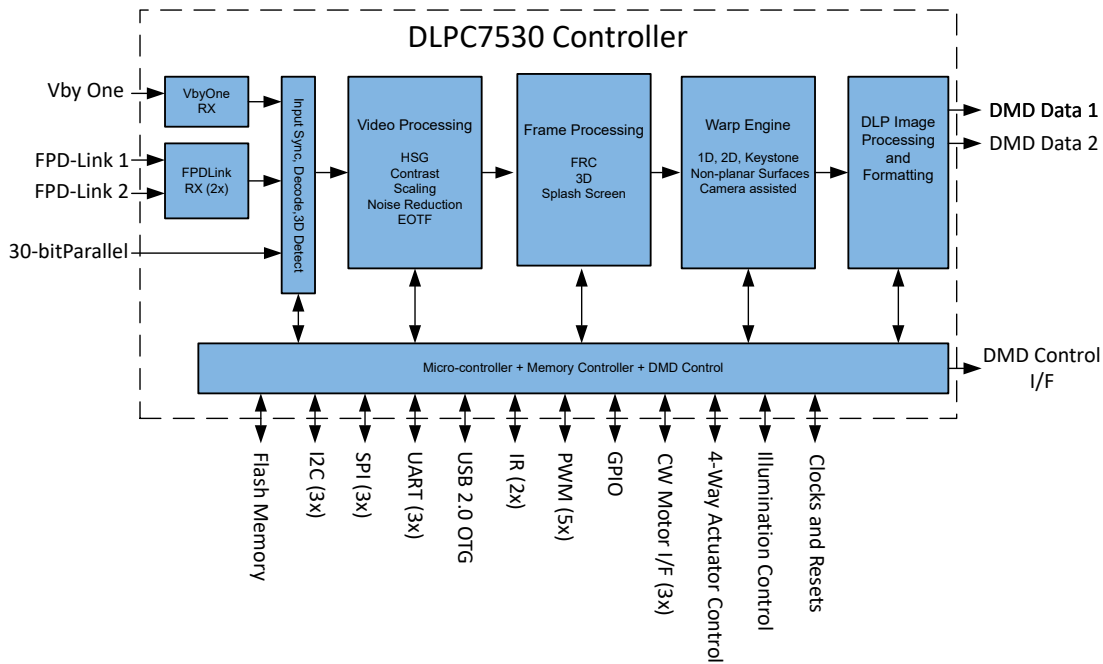


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Input Sources

Table 6-1. Supported Input Source Parameters ⁽¹⁾

INTERFACE	BITS/PIXEL ACCEPTED (MAX)	BITS/PIXEL PROCESSED (MAX)	SOURCE RESOLUTION: 2D		SOURCE RESOLUTION: 3D (PER EYE) ^{(2) (3)}
			MIN	MAX	MAX
FPD-Link	10	10	See ⁽⁴⁾ .	3840 × 2160	3840 × 2160 (FS) 3840 × 2160 (VP) 1024 × 1200 (HPH)
V-by-One	12	10	See ⁽⁵⁾ .	3840 × 2160	3840 × 2160 (FS) 3840 × 2160 (VP) 1024 × 1200 (HPH)
Parallel	10	10	640 × 480	2048 × 1080 or 1920 × 1200	2048 × 1080 or 1920 × 1200 (FS) 2048 × 1200 (VP) 1024 × 1200(HPH)

- (1) The user must ensure that the resolution desired for a specific interface (for example, FPD-Link) is within the bandwidth limits for that interface. Some resolutions at standard vertical rates (for example, 60Hz) may not be viable for all interfaces.
- (2) FS = Frame sequential (full resolution), VP = vertically packed (full resolution), HPH = horizontally packed (half resolution)
- (3) Using the low latency configuration, only frame sequential 3D sources are supported, which can be supported in only one of two ways (since the warp block is disabled when using the low latency configuration). These are:
 - For low frame rate 3D sources (for example, 48Hz, 60Hz per eye), the sequence must be used to increase the display rate up to an appropriate value (for example, 144Hz, 120Hz per eye).
 - For high frame rate 3D sources (for example, 120Hz per eye), the source is treated like a 2D source and just passed through, since the source is providing the appropriate display rate.
- (4) The minimum clock rate for the FPD-Link interface limits the smallest resolution that can be supported by this interface.
- (5) The minimum clock rate and link rate for the V-by-One interface, as well as byte mode, limits the smallest resolution that can be supported by this interface. This interface supports 3-byte, 4-byte, and 5-byte modes.

6.3.2 Processing Delays

The DLPC7530 introduces a variable number of field/frame delays dependent on the source type and selected processing steps performed on the source. For optimum audio/video synchronization, this delay must be matched in the audio path. The following tables define the various video delay scenarios to aid in audio matching.

Because the input and output rates are different when frame rate conversion (FRC) is employed, the delay through the FRC is variable.

6.3.3 Parallel Interface

The DLPC7530 Controller supports a single 30-bit parallel interface which complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC), horizontal sync signal (HSYNC), data valid signal (DATEN), a 30-bit data bus (PDATA_{xy}), and a pixel clock (PCLK). The polarity of both syncs is programmable. [Parallel Interface General Timing Requirements](#) shows the relationship between these signals. For data sources with fewer than 10 bits/component, data must be MSB justified per component.

Note

The input pins for FPD Ports A and B are shared by the Parallel Port. These pins can be used for FPD operation *or* Parallel Port operation, based on product configuration. It is not possible to switch between these two interface configurations during normal operation. Pins for FPD Port C are reserved for Parallel Port use, and can only be used when Parallel Port operation is configured

VSYNC must remain active at all times when the parallel port is in use. If VSYNC is lost, the DMD must be transitioned to a safe state. When the system detects a VSYNC loss, it switches to a test pattern or splash image as specified in flash by the Host.

The parallel port interface supports limited inter-channel remapping (specified in flash) that can help with board layout as needed. The inter-channel remapping allows the full data bus for channel A (PDATA_{Ax}), B (PDATA_{Bx}), or C (PDATA_{Cx}) to be remapped to either of the other two data channels. Each input channel can only be mapped to one unique destination channel. The typical mapping is shown in [Figure 6-2](#). An example of an alternate mapping is shown in [Figure 6-3](#). Parallel port channel remapping is specific to parallel port operation only, and is not applicable to FPD operation.

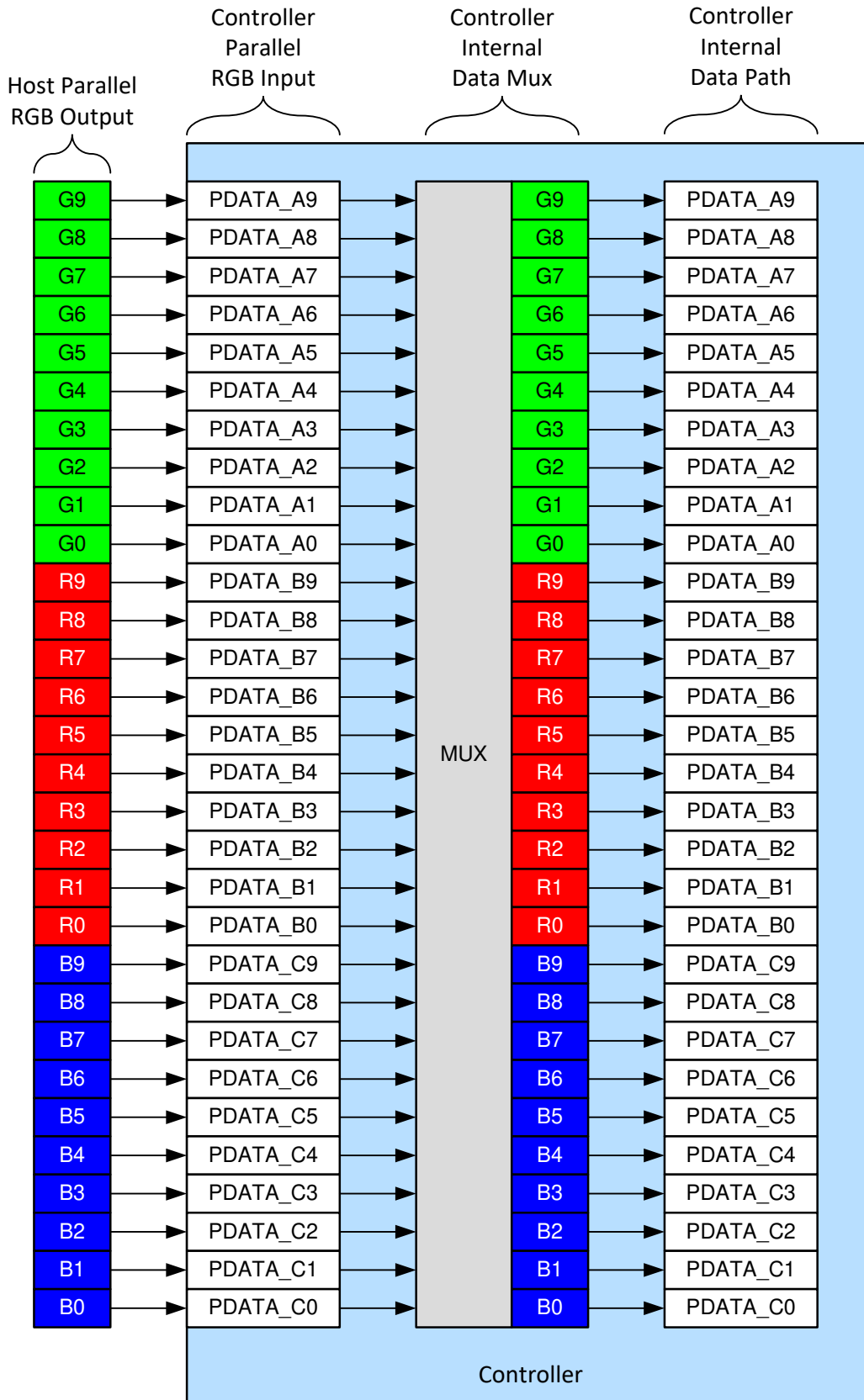


Figure 6-2. Standard Parallel Port Channel Mapping

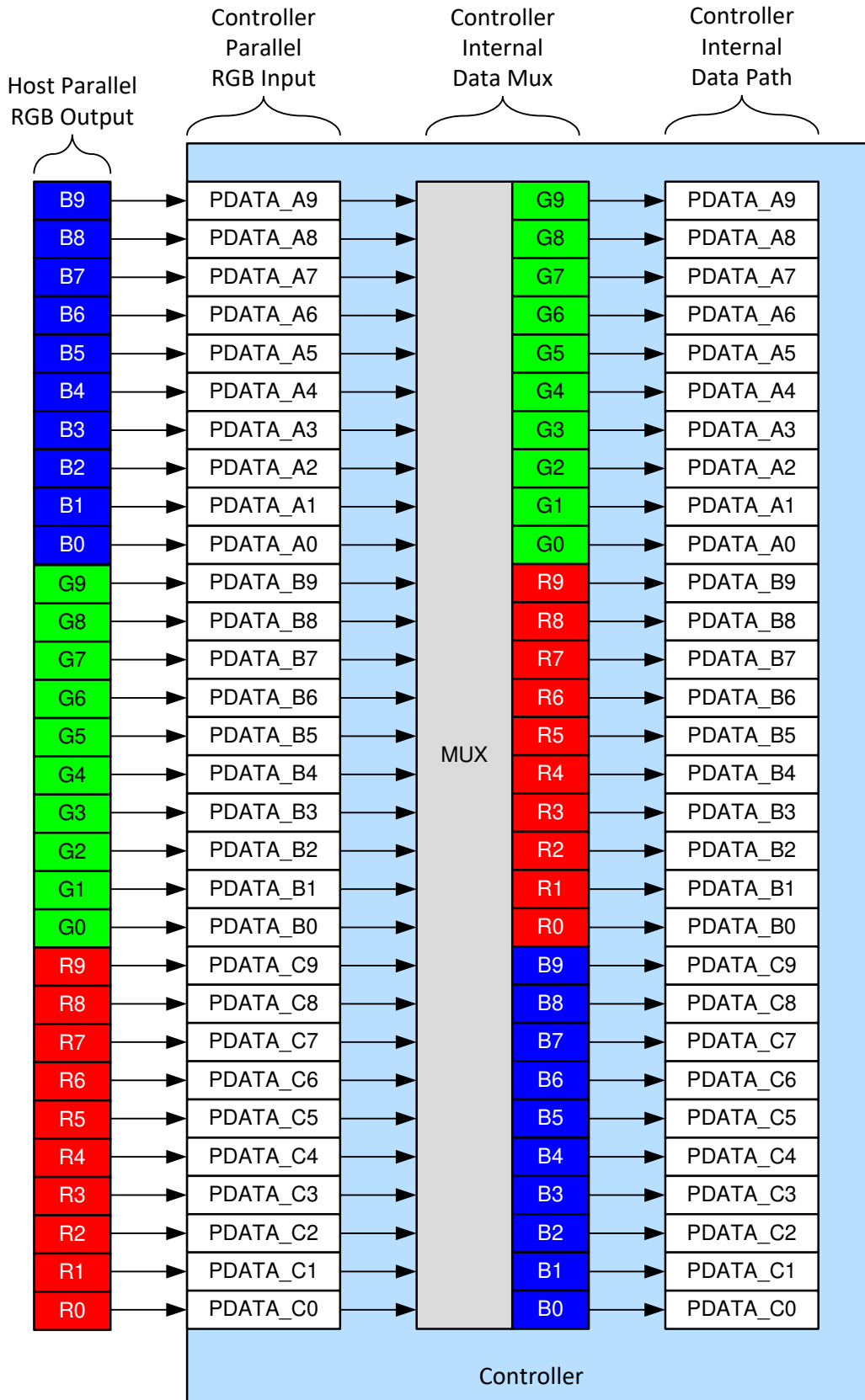


Figure 6-3. Example of Alternate Parallel Port Channel Mapping

6.3.4 FPD-Link Interface

The DLPC7530 supports two FPD-Link™ 5 lane ports, which can be configured for single port use (Port A or Port B), or for dual port use (Port A and Port B). The third FPD port (Port C) is reserved for parallel port use only. FPD ports A and B support a limited set of remapping options within each port, but there is no remapping between ports. When using this feature, each unique lane pair can only be mapped to one unique destination lane pair, and intra-lane remapping (that is, swapping P with N) is not supported. In addition, the A and B ports can be swapped. Lane and port remapping (specified in flash) can help with board layout as needed. The typical lane mapping is shown in Figure 6-4. An example of an alternate lane mapping is shown in Figure 6-5. The specific intra-port remapping options available are shown in Table 6-2.

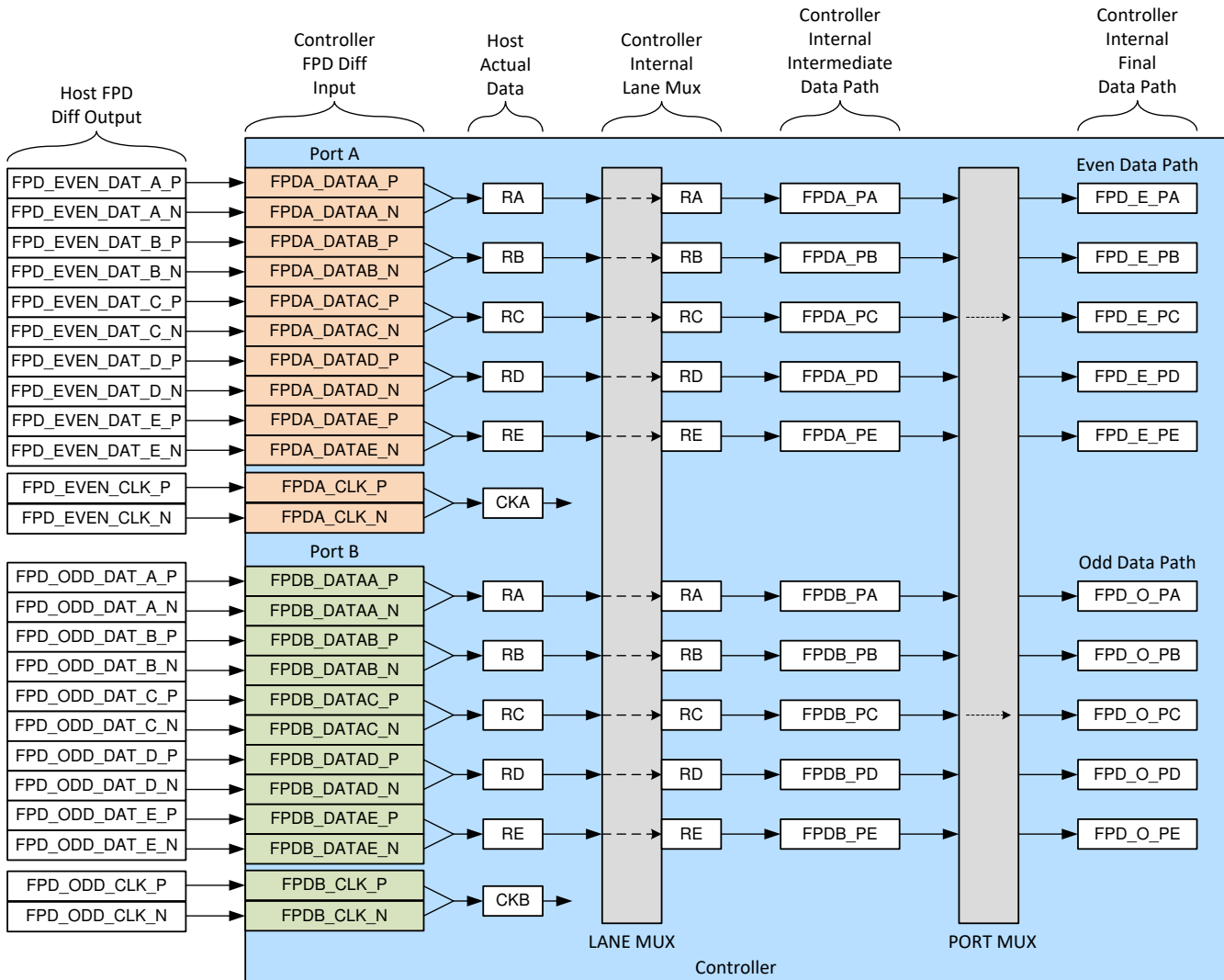


Figure 6-4. Example of Typical FPD-Link Port Lane Mapping

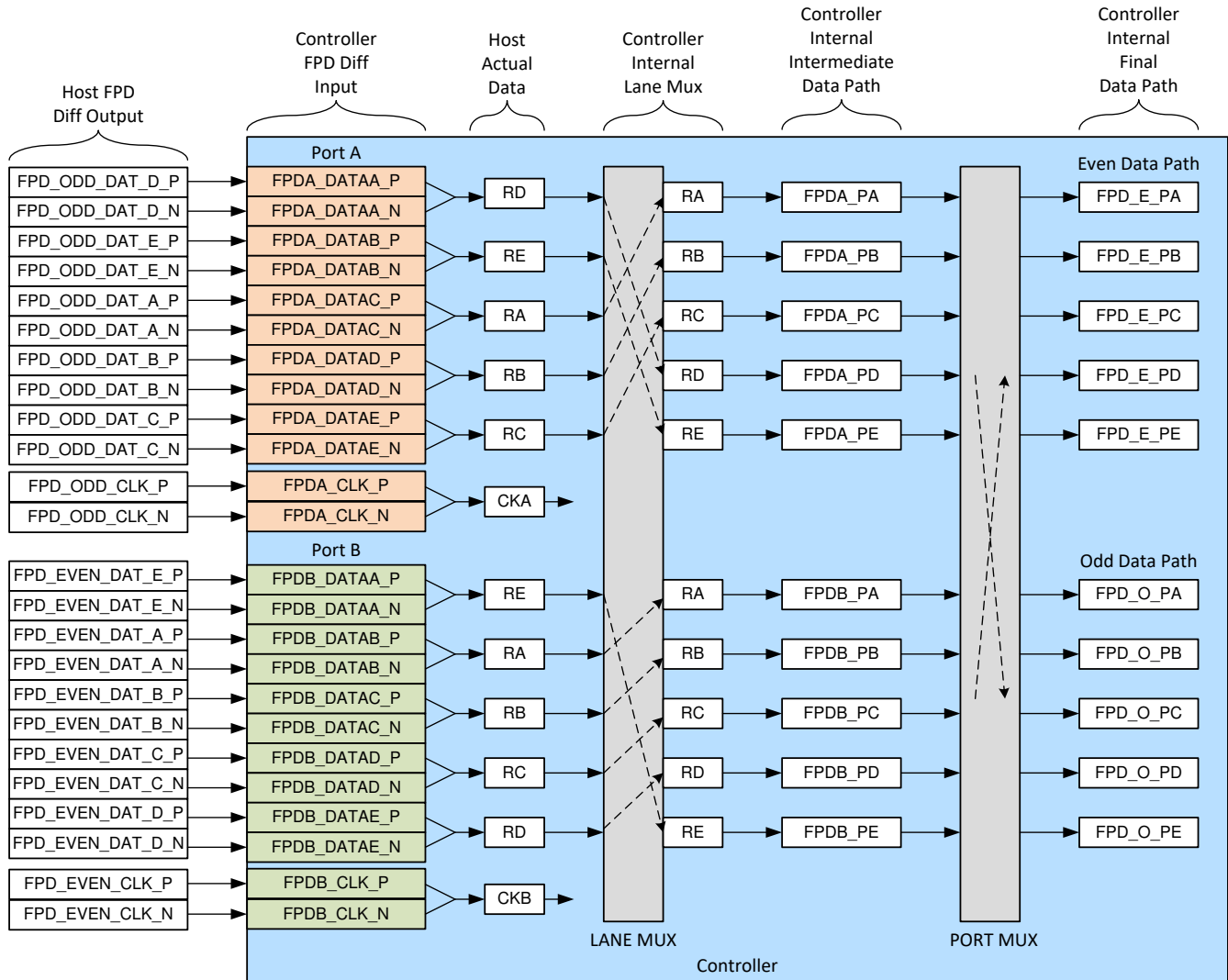


Figure 6-5. Example of Alternate FPD-Link Port Lane Mapping

Table 6-2. FPD-Link Intra-Port Data Mapping Options

MAPPING OPTIONS FOR PORTS A AND B	INPUT DATA PORT	INTERNAL FINAL DATA PATH
0	FPDx_DATAA_P/N	FPD_x_PA
1	FPDx_DATAAB_P/N	FPD_x_PA
2	FPDx_DATAAC_P/N	FPD_x_PA
3	FPDx_DATAD_P/N	FPD_x_PA
4	FPDx_DATAE_P/N	FPD_x_PA
4	FPDx_DATAA_P/N	FPD_x_PB
0	FPDx_DATAAB_P/N	FPD_x_PB
1	FPDx_DATAAC_P/N	FPD_x_PB
2	FPDx_DATAD_P/N	FPD_x_PB
3	FPDx_DATAE_P/N	FPD_x_PB
3	FPDx_DATAA_P/N	FPD_x_PC
4	FPDx_DATAAB_P/N	FPD_x_PC
0	FPDx_DATAAC_P/N	FPD_x_PC
1	FPDx_DATAD_P/N	FPD_x_PC
2	FPDx_DATAE_P/N	FPD_x_PC
2	FPDx_DATAA_P/N	FPD_x_PD
3	FPDx_DATAAB_P/N	FPD_x_PD
4	FPDx_DATAAC_P/N	FPD_x_PD
0	FPDx_DATAD_P/N	FPD_x_PD
1	FPDx_DATAE_P/N	FPD_x_PD
1	FPDx_DATAA_P/N	FPD_x_PE
2	FPDx_DATAAB_P/N	FPD_x_PE
3	FPDx_DATAAC_P/N	FPD_x_PE
4	FPDx_DATAD_P/N	FPD_x_PE
0	FPDx_DATAE_P/N	FPD_x_PE

Independent from the remapping of the physical FPD interface, the DLPC7530 supports a number of data mappings onto the actual physical interface. There are three different 30-bit data mappings, and two different 24-bit data mappings supported. FPD sources must match at least one of these mappings. These are shown in [Table 6-3](#), [Table 6-4](#), [Table 6-5](#), [Table 6-6](#), and [Table 6-7](#).

Table 6-3. FPD-Link Data Mapping onto Physical Interface (30-Bit Mode 0)

BIT MAPPING—30-BIT MODE 0 ⁽¹⁾ (30 BITS PER PIXEL)				
MAPPER INPUT	RGB/YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:0	MAPPER OUTPUT
PA-6	G/Y[4]	Y[4]	Y00[4]	A(4)
PA-5	R/Cr[9]	Cb/Cr[9]	Cb/C00r[9]	B(9)
PA-4	R/Cr[8]	Cb/Cr[8]	Cb/Cr00[8]	B(8)
PA-3	R/Cr[7]	Cb/Cr[7]	Cb/Cr00[7]	B(7)
PA-2	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(6)
PA-1	R/Cr[5]	Cb/Cr[5]	Cb/Cr00[5]	B(5)
PA-0	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(4)
PB-6	B/Cb[5]	Unused	Y01[5]	C(5)
PB-5	B/Cb[4]	Unused	Y01[4]	C(4)
PB-4	G/Y[9]	Y[9]	Y00[9]	A(9)
PB-3	G/Y[8]	Y[8]	Y00[8]	A(8)
PB-2	G/Y[7]	Y[7]	Y00[7]	A(7)
PB-1	G/Y[6]	Y[6]	Y00[6]	A(6)
PB-0	G/Y[5]	Y[5]	Y00[5]	A(5)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[9]	Unused	Y01[9]	C(9)
PC-2	B/Cb[8]	Unused	Y01[8]	C(8)
PC-1	B/Cb[7]	Unused	Y01[7]	C(7)
PC-0	B/Cb[6]	Unused	Y01[6]	C(6)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[3]	Unused	Y01[3]	C(3)
PD-4	B/Cb[2]	Unused	Y01[2]	C(2)
PD-3	G/Y[3]	Y[3]	Y00[3]	A(3)
PD-2	G/Y[2]	Y[2]	Y00[2]	A(2)
PD-1	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(3)
PD-0	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(2)
PE-6	Field	Field	Field	Field
PE-5	B/Cb[1]	Unused	Y01[1]	C(1)
PE-4	B/Cb[0]	Unused	Y01[0]	C(0)
PE-3	G/Y[1]	Y[1]	Y00[1]	A(1)
PE-2	G/Y[0]	Y[0]	Y00[0]	A(0)
PE-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(1)
PE-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(0)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

Table 6-4. FPD-Link Data Mapping onto Physical Interface (30-Bit Mode 1)

BIT MAPPING—30-BIT MODE 1 ⁽¹⁾ (30 BITS PER PIXEL)				
MAPPER INPUT	RGB/YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:0	MAPPER OUTPUT
PA-6	G/Y[2]	Y[2]	Y00[2]	A(2)
PA-5	R/Cr[7]	Cb/Cr[7]	Cb/C00r[7]	B(7)
PA-4	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(6)
PA-3	R/Cr[5]	Cb/Cr[5]	Cb/Cr00[5]	B(5)
PA-2	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(4)
PA-1	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(3)
PA-0	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(2)
PB-6	B/Cb[3]	Unused	Y01[3]	C(3)
PB-5	B/Cb[2]	Unused	Y01[2]	C(2)
PB-4	G/Y[7]	Y[7]	Y00[7]	A(7)
PB-3	G/Y[6]	Y[6]	Y00[6]	A(6)
PB-2	G/Y[5]	Y[5]	Y00[5]	A(5)
PB-1	G/Y[4]	Y[4]	Y00[4]	A(4)
PB-0	G/Y[3]	Y[3]	Y00[3]	A(3)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[7]	Unused	Y01[7]	C(7)
PC-2	B/Cb[6]	Unused	Y01[6]	C(6)
PC-1	B/Cb[5]	Unused	Y01[5]	C(5)
PC-0	B/Cb[4]	Unused	Y01[4]	C(4)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[9]	Unused	Y01[9]	C(9)
PD-4	B/Cb[8]	Unused	Y01[8]	C(8)
PD-3	G/Y[9]	Y[9]	Y00[9]	A(9)
PD-2	G/Y[8]	Y[8]	Y00[8]	A(8)
PD-1	R/Cr[9]	Cb/Cr[9]	Cb/Cr00[9]	B(9)
PD-0	R/Cr[8]	Cb/Cr[8]	Cb/Cr00[8]	B(8)
PE-6	Field	Field	Field	Field
PE-5	B/Cb[1]	Unused	Y01[1]	C(1)
PE-4	B/Cb[0]	Unused	Y01[0]	C(0)
PE-3	G/Y[1]	Y[1]	Y00[1]	A(1)
PE-2	G/Y[0]	Y[0]	Y00[0]	A(0)
PE-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(1)
PE-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(0)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

Table 6-5. FPD-Link Data Mapping onto Physical Interface (30-Bit Mode 2)

BIT MAPPING—30-BIT MODE 2 ⁽¹⁾ (30 BITS PER PIXEL)				
MAPPER INPUT	RGB/YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:0	MAPPER OUTPUT
PA-6	G/Y[0]	Y[0]	Y00[0]	A(0)
PA-5	R/Cr[5]	Cb/Cr[5]	Cb/C00r[5]	B(5)
PA-4	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(4)
PA-3	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(3)
PA-2	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(2)
PA-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(1)
PA-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(0)
PB-6	B/Cb[1]	Unused	Y01[1]	C(1)
PB-5	B/Cb[0]	Unused	Y01[0]	C(0)
PB-4	G/Y[5]	Y[5]	Y00[5]	A(5)
PB-3	G/Y[4]	Y[4]	Y00[4]	A(4)
PB-2	G/Y[3]	Y[3]	Y00[3]	A(3)
PB-1	G/Y[2]	Y[2]	Y00[2]	A(2)
PB-0	G/Y[1]	Y[1]	Y00[1]	A(1)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[5]	Unused	Y01[5]	C(5)
PC-2	B/Cb[4]	Unused	Y01[4]	C(4)
PC-1	B/Cb[3]	Unused	Y01[3]	C(3)
PC-0	B/Cb[2]	Unused	Y01[2]	C(2)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[7]	Unused	Y01[7]	C(7)
PD-4	B/Cb[6]	Unused	Y01[6]	C(6)
PD-3	G/Y[7]	Y[7]	Y00[7]	A(7)
PD-2	G/Y[6]	Y[6]	Y00[6]	A(6)
PD-1	R/Cr[7]	Cb/Cr[7]	Cb/Cr00[7]	B(7)
PD-0	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(6)
PE-6	Field	Field	Field	Field
PE-5	B/Cb[9]	Unused	Y01[9]	C(9)
PE-4	B/Cb[8]	Unused	Y01[8]	C(8)
PE-3	G/Y[9]	Y[9]	Y00[9]	A(9)
PE-2	G/Y[8]	Y[8]	Y00[8]	A(8)
PE-1	R/Cr[9]	Cb/Cr[9]	Cb/Cr00[9]	B(9)
PE-0	R/Cr[8]	Cb/Cr[8]	Cb/Cr00[8]	B(8)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

Table 6-6. FPD-Link Data Mapping onto Physical Interface (24-Bit Mode 0) ⁽¹⁾

BIT MAPPING—24-BIT MODE 0 ⁽²⁾ (24 BITS PER PIXEL)				
MAPPER INPUT	RGB/YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:0	MAPPER OUTPUT
PA-6	G/Y[0]	Y[0]	Y00[0]	A(2)
PA-5	R/Cr[5]	Cb/Cr[5]	Cb/C00r[5]	B(7)
PA-4	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(6)
PA-3	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(5)
PA-2	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(4)
PA-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(3)
PA-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(2)
PB-6	B/Cb[1]	Unused	Y01[1]	C(3)
PB-5	B/Cb[0]	Unused	Y01[0]	C(2)
PB-4	G/Y[5]	Y[5]	Y00[5]	A(7)
PB-3	G/Y[4]	Y[4]	Y00[4]	A(6)
PB-2	G/Y[3]	Y[3]	Y00[3]	A(5)
PB-1	G/Y[2]	Y[2]	Y00[2]	A(4)
PB-0	G/Y[1]	Y[1]	Y00[1]	A(3)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[5]	Unused	Y01[5]	C(7)
PC-2	B/Cb[4]	Unused	Y01[4]	C(6)
PC-1	B/Cb[3]	Unused	Y01[3]	C(5)
PC-0	B/Cb[2]	Unused	Y01[2]	C(4)
PD-6	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_Ref or Field
PD-5	B/Cb[7]	Unused	Y01[7]	C(9)
PD-4	B/Cb[6]	Unused	Y01[6]	C(8)
PD-3	G/Y[7]	Y[7]	Y00[7]	A(9)
PD-2	G/Y[6]	Y[6]	Y00[6]	A(8)
PD-1	R/Cr[7]	Cb/Cr[7]	Cb/Cr00[7]	B(9)
PD-0	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(8)
PE-6	Unused	Unused	Unused	Unused
PE-5	Unused	Unused	Unused	Unused
PE-4	Unused	Unused	Unused	Unused
PE-3	Unused	Unused	Unused	Unused
PE-2	Unused	Unused	Unused	Unused
PE-1	Unused	Unused	Unused	Unused
PE-0	Unused	Unused	Unused	Unused

- (1) To support 24-bit data, the mapper shifts each 8-bit color up by two bits, and forces output bits A[1], A[0], B[1], B[0], C[1], and C[0] to value '0'.
- (2) Input data bits are defined with bit[7] as the most significant bit, and bit[0] as the least significant bit.

Table 6-7. FPD-Link Data Mapping onto Physical Interface (24-Bit Mode 1) ⁽¹⁾

BIT MAPPING - 24-BIT MODE 1 ⁽²⁾ (24 BITS PER PIXEL)				
MAPPER INPUT	RGB/YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:0	MAPPER OUTPUT
PA-6	G/Y[2]	Y[2]	Y00[2]	A(4)
PA-5	R/Cr[7]	Cb/Cr[7]	Cb/C00r[7]	B(9)
PA-4	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(8)
PA-3	R/Cr[5]	Cb/Cr[5]	Cb/Cr00[5]	B(7)
PA-2	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(6)
PA-1	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(5)
PA-0	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(4)
PB-6	B/Cb[3]	Unused	Y01[3]	C(5)
PB-5	B/Cb[2]	Unused	Y01[2]	C(4)
PB-4	G/Y[7]	Y[7]	Y00[7]	A(9)
PB-3	G/Y[6]	Y[6]	Y00[6]	A(8)
PB-2	G/Y[5]	Y[5]	Y00[5]	A(7)
PB-1	G/Y[4]	Y[4]	Y00[4]	A(6)
PB-0	G/Y[3]	Y[3]	Y00[3]	A(5)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[7]	Unused	Y01[7]	C(9)
PC-2	B/Cb[6]	Unused	Y01[6]	C(8)
PC-1	B/Cb[5]	Unused	Y01[5]	C(7)
PC-0	B/Cb[4]	Unused	Y01[4]	C(6)
PD-6	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_Ref or Field
PD-5	B/Cb[1]	Unused	Y01[1]	C(3)
PD-4	B/Cb[0]	Unused	Y01[0]	C(2)
PD-3	G/Y[1]	Y[1]	Y00[1]	A(3)
PD-2	G/Y[0]	Y[0]	Y00[0]	A(2)
PD-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(3)
PD-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(2)
PE-6	Unused	Unused	Unused	Unused
PE-5	Unused	Unused	Unused	Unused
PE-4	Unused	Unused	Unused	Unused
PE-3	Unused	Unused	Unused	Unused
PE-2	Unused	Unused	Unused	Unused
PE-1	Unused	Unused	Unused	Unused
PE-0	Unused	Unused	Unused	Unused

- (1) To support 24-bit data, the mapper shifts each 8-bit color up by two bits, and forces output bits A[1], A[0], B[1], B[0], C[1], and C[0] to value '0'.
- (2) Input data bits are defined with bit[7] as the most significant bit, and bit[0] as the least significant bit.

6.3.5 V-by-One Interface

The DLPC7530 controller supports a single 8 lane V-by-One port that can be configured for 1, 2, 4, or 8 lane use. This interface supports limited lane remapping, which is shown in [Table 6-8](#) . Intra-lane remapping (that is, swapping P with N) is not supported.

Table 6-8. V-by-One Interface Lane Remapping Options

CONFIGURATION N ⁽¹⁾	# OF LANES	V-BY-ONE PORT PHYSICAL LANES ⁽¹⁾							
		LANE 7	LANE 6	LANE 5	LANE 4	LANE 3	LANE 2	LANE 1	LANE 0
1	8	7	6	5	4	3	2	1	0
2	8	1	0	2	3	4	5	6	7

(1) There are two controller lane mapping options, with the option to use fewer than the full eight lanes for each of these.

Independent from the remapping of the physical V-by-One interface, the DLPC7530 supports a number of data mappings onto the actual physical interface as specified by the standard. V-by-One sources must match at least one of these mappings. These are shown in [Table 6-9](#), [Table 6-10](#), [Table 6-11](#), [Table 6-12](#), [Table 6-13](#), [Table 6-14](#), [Table 6-15](#), [Table 6-16](#), [Table 6-17](#), and [Table 6-18](#).

Table 6-9. V-by-One Data Mapping for 36bpp/30bpp RGB/YCbCr 4:4:4

V-by-One DATA MAP MODE 0			
V-by-One INPUT DATA BIT	36bpp RGB/YCbCr 4:4:4 ⁽¹⁾	30bpp RGB/YCbCr 4:4:4	MAPPER OUTPUT
D[0]	R/Cr[4]	R/Cr[2]	B(2)
D[1]	R/Cr[5]	R/Cr[3]	B(3)
D[2]	R/Cr[6]	R/Cr[4]	B(4)
D[3]	R/Cr[7]	R/Cr[5]	B(5)
D[4]	R/Cr[8]	R/Cr[6]	B(6)
D[5]	R/Cr[9]	R/Cr[7]	B(7)
D[6]	R/Cr[10]	R/Cr[8]	B(8)
D[7]	R/Cr[11]	R/Cr[9]	B(9)
D[8]	G/Y[4]	G/Y[2]	A(2)
D[9]	G/Y[5]	G/Y[3]	A(3)
D[10]	G/Y[6]	G/Y[4]	A(4)
D[11]	G/Y[7]	G/Y[5]	A(5)
D[12]	G/Y[8]	G/Y[6]	A(6)
D[13]	G/Y[9]	G/Y[7]	A(7)
D[14]	G/Y[10]	G/Y[8]	A(8)
D[15]	G/Y[11]	G/Y[9]	A(9)
D[16]	B/Cb[4]	B/Cb[2]	C(2)
D[17]	B/Cb[5]	B/Cb[3]	C(3)
D[18]	B/Cb[6]	B/Cb[4]	C(4)
D[19]	B/Cb[7]	B/Cb[5]	C(5)
D[20]	B/Cb[8]	B/Cb[6]	C(6)
D[21]	B/Cb[9]	B/Cb[7]	C(7)
D[22]	B/Cb[10]	B/Cb[8]	C(8)
D[23]	B/Cb[11]	B/Cb[9]	C(9)
D[24]	-	-	-
D[25]	-	-	-
D[26]	B/Cb[2]	B/Cb[1]	C[0]
D[27]	B/Cb[3]	B/Cb[0]	C[1]
D[28]	G/Y[2]	G/Y[1]	A[0]
D[29]	G/Y[3]	G/Y[0]	A[1]
D[30]	R/Cr[2]	R/Cr[1]	B[0]
D[31]	R/Cr[3]	R/Cr[0]	B[1]

(1) For 36-bit inputs, the 12 bits per color truncate to 10-bits per color with the two least significant bits per color being discarded.

Table 6-10. V-by-One Data Mapping for 27bpp RGB/YCbCr 4:4:4

V-by-One DATA MAP MODE 1		
V-by-One INPUT DATA BIT	27bpp RGB/YCbCr 4:4:4 ⁽¹⁾	MAPPER OUTPUT
D[0]	R/Cr[1]	B(2)
D[1]	R/Cr[2]	B(3)
D[2]	R/Cr[3]	B(4)
D[3]	R/Cr[4]	B(5)
D[4]	R/Cr[5]	B(6)
D[5]	R/Cr[6]	B(7)
D[6]	R/Cr[7]	B(8)
D[7]	R/Cr[8]	B(9)
D[8]	G/Y[1]	A(2)
D[9]	G/Y[2]	A(3)
D[10]	G/Y[3]	A(4)
D[11]	G/Y[4]	A(5)
D[12]	G/Y[5]	A(6)
D[13]	G/Y[6]	A(7)
D[14]	G/Y[7]	A(8)
D[15]	G/Y[8]	A(9)
D[16]	B/Cb[1]	C(2)
D[17]	B/Cb[2]	C(3)
D[18]	B/Cb[3]	C(4)
D[19]	B/Cb[4]	C(5)
D[20]	B/Cb[5]	C(6)
D[21]	B/Cb[6]	C(7)
D[22]	B/Cb[7]	C(8)
D[23]	B/Cb[8]	C(9)
D[24]	-	-
D[25]	-	-
'0'	—	C[0]
D[27]	B/Cb[0]	C[1]
'0'	—	A[0]
D[29]	G/Y[0]	A[1]
'0'	—	B[0]
D[31]	R/Cr[0]	B[1]

(1) For 27-bit inputs, the 9 bits for each color shifts up one bit, and the least significant bit of each color is set to '0'.

Table 6-11. V-by-One Data Mapping for 24bpp RGB/YCbCr 4:4:4

V-by-One DATA MAP MODE 2		
V-by-One INPUT DATA BIT	24bpp RGB/YCbCr 4:4:4 ⁽¹⁾	MAPPER OUTPUT
D[0]	R/Cr[0]	B(2)
D[1]	R/Cr[1]	B(3)
D[2]	R/Cr[2]	B(4)
D[3]	R/Cr[3]	B(5)
D[4]	R/Cr[4]	B(6)
D[5]	R/Cr[5]	B(7)
D[6]	R/Cr[6]	B(8)
D[7]	R/Cr[7]	B(9)
D[8]	G/Y[0]	A(2)
D[9]	G/Y[1]	A(3)
D[10]	G/Y[2]	A(4)
D[11]	G/Y[3]	A(5)
D[12]	G/Y[4]	A(6)
D[13]	G/Y[5]	A(7)
D[14]	G/Y[6]	A(8)
D[15]	G/Y[7]	A(9)
D[16]	B/Cb[0]	C(2)
D[17]	B/Cb[1]	C(3)
D[18]	B/Cb[2]	C(4)
D[19]	B/Cb[3]	C(5)
D[20]	B/Cb[4]	C(6)
D[21]	B/Cb[5]	C(7)
D[22]	B/Cb[6]	C(8)
D[23]	B/Cb[7]	C(9)
D[24]		
D[25]	-	-
'0'	—	C[0]
'0'	—	C[1]
'0'	—	A[0]
'0'	—	A[1]
'0'	—	B[0]
'0'	—	B[1]

(1) For 24-bit inputs, the 8 bits for each color shift up two bits, and the two least significant bits of each color are set to '0'.

Table 6-12. V-by-One Data Mapping for 32bpp/24bpp/20bpp YCbCr 4:2:2 ⁽¹⁾

V-by-One DATA MAP MODE 3				
V-by-One INPUT DATA BIT	32bpp YCbCr 4:2:2 ⁽²⁾	24bpp YCbCr 4:2:2 ⁽³⁾	20bpp YCbCr 4:2:2	MAPPER OUTPUT
D[0]	CbCr[8]	CbCr[4]	CbCr[2]	B(2)
D[1]	CbCr[9]	CbCr[5]	CbCr[3]	B(3)
D[2]	CbCr[10]	CbCr[6]	CbCr[4]	B(4)
D[3]	CbCr[11]	CbCr[7]	CbCr[5]	B(5)
D[4]	CbCr[12]	CbCr[8]	CbCr[6]	B(6)
D[5]	CbCr[13]	CbCr[8]	CbCr[7]	B(7)
D[6]	CbCr[14]	CbCr[10]	CbCr[8]	B(8)
D[7]	CbCr[15]	CbCr[11]	CbCr[9]	B(9)
D[8]	Y[8]	Y[4]	Y[2]	A(2)
D[9]	Y[9]	Y[5]	Y[3]	A(3)
D[10]	Y[10]	Y[6]	Y[4]	A(4)
D[11]	Y[11]	Y[7]	Y[5]	A(5)
D[12]	Y[12]	Y[8]	Y[6]	A(6)
D[13]	Y[13]	Y[9]	Y[7]	A(7)
D[14]	Y[14]	Y[10]	Y[8]	A(8)
D[15]	Y[15]	Y[11]	Y[9]	A(9)
'0'	—	—	—	C(2)
'0'	—	—	—	C(3)
'0'	—	—	—	C(4)
'0'	—	—	—	C(5)
'0'	—	—	—	C(6)
'0'	—	—	—	C(7)
'0'	—	—	—	C(8)
'0'	—	—	—	C(9)
D[24]	-			
D[25]		-	-	-
'0'	—	—	—	C[0]
'0'	—	—	—	C[1]
D[28]	Y[6]	Y[2]	Y[2]	A[0]
D[29]	Y[7]	Y[3]	Y[3]	A[1]
D[30]	CbCr[6]	CbCr[2]	CbCr[2]	B[0]
D[31]	CbCr[7]	CbCr[3]	CbCr[3]	B[1]

- (1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
- (2) For 32-bit inputs, the 16 bits per color truncate to 10-bit per color, with the six least significant bits per color discarded.
- (3) For 24-bit inputs, the 12 bits per color truncate to 10-bit per color, with the two least significant bits per color discarded.

Table 6-13. V-by-One Data Mapping for 18bpp YCbCr 4:2:2⁽¹⁾

V-by-One DATA MAP MODE 4		
V-by-One INPUT DATA BIT	18bpp YCbCr 4:2:2 ⁽²⁾	MAPPER OUTPUT
D[0]	CbCr[1]	B(2)
D[1]	CbCr[2]	B(3)
D[2]	CbCr[3]	B(4)
D[3]	CbCr[4]	B(5)
D[4]	CbCr[5]	B(6)
D[5]	CbCr[6]	B(7)
D[6]	CbCr[7]	B(8)
D[7]	CbCr[8]	B(9)
D[8]	Y[1]	A(2)
D[9]	Y[2]	A(3)
D[10]	Y[3]	A(4)
D[11]	Y[4]	A(5)
D[12]	Y[5]	A(6)
D[13]	Y[6]	A(7)
D[14]	Y[7]	A(8)
D[15]	Y[8]	A(9)
'0'	—	C(2)
'0'	—	C(3)
'0'	—	C(4)
'0'	—	C(5)
'0'	—	C(6)
'0'	—	C(7)
'0'	—	C(8)
'0'	—	C(9)
D[24]		
D[25]	-	-
'0'	—	C[0]
'0'	—	C[1]
'0'	—	A[0]
D[29]	Y[0]	A[1]
'0'	—	B[0]
D[31]	CbCr[0]	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".

(2) For 18-bit inputs, the 9 bits for each color shift up one bit, and the least significant bits of each color is set to '0'.

Table 6-14. V-by-One Data Mapping for 16bpp YCbCr 4:2:2⁽¹⁾

V-by-One DATA MAP MODE 5		
V-by-One INPUT DATA BIT	16bpp YCbCr 4:2:2 ⁽²⁾	MAPPER OUTPUT
D[0]	CbCr[0]	B(2)
D[1]	CbCr[1]	B(3)
D[2]	CbCr[2]	B(4)
D[3]	CbCr[3]	B(5)
D[4]	CbCr[4]	B(6)
D[5]	CbCr[5]	B(7)
D[6]	CbCr[6]	B(8)
D[7]	CbCr[7]	B(9)
D[8]	Y[0]	A(2)
D[9]	Y[1]	A(3)
D[10]	Y[2]	A(4)
D[11]	Y[3]	A(5)
D[12]	Y[4]	A(6)
D[13]	Y[5]	A(7)
D[14]	Y[6]	A(8)
D[15]	Y[7]	A(9)
'0'	—	C(2)
'0'	—	C(3)
'0'	—	C(4)
'0'	—	C(5)
'0'	—	C(6)
'0'	—	C(7)
'0'	—	C(8)
'0'	—	C(9)
D[24]		
D[25]	-	-
'0'	—	C[0]
'0'	—	C[1]
'0'	—	A[0]
'0'	—	A[1]
'0'	—	B[0]
'0'	—	B[1]

- (1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
(2) For 16-bit inputs, the 8 bits for each color shift up one bit, and the least significant bit of each color is set to '0'.

Table 6-15. V-by-One Data Mapping Example for 12bpp/10bpp YCbCr 4:2:0⁽¹⁾

V-by-One DATA MAP MODE 6					
V-by-One INPUT DATA BIT	12bpp YCbCr 4:2:0 EVEN LINE ⁽²⁾	12bpp YCbCr 4:2:0 Odd Line ⁽²⁾	10bpp YCbCr 4:2:0 EVEN LINE	10bpp YCbCr 4:2:0 ODD LINE	MAPPER OUTPUT
D[0]	Y01[4]	Y01[4]	Y01[2]	Y11[2]	C(2)
D[1]	Y01[5]	Y01[5]	Y01[3]	Y11[3]	C(3)
D[2]	Y01[6]	Y01[6]	Y01[4]	Y11[4]	C(4)
D[3]	Y01[7]	Y01[7]	Y01[5]	Y11[5]	C(5)
D[4]	Y01[8]	Y01[8]	Y01[6]	Y11[6]	C(6)
D[5]	Y01[9]	Y01[9]	Y01[7]	Y11[7]	C(7)
D[6]	Y01[10]	Y01[10]	Y01[8]	Y11[8]	C(8)
D[7]	Y01[11]	Y01[11]	Y01[9]	Y11[9]	C(9)
D[8]	Y00[4]	Y00[4]	Y00[2]	Y10[2]	A(2)
D[9]	Y00[5]	Y00[5]	Y00[3]	Y10[3]	A(3)
D[10]	Y00[6]	Y00[6]	Y00[4]	Y10[4]	A(4)
D[11]	Y00[7]	Y00[7]	Y00[5]	Y10[5]	A(5)
D[12]	Y00[8]	Y00[8]	Y00[6]	Y10[6]	A(6)
D[13]	Y00[9]	Y00[9]	Y00[7]	Y10[7]	A(7)
D[14]	Y00[10]	Y00[10]	Y00[8]	Y10[8]	A(8)
D[15]	Y00[11]	Y00[11]	Y00[9]	Y10[9]	A(9)
D[16]	Cb00[4]	Cr00[4]	Cb00[2]	Cr00[2]	B(2)
D[17]	Cb00[5]	Cr00[5]	Cb00[3]	Cr00[3]	B(3)
D[18]	Cb00[6]	Cr00[6]	Cb00[4]	Cr00[4]	B(4)
D[19]	Cb00[7]	Cr00[7]	Cb00[5]	Cr00[5]	B(5)
D[20]	Cb00[8]	Cr00[8]	Cb00[6]	Cr00[6]	B(6)
D[21]	Cb00[9]	Cr00[9]	Cb00[7]	Cr00[7]	B(7)
D[22]	Cb00[10]	Cr00[10]	Cb00[8]	Cr00[8]	B(8)
D[23]	Cb00[11]	Cr00[11]	Cb00[9]	Cr00[9]	B(9)
D[24]	-	-	-	-	-
D[25]	-	-	-	-	-
D[26]	Cb00[2]	Cr00[2]	Cb00[0]	Cr00[0]	B[0]
D[27]	Cb00[3]	Cr00[3]	Cb00[1]	Cr00[1]	B[1]
D[28]	Y00[2]	Y10[2]	Y00[0]	Y10[0]	A[0]
D[29]	Y00[3]	Y10[3]	Y00[1]	Y10[1]	A[1]
D[30]	Y01[2]	Y11[2]	Y01[0]	Y11[0]	C[0]
D[31]	Y01[3]	Y11[3]	Y01[1]	Y11[1]	C[1]

- (1) For all YCbCr 4:2:0 inputs, two consecutive pixel luma values are brought in on each clock. Even lines carry the Cb values, and odd lines carry the Cr values.
- (2) For 12bpp YCbCr 4:2:0 inputs, the 12 bits per color truncate to 10 bits per color with the two least significant bits per color discarded.

Table 6-16. V-by-One Data Mapping Example for 8bpp YCbCr 4:2:0⁽¹⁾

V-by-One DATA MAP MODE 7			
V-by-One INPUT DATA BIT	8bpp YCbCr 4:2:0 EVEN LINE ⁽²⁾	8bpp YCbCr 4:2:0 ODD LINE ⁽²⁾	MAPPER OUTPUT
D[0]	Y01[0]	Y11[0]	C(2)
D[1]	Y01[1]	Y11[1]	C(3)
D[2]	Y01[2]	Y11[2]	C(4)
D[3]	Y01[3]	Y11[3]	C(5)
D[4]	Y01[4]	Y11[4]	C(6)
D[5]	Y01[5]	Y11[5]	C(7)
D[6]	Y01[6]	Y11[6]	C(8)
D[7]	Y01[7]	Y11[7]	C(9)
D[8]	Y00[0]	Y10[0]	A(2)
D[9]	Y00[1]	Y10[1]	A(3)
D[10]	Y00[2]	Y10[2]	A(4)
D[11]	Y00[3]	Y10[3]	A(5)
D[12]	Y00[4]	Y10[4]	A(6)
D[13]	Y00[5]	Y10[5]	A(7)
D[14]	Y00[6]	Y10[6]	A(8)
D[15]	Y00[7]	Y10[7]	A(9)
D[16]	Cb00[0]	Cr00[0]	B(2)
D[17]	Cb00[1]	Cr00[1]	B(3)
D[18]	Cb00[2]	Cr00[2]	B(4)
D[19]	Cb00[3]	Cr00[3]	B(5)
D[20]	Cb00[4]	Cr00[4]	B(6)
D[21]	Cb00[5]	Cr00[5]	B(7)
D[22]	Cb00[6]	Cr00[6]	B(8)
D[23]	Cb00[7]	Cr00[7]	B(9)
D[24]	-	-	-
D[25]	-	-	-
'0'	—	—	B[0]
'0'	—	—	B[1]
'0'	—	—	A[0]
'0'	—	—	A[1]
'0'	—	—	C[0]
'0'	—	—	C[1]

- (1) For all YCbCr 4:2:0 inputs, two consecutive pixel luma values are brought in on each clock. Even lines carry the Cb values, and odd lines carry the Cr values.
- (2) For 8bpp YCbCr 4:2:0 inputs, the 8 bits for each color shift up two bits, and the two least significant bits of each color are set to '0'.

Table 6-17. V-by-One Data Mapping Example for 10bpp YCbCr 4:2:0 ⁽¹⁾

V-by-One DATA MAP MODE 8			
V-by-One INPUT DATA BIT	10bpp YCbCr 4:2:0 EVEN LINE	10bpp YCbCr 4:2:0 ODD LINE	MAPPER OUTPUT
D[0]	Y00[2]	Y10[2]	A(2)
D[1]	Y00[3]	Y10[3]	A(3)
D[2]	Y00[4]	Y10[4]	A(4)
D[3]	Y00[5]	Y10[5]	A(5)
D[4]	Y00[6]	Y10[6]	A(6)
D[5]	Y00[7]	Y10[7]	A(7)
D[6]	Y00[8]	Y10[8]	A(8)
D[7]	Y00[9]	Y10[9]	A(9)
D[8]	Cb00[2]	Cr00[2]	B(2)
D[9]	Cb00[3]	Cr00[3]	B(3)
D[10]	Cb00[4]	Cr00[4]	B(4)
D[11]	Cb00[5]	Cr00[5]	B(5)
D[12]	Cb00[6]	Cr00[6]	B(6)
D[13]	Cb00[7]	Cr00[7]	B(7)
D[14]	Cb00[8]	Cr00[8]	B(8)
D[15]	Cb00[9]	Cr00[9]	B(9)
D[16]	Y01[2]	Y11[2]	C(2)
D[17]	Y01[3]	Y11[3]	C(3)
D[18]	Y01[4]	Y11[4]	C(4)
D[19]	Y01[5]	Y11[5]	C(5)
D[20]	Y01[6]	Y11[6]	C(6)
D[21]	Y01[7]	Y11[7]	C(7)
D[22]	Y01[8]	Y11[8]	C(8)
D[23]	Y01[9]	Y11[9]	C(9)
D[24]	-	-	-
D[25]	-	-	-
D[26]	Y01[0]	Y11[0]	C[0]
D[27]	Y01[1]	Y11[1]	C[1]
D[28]	Cb00[0]	Cr00[0]	B[0]
D[29]	Cb00[1]	Cr00[1]	B[1]
D[30]	Y00[0]	Y10[0]	A[0]
D[31]	Y00[1]	Y10[1]	A[1]

- (1) For all YCbCr 4:2:0 inputs, two consecutive pixel luma values are brought in on each clock. Even lines carry Cb values, and odd lines carry the Cr values.

Table 6-18. V-by-One Data Mapping Example for 8bpp YCbCr 4:2:0 ⁽¹⁾

V-by-One DATA MAP MODE 9			
V-by-One INPUT DATA BIT	8bpp YCbCr 4:2:0 EVEN LINE ⁽²⁾	8bpp YCbCr 4:2:0 ODD LINE ⁽²⁾	MAPPER OUTPUT
D[0]	Y00[0]	Y10[0]	A(2)
D[1]	Y00[1]	Y10[1]	A(3)
D[2]	Y00[2]	Y10[2]	A(4)
D[3]	Y00[3]	Y10[3]	A(5)
D[4]	Y00[4]	Y10[4]	A(6)
D[5]	Y00[5]	Y10[5]	A(7)
D[6]	Y00[6]	Y10[6]	A(8)
D[7]	Y00[7]	Y10[7]	A(9)
D[8]	Cb00[0]	Cr00[0]	B(2)
D[9]	Cb00[1]	Cr00[1]	B(3)
D[10]	Cb00[2]	Cr00[2]	B(4)
D[11]	Cb00[3]	Cr00[3]	B(5)
D[12]	Cb00[4]	Cr00[4]	B(6)
D[13]	Cb00[5]	Cr00[5]	B(7)
D[14]	Cb00[6]	Cr00[6]	B(8)
D[15]	Cb00[7]	Cr00[7]	B(9)
D[16]	Y01[0]	Y11[0]	C(2)
D[17]	Y01[1]	Y11[1]	C(3)
D[18]	Y01[2]	Y11[2]	C(4)
D[19]	Y01[3]	Y11[3]	C(5)
D[20]	Y01[4]	Y11[4]	C(6)
D[21]	Y01[5]	Y11[5]	C(7)
D[22]	Y01[6]	Y11[6]	C(8)
D[23]	Y01[7]	Y11[7]	C(9)
D[24]	-	-	-
D[25]	-	-	-
'0'	—	—	C[0]
'0'	—	—	C[1]
'0'	—	—	B[0]
'0'	—	—	B[1]
'0'	—	—	A[0]
'0'	—	—	A[1]

- (1) For all YCbCr 4:2:0 inputs, two consecutive pixel luma values are brought in on each clock. Even lines carry the Cb values, and odd lines carry the Cr values.
- (2) For 8bpp YCbCr 4:2:0 inputs, the 8 bits for each color shift up two bits, and the two least significant bits of each color are set to '0'.

6.3.6 DMD (HSSI) Interface

The DLPC7530 Controller DMD interface supports two High Speed Serial Interface (HSSI) output-only interfaces for data transmission, a single low speed LVDS output-only interface for command write transactions, as well as a low speed single-ended input interface used for command read transactions. Each HSSI port supports full data-only inter-lane remapping within the port, but not between ports. When utilizing this feature, each unique data lane pair can only be mapped to one unique destination data lane pair, and Intra-lane remapping (i.e. swapping P with N) is not supported. In addition, the two HSSI ports can also be swapped. Lane and port remapping (specified in flash) can help with board layout as needed. The number of HSSI ports and number of HSSI lanes/per HSSI port required are based on DMD type and DMD display resolution. [Table 6-19](#) shows some remapping examples. When both ports are used, they do not need to have the same pin mapping.

Table 6-19. Controller to DMD Pin Mapping Examples

DLPC7530 Controller PINS - REMAPPING EXAMPLES TO DMD PINS				
BASELINE	FLIP HSSI0 180 No FLIP HSSI1	SWAP HSSI0 PORT WITH HSSI1 PORT	SWAP HSSI0 PORT WITH HSSI1 PORT AND MIXED REMAPPING	DMD PINS
DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N
DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N
DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N
DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N
DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N
DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N
DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N
DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N
DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N
DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N
DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N
DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N
DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N
DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N
DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N
DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N

6.3.7 Program Memory Flash Interface

The DLPC7530 provides three external program memory chip selects for devices to access the program memory interface. These are detailed in [Table 6-20](#).

Table 6-20. Program Memory Interface Chip Selects

CHIP SELECT NAME	CHIP SELECT USE	DATA BUS WIDTH	ACCESS TIME	MAXIMUM SIZE SUPPORTED ⁽¹⁾
PM_CSZ_0	Boot FLASH only - Required ⁽²⁾	16 bits	< = 120ns	256Mb
PM_CSZ_1	Additional Peripheral Device (or additional FLASH) - Optional	16 bits	< = 120ns	256Mb
PM_CSZ_2	Additional Peripheral Device - Optional	16 bits	< = 120ns	256Mb

(1) Using GPIO_47 as additional address bit

(2) Boot FLASH type supported is *Standard NOR parallel FLASH*, single or multi-bank.

FLASH access timing is software programmable with up to 31 wait states. Additional information about read and write wait state timing is provided in [Table 6-21](#) and [Figure 6-6](#).

Table 6-21. Program Memory Wait State Timing

PARAMETER	EQUATION ⁽¹⁾
T _{WSR} : Wait State Resolution	6ns
Read Wait States (Number of Read Wait States for each CSz read access)	ROUNDUP(MAX(T _{ACC} , T _{CE} , T _{OE})/T _{WSR-N}) ^{(2) (3)}
Write Wait States for T _{CS} and T _{AS} (Time from CS/Address activation to WRZ assertion)	ROUNDUP(MAX(T _{CS} +5ns, T _{AS} +5ns)/T _{WSR-N}) ⁽²⁾
Write Wait States for T _{WP} and T _{DS} (Time from WRZ assertion to WEZ de-assertion)	ROUNDUP(MAX(T _{WP} +5ns, T _{DS} +5ns)/T _{WSR-N}) ⁽²⁾
Write Wait States for T _{CH} and T _{DH} (Time from CS/Address activation to WRZ assertion)	ROUNDUP(MAX(T _{CH} +5ns, T _{DH} +5ns)/T _{WSR-N}) ⁽²⁾

- (1)
- T_{ACC}: Read Access Time (ADDR to DATA valid) – (address valid to DATA valid)
 - T_{CE}: Read Access Time (CSZ to DATA valid) – (chip select active to DATA valid)
 - T_{OE}: Read Access Time (OEZ to DATA valid) – (output enable active to DATA valid)
 - T_{CS}: CSZ Setup Time (Writes) – (chip select active before negedge(WEZ))
 - T_{CS}: Address Setup Time (Writes) – (address valid before negedge(WEZ))
 - T_{AS}: Address Setup Time (Writes) – (address valid before negedge(WEZ))
 - T_{WP}: Write Pulse Width (Writes) – (WEZ active low time)
 - T_{DS}: Data Setup Time (Writes) – (DATA valid before posedge(WEZ))
 - T_{CH}: CSZ Hold Time (Writes) – (CSZ held active after posedge(WEZ))
 - T_{DH}: Data Hold Time (Writes) – (DATA held valid after posedge(WEZ))

(2) Requires a minimum of at least 1 wait state

(3) Assumes a maximum single direction trace length of 90mm (3.5 inches)

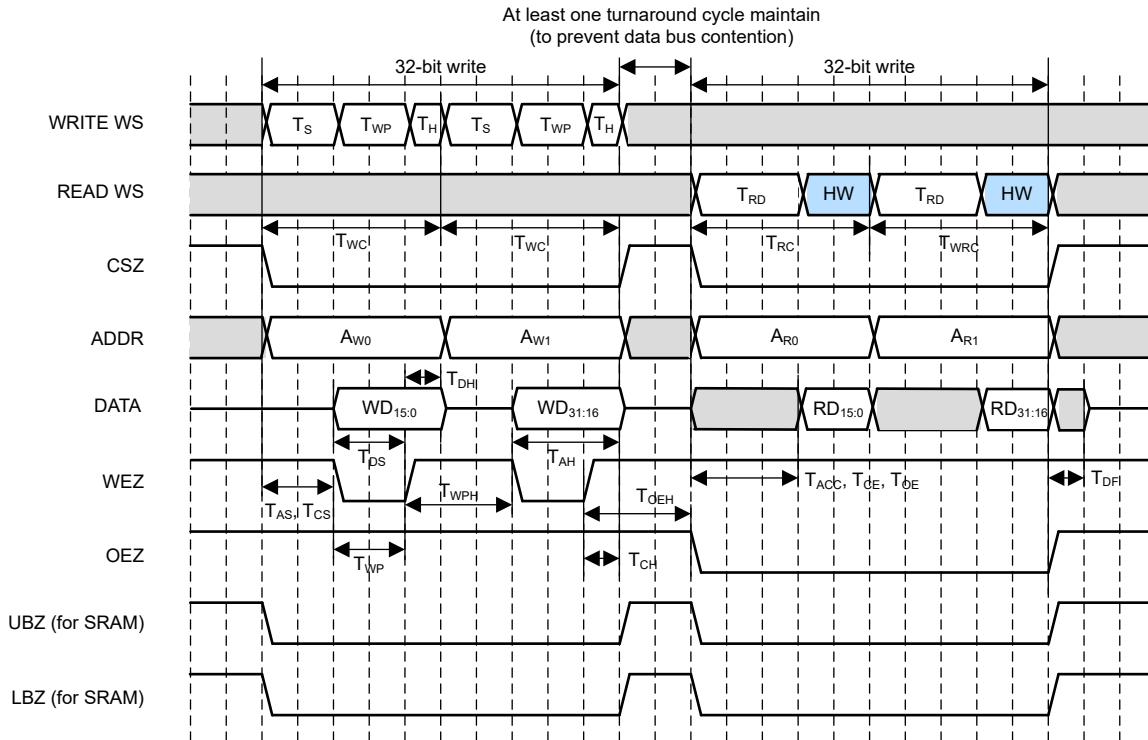


Figure 6-6. Program Memory Interface Timing Diagram

6.3.8 GPIO Supported Functionality

The DLPC7530 provides 88 general purpose I/O that are available to support a variety of functions for many different product configurations. In general, most of these I/O pins support only one specific function based on a specific product configuration, although that function can be different for a different product configuration. Most of these I/O can also be made available for TI test and debug use. Each of the following GPIO tables provide product specific details on the allocated use of each of the GPIO for a specific supported product configuration.

is

6.3.9 Debug Support

The DLPC7530 contains a test point output port, TSTPT_(7:0), which provides the Host with the ability to provide for Controller debug support. For initial debug operation, the four signals (TSTPT(3:0)) are sampled as inputs approximately 1.5 μ s after PWRGOOD goes high (or after a system reset). Once their input state has been sampled and captured, this information is used to setup the initial test mode output state of the TSTPT_(7:0) bus. [Table 6-22](#) defines the test mode selection for a few programmable output states for TSTPT_(7:0). Use the default state of 0000 (defined by the required external pulldown resistors) for normal operation (that is, no debug required).

To allow TI to make use of this debug capability, providing for the option of a jumper to an external pullup is recommended for TSTPT(3:0), as well as providing access to allow observation of the TSTPT bus outputs.

Table 6-22. Examples of Test Mode Selection Outputs Defined by TSTPT(3:0)⁽¹⁾

TSTPT_(7:0) OUTPUT	TSTPT(3:0) CAPTURED VALUES		
	0000 (DEFAULT) (NO SWITCHING ACTIVITY)	0101 CLOCK DEBUG	1000 SYSTEM CALIBRATION
TSTPT(0)	0	HIGH	Vertical Sync
TSTPT(1)	0	166.25 MHz	Delayed CW Index
TSTPT(2)	0	83.13 MHz	Sequence Index
TSTPT(3)	0	41.56 MHz	CW Spoke Test Point

Table 6-22. Examples of Test Mode Selection Outputs Defined by TSTPT(3:0)⁽¹⁾
(continued)

TSTPT_(7:0) OUTPUT	TSTPT(3:0) CAPTURED VALUES		
	0000 (DEFAULT) (NO SWITCHING ACTIVITY)	0101 CLOCK DEBUG	1000 SYSTEM CALIBRATION
TSTPT(4)	0	10.39 MHz	CW Revolution Test Point
TSTPT(5)	0	25.16 MHz	Reset Sequence Aux Bit 0
TSTPT(6)	0	133.00 MHz	Reset Sequence Aux Bit 1
TSTPT(7)	0	HIGH	Reset Sequence Aux Bit 2

(1) These are only the default output selections. Software can reprogram the selection at any time.

6.4 Device Operational Modes

The DLPC7530 has two operational modes which are enabled via software command via the Host control interface. These modes are Standby and Active.

6.4.1 Standby Mode

The system is powered up and active, however, most blocks within the Controller have been shut down to conserve power. Only the μ Processor and its peripherals are active (supporting a dormant projector waiting to be woken up). In this mode the DMD is parked and no image can be displayed.

6.4.2 Active Mode

The system is powered up and fully operational, capable of projecting internal or external source images.

6.4.2.1 Normal Configuration

This configuration enables the full functionality of the DLPC7530.

6.4.2.2 Low Latency Configuration

This configuration disables some of the capabilities of the DLPC7530 to reduce the overall system latency for certain applications which are sensitive to system latency. The key function that is disabled for this configuration is the Warping block, which removes a full frame of latency from the processing path.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DLPC7530 is the next generation high resolution display controller. It is part of the DLP472NE and DLP651NE chipsets. The controller integrates all system image processing and DMD control and data formatting onto a single integrated circuit (IC). It supports laser-phosphor, RGB-laser, LED and hybrid illumination systems. Standard image processing algorithms such as DynamicBlack or BrilliantColor™ are included. The DLPC7530 also includes a full featured image warping engine which can warp images on to arbitrary surfaces, as well as support image blending. The warp engine gives true 3D keystone correction. Applications of interest include 1080p enterprise projectors, laser TV, smart projectors, and digital signage.

7.2 Typical Application

The DLPC7530 controller is ideal for applications requiring high-performance, high-resolution displays. When the DLPC7530 display controller is combined with the DLP472NE and DLP651NE DMD, a power management and motor driver device (DLPA100), and other electrical, optical and mechanical components the chipset enables bright, affordable, full HD display solutions. A typical full HD or 1080p system application using the DLPC7530 controller and DLP472NE and DLP651NE DMD is shown in the figures below.

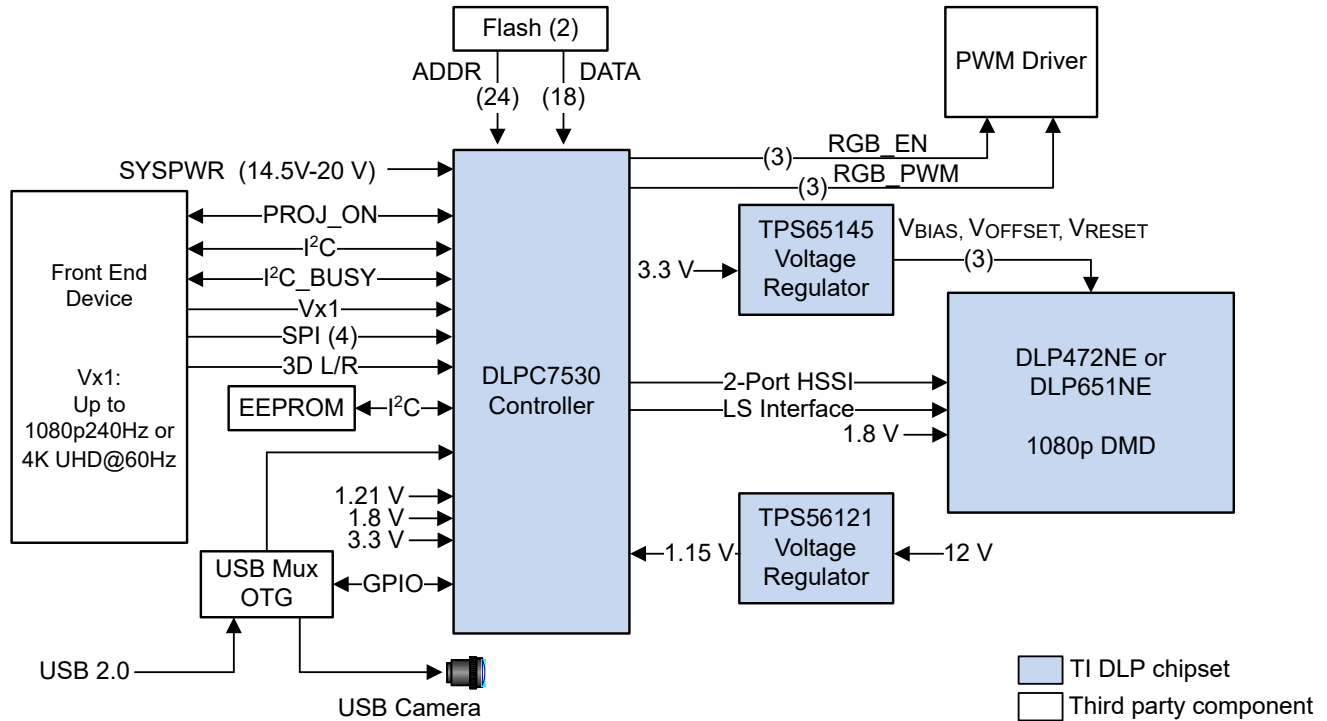


Figure 7-1. Typical 1080p LED System

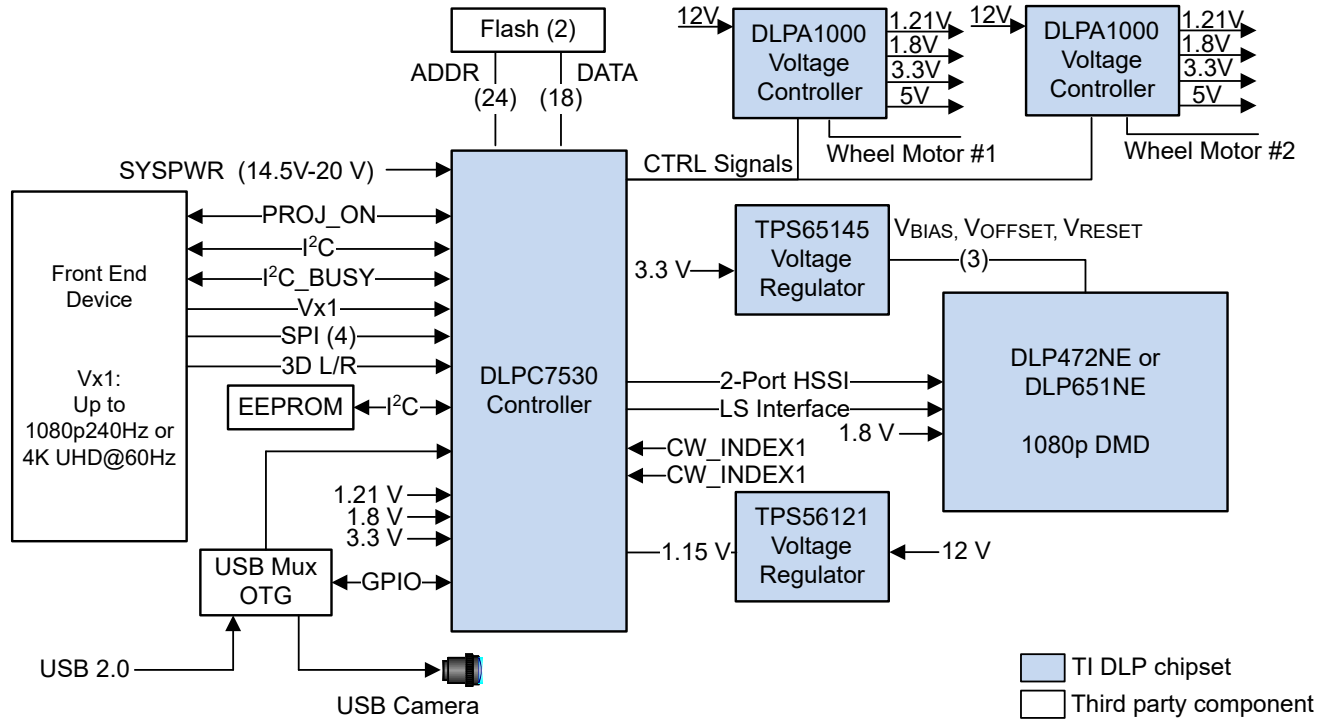


Figure 7-2. Typical 1080p LPCW System

7.2.1 Design Requirements

The display controller is the digital interface between the DMD and the rest of the system. The display controller takes digital V-by-One, FPD-Link or 30-bit parallel input from front end receiver and drives the DMD over a high speed interface. The display controller also generates the necessary signals (data, protocols, timings) required to display images on the DMD. Reliable operation of the DMD is only ensured when the DMD and the controller are used together in a system. In addition, other devices might be needed. Typically, a Flash part is needed to store the software and firmware and power supply management part required to power the DMD and the controller.

7.2.2 Detailed Design Procedure

For connecting the DLPC7530 controller and the DLP472NE and DLP651NE DMD together, see the board design files under the [DLPC7540EVM](#). It is essential to follow these layout guidelines for high-speed interfaces, V-by-One and the DMD HSSI in order to design a reliable projector. To complete the DLP system, an optical module or light engine is required that contains the DLP472NE and DLP651NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

8 Power Supply Recommendations

8.1 Power Supply Management

The DLPA100 manages power for the DLPC7530 and DMD. See [Section 5.13](#) for all power sequencing and timing requirements.

8.2 Hot Plug Usage

While the V-by-One, FPD-Link, and USB interfaces support hot plug usage (i.e. these interfaces can be connected and disconnected while the DLPC7530 is powered), the controller itself (and any DMD connected to the system) do not support Hot Plug use. As such, power down the system prior to removing the controller or DMD from any system.

8.3 Power Supplies for Unused Input Source Interfaces

While certain product configurations cannot offer or make use of all of the available input source interfaces (e.g. V-by-One, FPD-Link), *the power supplies that are associated with these unused input source interfaces must still be provided as if the interface was actually being used.* The only concession is that the ferrite based isolation filters for these supplies can be simplified down to simple de-coupling caps.

8.4 Power Supplies

8.4.1 1.15-V Power Supplies

The DLPC7530 can support a low cost power delivery system with a single 1.15-V power source derived from a switching regulator. To enable this approach, provide typical bulk (e.g. 10 μ F, 22 μ F) and high frequency (e.g. 0.1 μ F) filtering for the core 1.15-V power rail (VDD115). Ensure that the the high-frequency capacitors are evenly distributed amongst the power balls and that they are placed as close to the power balls as possible. Additional filtering must be provided for each of the uniquely defined 1.15-V power pins (e.g. VDD115_PLLMA, VAD115VX1). Filtering for the unique power pins is discussed further in [Section 9.1](#) of this document.

8.4.2 1.21V Power Supply

The DLPC7530 can support a low cost power delivery system with a single 1.21V power source derived from a switching regulator. To enable this approach, provide typical bulk (e.g. 10 μ F, 22 μ F) and high frequency (e.g. 0.1 μ F) filtering for the 1.21-V power rail (VDD121_SCS). Place the high-frequency filtering capacitors as close as possible to the VDD121_SCS power balls.

8.4.3 1.8-V Power Supplies

The DLPC7530 can support a low cost power delivery system with a single 1.8-V power source derived from a switching regulator. To enable this approach, appropriate filtering must be provided for each of the uniquely defined 1.8-V power pins (e.g. VDD18_PLLMA, VAD18_VX1). See [Section 9.1](#) for more information.

8.4.4 3.3-V Power Supplies

The DLPC7530 can support a low cost power delivery system with a single 3.3-V power source derived from a switching regulator. To enable this approach, provide typical bulk (e.g. 10 μ F, 22 μ F) and high frequency (e.g. 0.1 μ F) filtering for the main 3.3-V I/O power rail (VDD33). Ensure that the the high-frequency capacitors are evenly distributed amongst the power balls and that they are placed as close to the power balls as possible. Additional filtering must be provided for each of the uniquely defined 3.3-V power pins (e.g. VAD33_USB, VDD33_FPD). This is discussed further in [Section 9.1](#) of the document.

9 Layout

9.1 Layout Guidelines

9.1.1 General Layout Guidelines

In order to meet the thermal loads associated with the DLPC7530, TI recommends the following enhanced PCB design parameters.

- A minimum of 4 power and ground planes
 - Power layers: 1-oz. copper; Ground layers: 2-oz. copper
 - Copper coverage: 90%
 - Top and bottom signal layers: minimum 0.5-oz copper
 - Internal signal layers: 1-oz copper
- Thermal copper ground planes beneath the thermal ball array of package containing a via farm with the following attributes
 - Thermal via quantity to ground plane = 64 (as 8x8 array)
 - Thermal via size = 0.229mm - 0.25 mm (9mils - 10 mils)
 - Thermal via plating thickness = 0.025 mm (1 mil) wall thickness

For signal integrity reasons, FR370HR or equivalent high performance epoxy laminate and prepreg is also recommended.

9.1.2 Power Supply Layout Guidelines

The following filtering circuits are recommended for the power supply inputs listed below.

- VAD115_VX1
- VAD18_VX1
- VAD115_FPD
- VDD33_FPD
- VAD33_USB
- VDD18_SCS

Because the PBC layout is critical to the performance of the interfaces associated with these power supplies, it is vital that these power supplies be treated like an analog signal. Specifically:

- Place high-frequency components (such as ferrites and capacitors) as close to the power ball(s) as possible.
- Choose high-frequency ceramic capacitors (such as those with a value of 0.1 μF , 0.01 μF , and 100 nF) that have low ESR and ESL values. Design the leads as short as possible, and as such, place these capacitors under the package on the opposite side of the board.
- For each power pin, a single trace (as wide as possible) must be used from the controller to the capacitor and then through the series ferrite to the power source.
- For each power pin, add a 100-nF decoupling capacitor placed near the escape via. Add this decoupling capacitance to the capacitance recommended for filters. These are minimum recommendations, so different layouts could require additional capacitance.
- See [Table 9-1](#) for the recommended series ferrite component for these supplies.

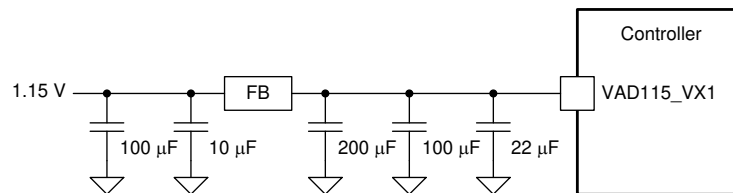


Figure 9-1. VAD115_VX1 (V-by-One) Recommended Filter

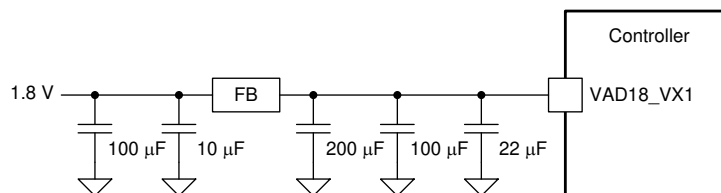


Figure 9-2. VAD18_VX1 (V-by-One) Recommended Filter

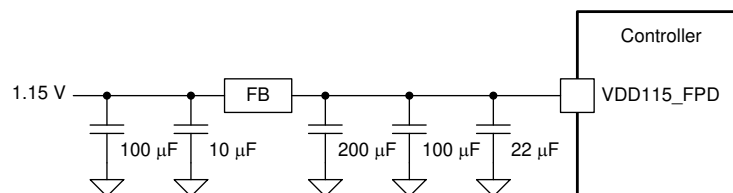


Figure 9-3. VAD115_FPD (FPD-Link) Recommended Filter

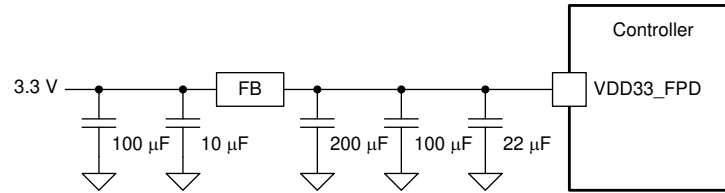


Figure 9-4. VDD33_FPD (FPD-Link) Recommended Filter

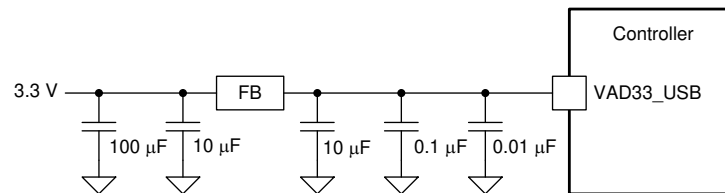


Figure 9-5. VAD33_USB (USB) Recommended Filter

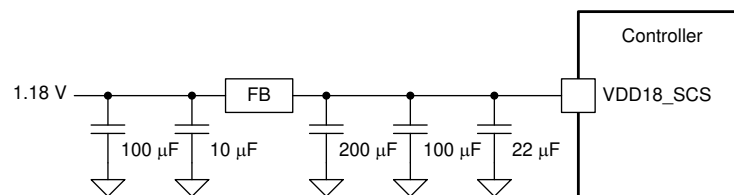


Figure 9-6. VDD18_SCS (SCS DRAM) Recommended Filter

9.1.3 Layout Guidelines for Internal Controller PLL Power

The following guidelines are recommended to achieve the desired Controller performance relative to the internal PLLs. The DLPC7530 contains multiple internal PLLs which have dedicated 1.15-V supply pins and 1.8-V supply pins which are listed below:

- VDD115_PLLMA
- VDD115_PLLMB
- VAD115_PLLS
- VAD115_HSSI0_PLL
- VAD115_HSSI1_PLL

and

- VAD18_PLLMA
- VAD18_PLLMB

It is important that each of these 1.15-V and 1.8-V supply pins have individual high frequency filtering in the form of a ferrite bead and a 0.1-μF ceramic capacitor. Ensure that the impedance of the ferrite bead is much greater than that of the capacitor at frequencies above 10 MHz. Locate these components very close to the individual PLL power supply balls. Recommended values, topology, and layout examples are shown in [Table 9-1](#), [Figure 9-7](#) and [Figure 9-8](#), and [Figure 9-9](#) respectively.

Table 9-1. Recommended PLL and Crystal Power Supply Filter Components

COMPONENT	PARAMETER	RECOMMENDED VALUE	UNIT
Shunt capacitor	Capacitance	0.1	μF
	Impedance at 100 MHz	> 100	Ω
Series ferrite	DC Resistance	< 0.40	Ω

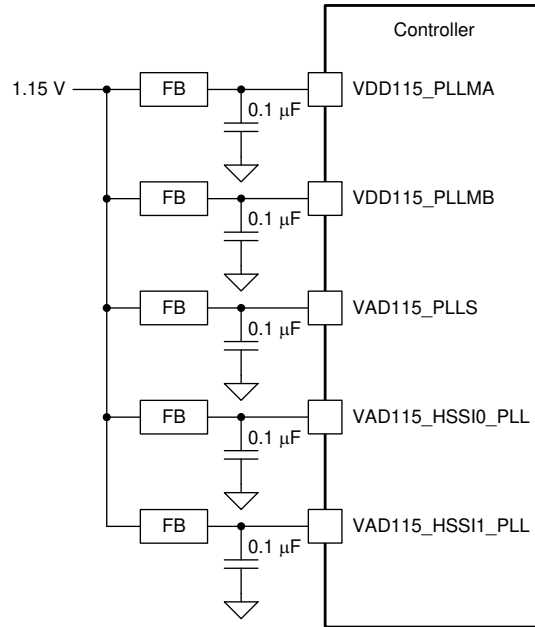


Figure 9-7. 1.15-V PLL Power Supply Filter Topology

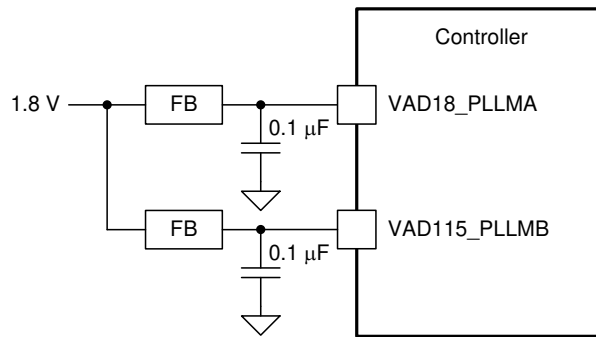


Figure 9-8. 1.8-V PLL Power Supply Filter Topology

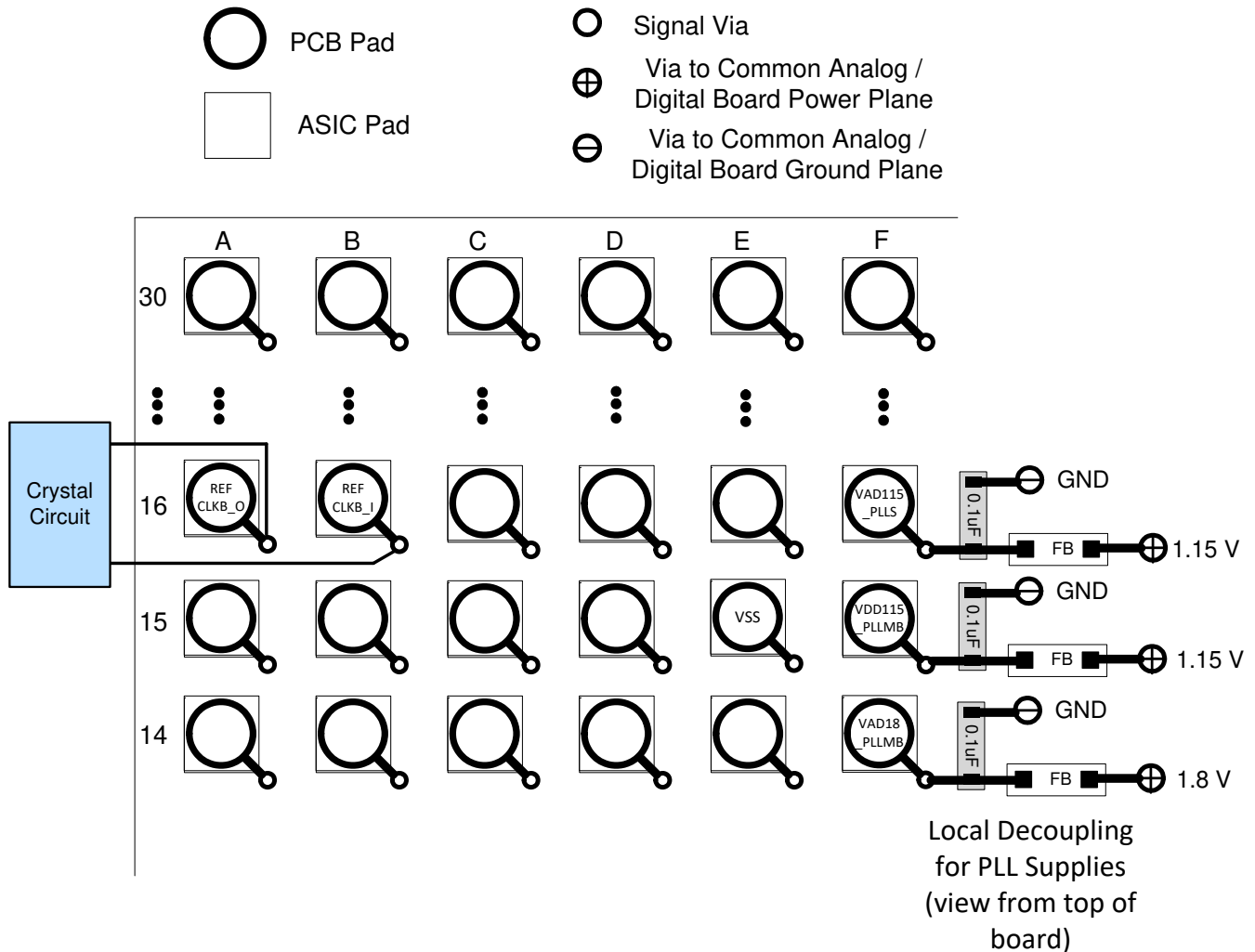


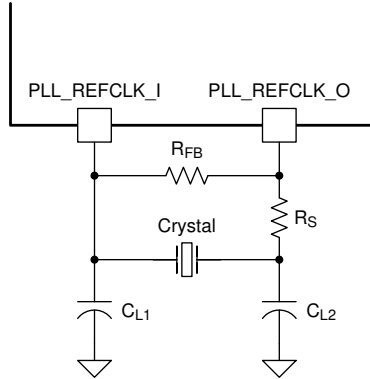
Figure 9-9. PLL Power Supply Filter Layout Examples

Since the PCB layout is critical to PLL performance, it is vital that the PLL power is treated like an analog signal. Additional design guidelines are as follows:

- Place all filter components as close as possible to each of the PLL supply package pins.
- Keep the leads of the high-frequency capacitors as short as possible, and as such, it is recommended that these capacitors be placed under the package on the opposite side of the board.
- Use a surface mount capacitor that is of high quality, low ESR, and monolithic.
- For each PLL power pin, a single trace (as wide as possible) must be used from the DLPC7530 to the capacitor and then through the series ferrite to the power source.

9.1.4 Layout Guideline for DLPC7530 Reference Clock

The DLPC7530 requires two external reference clocks to feed its internal PLLs. A crystal or oscillator can supply these references. The recommended crystal configurations and reference clock frequencies are listed in [Table 9-2](#), with additional required discrete components shown in [Figure 9-10](#) and defined in [Table 9-2](#).



C_L = Crystal load capacitance

R_{FB} = Feedback Resistor

Figure 9-10. Discrete Components Required for Crystal

9.1.4.1 Recommended Crystal Oscillator Configuration

Table 9-2. Recommended Crystal Configurations

PARAMETER	CRYSTAL A	CRYSTAL B	UNIT
Crystal circuit configuration	Parallel resonant	Parallel resonant	
Crystal type	Fundamental (first harmonic)	Fundamental (first harmonic)	
Crystal nominal frequency	40	38	MHz
Crystal frequency tolerance ⁽¹⁾	±100 (200 p-p max)	±100 (200 p-p max)	PPM
Crystal equivalent series resistance (ESR)	60 (Max)	60 (Max)	Ω
Crystal load capacitance	20 (Max)	20 (Max)	pF
Crystal Shunt Load capacitance	7 (Max)	7 (Max)	pF
Temperature range	–40°C to +85°C	–40°C to +85°C	°C
Drive level	100 (Nominal)	100 (Nominal)	μW
R_{FB} feedback resistor (nominal)	1 Meg (Nominal)	1 Meg (Nominal)	Ω
C_{L1} external crystal load capacitor	See equation in ⁽²⁾ .	See equation in ⁽²⁾ .	pF
C_{L2} external crystal load capacitor	See equation in ⁽³⁾ .	See equation in ⁽³⁾ .	pF
PCB layout	A ground isolation ring around the crystal is recommended.	A ground isolation ring around the crystal is recommended.	

(1) Crystal frequency tolerance to include accuracy, temperature, aging, and trim sensitivity. These are typically specified separately and the sum of all required to meet this requirement.

(2) $CL1 = 2 \times (CL - C_{stray_pll_refclk_i})$, where: $C_{stray_pll_refclk_i}$ = Sum of package and PCB stray capacitance at the crystal pin associated with the Controller pin REFCLKx_I. See [Table 9-3](#).

(3) $CL2 = 2 \times (CL - C_{stray_pll_refclk_o})$, where: $C_{stray_pll_refclk_o}$ = Sum of package and PCB stray capacitance at the crystal pin associated with the Controller pin REFCLKx_O. See [Table 9-3](#).

Table 9-3. Crystal Pin Capacitance

PARAMETER		MIN	NOM	MAX	UNITS
Cstray_pll_refclkA_i	Sum of package and PCB stray capacitance at REFCLKA_I		4.5		pF
Cstray_pll_refclkA_o	Sum of package and PCB stray capacitance at REFCLKA_O		4.5		pF
Cstray_pll_refclkB_i	Sum of package and PCB stray capacitance at REFCLKB_I		4.5		pF
Cstray_pll_refclkB_o	Sum of package and PCB stray capacitance at REFCLKB_O		4.5		pF

The crystal circuits in the DLPC7530 have dedicated power (VAD33_OSCA and VAD33_OSCB) pins, with the recommended filtering for each shown in [Figure 9-11](#), and recommended values shown in [Table 9-1](#).

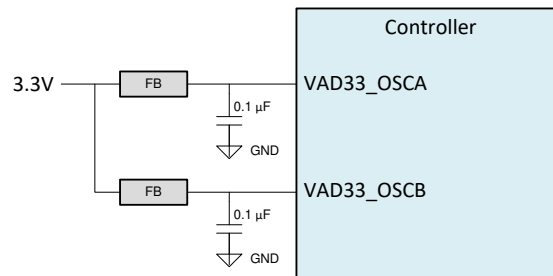


Figure 9-11. Crystal Power Supply Filtering

Table 9-4. DLPC7530 Recommended Crystal Parts

MANUFACTURER	PART NUMBER	NOMINAL FREQUENCY	FREQUENCY TOLERANCE, FREQUENCY STABILITY, AGING/YEAR	ESR	LOAD CAPACITANCE	OPERATING TEMPERATURE	DRIVE LEVEL
TXC	7M38070001 ⁽¹⁾	38 MHz	Freq Tolerance: ±20 ppm	30-Ω max	12 pF	-40°C to +85°C	100 µW
			Freq Stability: ±20 ppm				
			Aging/Year: ±3 ppm				
TXC	7M40070041 ⁽²⁾	40 MHz	Freq Tolerance: ±20 ppm	30-Ω max	12 pF	-40°C to +85°C	100 µW
			Freq Stability: ±20 ppm				
			Aging/Year: ±3 ppm				

- (1) This device requires an R_S resistor with value = 0.
- (2) This device requires an R_S resistor with value = 0.

9.1.5 V-by-One Interface Layout Considerations

The DLPC7530 V-by-One SERDES differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC7530 I/O timing parameters, V-by-One transmitter timing parameters, as well as Thine specific timing requirements can be found in their corresponding data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB related requirements for V-by-One are provided in [Table 9-5](#) as a starting point for the customer.

Table 9-5. V-by-One Interface PBC Related Requirements (1)

PARAMETER	MIN	TYP	MAX	UNIT
Intra-lane cross-talk (between VX1_DATAx_P and VX1_DATAx_N)			< 1.5	mVpp
Inter-lane cross-talk (between data lane pairs)			< 1.5	mVpp
Cross-talk between data lanes and other signals			< 1.5	mVpp
Intra-lane skew			< 40	ps
Inter-lane skew			< 5	UI
Differential Impedance	90	100	110	Ω

(1) If using the minimum trace width and spacing to escape the Controller ball field, widening these out after escape is desirable if practical to achieve the target 100 Ω impedance (e.g. to reduce transmission line losses).

Additional V-by-One layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a Micro-strip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair, and between each pair, in order to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pairs are between 135° and 225°(See [Figure 9-12](#)).

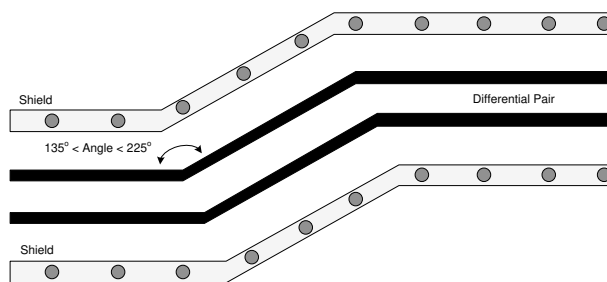


Figure 9-12. V-by-One Routing Example

9.1.6 FPD-Link Interface Layout Considerations

The DLPC7530 FPD-Link differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC7530 I/O timing parameters as well as the FPD-Link transmitter timing parameters can be found in their corresponding data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB related requirements for FPD-Link are provided in [Table 9-6](#) as a starting point for the customer.

Table 9-6. FPD-Link Interface PBC Related Requirements

PARAMETER	MIN	TYP	MAX	UNIT
Intra-lane Cross-talk (between FPDz_DATAx_P and FPDz_DATAx_N)			< 2.0	mVpp
Inter-lane Cross-talk (between data lane pairs)			< 2.0	mVpp
Cross-talk between data lanes and other signals			< 2.0	mVpp
Intra-lane skew			< 40	ps
Inter-lane skew			± 40	ps
Differential Impedance	90	100	110	Ω

Additional FPD-Link layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a Micro-strip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair, and between each pair, in order to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pairs are between 135° and 225° (See [Figure 9-13](#)).

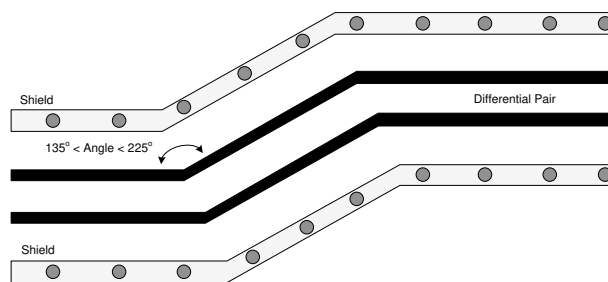


Figure 9-13. FPD-Link Routing Example

9.1.7 USB Interface Layout Considerations

The DLPC7530 USB differential interface waveform quality and timing are dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well-matched the lengths are across the interface. Thus, ensuring a positive timing margin requires attention to many factors.

DLPC7530 I/O timing parameters, USB transmitter, and receiver timing parameters, as well as USB-specific timing requirements can be found in their corresponding data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB-related requirements for USBs are provided in [Table 9-7](#) as a starting point for the customer.

Table 9-7. USB Interface PBC Related Requirements (1)(2)

PARAMETER	MIN	TYP	MAX	UNIT
Cross-talk between data lane (USB_DAT_P, USB_DAT_N) and other signals			< 1.5	mVpp
Intra-lane skew (USB_DAT_P, USB_DAT_N)			< 20	ps
Differential Impedance (USB_DAT_P, USB_DAT_N)	76.5	90	103.5	Ω
Single Mode impedance (USB_DAT_P, USB_DAT_N)		45		Ω
Common Mode Impedance (USB_DAT_P, USB_DAT_N)	21	30	39	Ω
Parasitic resistance (USB_DAT_P, USB_DAT_N)			≤ 0.5	Ω
Total capacitance (USB_DAT_P, USB_DAT_N)			< 4	pF
Differences of trace capacitance between USB_DAT_P, USB_DAT_N			< 1	pF
TXRTUNE resistor	172.26	174	175.74	Ω

- (1) If using the minimum trace width and spacing to escape the Controller ball field, widening these out after escape is desirable if practical to achieve the target 100 Ω impedance (that is, to reduce transmission line losses).
- (2) One PCB layout example for the differential pair is shown in [Figure 9-14](#).

Additional layout guidelines for USB_DAT_P/USB_DAT_N:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a Micro-strip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair, and between each pair, to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pair are between 135° and 225°. (See [Figure 9-15](#).)
- Minimize the length where the differential signal pair is parallel to clocks or digital signals.
- Do not route the differential signal pair under an IC that uses a quartz crystal, oscillator, clock synchronization circuit, magnetic device, or clock.

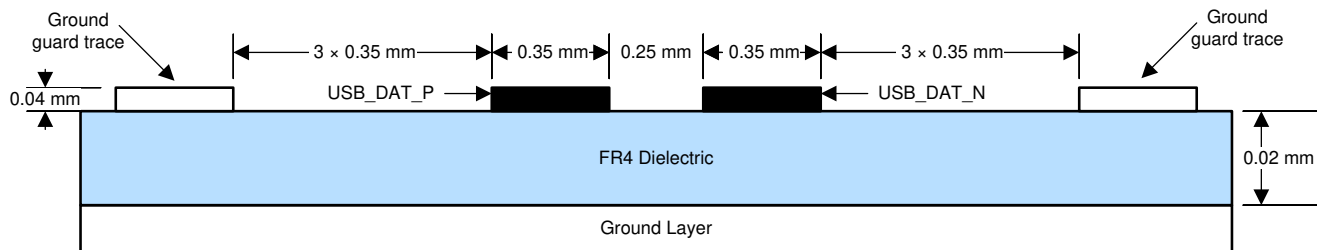


Figure 9-14. USB Layout Example

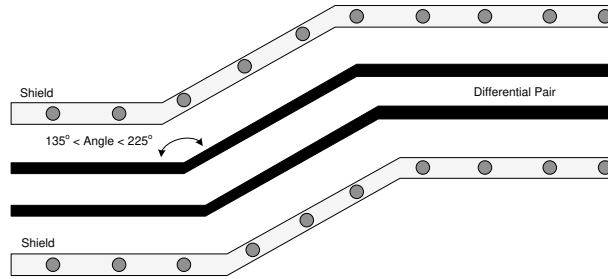


Figure 9-15. USB Routing Example

Additional USB layout guidelines for TXRTUNE

- Use the shortest possible connection lengths for the resistor between TXRTUNE and ground.
- Use ground layer and ground guard traces to shield the wires and resistor.

9.1.8 DMD Interface Layout Considerations

The DLPC7530 controller HSSI differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring a positive timing margin requires attention to many factors.

DLPC7530 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB design recommendations are provided in [Table 9-8](#), [Figure 9-16](#), and the paragraph below as a starting point for the customer.

Table 9-8. PCB Recommendations for DMD Interface⁽¹⁾⁽²⁾

PARAMETER	MIN	MAX	UNIT
T_W Trace Width	5.7		mils
T_S Intra-lane Trace Spacing	5.3		mils
T_{SPP} Inter-lane trace spacing ⁽³⁾	48.3		mils

- (1) Recommendations to achieve the desired nominal differential impedance as specified by R_{DIFF} in [Section 5.7](#).
- (2) These parameters show recommendations based on the micro-strip design shown in [Figure 9-16](#). This design minimizes signal loss to support longer trace lengths at the expense of electromagnetic interference (EMI). The designer has the option to use a stripline design for shorter trace lengths and to target minimizing EMI at the expense of signal loss.
- (3) A reduced inter-lane spacing can be used to escape the controller ball field, however, widen this spacing to at least the stated minimum after the escape.

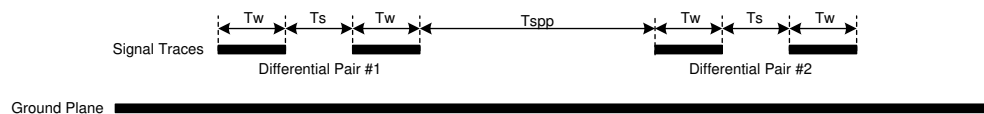


Figure 9-16. DMD Differential Layout Recommendations

Additional DMD interface layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two. If two are required, place one at each end of the line (one at the controller and one at the DMD).
- Route the differential signal pairs over a single ground or power plane using a Micro-strip line configuration.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Ensure the bend angles associated with the differential signal pairs are between 135° and 225°.
- Route the single-ended signal in a way that minimizes the number of vias required. Limit the number of necessary vias to two. If two are required, place one at each end of the line (one at the controller and one at the DMD).
- Avoid stubs.

- No external termination resistors are required on the DMD_HSSI or DMD_LS differential signals.
- Include a series termination resistor (with a value of 30.1Ω, for example) to the DMD_LS0_RDATA and DMD_LS1_RDATA single-ended signal paths. Place the resistor as close as possible to the corresponding DMD pin.
- The DMD_DEN_ARSTZ does not typically require a series resistor; however, for a long trace, one might be needed to reduce undershoot or overshoot.

9.1.9 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potential damage to unused video source inputs and unused GPIO, the instructions specifically noted in the associated [Section 4](#) must be followed. For those unused inputs without specific instructions, TI recommends that these input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. Unused output-only pins can remain open. Never tie unused output-only pins directly to power or ground. For controller inputs with an internal pullup or pulldown resistor, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Internal pullup and pulldown resistors are weak and cannot be expected to drive the external line. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value specified in [Table 4-14](#).

There are also power supply considerations that must be followed for any unused video sources. These are detailed in [Section 8.3](#).

9.1.10 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 9-9. Max Pin-to-Pin PCB Interconnect Recommendations—DMD

CONTROLLER INTERFACE	SIGNAL INTERCONNECT TOPOLOGY ⁽¹⁾ ⁽²⁾ ⁽³⁾		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HSSI0_CLK_P DMD_HSSI0_CLK_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI0_D0_P DMD_HSSI0_D0_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI0_D1_P DMD_HSSI0_D1_N			
DMD_HSSI0_D2_P DMD_HSSI0_D2_N			
DMD_HSSI0_D3_P DMD_HSSI0_D3_N			
DMD_HSSI0_D4_P DMD_HSSI0_D4_N			
DMD_HSSI0_D5_P DMD_HSSI0_D5_N			
DMD_HSSI0_D6_P DMD_HSSI0_D6_N			
DMD_HSSI0_D7_P DMD_HSSI0_D7_N			
DMD_HSSI1_CLK_P DMD_HSSI1_CLK_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI1_D0_P DMD_HSSI1_D0_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI1_D1_P DMD_HSSI1_D1_N			
DMD_HSSI1_D2_P DMD_HSSI1_D2_N			
DMD_HSSI1_D3_P DMD_HSSI1_D3_N			
DMD_HSSI1_D4_P DMD_HSSI1_D4_N			
DMD_HSSI1_D5_P DMD_HSSI1_D5_N			
DMD_HSSI1_D6_P DMD_HSSI1_D6_N			
DMD_HSSI1_D7_P DMD_HSSI1_D7_N			
DMD_LS0_CLK_P DMD_LS0_CLK_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS0_WDATA_P DMD_LS0_WDATA_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS1_CLK_P DMD_LS1_CLK_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS1_WDATA_P DMD_LS1_WDATA_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS0_RDATA	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS1_RDATA	18 (457.2)	18 (457.2)	inch (mm)

Table 9-9. Max Pin-to-Pin PCB Interconnect Recommendations—DMD (continued)

CONTROLLER INTERFACE	SIGNAL INTERCONNECT TOPOLOGY ^{(1) (2) (3)}		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

- (1) Max signal routing length includes escape routing.
- (2) Multi-board DMD routing lengths shown are the combination that was analyzed by TI.
- (3) Due to board variations, create a SPICE simulation for all board designs with the Controller IBIS models to ensure signal routing lengths do not exceed signal requirements.

Table 9-10. High-Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING ^{(1) (2)}				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH ⁽³⁾	UNIT
DMD ⁽⁴⁾	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI0_CLK_P DMD_HSSI0_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HSSI0_D1_P DMD_HSSI0_D1_N			
	DMD_HSSI0_D2_P DMD_HSSI0_D2_N			
	DMD_HSSI0_D3_P DMD_HSSI0_D3_N			
	DMD_HSSI0_D4_P DMD_HSSI0_D4_N			
	DMD_HSSI0_D5_P DMD_HSSI0_D5_N			
	DMD_HSSI0_D6_P DMD_HSSI0_D6_N			
	DMD_HSSI0_D7_P DMD_HSSI0_D7_N			
DMD ⁽⁵⁾	DMD_HSSI0_x_P	DMD_HSSI0_x_N	±0.01 (±0.254)	inch (mm)
DMD ⁽⁴⁾	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI1_CLK_P DMD_HSSI1_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HSSI1_D1_P DMD_HSSI1_D1_N			
	DMD_HSSI1_D2_P DMD_HSSI1_D2_N			
	DMD_HSSI1_D3_P DMD_HSSI1_D3_N			
	DMD_HSSI1_D4_P DMD_HSSI1_D4_N			
	DMD_HSSI1_D5_P DMD_HSSI1_D5_N			
	DMD_HSSI1_D6_P DMD_HSSI1_D6_N			
	DMD_HSSI1_D7_P DMD_HSSI1_D7_N			
DMD ⁽⁵⁾	DMD_HSSI1_x_P	DMD_HSSI1_x_N	±0.01 (±0.254)	inch (mm)
DMD ⁽⁶⁾	DMD_HSSI0_CLK_P	DMD_HSSI1_CLK_P	±0.05 (±1.27)	inch (mm)
DMD ⁽⁶⁾	DMD_HSSI0_CLK_N	DMD_HSSI1_CLK_N	±0.05 (±1.27)	inch (mm)
DMD ⁽⁴⁾	DMD_LS0_WDATA_P DMD_LS0_WDATA_N	DMD_LS0_CLK_P DMD_LS0_CLK_N	±1.0 (±25.4)	inch (mm)

Table 9-10. High-Speed PCB Signal Routing Matching Requirements (continued)

SIGNAL GROUP LENGTH MATCHING ^{(1) (2)}				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH ⁽³⁾	UNIT
DMD ⁽⁵⁾	DMD_LS0_x_P	DMD_LS0_x_N	±0.025 (±0.635)	inch (mm)
DMD ⁽⁴⁾	DMD_LS1_WDATA_P DMD_LS1_WDATA_N	DMD_LS1_CLK_P DMD_LS1_CLK_N	±1.0 (±25.4)	inch (mm)
DMD ⁽⁵⁾	DMD_LS1_x_P	DMD_LS1_x_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS0_RDATA DMD_LS1_RDATA	N/A	N/A ⁽⁷⁾	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

- (1) These routing requirements are specific to the PCB routing. Internal package routing mismatches in the DLPC7530 and DLP472NE and DLP651NE have already been accounted for in these requirements.
- (2) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
- (3) This requirement must be maintained from the controller to the DMD, even if the signals traverse multiple boards.
- (4) This is an inter-pair specification (that is, differential pair to differential pair within the group).
- (5) This is an intra-pair specification (that is, length mismatch between P and N for the same pair). This is applicable to both clock and data.
- (6) This is a channel to channel skew specification.
- (7) The low speed read control interface from the DMD is single ended, and makes use of the differential write clock. As such, a routing mismatch between these is not applicable.

9.2 Thermal Considerations

The underlying thermal requirement for the DLPC7530 is that the maximum operating junction temperature (T_J) not be exceeded (defined in the [Section 5.3](#)). This temperature is dependent on the operating ambient temperature, heatsink, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC7530, and power dissipation of surrounding components. The DLPC7530's package is designed to extract heat via the package heat slug to the heatsink, through the thermal balls, and the power and ground planes of the PCB. Thus, heatsink, copper content, and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on the maximum DLPC7530 power dissipation and $R_{\theta JA}$ at 0m/s, 1m/s, and 2m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using the test board described in [Section 9.1.1](#). This test PCB is not necessarily representative of the customer PCB and thus the reported thermal resistance can differ from the actual product application. Although the actual thermal resistance can be different, it is the best information available during the design phase to estimate thermal performance. TI highly recommends that once the host PCB is designed and built, the thermal performance be measured and validated.

To do this, measure the top center case temperature under the worst-case product scenario (max power dissipation, max voltage, max ambient temperature) and validate that the maximum recommended case temperature (T_C) is not exceeded. This specification is based on the measured ϕ_{JT} for the DLPC7530 package provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. Ensure that the bead and thermocouple wire contact the top of the package. Cover the bead and thermocouple wire with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

10 Device and Documentation Support

10.1 Device Support

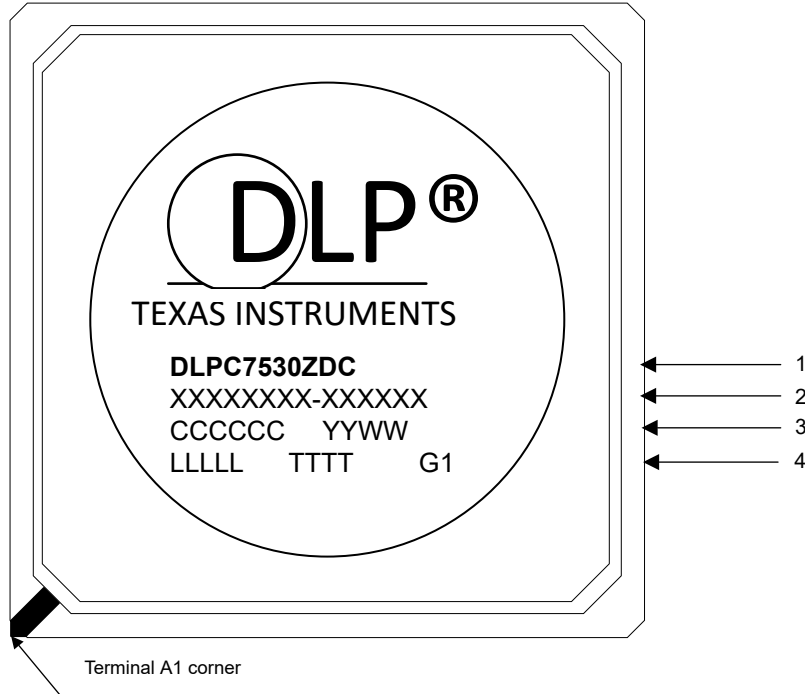
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10.1.2 Device Nomenclature

10.1.2.1 Device Markings



Marking Definitions:

Line 1:	TI Part Number: Engineering Samples	DLPC7530 = Device ID blank or A, B, C ... = Part Revision ZDC = Package designator
	TI Part Number: Production	DLPC7530 = Device ID blank or A, B, C ... = Part Revision ZDC = Package designator
Line 2:	Vendor Information	XXXXXXXX-XXXXXX
Line 3:	Vendor Country Year and Week code	CCCCCC = Country YY = Year WW = Week May also include 3 character Site Code after WW ZZZ=Site Code
Line 4:	Vendor Lot and Trace Code	LLLLL = Lot code TTTT = Trace code (may be blank)

10.1.2.2 Package Data

Table 10-1. Package Information

PARAMETER	VALUE	UNITS
Number of balls (signal/thermal)	612 / 64	
Ball pitch	1.00	mm
UBM (under bump metallurgy)	0.48 (See Figure 10-1)	mm
BPD (ball pad diameter)	0.58 (See Figure 10-1)	mm
Body dimension	See Mechanical Drawing	mm
Mold compound dimensions	See Mechanical Drawing	mm

Table 10-1. Package Information (continued)

PARAMETER	VALUE	UNITS
Package volume class	350 - 2000 (J-STD-20D)	mm ³
Approximate weight	5.64	g
Substrate circuit	Pb-free	
Package balls	Pb-free	
Solder paste	Pb-free	
Solder profile	T _C = 250°C, T _P = 253°C (J-STD-20D)	
Moisture sensitivity level	MSL Level 3 (J-STD-20D)	
Solder ball composition	SAC305	
Wirebond	Cu	
Mounting technique	a) Hot air reflow (including the combination of long and/or medium infrared ray reflow) b) Long or medium infrared ray reflow	

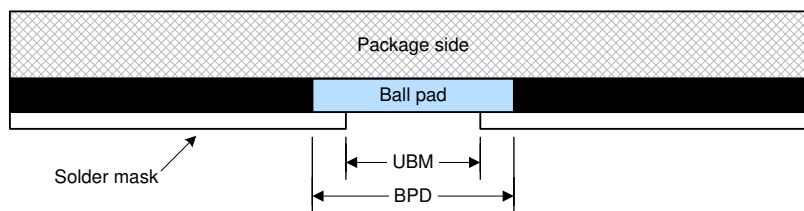


Figure 10-1. Package Ball Parameters

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

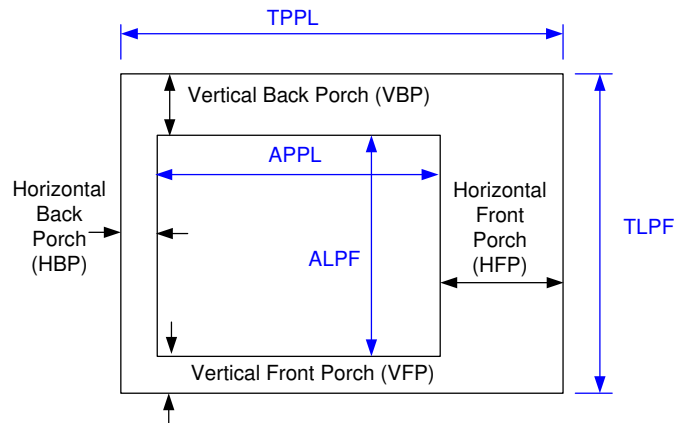
10.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10.6.1 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF)	Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.
Active Pixels Per Line (APPL)	Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.
Horizontal Back Porch (HBP) Blanking	Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.
Horizontal Front Porch (HFP) Blanking	Number of blank pixel clocks after the last active pixel but before Horizontal Sync.
Horizontal Sync (HS)	Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.
Total Lines Per Frame (TLPF)	Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).
Total Pixel Per Line (TPPL)	Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
Vertical Sync (VS)	Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.
Vertical Back Porch (VBP) Blanking	Number of blank lines after vertical sync but before the first active line.
Vertical Front Porch (VFP) Blanking	Number of blank lines after the last active line but before vertical sync.



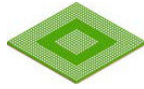
11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

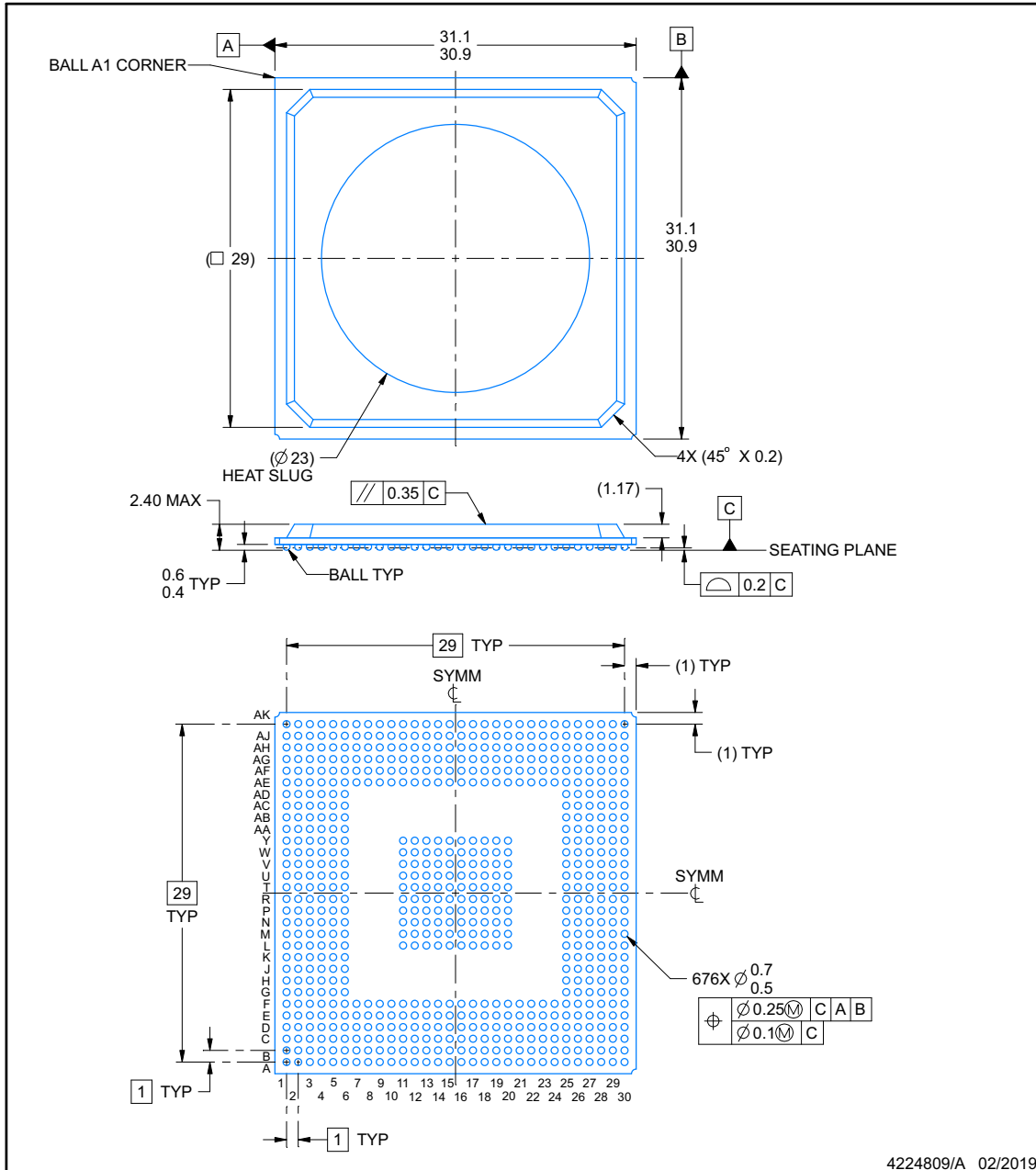


PACKAGE OUTLINE

ZDC0676A

PBGA - 2.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

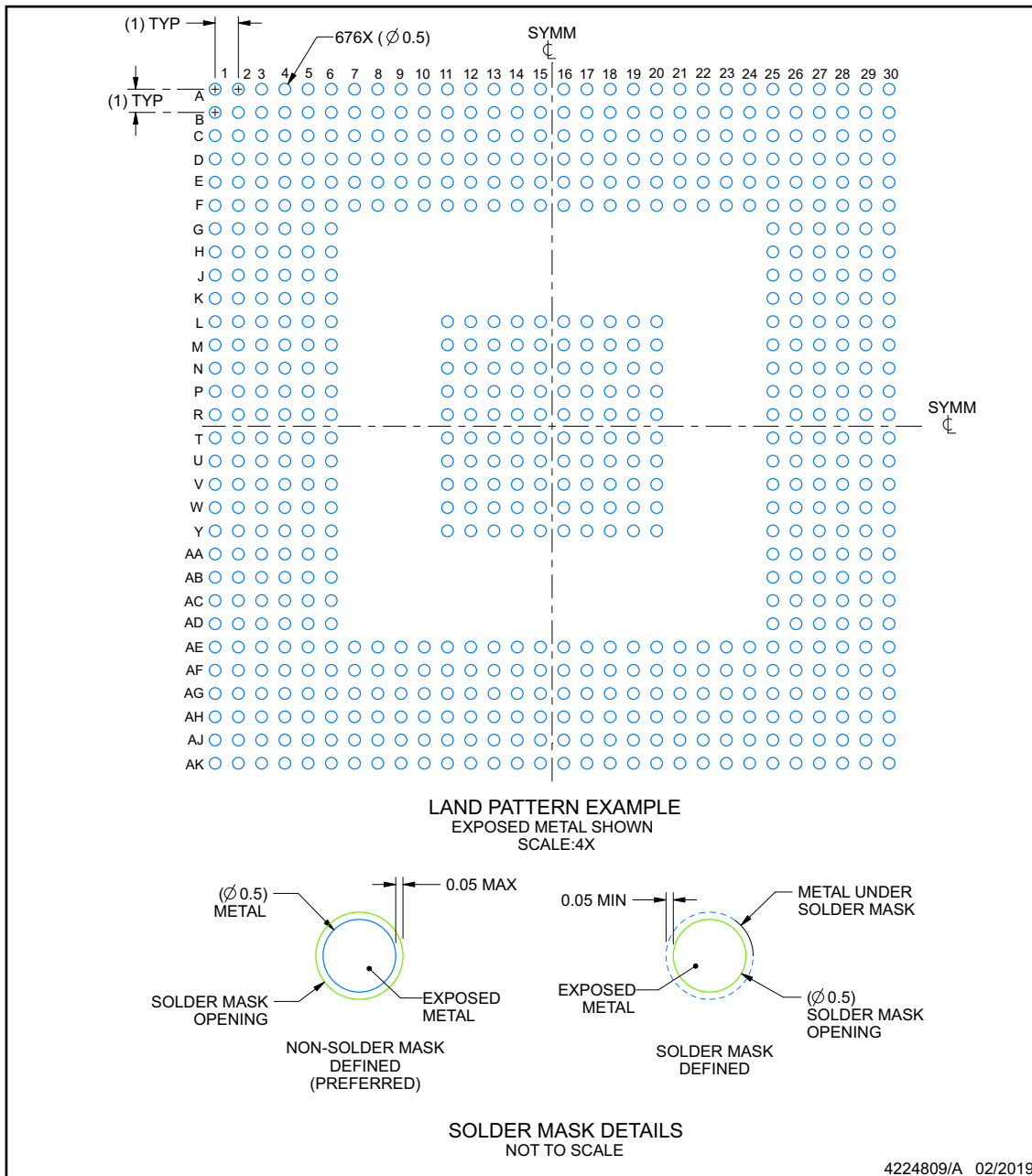
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZDC0676A

PBGA - 2.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

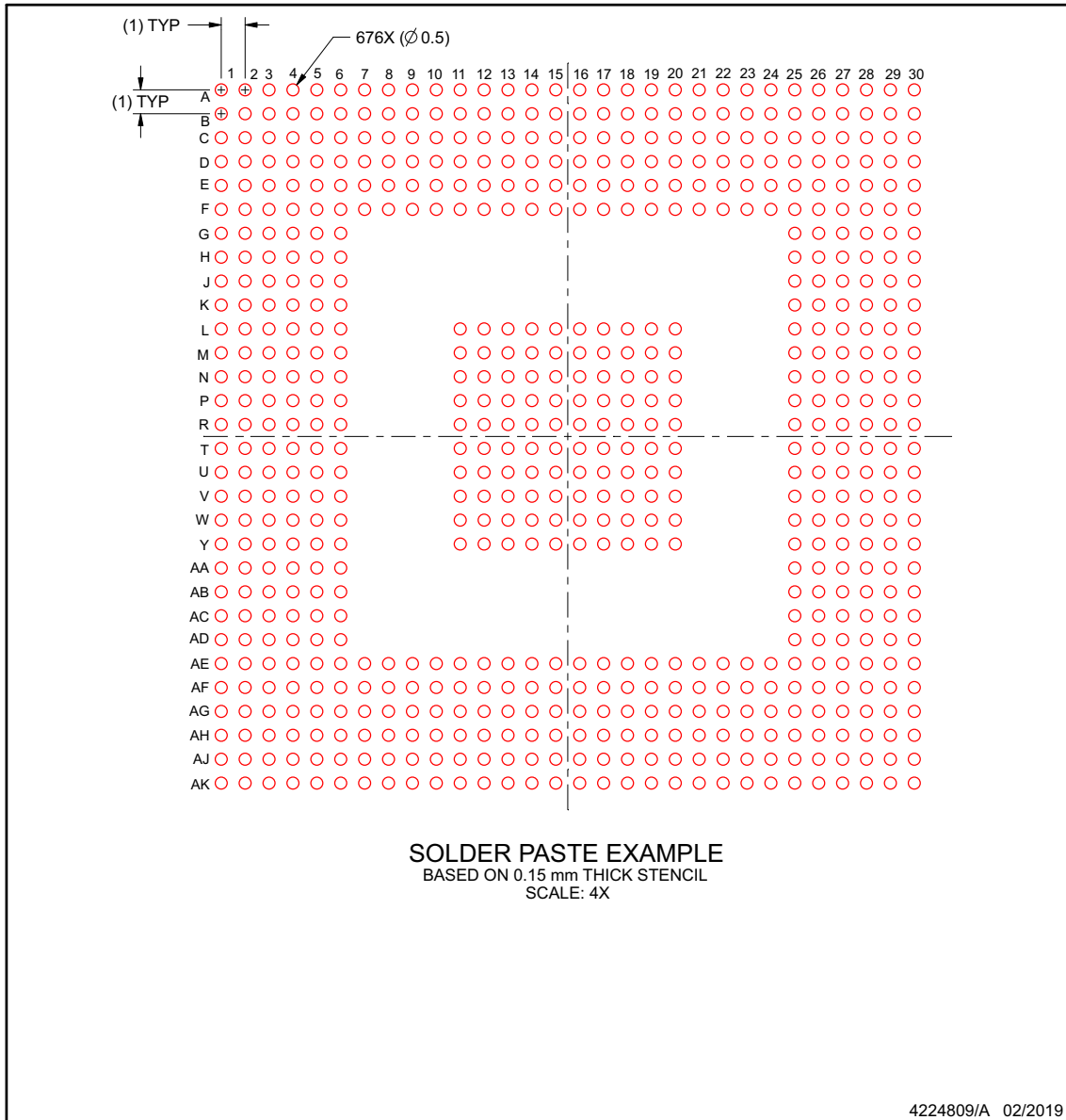
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).

EXAMPLE STENCIL DESIGN

ZDC0676A

PBGA - 2.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC7530ZDC	ACTIVE	BGA	ZDC	676	40	TBD	Call TI	Call TI	0 to 55		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

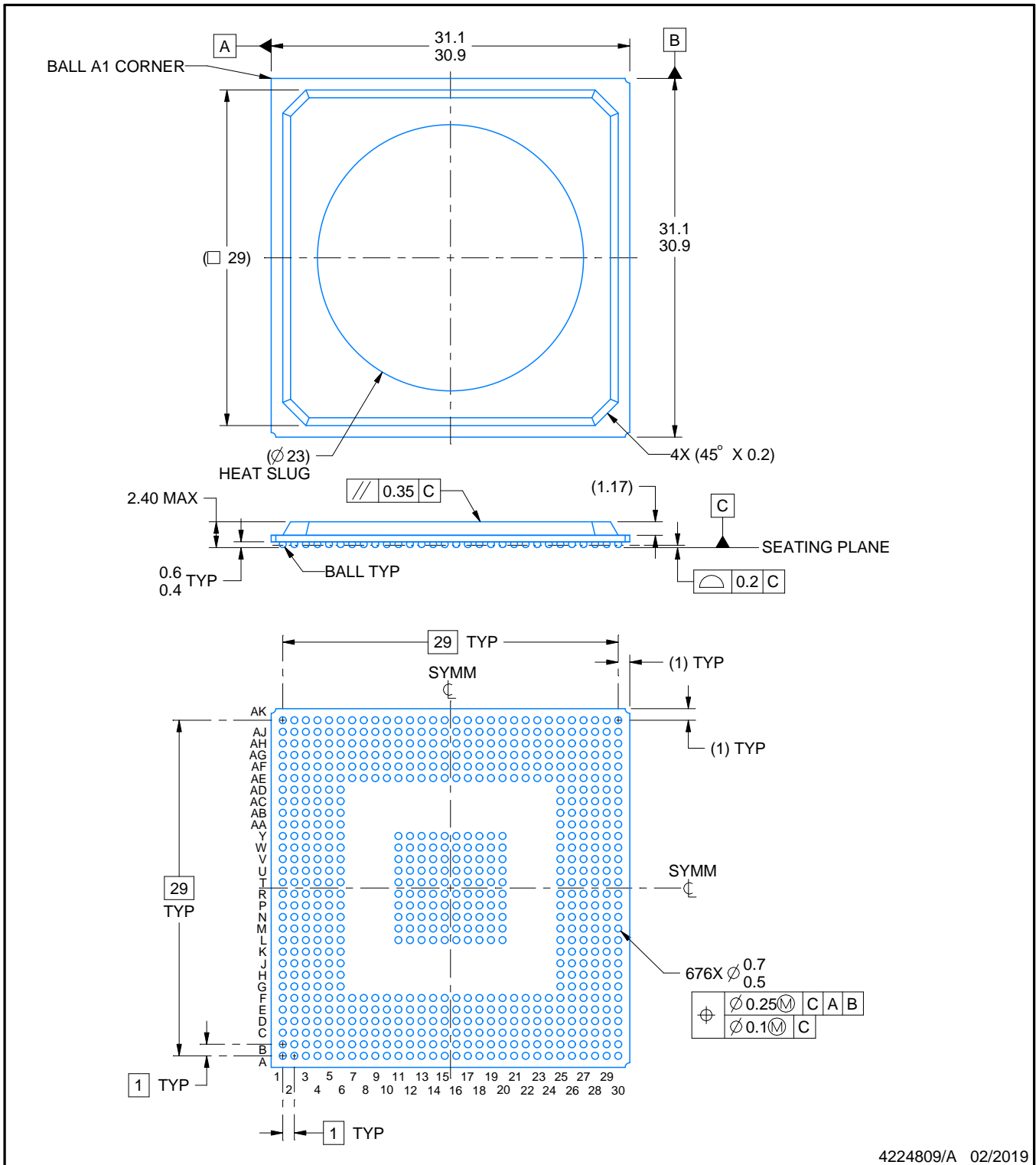
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

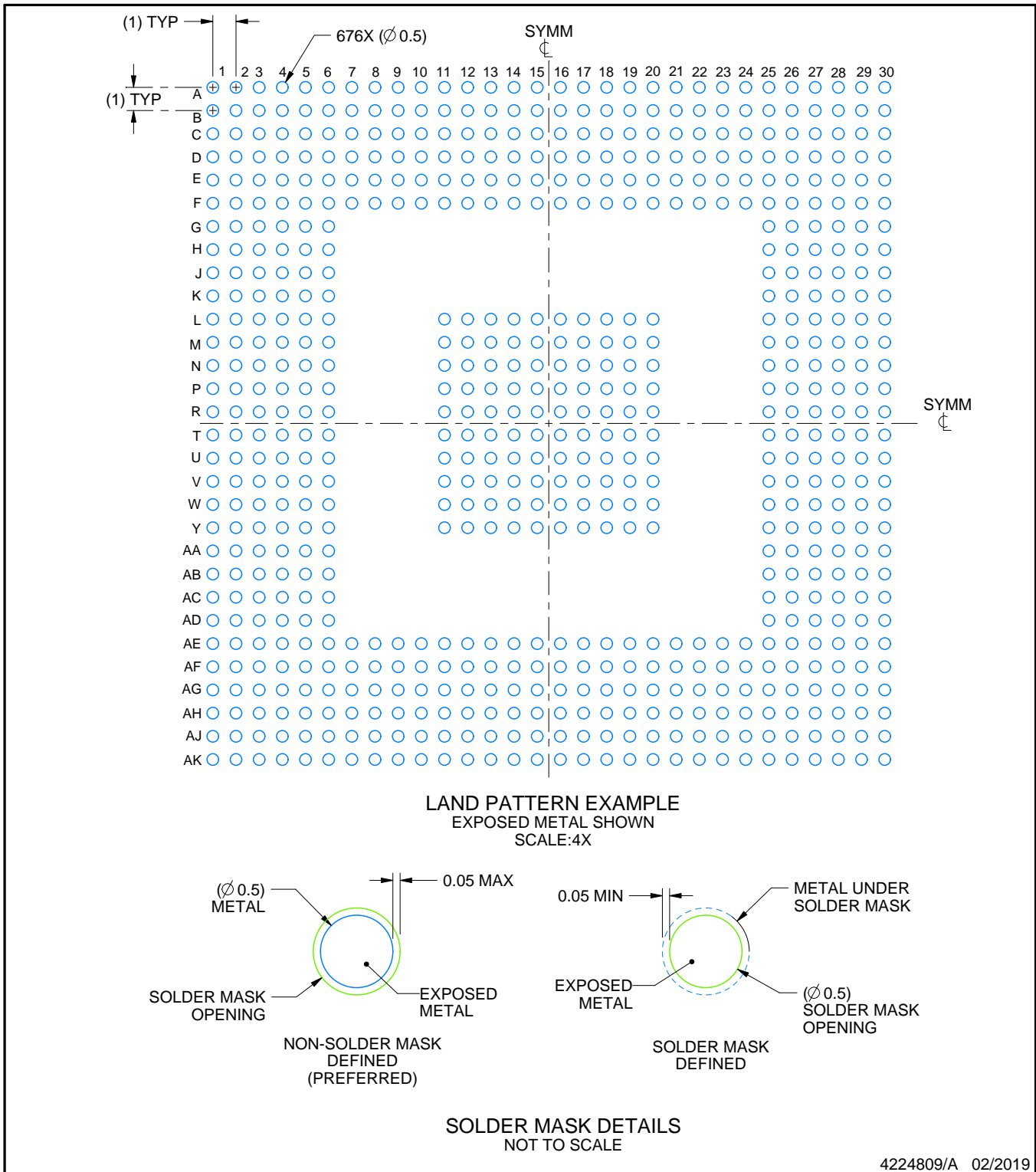
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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EXAMPLE BOARD LAYOUT

ZDC0676A

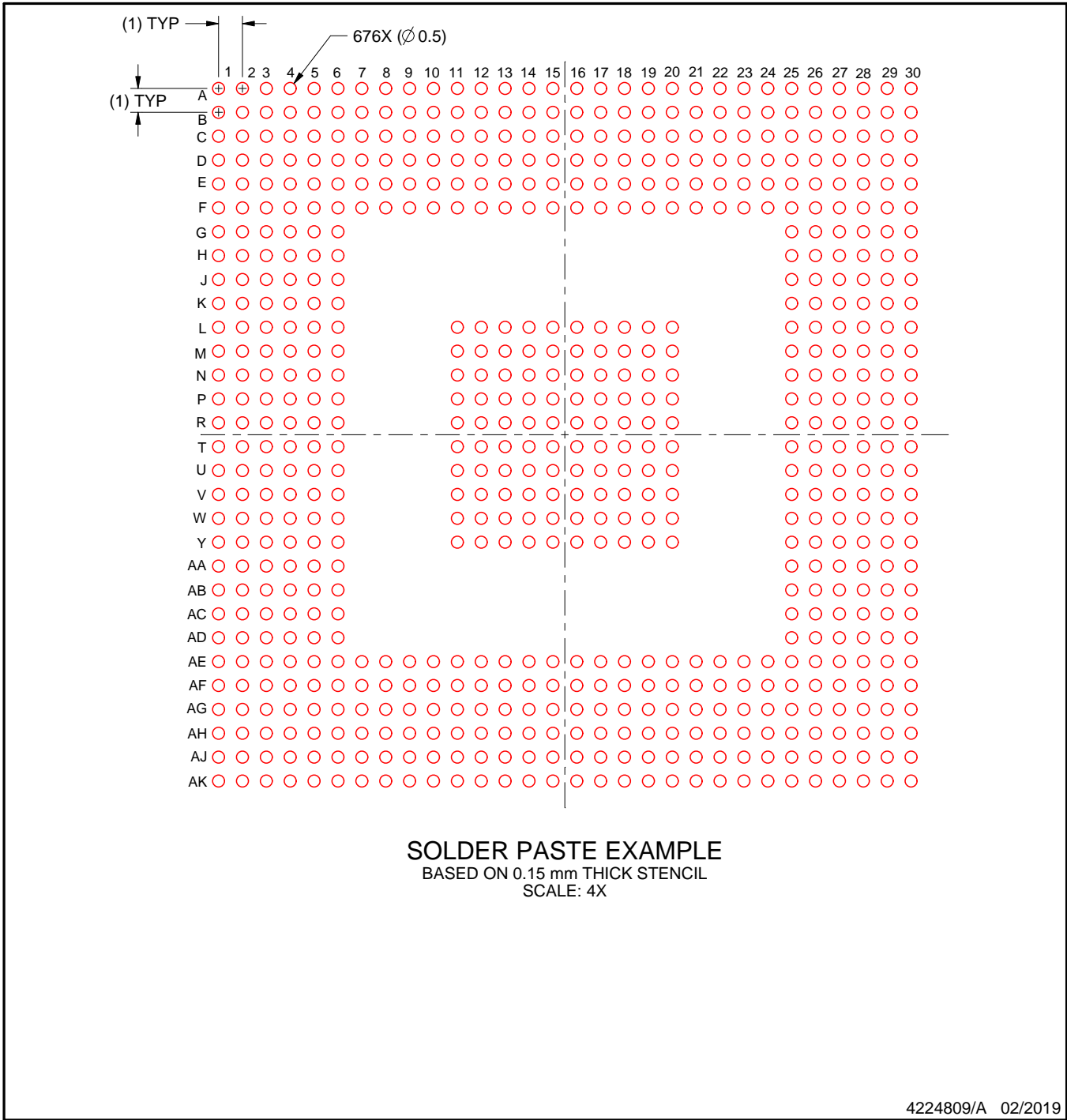
PBGA - 2.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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