DRV8329-Q1 4.5 to 60V Three-phase BLDC Gate Driver

1 Features

- 65V Three Phase Half-Bridge Gate Driver
  - Drives 3 High-Side and 3 Low-Side N-Channel MOSFETs (NMOS)
  - 4.5 to 60V Operating Voltage Range
  - Supports 100% PWM Duty Cycle with Trickle Charge pump
- Bootstrap based Gate Driver Architecture
  - 1000mA Maximum Peak Source Current
  - 2000mA Maximum Peak Sink Current
- Integrated Current Sense Amplifier with low input offset (optimized for 1 shunt)
  - Adjustable Gain (5, 10, 20, 40V/V)
- Hardware interface provides simple configuration
- Ultra-low power sleep mode <1uA at 25℃
- 4ns (typ) propagation delay matching between phases
- Independent driver shutdown path (DRVOFF)
- 65V tolerant wake pin (nSLEEP)
- Supports negative transients upto -10V on SHx
- 6x and 3x PWM Modes
- Supports 3.3V, and 5V Logic Inputs
- Accurate LDO (AVDD), 3.3V ±3%, 80mA
- Compact QFN Packages and Footprints
- Adjustable VDS overcurrent threshold through VDSLVL pin
- Adjustable deadtime through DT pin
- Efficient System Design With Power Blocks
- Integrated Protection Features
  - PVDD Undervoltage Lockout (PVDDUV)
  - GVDD Undervoltage (GVDDUV)
  - Bootstrap Undervoltage (BST_UV)
  - Overcurrent Protection (VDS_OCP, SEN_OCP)
  - Thermal Shutdown (OTSD)
  - Fault Condition Indicator (nFAULT)

2 Applications

- Brushless-DC (BLDC) Motor Modules and PMSM
- Automotive Pumps
- Automotive HVAC fans
- E-Bikes, E-Scooters, and E-Mobility
- Automotive Body Electronics (Window, Door, Sunroof, Seat, Wiper) Modules

3 Description

The DRV8329-Q1 family of devices is an integrated gate driver for three-phase applications. The devices provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The device generates the correct gate drive voltages using an internal charge pump and enhances the high-side MOSFETs using a bootstrap circuit. A trickle charge pump is included to support 100% duty cycle. The Gate Drive architecture supports peak gate drive currents up to 1A source and 2A sink. The DRV8329-Q1 can operate from a single power supply and supports a wide input supply range of 4.5 to 60V.

The 6x and 3x PWM modes allow for simple interfacing to controller circuits. The device has integrated accurate 3.3V LDO that can be used to power external controller and can be used as reference for CSA. The configuration settings for the device are configurable through hardware (H/W) pins.

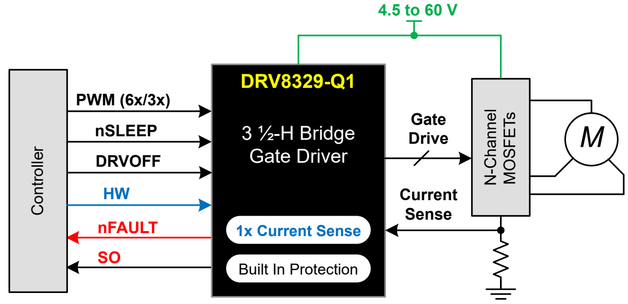
The DRV8329-Q1 devices integrate low-side current sense amplifier that allow current sensing for sum of current from all three phases of the drive stage.

A low-power sleep mode is provided to achieve low quiescent current by shutting down most of the internal circuitry. Internal protection functions are provided for undervoltage lockout, GVDD fault, MOSFET overcurrent, MOSFET short circuit, and overtemperature. Fault conditions are indicated on nFAULT pin.

Device Information (1)

PART NUMBER	PACKAGE	PACKAGE SIZE (NOM)
DRV8329ARGF-Q1	WQFN (40)	7.00mm × 5.00mm
DRV8329BRGF-Q1	WQFN (40)	7.00mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV8329-Q1 Simplified Schematic

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4 Device Comparison Table

Table 4-1. Different Device Variants

DEVICE	DEVICE VARIANT	Package	LDO output	DT pin and VDSLVL	PWM_MODE
DRV8329-Q1	DRV8329A-Q1	40-pin QFN (7.00mm x 5.00mm)	3.3V	Available	6x
	DRV8329B-Q1				3x

5 Pin Configuration and Functions

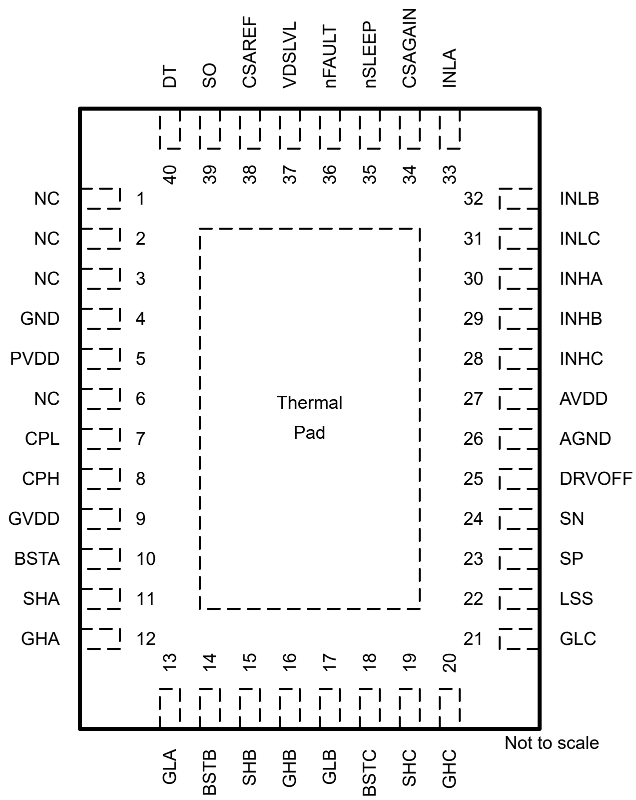

Figure 5-1. DRV8329 RGF Package 40-pin VQFN With Exposed Thermal Pad Top View

Table 5-1. Pin Functions—40-Pin DRV8329-Q1 Devices

NAME	PIN NO.	TYPE[(1)]	DESCRIPTION
	DRV8329		
NC	1	—	No connection.
NC	2	—	No connection.
NC	3	—	No connection.
GND	4	PWR	Device ground. Refer Section 8.4.1 for the recommendation on connection.
PVDD	5	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1µF, >2x PVDD-rated ceramic and >10uF local capacitance between the PVDD and GND pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
NC	6	—	No connection.
CPL	7	PWR	Charge pump switching node. Connect a X5R or X7R, PVDD-rated ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
CPH	8	PWR	
GVDD	9	PWR-O	Gate driver power supply output. Connect a X5R or X7R, 30V rated ceramic ≥ 10-uF local capacitance between the GVDD and GND pins. TI recommends a capacitor value of >10x C_{BSTx} and voltage rating at least twice the normal operating voltage of the pin.
BSTA	10	O	Bootstrap output pin. Connect a X5R or X7R, 1µF, 25V ceramic capacitor between BSTA and SHA
SHA	11	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
GHA	12	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.

Table 5-1. Pin Functions—40-Pin DRV8329-Q1 Devices (continued)

NAME	PIN NO. DRV8329	TYPE(1)	DESCRIPTION
GLA	13	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
BSTB	14	O	Bootstrap output pin. Connect a X5R or X7R, 1µF, 25V ceramic capacitor between BSTB and SHB
SHB	15	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLB	17	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
BSTC	18	O	Bootstrap output pin. Connect a X5R or X7R, 1µF, 25V ceramic capacitor between BSTC and SHC
SHC	19	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
GHC	20	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLC	21	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
LSS	22	PWR	Low side source pin, connect all sources of the external low-side MOSFETs here. This pin is the sink path for the low-side gate driver, and serves as an input to monitor the low-side MOSFET VDS voltage and VSEN_OCP voltage.
SP	23	I	Current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SN	24	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
DRVOFF	25	I	Independent driver shutdown path. Pulling DRVOFF high turns off all external MOSFETs by putting the gate drivers into the pull-down state. This signal bypasses and overrides the digital core of DRV8329.
AGND	26	PWR	Device analog ground. Refer Section 8.4.1 for the recommendation on connection.
AVDD	27	PWR-O	3.3V regulator output. Connect a X5R or X7R, 1µF, >6.3V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 80mA externally. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
INHC	28	I	High-side gate driver control input for Phase C. This pin controls the output of the high-side FET (DRV8329A) or controls the output of the half-bridge (DRV8329B).
INHB	29	I	High-side gate driver control input for Phase B. This pin controls the output of the high-side FET (DRV8329A) or controls the output of the half-bridge (DRV8329B).
INHA	30	I	High-side gate driver control input for Phase A. This pin controls the output of the high-side FET (DRV8329A) or controls the output of the half-bridge (DRV8329B).
INLC	31	I	Low-side gate driver control input for Phase C. This pin controls the output of the low-side FET (DRV8329A) or controls high-Z mode for the half bridge (DRV8329B).
INLB	32	I	Low-side gate driver control input for Phase B. This pin controls the output of the low-side FET (DRV8329A) or controls high-Z mode for the half bridge (DRV8329B).
INLA	33	I	Low-side gate driver control input for Phase A. This pin controls the output of the low-side FET (DRV8329A) or controls high-Z mode for the half bridge (DRV8329B).
CSAGAIN	34	I	Gain settings for Current sense amplifier. The pin is a 4 level input pin set by an external resistor. See Section 7.3.4 for more information.
nSLEEP	35	I	Sleep mode entry pin. When this pin is pulled logic low the device goes to a low-power sleep mode. An 1 to 1.2µs low pulse can be used to reset fault conditions without entering sleep mode.
nFAULT	36	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor to 3.3V to 5.0V.
VDSLVL	37	I	VDS monitor trip point setting. Connect an analog level input from 0.1V to 2.5V to set a VDS monitor trip point setting for MOSFET overcurrent protection. See Section 8.2.1.1.7 for more information.
CSAREF	38	I	Current sense amplifier reference. Connect a X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the CSAREF and AGND pins.
SO	39	O	Current sense amplifier output. Supports capacitive load or low pass filter (resistor in series and capacitor to AGND)
DT	40	I	Gate drive deadtime setting. Connect a resistor of value between 10kΩ to 390kΩ between DT and AGND to adjust deadtime between 100ns to 2000ns. If pin is left floating or connected to AGND fixed value of 55ns deadtime is inserted.

Table 5-1. Pin Functions—40-Pin DRV8329-Q1 Devices (continued)

NAME	PIN NO.	TYPE[(1)]	DESCRIPTION
	DRV8329		
Thermal Pad		PWR	Must be connected to GND

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

6 Specification

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	-0.3	65	V
Bootstrap pin voltage	BSTx	-0.3	80	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	20	V
Bootstrap pin voltage	BSTx with respect to GHx	-0.3	20	V
Charge pump pin voltage	CPL, CPH	-0.3	V_{GVDD}	V
Gate driver regulator pin voltage	GVDD	-0.3	20	V
Analog regulator pin voltage	AVDD	-0.3	4	V
Logic pin voltage (nSLEEP)	nSLEEP	-0.3	65	V
Logic pin voltage	DRVOFF, DT, INHx, INLx, nFAULT, VDSLVL	-0.3	6	V
High-side gate drive pin voltage	GHx	-8	80	V
Transient 500-ns high-side gate drive pin voltage	GHx	-10	80	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	20	V
High-side source pin voltage	SHx	-8	70	V
Transient 500-ns high-side source pin voltage	SHx	-10	72	V
Low-side gate drive pin voltage	GLx with respect to LSS	-0.3	20	V
Transient 500-ns low-side gate drive pin voltage(2)	GLx with respect to LSS	-1	20	V
Low-side gate drive pin voltage	GLx with respect to GVDD		0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx with respect to GVDD		1	V
Low-side source sense pin voltage	LSS	-1	1	V
Transient 500-ns low-side source sense pin voltage	LSS	-10	8	V
Gate drive current	GHx, GLx	Internally Limited	Internally Limited	A
Current sense amplifer reference input pin voltage	CSAREF	-0.3	5.5	V
Shunt amplifier input pin voltage	SN, SP	-1	1	V
Transient 500-ns shunt amplifier input pin voltage	SN, SP	-10	8	V
Shunt amplifier output pin voltage	SO	-0.3	V_{CSAREF} + 0.3	V
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) Supports upto 5A for 500 nS when GLx-LSS is negative

6.2 ESD Ratings Auto

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Power supply voltage	PVDD	4.5		60	V
V_{PVDD_RAMP}	Power supply voltage ramp rate at power up	PVDD			30	V/us
V_{PVDD_RAMP}	Power supply voltage ramp rate during operation	PVDD			4	V/us
V_{BST}	Bootstrap pin voltage with respect to SHx	nSLEEP = High, INHx is switching	4		20	V
I_{AVDD} (1)	Regulator external load current	AVDD			80	mA
$I_{TRICKLE}$	Trickle charge pump external load current	BSTx			2	µA
V_{IN}	Logic input voltage	DRVOFF, INHx, INLx, nSLEEP	0		5.5	V
V_{IN}	Logic input voltage	DT, VDSLVL	0		3.4	V
f_{PWM}	PWM frequency	INHx, INLx	0		200	kHz
V_{OD}	Open drain pullup voltage	nFAULT			5.5	V
I_{OD}	Open drain output current	nFAULT			-10	mA
I_{GS} (1)	Total average gate-drive current (Low Side and High Side Combined)	I_{GHx}, I_{GLx}			30	mA
V_{CSAREF}	Current sense amplifier reference voltage	CSAREF	2.8		5.5	V
V_{SHSL}	Slew Rate on SHx pins				4	V/ns
C_{BSTx}	Capacitor between BSTx and SHx				4.7 (2)	µF
C_{GVDD}	Capacitor between GVDD and GND				130	µF
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed
(2) Current flowing through boot diode (DBOOT) needs to be limited for C_{BSTx} > 4.7µF.

6.4 Thermal Information 2pkg

THERMAL METRIC(1)		DEVICE	UNIT
		RGF (VQFN)	
		40	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (AVDD, PVDD, GVDD)						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} =24V, nSLEEP = 0, T_A = 25°C			1	µA
		nSLEEP = LOW			2	µA
I_{PVDDS}	PVDD standby mode current	V_{PVDD} = 24 V; nSLEEP = HIGH, INHx = INLX = LOW, DRVOFF = HIGH		2	4	mA
		nSLEEP = HIGH, INHx = INLX = LOW, DRVOFF = HIGH		3	5.5	mA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 24 V, nSLEEP = HIGH, INHx = INLX = Switching@20kHz, No FETs connected		4	7	mA
		nSLEEP = HIGH, INHx = INLX = Switching@20kHz, No FETs connected		5	10	mA
		V_{PVDD} = 8 V, nSLEEP = HIGH, INHx = INLX = LOW, No FETs connected		5	10	mA
		V_{PVDD} = 24 V, nSLEEP = HIGH, INHx = INLX = LOW, No FETs connected		5	7	mA
IL_{BSx}	Bootstrap pin leakage current	V_{BSTx} = V_{SHx} = 60V, V_{GVDD} = 0V, nSLEEP = LOW	5	10	16	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	INLx = INHx = Switching@20kHz, No FETs connected	60	115	300	µA
$IL_{BS\_DC\_SRC}$	Bootstrap pin active mode leakage static source current	INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V_{PVDD} = V_{SHX} = V_{GVDD} = 12V, V_{BSTx} - V_{SHx} = 5V	135	200	280	µA
		INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V_{PVDD} = V_{SHX} = V_{GVDD} = 12V, V_{BSTx} - V_{SHx} = 7V	70	105	145	µA
		INHx = LOW, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V_{PVDD} = V_{SHX} = V_{GVDD} = 12V, V_{BSTx} - V_{SHx} = 5V	25	50	90	µA
		INHx = LOW, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V_{PVDD} = V_{SHX} = V_{GVDD} = 12V, V_{BSTx} - V_{SHx} = 7V	16	28	50	µA
$IL_{BS\_DC\_SINK}$	Bootstrap pin active mode leakage static sink current	INHx = LOW, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V_{PVDD} = V_{SHX} = V_{GVDD} = 12V, V_{BSTx} - V_{SHx} = 12V	10	40	90	µA
		INHx = High, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V_{PVDD} = V_{SHX} = V_{GVDD} = 12V, V_{BSTx} - V_{SHx} = 12V	14	45	91	µA
IL_{SHx}	Source pin leakage current	INHx = INLx = LOW, V_{BSTx} - V_{SHx} = 15, V_{SHx} = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW	80	145	210	µA
		INHx = INLx = LOW, V_{BSTx} - V_{SHx} = 11, V_{SHx} = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW	15	20	30	µA
		INHx = High, INLx = LOW, V_{BSTx} - V_{SHx} = 15, V_{SHx} = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW	80	145	210	µA
		INHx = HIGH, INLx = LOW, V_{BSTx} - V_{SHx} = 11, V_{SHx} = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW	13	25	35	µA

$4.5\ V \le V_{PVDD} \le 60\ V$, $–40°C \le T_J \le 150°C$ (unless otherwise noted). Typical limits apply for $T_A = 25°C$, $V_{PVDD} = 24\ V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WAKE}	Turnon time (nSLEEP)	nSLEEP = HIGH to Active mode (Outputs Ready), DRVOFF = LOW, C_{GVDD} = 10 uF, C_{BSTx} = 1 uF		1	2	ms
		nSLEEP = High to Active mode (Outputs Ready). C_{GVDD} = 100 uF, C_{AVDD} = 10 uF, C_{BSTx} = 10 uF		10	15	ms
		V_{PVDD} = 12V, nSLEEP = HIGH to Active mode (Outputs Ready), DRVOFF = LOW, C_{GVDD} = 10 uF		1	2	ms
	Turnon time (DRVOFF)	DRVOFF = LOW to Active mode (Outputs Ready), nSLEEP = High		0.05	0.1	ms
t_{SLEEP}	Turnoff time	nSLEEP = LOW to Sleep mode			20	us
t_{RST}	Minimum Reset Pulse Time	nSLEEP = LOW period to reset faults	1		1.2	us
V_{GVDD_RT}	GVDD Gate driver regulator voltage (Room Temperature)	$V_{PVDD} \ge 40$ V, I_{GS} = 10 mA, T_J= 25°C	11.8	13	15	V
		22 V $\le V_{PVDD} \le$ 40 V, I_{GS} = 30 mA, T_J= 25°C	11.8	13	15	V
		8 V $\le V_{PVDD} \le$ 22 V, I_{GS} = 30 mA, T_J= 25°C	11.8	13	15	V
		6.75 V $\le V_{PVDD} \le$ 8 V, I_{GS} = 10 mA, T_J= 25°C	11.8	13	14.5	V
		4.5 V $\le V_{PVDD} \le$ 6.75 V, I_{GS} = 10 mA, T_J= 25°C	2*V_{PVDD} - 1		13.5	V
V_{GVDD}	GVDD Gate driver regulator voltage	$V_{PVDD} \ge 40$ V, I_{GS} = 10 mA	11.5		15.5	V
		22 V $\le V_{PVDD} \le$ 40 V, I_{GS} = 30 mA	11.5		15.5	V
		8 V $\le V_{PVDD} \le$ 22 V; I_{GS} = 30 mA	11.5		15.5	V
		6.75 V $\le V_{PVDD} \le$ 8 V, I_{GS} = 10 mA	11.5		14.5	V
		4.5 V $\le V_{PVDD} \le$ 6.75 V, I_{GS} = 10 mA	2*V_{PVDD} - 1.4		13.5	V
V_{AVDD_RT}	AVDD Analog regulator voltage (Room Temperature)	$V_{PVDD} \ge 6$ V, 0 mA $\le I_{AVDD} \le$ 30 mA, T_J= 25°C	3.26	3.3	3.33	V
		$V_{PVDD} \ge 6$ V, 30 mA $\le I_{AVDD} \le$ 80 mA, T_J= 25°C	3.2	3.3	3.4	V
		$V_{PVDD} \le 6$ V, 0 mA $\le I_{AVDD} \le$ 50 mA, T_J= 25°C	3.13	3.3	3.46	V
V_{AVDD}	AVDD Analog regulator voltage	$V_{PVDD} \ge 6$ V, 0 mA $\le I_{AVDD} \le$ 80 mA	3.2	3.3	3.4	V
		$V_{PVDD} \le 6$ V, 0 mA $\le I_{AVDD} \le$ 50 mA	3.125	3.3	3.5	V
LOGIC-LEVEL INPUTS (DRVOFF, INHx, INLx, nSLEEP etc)						
V_{IL}	Input logic low voltage	DRVOFF			0.8	V
		INLx, INHx pins			0.8	V
V_{IH}	Input logic high voltage	DRVOFF	2.2			V
		INLx, INHx pins	2.2			V
V_{HYS}	Input hysteresis	DRVOFF	200	400	650	mV
		INLx, INHx pins	45	240	350	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V;	-1	0	1	µA
I_{IH}	Input logic high current	nSLEEP, V_{PIN} (Pin Voltage) = 65 V;	3	6.5	10	µA
		nSLEEP, V_{PIN} (Pin Voltage) = 5 V;	3	6	10	µA
		Other pins, V_{PIN} (Pin Voltage) = 5 V;	7	20	35	µA
R_{PD_DRVOFF}	Input pulldown resistance	DRVOFF To GND	100	200	300	kΩ
R_{PD_nSLEEP}	Input pulldown resistance	nSLEEP To GND	500	800	1500	kΩ
R_{PD}	Input pulldown resistance	All other pins To GND	150	250	350	kΩ

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOUR-LEVEL INPUTS (GAIN)						
V_{L1}	Input level 1 voltage	Tied to GND	0		0.18*AVDD	V
V_{L2}	Input level 2 voltage	50 kΩ +/- 5% tied to GND	0.48*AVDD	0.5*AVDD	0.52*AVDD	V
V_{L3}	Input level 3 voltage	200 kΩ +/- 5% tied to GND	0.82*AVDD	0.833*AVDD	0.85*AVDD	V
V_{L4}	Input level 4 voltage	HiZ or Connect to AVDD		AVDD		V
R_{PU}	Input pullup resistance	GAIN To AVDD	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (nFAULT etc)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 5 V	-1		1	µA
C_{OD}	Output capacitance	V_{OD} = 5 V			30	pF
GATE DRIVERS (GHx, GLx, SHx, SLx)						
V_{GSHx_LO}	High-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0.05	0.11	0.24	V
V_{GSHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.28	0.44	0.82	V
V_{GSLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0.05	0.11	0.27	V
V_{GSLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.28	0.44	0.82	V
$V_{GSH\_100\_PH}$	High-side gate drive voltage in steady state with 100 % duty cycle (GHx- SHx)	INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, V_{PVDD} >15V, V_{GVDD} ≥11.5V	8.4	9.6	11.1	V
		INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, V_{GVDD} ≥11.5V	7.5	8.3	9	V
		INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, 7V ≥V_{GVDD} ≥ 8V	5.7	6.5	7.6	V
$R_{DS(ON)\_PU\_HS}$	High-side pullup switch resistance	I_{GHx} = 100 mA; V_{GVDD}= 12V	2.7	4.5	8.4	Ω
$R_{DS(ON)\_PD\_HS}$	High-side pulldown switch resistance	I_{GHx} = 100 mA; V_{GVDD} = 12V	0.2	1.1	2.4	Ω
$R_{DS(ON)\_PU\_LS}$	Low-side pullup switch resistance	I_{GLx} = 100 mA; V_{GVDD} = 12V	2.7	4.5	8.3	Ω
$R_{DS(ON)\_PD\_LS}$	Low-side pulldown switch resistance	I_{GLx} = 100 mA; V_{GVDD} = 12V	0.2	1.1	2.8	Ω
I_{DRIVEP_HS}	High-side peak source gate current	V_{GSHx} = 12V	550	1000	1575	mA
I_{DRIVEN_HS}	High-side peak sink gate current	V_{GSHx} = 0V	1150	2000	2675	mA
I_{DRIVEP_LS}	Low-side peak source gate current	V_{GSLx} = 12V	550	1000	1575	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	V_{GSLx} = 0V	1150	2000	2675	mA
R_{PD_LS}	Low-side passive pull down	GLx to LSS	80	100	120	kΩ
R_{PDSA_HS}	High-side semiactive pull down	GHx to SHx, V_{GSHx} = 2V	8	10	12.5	kΩ
GATE DRIVERS TIMINGS						
t_{PDR_LS}	Low-side rising propagation delay	INLx to GLx rising, V_{GVDD} > 8V	70	100	145	ns
t_{PDF_LS}	Low-side falling propagation delay	INLx to GLx falling, V_{GVDD} > 8V	70	100	135	ns
t_{PDR_HS}	High-side rising propagation delay	INHx to GHx rising, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V	65	100	145	ns
t_{PDF_HS}	High-side falling propagation delay	INHx to GHx falling, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V	70	100	140	ns

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD\_MATCH\_PH}$	Matching propagation delay per phase	GLx turning ON to GLx turning OFF, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-25	±4	25	ns
		GLx turning OFF to GHx turning ON, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-28	±4	28	ns
		GHx turning ON to GHx turning OFF, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-25	±4	25	ns
		GHx turning OFF to GLx turning ON, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-25	±4	25	ns
$t_{PD\_MATCH\_PH\_PH}$	Matching propagation delay phase to phase	GHx turning ON to GHy turning ON, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-10	±4	10	ns
		GLx turning ON to GLy turning ON, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-10	±4	10	ns
		GHx turning OFF to GHy turning OFF, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-15	±4	15	ns
		GLx turning OFF to GLy turning OFF, V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V to 60V, No load on GHx and GLx	-10	±4	10	ns
t_{PW_MIN}	Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx		18	32	45	ns
t_{DEAD}	Gate drive dead time configurable range		50		2000	ns
t_{DEAD}	Gate drive dead time	DT pin floating	35	55	90	ns
		DT pin connected to GND	25	55	80	ns
		10 kΩ between DT pin and GND	75	100	140	ns
		390 kΩ between DT pin and GND	1350	2000	2650	ns
BOOTSTRAP DIODES						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA			0.8	V
		I_{BOOT} = 100 mA			1.6	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 50 mA	4.5	5.5	9	Ω
CURRENT SHUNT AMPLIFIERS (SNx, SOx, SPx, CSAREF)						
A_{CSA}	Sense amplifier gain	CSAGAIN = Tied to GND	4.92	5	5.05	V/V
		CSAGAIN = 50kΩ ±5% tied to GND	9.9	10	10.1	V/V
		CSAGAIN = 200kΩ ±5% tied to GND	19.75	20	20.2	V/V
		CSAGAIN =Hi-Z;	39.6	40	40.6	V/V
A_{CSA_ERR}	Sense amplifier gain error	T_J = 25℃	-1.5		1.5	%
$A_{CSA\_ERR\_DRIFT}$	Sense amplifier gain error temperature drift		-20		20	ppm/℃
NL	Non linearity Error			0.01	0.05	%

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{LOAD} = 500pF		0.6	1	µs
		V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{LOAD} = 500pF		0.6	1.1	µs
		V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, C_{LOAD} = 500pF		0.7	1.2	µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{LOAD} = 500pF		0.8	1.7	µs
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{LOAD} = 60pF		0.3	0.5	µs
		V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{LOAD} = 60pF		0.3	0.5	µs
		V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, C_{LOAD} = 60pF		0.3	0.65	µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{LOAD} = 60pF		0.3	0.8	µs
BW	Bandwidth	A_{CSA} = 5 V/V, C_{LOAD} = 60-pF, small signal -3 dB	3	5	7	MHz
		A_{CSA} = 10 V/V, C_{LOAD} = 60-pF, small signal -3 dB	2.5	4.8	6.6	MHz
		A_{CSA} = 20 V/V, C_{LOAD} = 60-pF, small signal -3 dB	2	4	5.4	MHz
		A_{CSA} = 40 V/V, C_{LOAD} = 60-pF, small signal -3 dB	1.75	3	4.2	MHz
t_{SR}	Output slew rate	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{LOAD} = 60-pF, low to high transition		12		V/µs
		V_{STEP} = 1.6 V, A_{CSA} = 10 V/V, C_{LOAD} = 60-pF, low to high transition		13		V/µs
		V_{STEP} = 1.6 V, A_{CSA} = 20 V/V, C_{LOAD} = 60-pF, low to high transition		11		V/µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{LOAD} = 60-pF, low to high transition		11		V/µs
V_{SWING}	Output voltage range	V_{CSAREF} = 3	0.25		2.75	V
V_{SWING}	Output voltage range	V_{CSAREF} = 5.5	0.25		5.25	V
V_{SWING}	Output voltage range	V_{CSAREF} = 3 to 5.5 V	0.25		V_{CSAREF} - 0.25	V
V_{COM}	Common-mode input range		-0.15		0.15	V
V_{DIFF}	Differential-mode input range		-0.3		0.3	V
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = -40℃, CSA_VREF = 0	-2.0		2.0	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = 25℃, CSA_VREF = 0	-1.9		1.9	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = 175℃, CSA_VREF= 0	-2.0		2.0	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND	-2.0		2.0	mV
V_{OFF_DRIFT}	Input drift offset voltage	V_{SP} = V_{SN} = GND		8		µV/℃
V_{BIAS}	Output voltage bias ratio	V_{SP} = V_{SN} = GND	0.122	0.125	0.128	V
V_{BIAS_ACC}	Output voltage bias ratio accuracy	V_{SP} = V_{SN} = GND	-1.2		1.2	%
I_{BIAS}	Input bias current	V_{SP} = V_{SN} = GND, V_{CSAREF} = 3V to 5.5V			100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SP} – I_{SN}	-1		1	µA
I_{CSASRC}	SO ouput sink current capability		5	7	11	mA

$4.5\ V \le V_{PVDD} \le 60\ V$, $-40°C \le T_J \le 150°C$ (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CSASRC}	SO ouput source current capability		2	3.7	6.6	mA
CMRR	Common-mode rejection ratio	DC		80		dB
		20 kHz		65		dB
PSRR	Power-supply rejection ratio (CSAREF)	CSAREF to SOx, DC, Differential		80		dB
		CSAREF to SOx, 20 kHz, Differential		70		dB
PSRR	Power-supply rejection ratio (CSAREF)	CSAREF to SOx, 20 kHz, Single Ended		40		dB
I_{CSA_SUP}	Supply current for CSA	V_{CSAREF} = 3.V to 5.5V		1.5	2.1	mA
T_{CMREC}	Common mode recovery time			0.6	0.7	us
C_{LOAD}	Maximum load capacitance			10		nF
V_{OFF_OUT}	Output offset error	A_{CSA} = 5 V/V	-3		3	mV
		A_{CSA} = 10 V/V	-4		4	mV
		A_{CSA} = 20 V/V	-5		5	mV
		A_{CSA} = 40 V/V	-6		6	mV
PROTECTION CIRCUITS						
V_{PVDD_UV}	PVDD undervoltage lockout threshold	V_{PVDD} rising	4.3	4.4	4.5	V
		V_{PVDD} falling	4	4.1	4.25	
$V_{PVDD\_UV\_HYS}$	PVDD undervoltagelockout hysteresis	Rising to falling threshold	225	265	325	mV
$t_{PVDD\_UV\_DG}$	PVDD undervoltage deglitch time		10	20	30	µs
V_{AVDD_POR}	AVDD supply POR threshold	AVDD rising	2.7	2.85	3.0	V
		AVDD falling	2.5	2.65	2.8	
$V_{AVDD\_POR\_HYS}$	AVDD POR hysteresis	Rising to falling threshold	170	200	250	mV
$t_{AVDD\_POR\_DG}$	AVDD POR deglitch time		7	12	22	µs
V_{GVDD_UV}	GVDD undervoltage threshold	V_{GVDD} rising	7.3	7.5	7.8	V
		V_{GVDD} falling	6.4	6.7	6.9	V
$V_{GVDD\_UV\_HYS}$	GVDD undervoltage hysteresis	Rising to falling threshold	800	900	1000	mV
$t_{GVDD\_UV\_DG}$	GVDD undervoltage deglitch time		5	10	15	µs
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} rising	3.9	4.45	5	V
		V_{BSTx}- V_{SHx}; V_{BSTx} falling	3.7	4.2	4.8	V
$V_{BST\_UV\_HYS}$	Bootstrap undervoltage hysteresis	Rising to falling threshold	150	220	285	mV
$t_{BST\_UV\_DG}$	Bootstrap undervoltage deglitch time		2	4	6	µs
$V_{DS\_LVL\_RNG}$	V_{DS} overcurrent protection threshold linear range		0.1		2.5	V
V_{DS_DIS}	V_{DS} overcurrent protection disable resistor	VDSLVL pin to GVDD	70	100	500	kΩ
V_{DS_LVL}	V_{DS} overcurrent protection threshold Reference	VDSLVL = 100 kΩ to GVDD	3	4.2	5.5	V
		VDSLVL = 0.1V	0.065	0.1	0.145	V
		VDSLVL pin = 2.5V	2.2	2.5	2.8	
V_{SENSE_LVL}	V_{SENSE} overcurrent protection threshold	LSS to GND pin = 0.5V	0.48	0.5	0.52	V
t_{DS_BLK}	V_{DS} overcurrent protection blanking time		0.5	1	2.7	µs
t_{DS_DG}	V_{DS} and V_{SENSE} overcurrent protection deglitch time		1.5	3	5	µs
$t_{SD\_SINK\_DIG}$	DRVOFF peak sink current duration		3	5	7	µs
t_{SD_DIG}	DRVOFF digital shutdown delay		0.5	1.5	2.2	µs

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SD}	DRVOFF analog shutdown delay		7	14	21	µs
T_{OTSD}	Thermal shutdown temperature	T_J rising;	160	170	187	°C
T_{HYS}	Thermal shutdown hysteresis		16	20	23	°C

6.6 Typical Characteristics

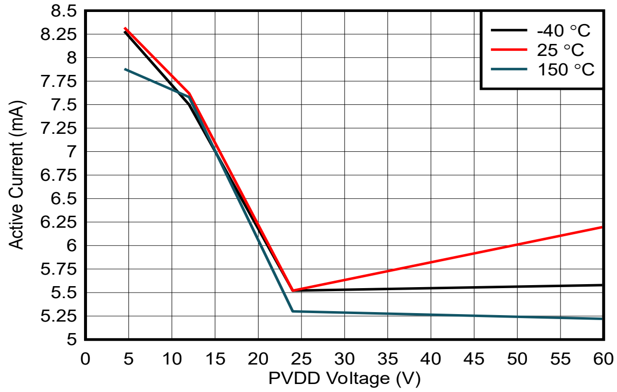

Figure 6-1. Supply Current over PVDD Voltage

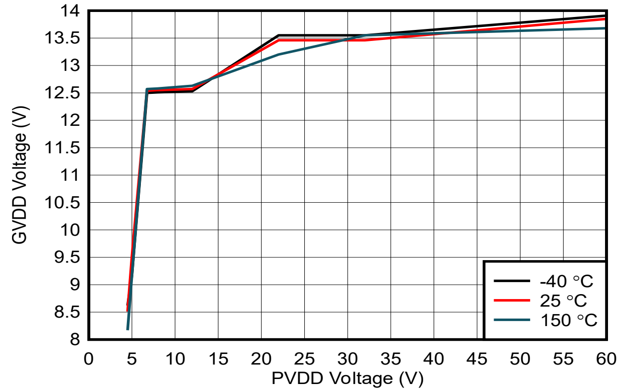

Figure 6-2. GVDD Voltage over PVDD Voltage

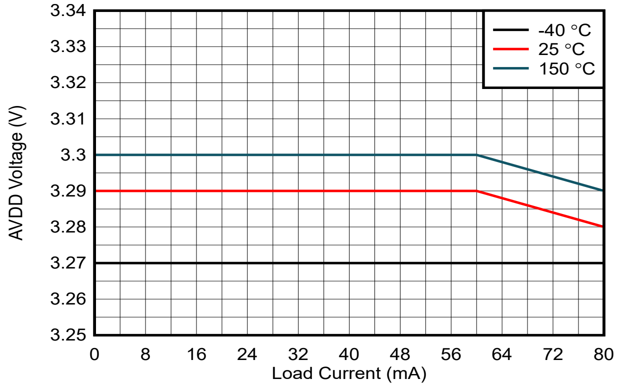

Figure 6-3. AVDD Voltage over Load Current

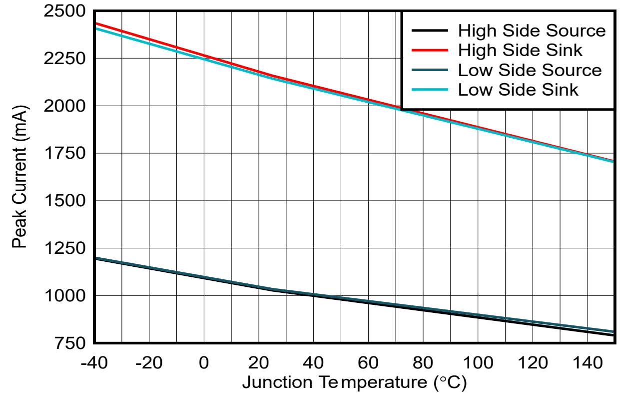

Figure 6-4. Driver Peak Current over Junction Temperature

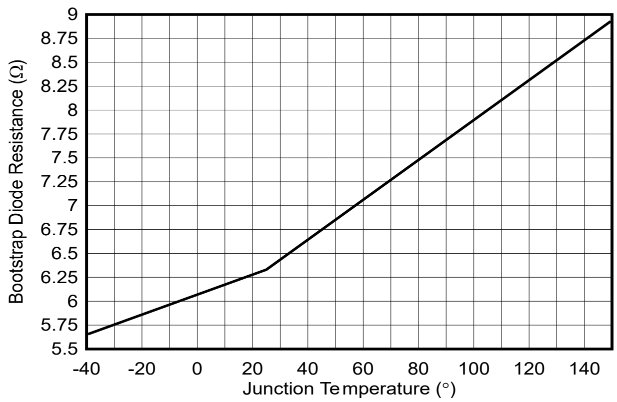

Figure 6-5. Bootstrap Diode Resistance over Junction Temperature

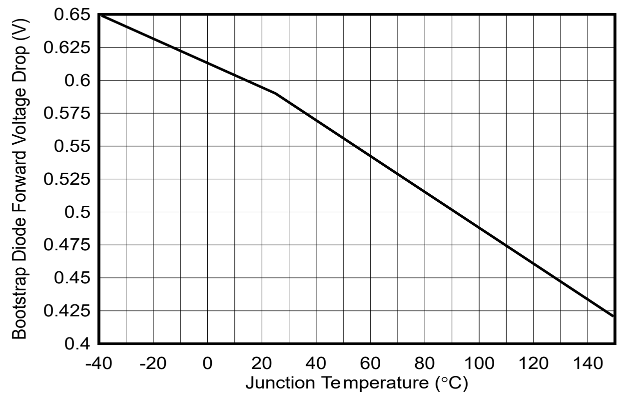

Figure 6-6. Bootstrap Diode Forward Voltage Drop over Junction Temperature

7 Detailed Description

7.1 Overview

The DRV8329-Q1 family of devices is an integrated three-phase gate driver supporting an input voltage range of 4.5V to 60V. These devices decrease system component count, cost, and complexity by integrating three independent half-bridge gate drivers, trickle charge pump, and a charge pump with linear regulator for the supply voltages of the high-side and low-side gate drivers. DRV8329-Q1 also integrates an accurate low voltage regulator (AVDD) capable of supporting 3.3V at 80mA output. A hardware interface allows for simple configuration of the motor driver and control of the motor.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1A source, 2A sink peak gate drive currents with a 30mA average output current. A bootstrap circuit with capacitor generates the supply voltage of the high-side gate drive and a trickle charge pump is employed to support 100% duty cycle. The supply voltage of the low-side gate driver is generated using a charge pump with linear regulator GVDD from the PVDD power supply that regulates to 12V.

In addition to the high level of device integration, the DRV8329-Q1 family of devices provides a wide range of integrated protection features. These features include power supply undervoltage lockout (PVDDUV), regulator undervoltage lockout (GVDDUV), Bootstrap Voltage undervoltage lockout (BSTUV), V_{DS} overcurrent monitoring (OCP), Sense resistor overcurrent monitoring (SEN_OCP) and overtemperature shutdown (TSD). Fault events are indicated by the nFAULT pin.

The DRV8329-Q1 is available in 0.5mm pitch, 5 × 7mm 40-pin QFN surface-mount packages.

7.2 Functional Block Diagram

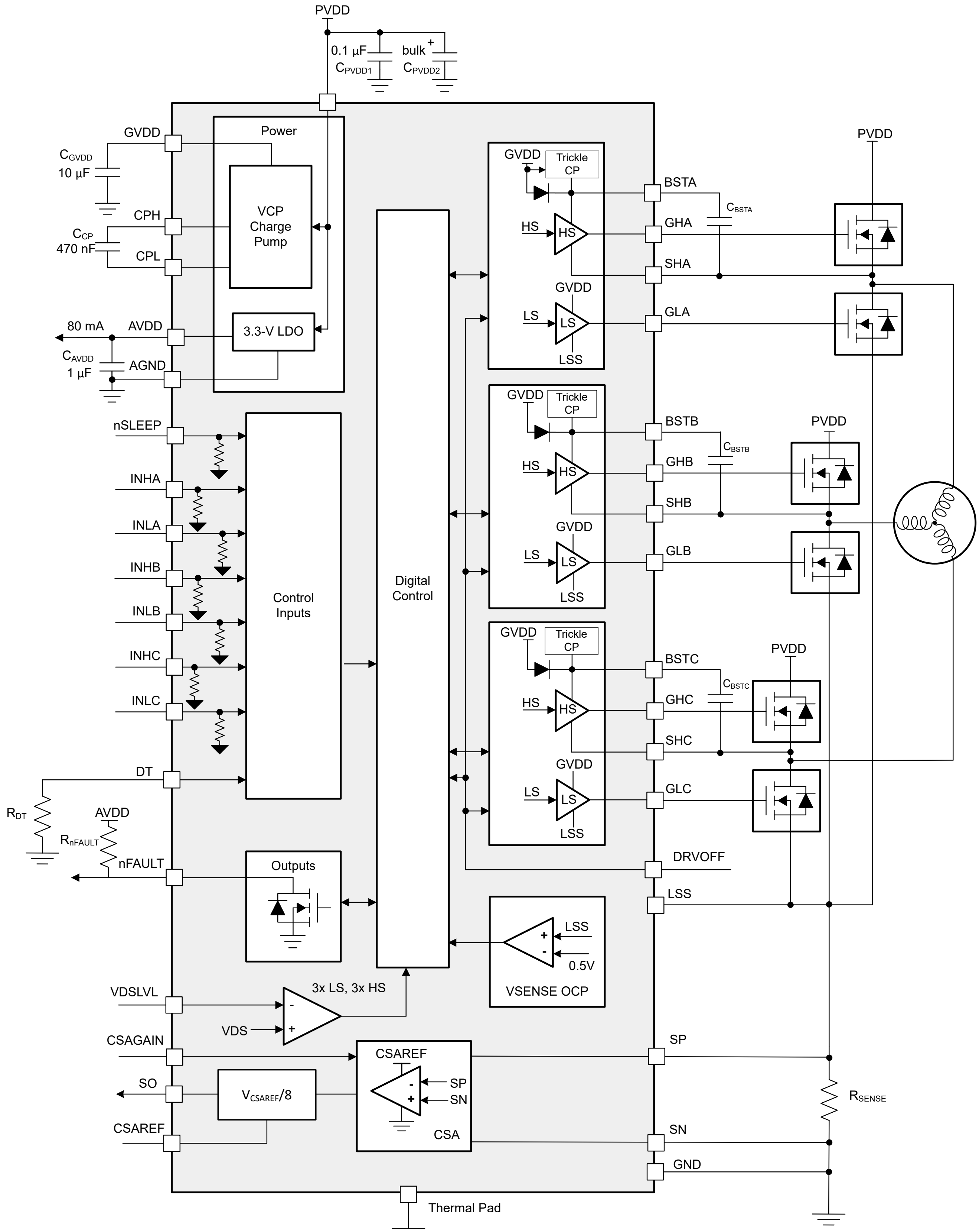

Figure 7-1. Block Diagram of DRV8329

7.3 Feature Description

Table 7-1 lists the recommended values of the external components for the gate driver and the buck regulator.

Table 7-1. DRV8329-Q1 External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	PGND	X5R or X7R, 0.1µF, >2x PVDD-rated capacitor
C_{PVDD2}	PVDD	PGND	≥ 10µF, >2x PVDD-rated capacitor
C_{CP}	CPH	CPL	X5R or X7R, 470nF, PVDD-rated capacitor
C_{GVDD}	GVDD	GND	X5R or X7R, ≥10-uF, 25V-rated capacitor
C_{AVDD}	AVDD	AGND	X5R or X7R, ≥1µF, 6.3V capacitor
C_{BSTx}	BSTx	SHx	X5R or X7R, 1µF (typical), 25V-rated capacitor
R_{nFAULT}	VCC(1)	nFAULT	Pullup resistor (10kΩ)
R_{DT}	DT	AGND	Hardware interface resistor. Refer to Deadtime and Cross-Conduction Prevention for the details.

(1) The VCC pin is not a pin on the DRV8329-Q1 , but a VCC supply voltage pullup is required for the open-drain output, nFAULT. This pin can also be pulled up to AVDD.

7.3.1 Three BLDC Gate Drivers

The DRV8329-Q1 family of devices integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A charge pump is used to generate the GVDD to supply the correct gate bias voltage across a wide operating voltage range. The low side gate outputs are driven directly from GVDD, while the high side gate outputs are driven using a bootstrap circuit with an integrated diode. An internal trickle charge pump provides support for 100% duty cycle operation. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

7.3.1.1 PWM Control Modes

7.3.1.1.1 6x PWM Mode

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in Table 7-2.

Table 7-2. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

7.3.1.1.2 3x PWM Mode

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 7-3.

Table 7-3. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

7.3.1.2 Device Hardware Interface

The DRV8329-Q1 utilize a hardware interface to configure different device settings. These hardware configurable inputs are DT and VDSLVL. General fault information is reported on the nFAULT pin.

- The DT pin configures the gate drive dead time. The dead time can adjusted by changing the resistor value from the DT pin to GND.
- The VDSLVL pin configures the voltage threshold of the V_{DS} overcurrent monitors. The voltage applied to the VDSLVL pin is directly used as reference for the VDS comparator

For more information on the hardware interface, see *Section 7.3.3*.

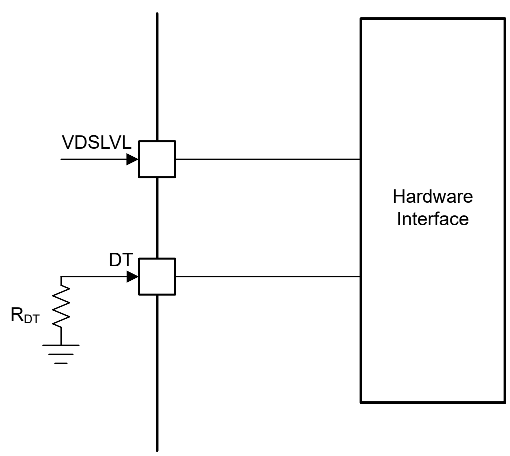

Figure 7-2. Hardware Interface

7.3.1.3 Gate Drive Architecture

The gate driver device use a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD regulator supply. The operating mode of GVDD depends on the voltage of PVDD, when the PVDD >18V, the GVDD voltage is generated by an LDO, whereas PVDD < 18V, the GVDD voltage is generated by a charge pump. For the high-side gate drivers a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used between BSTx and SHx pins. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent voltage drop due to the leakage currents of the driver and external MOSFET.

The high-side gate driver has a semi-active pulldown and low side gate has passive pulldown to help prevent the external MOSFET from turning ON during sleep state or when the power supply is disconnected.

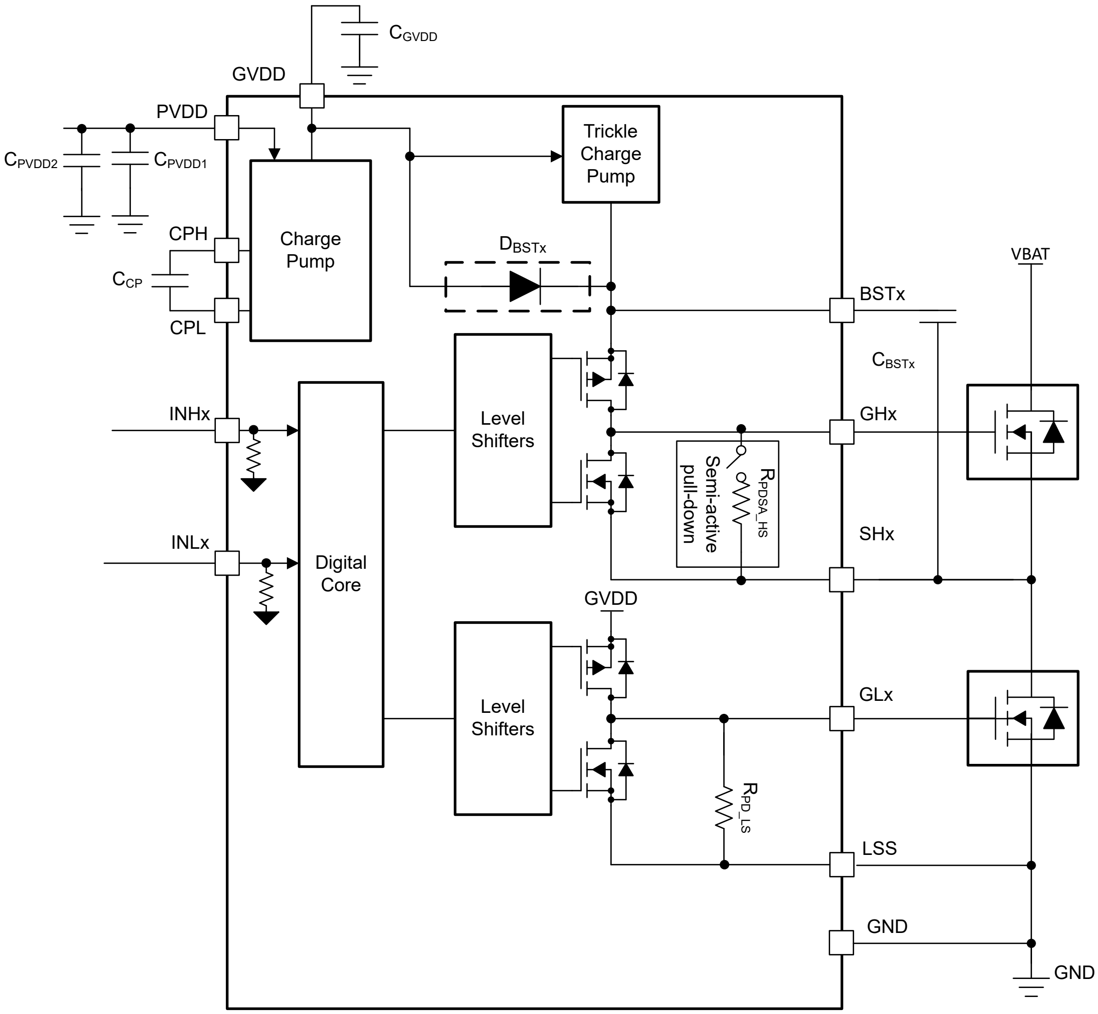

Figure 7-3. Gate Driver Block Diagram

7.3.1.3.1 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the digital propagation delay, and the delay through the analog gate drivers.

To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

7.3.1.3.2 Deadtime and Cross-Conduction Prevention

In the DRV8329-Q1, high- and low-side inputs operate independently, with an exception to prevent cross conduction when the high and low side of the same half-bridge are turned ON at same time. The device turns OFF high- and low- side output to prevent shoot through when high- and low-side inputs are logic high at same time.

The DRV8329-Q1 also provides dead time insertion to prevent both external MOSFETs of each half-bridge from switching on at the same time. In devices with a DT pin, deadtime can be linearly adjusted between 100 ns and 2000 ns by connecting s resistor between DT and ground. When the DT pin is left floating or connected to GND, a fixed deadtime of 55 ns (typical value) is inserted. The value of the resistor can be calculated using following equation.

$$R_{DT}\left(k\Omega\right) = \frac{Deadtime\ (ns)}{5} - 10\ k\Omega \quad (1)$$

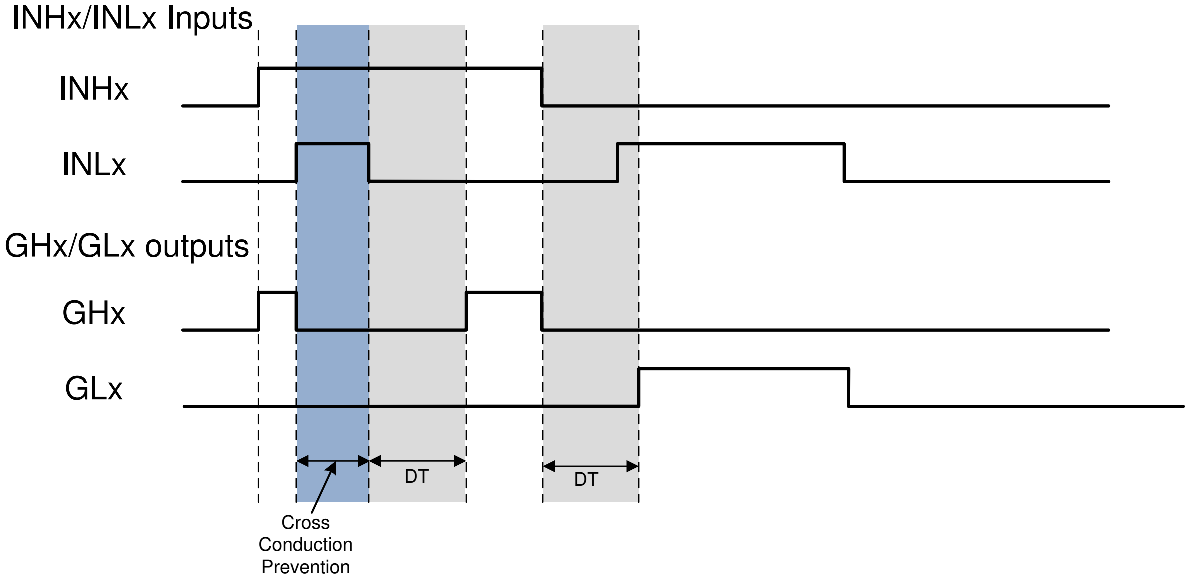

Figure 7-4. Cross Conduction Prevention and Deadtime Insertion

7.3.2 AVDD Linear Voltage Regulator

A 3.3V, 80mA linear regulator is available for use by external circuitry. The output of the LDO is fixed to 3.3V. This regulator can provide the supply voltage for a low-power MCU or other circuitry with low supply current needs. The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1µF, 6.3V ceramic capacitor routed back to the AGND pin.

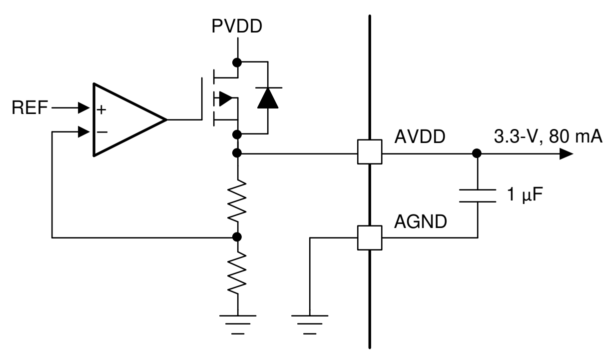

Figure 7-5. AVDD Linear Regulator Block Diagram

The power dissipated in the device by the AVDD linear regulator can be calculated as follows: $P = (V_{PVDD} - V_{AVDD}) \times I_{AVDD}$

For example, at a V_{PVDD} of 24V, drawing 20mA out of AVDD results in a power dissipation as shown in Equation 2.

$$P = \left(24\ V - 3.3\ V\right) \times 20\ mA = 414\ mW \quad (2)$$

7.3.3 Pin Diagrams

Figure 7-6 shows the input structure for the logic level pins, INHx and INLx. The input can be driven with a voltage or external resistor.

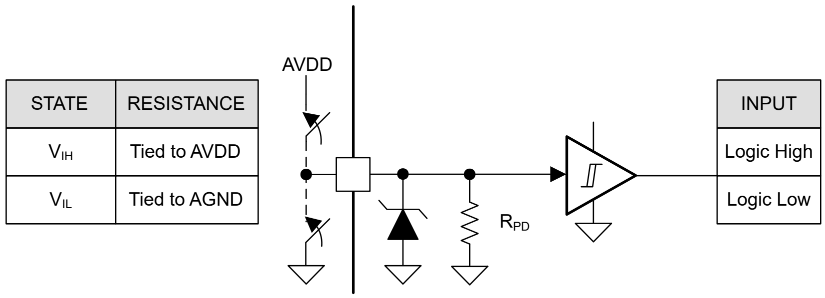

Figure 7-6. Logic-Level Input Pin Structure

Figure 7-7 shows the structure of the four level input pins, MODE and CSAGAIN, on hardware interface devices. The input can be set with an external resistor.

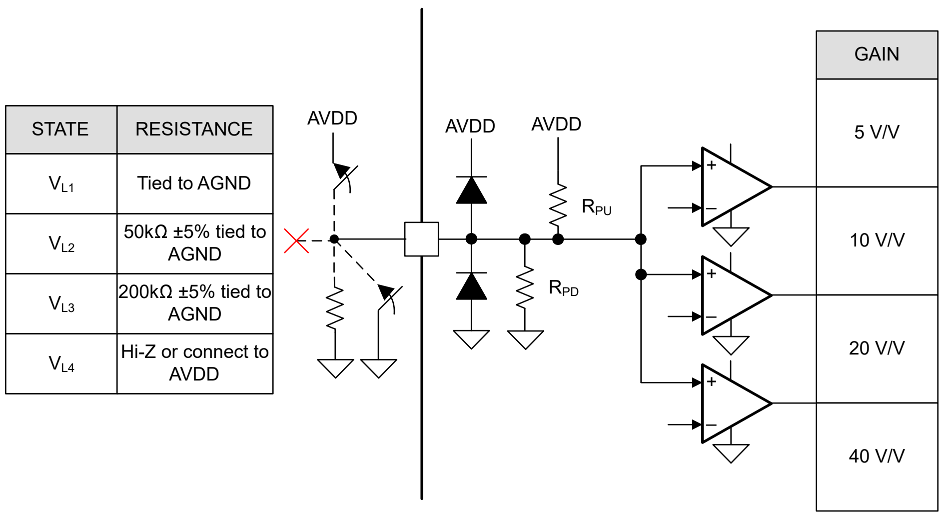

Figure 7-7. Four Level Input Pin Structure

Figure 7-8 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function correctly.

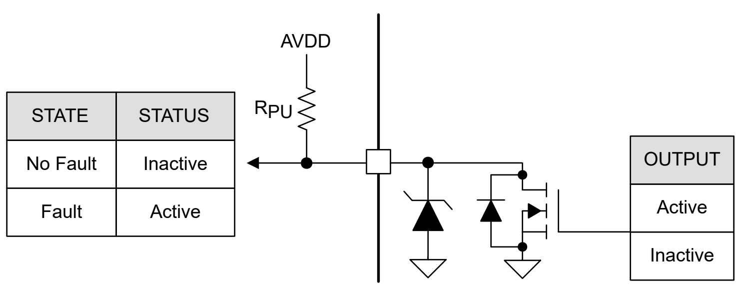

Figure 7-8. Open-Drain Output Pin Structure

7.3.4 Low-Side Current Sense Amplifiers

The DRV8329 integrates a high-performance low-side current sense amplifier for current measurements using a low-side shunt resistor. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. The current sense amplifier can be used to sense the sum of the half-bridge currents. The current sense amplifiers includes features such as configurable gain (CSAGAIN), and a voltage reference pin (CSAREF). The DRV8329 generates internally a common voltage of $V_{CSAREF}/8$.

The gain setting is adjustable between four different levels (5V/V, 10V/V, 20V/V, and 40V/V). Gain settings can be configured through CSAGAIN pin.

Table 7-4. CSA Gain setting

CSAGAIN pin	CSA Gain Setting
Connect to GND	5V/V
50kΩ +/- 5% to GND	10V/V
200kΩ +/- 5% to GND	20V/V
HiZ or Connect to AVDD	40V/V

7.3.4.1 Current Sense Operation

DRV8329 internally generates a common mode voltage of $V_{CSAREF}/8$ to obtain maximum resolution for current measurement. SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (CSAGAIN).

Use Equation 3 to calculate the current through the shunt resistor (R_{SENSE}).

$$I = \frac{V_{SO} - \frac{V_{CSAREF}}{8}}{CSAGAIN \times R_{SENSE}} \tag{3}$$

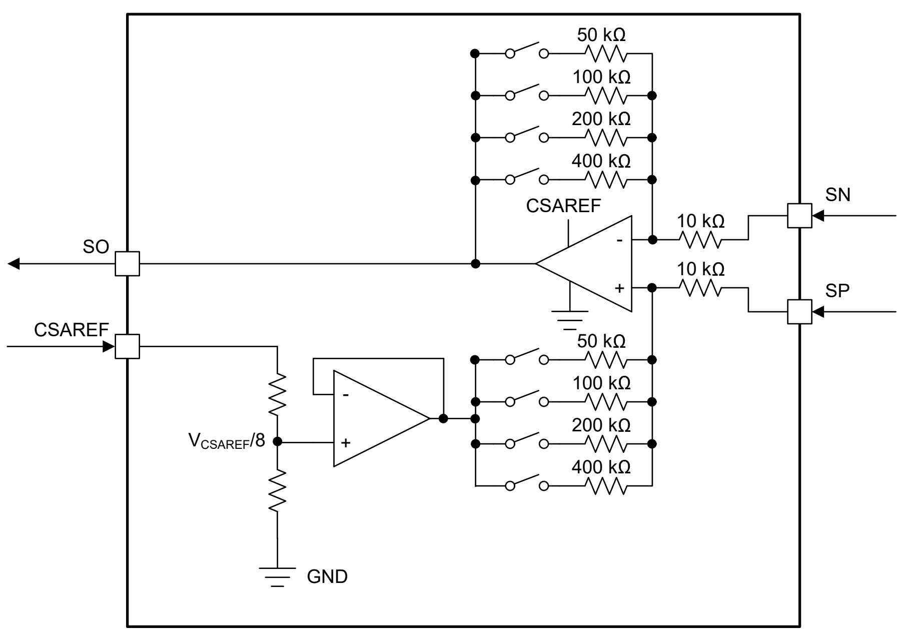

Figure 7-9. Current-Sense Configuration

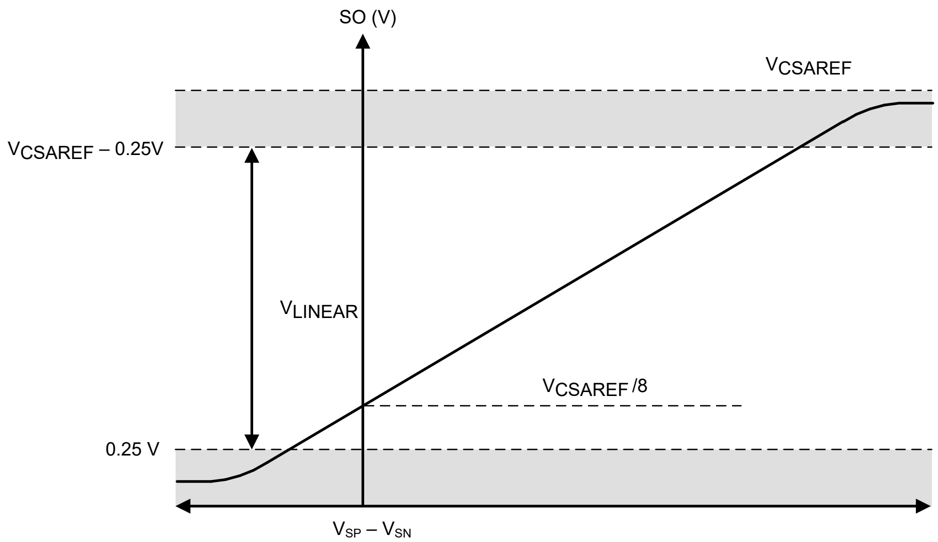

Figure 7-10. Current-Sense Output

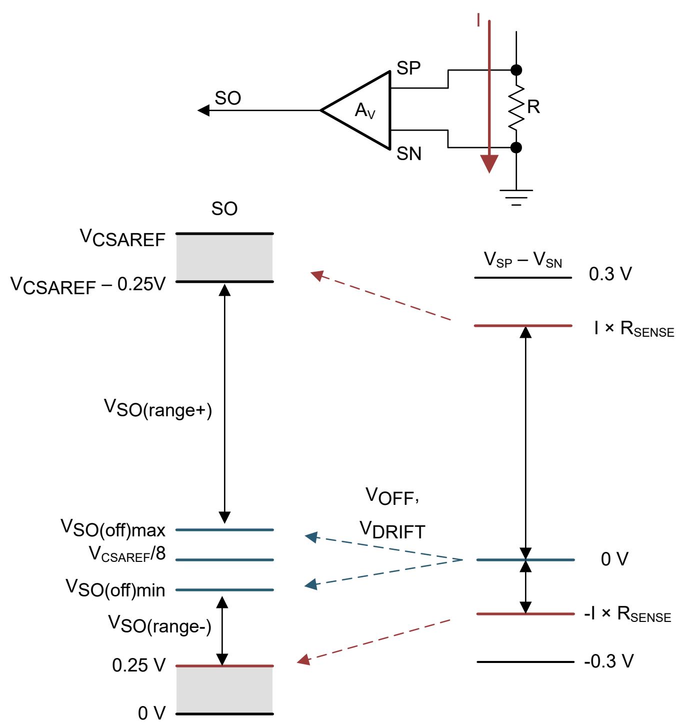

Figure 7-11. Current-Sense Regions

7.3.5 Gate Driver Shutdown Sequence (DRVOFF)

When DRVOFF is driven high, the gate driver goes into shutdown, overriding signals on inputs pins INHx and INLx. DRVOFF bypasses the digital control logic inside the device, and is connected directly to the gate driver output (see Figure 7-12). This pin provides a mechanism for externally monitored faults to disable the gate driver by directly bypassing an external controller or the internal control logic. When the DRV8329-Q1 detects that the DRVOFF pin is driven high, it disables the gate driver and puts it into pulldown mode (see Figure 7-13). The gate driver shutdown sequence proceeds as shown in Figure 7-13. When the gate driver initiates the shutdown sequence, the active driver pulldown is applied at I_{SINK} current for the $t_{SD\_SINK\_DIG}$ time, after which the gate driver moves to passive pulldown mode. nFAULT will be pulled low while DRVOFF is held high to indicate the shutdown state, and will be released when DRVOFF is driven low.

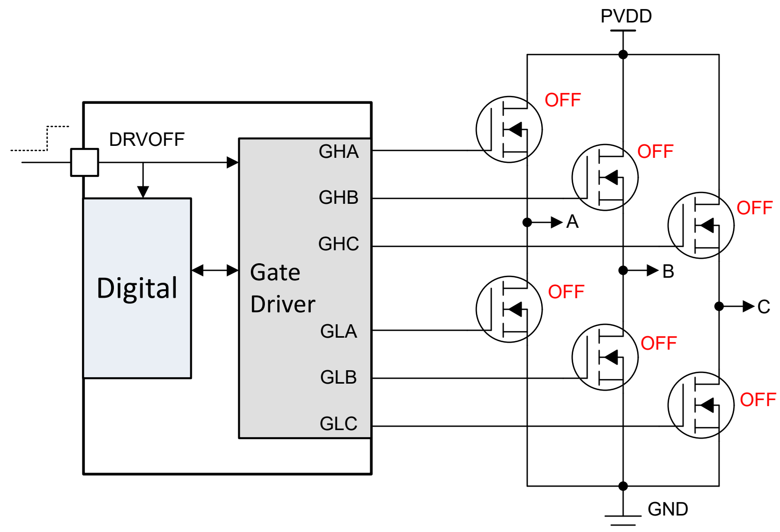

Figure 7-12. DRV8329-Q1 DRVOFF Gate Driver Output State

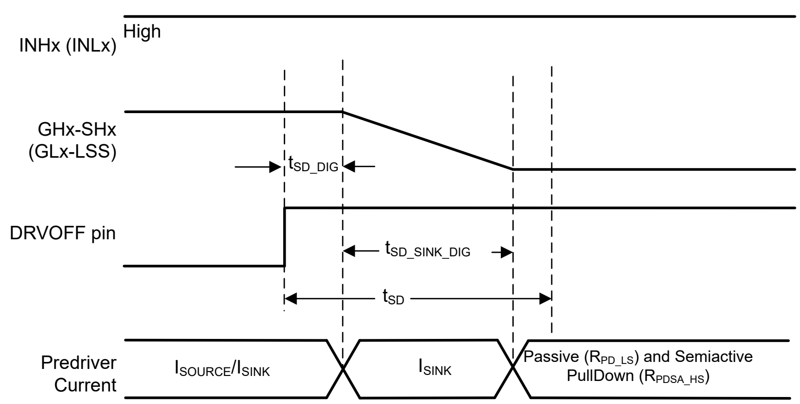

Figure 7-13. Gate Driver Shutdown Seqeunce

7.3.6 Gate Driver Protective Circuits

The DRV8329-Q1 is protected against PVDD undervoltage, AVDD power-on reset, bootstrap undervoltage, GVDD undervoltage, MOSFET V_{DS} and V_{SENSE} overcurrent events.

Table 7-5. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
PVDD undervoltage (PVDD_UV)	$V_{PVDD} < V_{PVDD\_UV}$	-	nFAULT	Disabled [1]	Disabled	Automatic: $V_{PVDD} > V_{PVDD\_UV}$
AVDD POR (AVDD_POR)	$V_{AVDD} < V_{AVDD\_POR}$	-	nFAULT	Disabled [1]	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_POR}$
GVDD undervoltage (GVDD_UV)	$V_{GVDD} < V_{GVDD\_UV}$	-	nFAULT	Pulled Low [2]	Active	Latched: nSLEEP Reset Pulse
BSTx undervoltage (BST_UV)	$V_{BSTx} - V_{SHx} < V_{BST\_UV}$ and INHx = High	-	nFAULT	Pulled Low [2]	Active	Latched: nSLEEP Reset Pulse
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{DS\_LVL}$	0.1V < V_{VDSLVL} < 2.5V	nFAULT	Pulled Low [2]	Active	Latched: nSLEEP Reset Pulse
		VDSLVL pin 100kΩ tied to GVDD	None	Active	Active	No action
V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SENSE\_LVL}$	-	nFAULT	Pulled Low [2]	Active	Latched: nSLEEP Reset Pulse
		VDSLVL pin 100kΩ tied to GVDD	None	Active	Active	No action
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	-	nFAULT	Pulled Low [2]	Active	Latched: nSLEEP Reset Pulse

1. Disabled: Passive pull down for GLx and semiactive pull down for GHx
2. Pulled Low: GHx and GLx are actively pulled low by the gate driver

7.3.6.1 PVDD Supply Undervoltage Lockout (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD\_UV\_DG}$ time, the device detects a PVDD undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, the charge pump is disabled, the internal digital logic is disabled, and the nFAULT pin is driven low. Normal operation starts again (the gate driver becomes operable and the nFAULT pin is released) when the PVDD pin rises above V_{PVDD_UV}.

7.3.6.2 AVDD Power on Reset (AVDD_POR)

If at any time the supply voltage on the AVDD pin falls below the V_{AVDD_POR} threshold for longer than the $t_{AVDD\_POR\_DG}$ time, the device enters an inactive state, disabling the gate driver, the charge pump, and the internal digital logic, and nFAULT is driven low. Normal operation (digital logic operational) requires nSLEEP to be asserted high and AVDD to exceed V_{AVDD_POR} level.

7.3.6.3 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold voltage for longer than the $t_{GVDD\_UV\_DG}$ time, the device detects a GVDD undervoltage event. After detecting the GVDD_UV undervoltage event, all of the gate driver outputs are driven low to disable the external MOSFETs, the charge pump is disabled and nFAULT pin is driven low. After the GVDD_UV condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse (t_{RST})

Note

After the GVDD_UV fault is cleared through an nSLEEP pin reset pulse, the nFAULT pin is held low until the GVDD capacitor is refreshed by the charge pump. After the GVDD capacitor is charged, the nFAULT pin is automatically released. The duration that the nFAULT pin is low after the fault is cleared will not exceed t_{WAKE} time.

7.3.6.4 BST Undervoltage Lockout (BST_UV)

If at any time the voltage across BSTx and SHx pins falls lower than the V_{BST_UV} threshold voltage for longer than the $t_{BST\_UV\_DG}$ time, the device detects a BST undervoltage event. Afer detecting the BST_UV event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. After the BST_UV condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse (t_{RST}).

7.3.6.5 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

The device has adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. The high-side VDS monitors measure between the PVDD and SHx pins and the low-side VDS monitors measure between the SHx and LSS pins. If the voltage across external MOSFET exceeds the V_{DS_LVL} threshold for longer than the t_{DS_DG} deglitch time, a VDS_OCP event is recognized. Afer detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The VDS threshold can be set between 0.1 V to 2.5 V by applying a voltage on the VDSLVL pin. VDS OCP can be disabled by connecting VDSLVL to GVDD through a 100 kΩ resistor. After the VDS_OCP condition is cleared, the fault state remains latched and can be cleared through the nSLEEP pin reset pulse (t_{RST}).

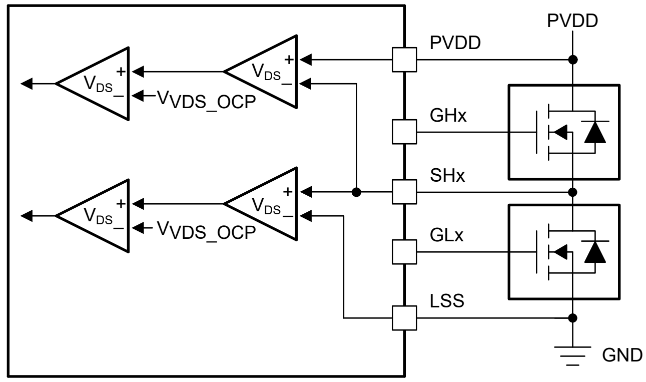

Figure 7-14. DRV8329-Q1 V_{DS} Monitors

7.3.6.6 V_{SENSE} Overcurrent Protection (SEN_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between the LSS and GND pins. If at any time the voltage on the LSS input exceeds the V_{SEN_OCP} threshold for longer than the t_{DS_DEG} deglitch time, a SEN_OCP event is recognized. Afer detecting the SEN_OCP overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and the nFAULT pin is driven low. The V_{SENSE} threshold is fixed at 0.5 V and deglitch time is fixed to 3 µs. After the SEN_OCP condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse (t_{RST}). SEN_OCP can be disabled by connecting VDSLVL to GVDD through a 100 kΩ resistor.

7.3.6.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), an OTSD event is recognized. After detecting the OTSD overtemperature event, all of the gate driver outputs are driven low to disable the external MOSFETs, charge pump is disabled and nFAULT pin is driven low. After OTSD condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse (t_{RST})

7.4 Device Functional Modes

7.4.1 Gate Driver Functional Modes

7.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8329-Q1. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the GVDD regulator is disabled and the AVDD regulator is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

Note

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are not active. After the regulators have been active, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

7.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{PVDD} voltage is greater than the V_{PVDD_UV} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the GVDD regulator and AVDD regulator are active.

7.4.1.3 Fault Reset (nSLEEP Reset Pulse)

In the case of device latched faults, the DRV8329-Q1 goes into a partial shutdown state to help protect the external power MOSFETs and system.

Note

If the user wants to put the device into sleep state after latched fault event, the inputs INHx and INLx needs to be pulled low prior to driving the nSLEEP pin. If the inputs INHx and INLx are not driven low, then the fault is reset after nSLEEP is driven low for the t_{RST} time and there can be pulses on gate driver outputs GHx and GLx prior to device entering sleep. The duration of pulses on GHx and GLx can be of duration t_{SLEEP} if INHx and INLx are not pulled low.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8329-Q1 family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Section 8.2* section highlight how to use and configure the DRV8329-Q1 family of devices.

8.2 Typical Application

8.2.1 Three Phase Brushless-DC Motor Control

In this application, the DRV8329-Q1 is used to drive a three-phase Brushless-DC motor.

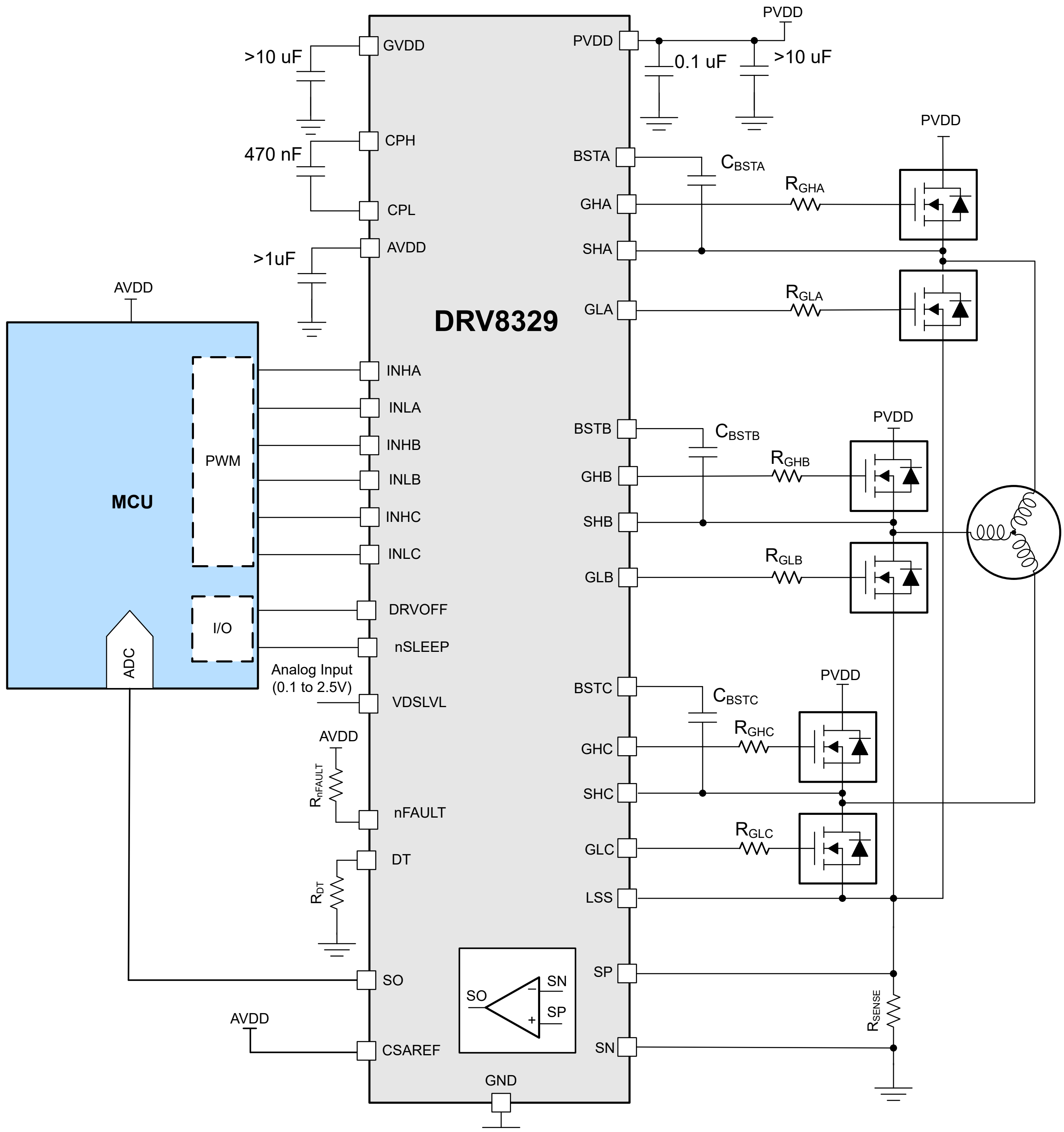


Figure 8-1. DRV8329-Q1 Application Diagram

8.2.1.1 Detailed Design Procedure

Section 8.2.1.1 lists the example input parameters for the system design.

Table 8-1. Design parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{PVDD}	24 V

Table 8-1. Design parameters (continued)

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Motor peak current	I_{PEAK}	20 A
PWM Frequency	f_{PWM}	20 kHz
MOSFET VDS Slew Rate	SR	120 V/us
MOSFET input gate capacitance	Q_G	54 nC
MOSFET input gate capacitance	Q_{GD}	14 nC
Dead time	t_{dead}	200 ns
Overcurrent protection	I_{OCP}	30 A

8.2.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 18-V, 24-V or 36-V). The DRV8329-Q1 allows for a range of possible operating voltages from 4.5-V to 60-V.

8.2.1.1.2 Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 4 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \tag{4}$$

=12 V – 0.85 V – 4.45 V = 6.7 V

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.7 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with Equation 5:

$$Q_{TOT} = Q_G + \frac{IL_{BS\_TRAN}}{f_{SW}} \tag{5}$$

=54 nC + 115 µA/20 kHz = 54 nC + 5.8 nC = 59.8nC

where

- Q_G is the total MOSFET gate charge
- I_{LBS_TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor can then be estimated as below assuming 1V of ΔV_{BSTx}:

$$C_{BST\_MIN} = {}^{Q_{TOT}}/_{\Delta V_{BSTX}} \tag{6}$$

= 59.8 nC / 1 V = 59.8 nF

The calculated value of minimum bootstrap capacitor is 59.8 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \tag{7}$$

= 10*100 nF= 1 μF

For this example application, choose a 1-μF C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long-term reliability of the system.

Note

For higher power system requiring 100% duty cycle support for longer duration it is recommended to use C_{BSTx} of ≥1μF and C_{GVDD} of ≥10 μF.

8.2.1.1.3 Gate Drive Current

Selecting an appropriate gate drive current is essential when turning on or off power MOSFETs gates to switch motor current. The amount of gate drive current and input capacitance of the MOSFETs determines the drain-to-source voltage slew rate (V_{DS}). Gate drive current can be sourced from GVDD into the MOSFET gate (I_{SOURCE}) or sunk from the MOSFET gate into SHx or LSS (I_{SINK}).

Using too high of a gate drive current can turn on MOSFETs too quickly which may cause excessive ringing, dV/dt coupling, or cross-conduction from switching large amounts of current. If parasitic inductances and capacitances exist in the system, voltage spiking or ringing may occur which can damage the MOSFETs or DRV8329-Q1 device.

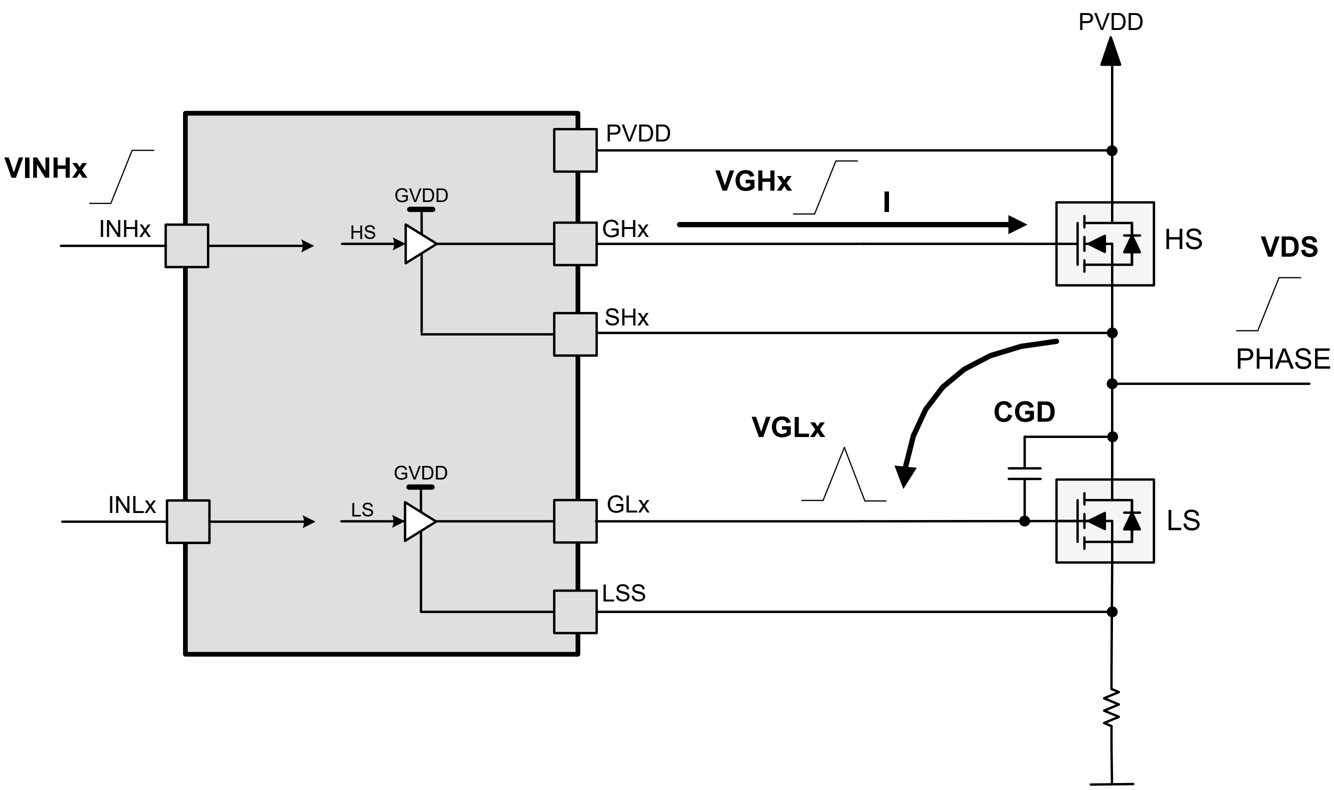


Figure 8-2. Effects of high gate drive current

On the other hand, using too low of a gate drive current causes long V_{DS} slew rates. Turning on the MOSFETs too slowly may heat up the MOSFETs due to $R_{DS,on}$ switching losses.

The relationship between gate drive current I_{GATE}, MOSFET gate-to-drain charge Q_{GD}, and V_{DS} slew rate switching time $t_{rise,fall}$ are described by the following equations:

$$SR_{DS} = \frac{V_{DS}}{t_{rise,fall}} \tag{8}$$

$$I_{GATE} = \frac{Q_{gd}}{t_{rise,fall}} \tag{9}$$

It is recommend to evaluate at lower gate drive currents and increase gate drive current settings to avoid damage from unintended operation during initial evaluation.

8.2.1.1.4 Gate Resistor Selection

The slew rate of the SHx connection will be dependent on the rate at which the gate of the external MOSFETs is controlled. The pull-up/pull-down strength of the DRV8329-Q1 is fixed internally, hence the slew rate of gate voltage can be controlled with an external series gate resistor. In some applications, the gate charge of the MOSFET, which is the load on gate driver device, is significantly larger than the gate driver peak output current capability. In such applications, external gate resistors can limit the peak output current of the gate driver. External gate resistors are also used to dampen ringing and noise.

The specific parameters of the MOSFET, system voltage, and board parasitics will all affect the final SHx slew rate, so generally selecting an optimal value or configuration of external gate resistor is an iterative process.

To lower the gate drive current, a series resistor R_{GATE} can be placed on the gate drive outputs to control the current for the source and sink current paths. A single gate resistor will have the same gate path for source and sink gate current, so larger R_{GATE} values will yield similar SHx slew rates. Note that gate drive current varies by PVDD voltage, junction temperature, and process variation of the device. Gate resistor values can be estimated with +/-30% accuracy using the Gate Resistor Calculator.

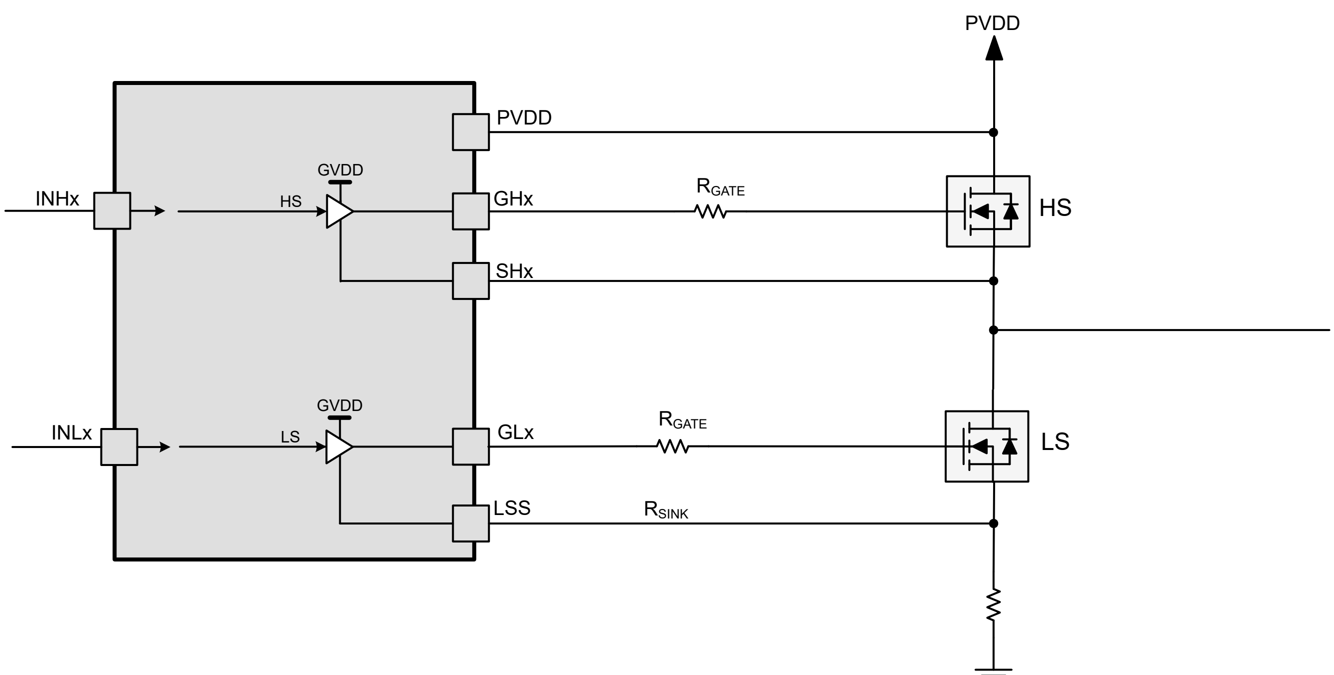


Figure 8-3. Gate driver outputs with series resistors

Typically, it is recommended to have the sink current be twice the source current to implement a strong pulldown from gate to the source to ensure the MOSFET stays off while the opposite FET is switching. This can be implemented discretely by providing a separate path through a resistor for the source and sink currents by placing a diode and sink resistor (R_{SINK}) in parallel to the source resistor (R_{SOURCE}). Using the same value of source and sink resistors results in half the equivalent resistance for the sink path. This yields twice the gate drive sink current compared to the source current, and SHx will slew twice as fast when turning off the MOSFET.

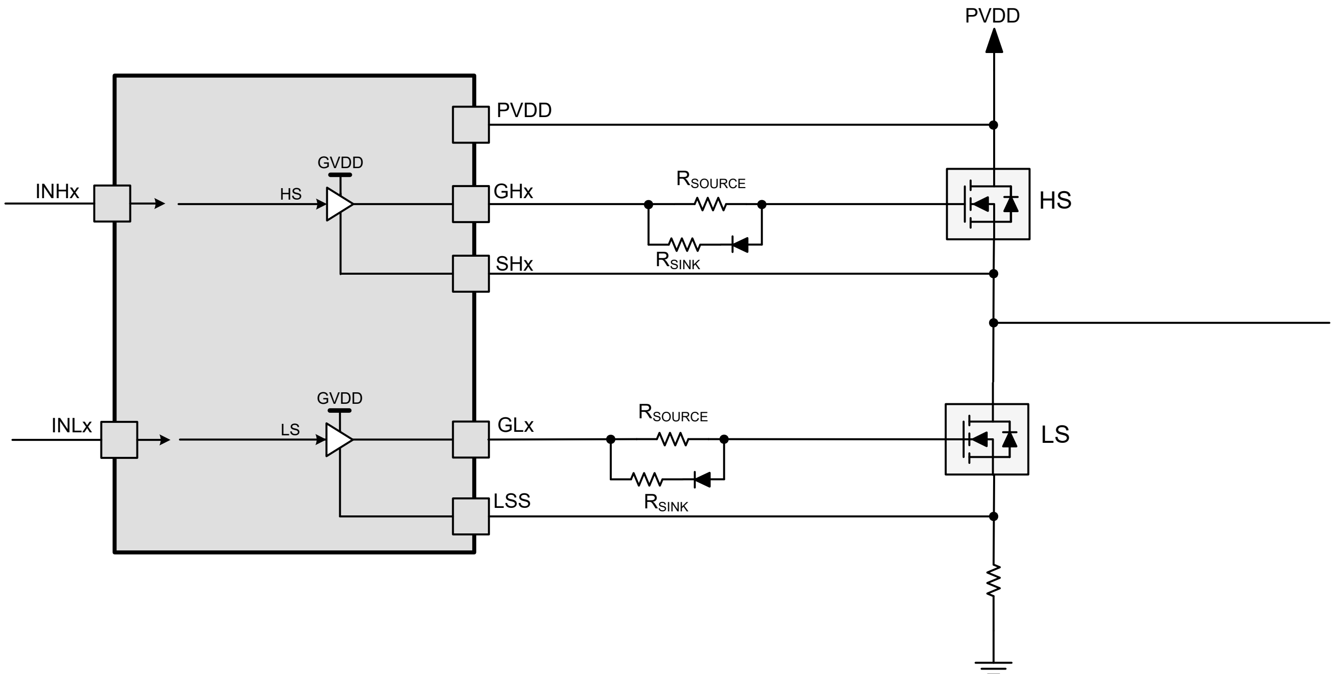


Figure 8-4. Gate driver outputs with separate source and sink current paths

8.2.1.1.5 System Considerations in High Power Designs

Higher power system designs can require design and application considerations that are not regarded in lower power system designs. It is important to combat the volatile nature of higher power systems by implementing troubleshooting guidelines, external components and circuits, driver product features, or layout techniques. For more information, please visit the System Design Considerations for High-Power Motor Driver Applications application note.

8.2.1.1.5.1 Capacitor Voltage Ratings

Use capacitors with voltage ratings that are 2x the supply voltage (PVDD, GVDD, AVDD, etc). Capacitors can experience up to half the rated capacitance due to poor DC voltage rating performance.

For example, since the bootstrap voltage is around 12 to 13-V with respect to SHx (BSTx-SHx) then the BSTx-SHx capacitor should be rated for 25-V or greater.

8.2.1.1.5.2 External Power Stage Components

External components in the power stage are not required by design but are helpful in suppressing transients, managing inductor coil energy, mitigating supply pumping, dampening phase ringing, or providing strong gate-to-source pulldown paths. These components are used for system tuning and debuggability so the BLDC motor system is robust while avoiding damage to the DRV8329-Q1 device or external MOSFETs.

Figure 8-5 shows examples of power stage components that can be optimally placed in the design.

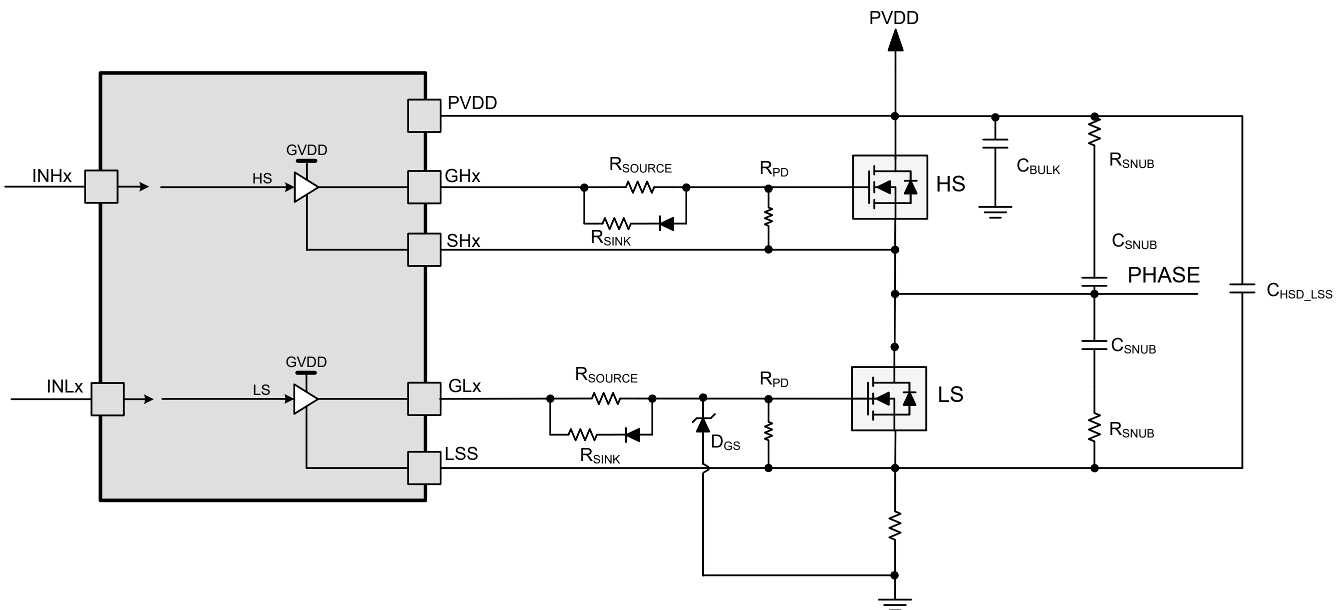


Figure 8-5. Optional external power stage components

Some examples of issues and external components that can resolve those issues are found in Table 8-2:

Table 8-2. Common issues and resolutions for power stage debugging

Issue	Resolution	Component(s)
Gate drive current required is too large, resulting in very fast MOSFET V_{DS} slew rate	Series resistors required for gate drive current adjustability	0-100 Ω series resistors (RGATE/RSOURCE) at gate driver outputs (GHx/GLx), optional sink resistor (RSINK) and diode in parallel with gate resistor for adjustable sink current
Ringing at phase's switch node (SHx) resulting in high EMI emissions	RC snubbers placed in parallel to each HS/LS MOSFET to dampen oscillations	Resistor (RSNUB) and Capacitor (CSNUB) placed parallel to the MOSFET, calculate RC values based on ringing frequency using Proper RC Snubber Design for Motor Drivers
Negative transients at low-side source (LSS) below minimum specification	HS drain to LS source capacitor to suppress negative bouncing	0.01uF-1uF, VM-rated capacitor from PVDD-LSS (CHSD_LSS) placed near LS MOSFET's source
Negative transient at low-side gate (GLx) below minimum specification	Gate-to-ground Zener diode to clamp negative voltage	GVDD voltage rated Zener diode (DGS) with anode connected to GND and cathode connected to GLx
Extra protection required to ensure MOSFET is turned off if gate drive signals are Hi-Z	External gate-to-source pulldown resistors (after series gate resistors)	10 kΩ to 100 kΩ resistor (RPD) connected from gate to source for each MOSFET

8.2.1.1.5.3 Parallel MOSFET Configuration

If higher MOSFET continuous drain current ratings are required for the motor, parallel MOSFETs can be used for higher current capability. However, this requires special schematic and layout design requirements to switch both MOSFETs simultaneously because one MOSFET may turn on faster than the other due to process variation.

It is recommended to place the MOSFETs close together with a common gate signal that splits as close as possible to the MOSFETs gates. If gate resistance is required, calculate the equivalent resistance required for the equivalently rated MOSFET, and place the gate resistors as close as possible to the MOSFET's gate input to dampen any coupling into the gate driver.

For more information, please visit the Driving Parallel MOSFETs application brief.

8.2.1.1.6 Dead Time Resistor Selection

Dead time insertion is available in the DRV8329-Q1 via a resistor (R_{DT}) from the DT pin to ground as shown in Figure 8-6. The ranges of dead time in the DRV8329-Q1 is 100 ns to 2000 ns when R_{DT} is tied to GND from the DT pin. A linear interpolation of the resistance value is used to set the appropriate dead time.

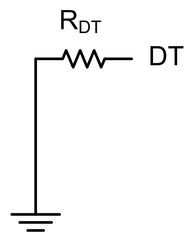


Figure 8-6. Dead time resistor

Dead time (in nanoseconds) can be calculated from the dead time resistor calculation in Equation 1.

Dead time can also be implemented from the PWM inputs generated by an MCU. If dead time is inserted at the PWM inputs and the DRV8329-Q1, then the driver output PWM dead time is the larger of the two dead times. For instance, if 200 ns dead time is inserted at the MCU inputs and 50 ns dead time is inserted in the DRV8329-Q1 via the DT pin, then the output driver PWM dead time will be 200 ns.

8.2.1.1.7 VDSLVL Selection

VDSLVL is an analog voltage used to directly set the VDS overcurrent threshold for overcurrent protection. It can be sourced directly from an analog voltage source (such as a digital-to-analog converter) or divided down from a voltage rail (such as a resistor divider from AVDD) as shown in Figure 8-7.

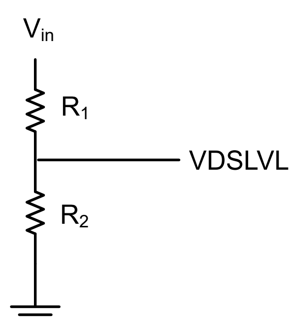


Figure 8-7. Resistor divider to set VDSLVL from a voltage rail

Equation 10 and Equation 11 can be used to set the required VDSLVL voltage using a resistor divider from a voltage source to establish an overcurrent limit given the $R_{DS,on}$ of the MOSFETs used:

$$V_{VDSLVL} = I_{OC} \times R_{ds(on)} \tag{10}$$

$$\frac{R_1}{R_2} = \frac{V_{in}}{V_{VDSLVL}} - 1 \tag{11}$$

where:

- V_{VDSLVL} = VDSLVL voltage
- I_{OCP} = VDS overcurrent limit
- $R_{DS,on}$ = MOSFET on-resistance
- V_{IN} = voltage source for VDSLVL voltage divider
- R1/R2 = resistor ratio for setting VDSLVL

For example, if a resistor divider from AVDD is used to set an overcurrent trip threshold of 30-A and the MOSFET $R_{DS(ON)}$ = 10mΩ, then VDSLVL = 0.3V.

In some applications, there will be a difference between battery voltage (VBAT) to directly drive motor power and PVDD voltage to power the DRV8329-Q1. Because high-side VDS monitoring is referenced from PVDD-SHx, VDSLVL needs to be selected appropriately to accommodate for the difference in VBAT and PVDD.

Equation 12 helps select an appropriate VDSLVL if there is a difference between PVDD and VDSLVL:

$$VDSLVL = \left(VBAT - PVDD\right) + I_{OC}{}^{*}R_{DS(ON)} \tag{12}$$

For instance, if VBAT = 24.0 V, PVDD = 23.3 V, Rdson = 10-mΩ, and I_OC = 30-A, then VDSLVL should equal 1.0V to detect a 30-A overcurrent event across the high-side FET and a 100-A overcurrent event across the low-side FET.

8.2.1.1.8 AVDD Power Losses

An integrated LDO can supply 3.3-V (up to 80-mA) as power rails for external ICs or supply the pullup voltages for resistors and switches. The power loss from AVDD with respect to PVDD, AVDD voltage, and AVDD current is $P_{AVDD} = (V_{PVDD} - V_{AVDD}) \times I_{AVDD}$.

Higher power losses occur due larger dropout from PVDD to 3.3 V or increased AVDD load current.

8.2.1.1.9 Current Sensing and Output Filtering

The SO pin is typically sampled by an analog-to-digital converter in the MCU to calculate the total motor phase current. A phase current calculation is used for closed-loop feedback such as overcurrent protection or sensorless trapezoidal or Field-oriented control commutation

An example calculation for phase current is shown below for a system using V_{SO} = 1.4 V, V_{CSAREF} = 3.3V, CSAGAIN = 20 V/V, and R_{SENSE} = 1 mΩ.

$$I = \frac{V_{SO} - \frac{V_{CSAREF}}{8}}{CSAGAIN \times R_{SENSE}} \tag{13}$$

$$I = \frac{1.4\,V - \frac{3.3\,V}{8}}{20\,V/V \times 0.001} \tag{14}$$

$$I = 49.375\,A \tag{15}$$

Sometimes high frequency noise can appear at the SO signals based on voltage ripple at VREF, added inductance at the SO traces, or routing of SO traces near high frequency components. It is recommended to add a low-pass RC filter close to the MCU with cutoff frequency at least 10 times the PWM switching frequency for trapezoidal commutation and 100 times the PWM switching frequency for sinusoidal commutation to filter high frequency noise. A recommended RC filter is 330-ohms, 470-pF to add minimal parallel capacitance to the ADC and current mirroring circuitry. The cutoff frequency for the low-pass RC filter is in Equation 16.

$$f_c = \frac{1}{2\pi RC} \tag{16}$$

8.2.1.1.10 Power Dissipation and Junction Temperature Losses

To calculate the junction temperature of the DRV8329-Q1 from power losses, use Equation 17. Note that the thermal resistance θ_{JA} depends on PCB configurations such as the ambient temperature, numbers of PCB layers, copper thickness on top and bottom layers, and the PCB area.

$$T_J[°C] = P_{loss}[W] \times \theta_{JA}\left[\frac{°C}{W}\right] + T_A\left[°C\right] \tag{17}$$

The table below shows summary of equations for calculating each loss in the DRV8329-Q1.

Table 8-3. DRV8329-Q1 Power Losses

Loss type	Equation
Standby power	$P_{standby} = V_{PVDD} \times I_{PVDDS}$
GVDD CP mode (PVDD < 18V)	$P_{LDO} = 2 \times V_{PVDD} \times I_{GVDD} - V_{GVDD} \times I_{GVDD}$
GVDD LDO mode (PVDD > 18V)	$P_{LDO} = (V_{PVDD} - V_{GVDD}) \times I_{GVDD}$
AVDD LDO	$P_{LDO} = (V_{PVDD} - V_{AVDD}) \times I_{AVDD}$

8.2.2 Application Curves

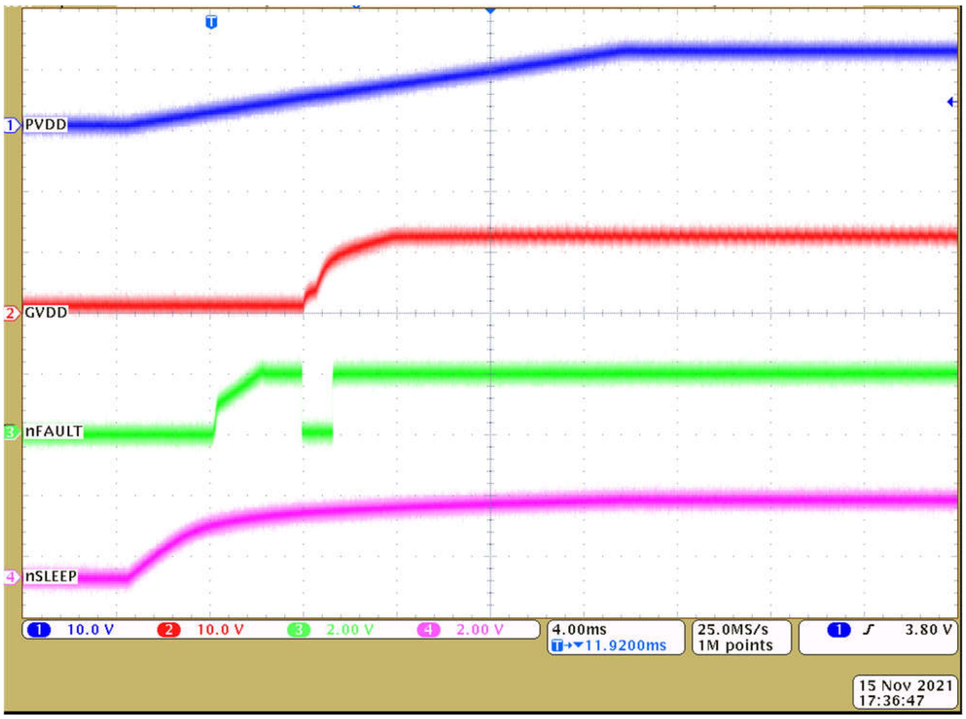


Figure 8-8. Device Powerup with PVDD

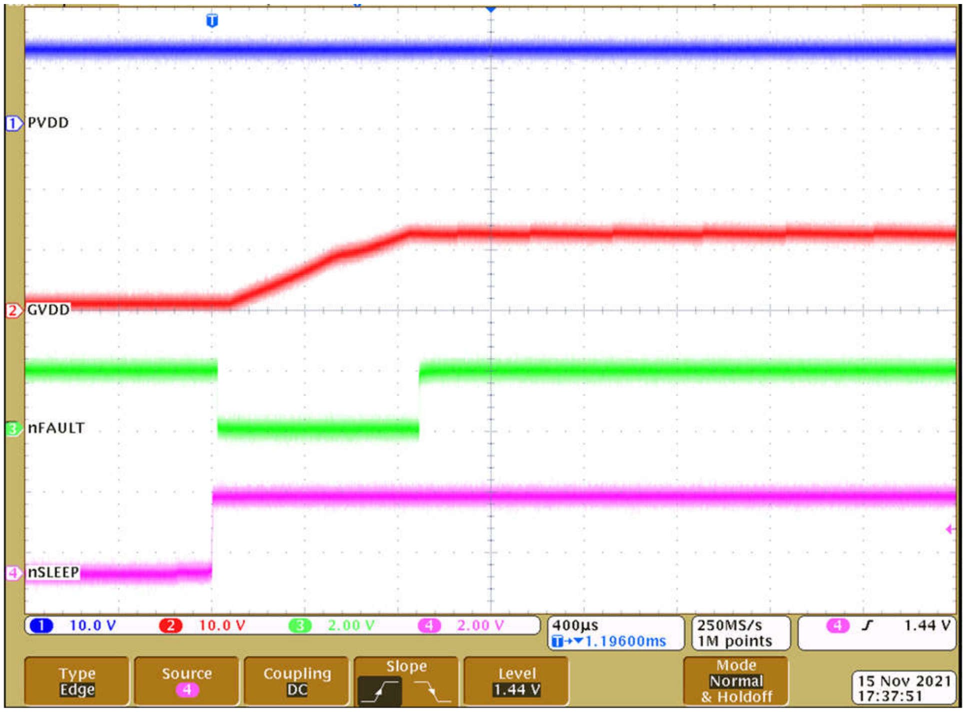


Figure 8-9. Device Powerup with nSLEEP

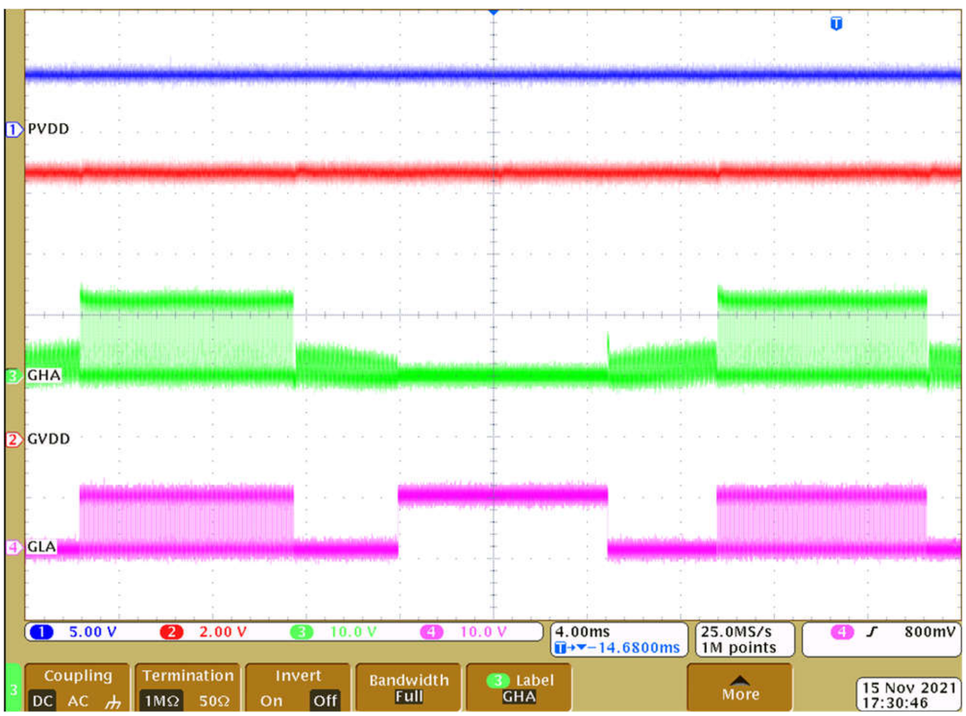


Figure 8-10. GVDD voltage threshold (PVDD = 4.5 V)

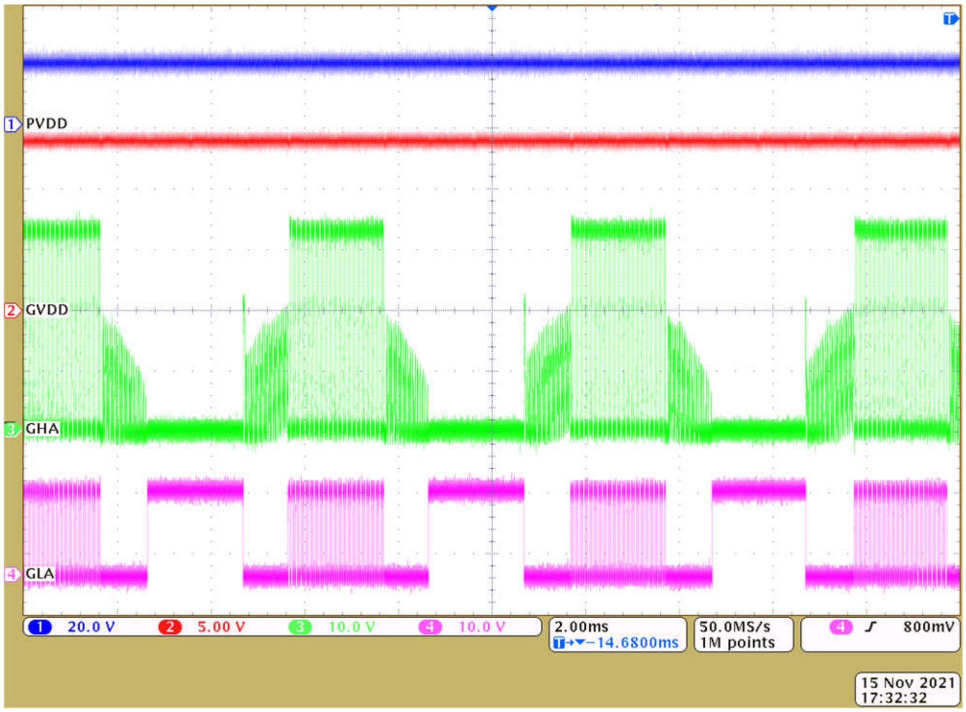


Figure 8-11. GVDD voltage threshold (PVDD = 20V)

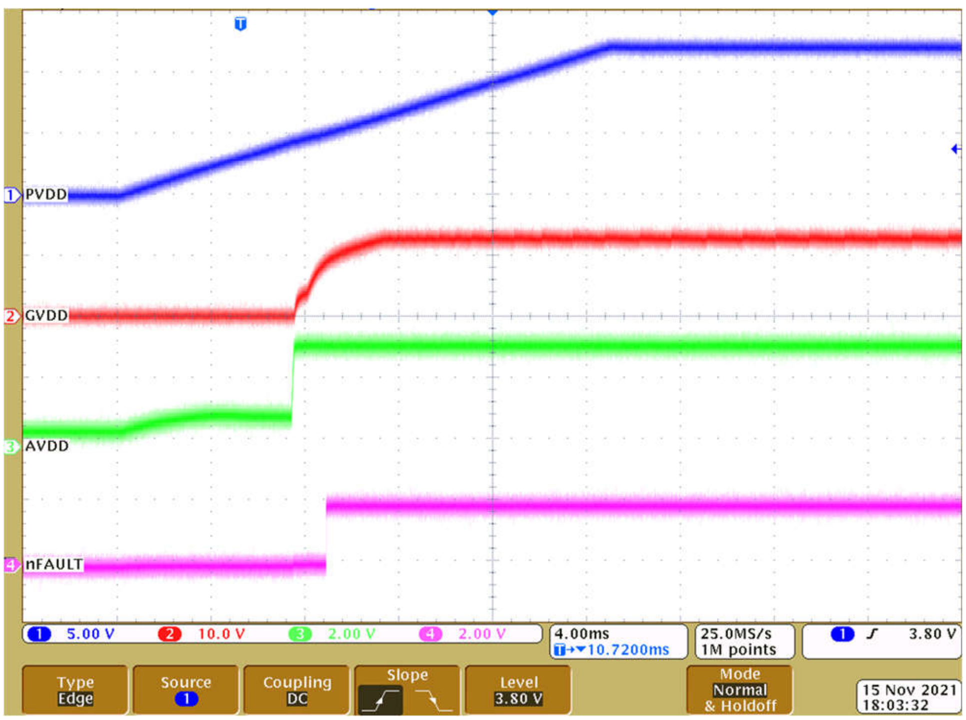


Figure 8-12. AVDD powerup

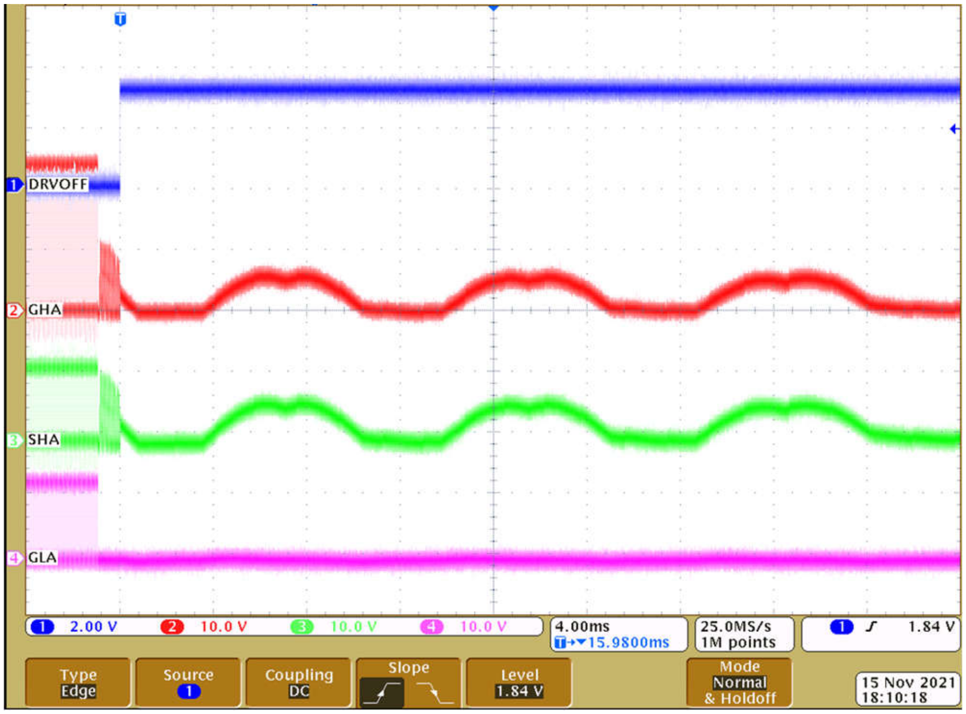


Figure 8-13. DRVOFF operation

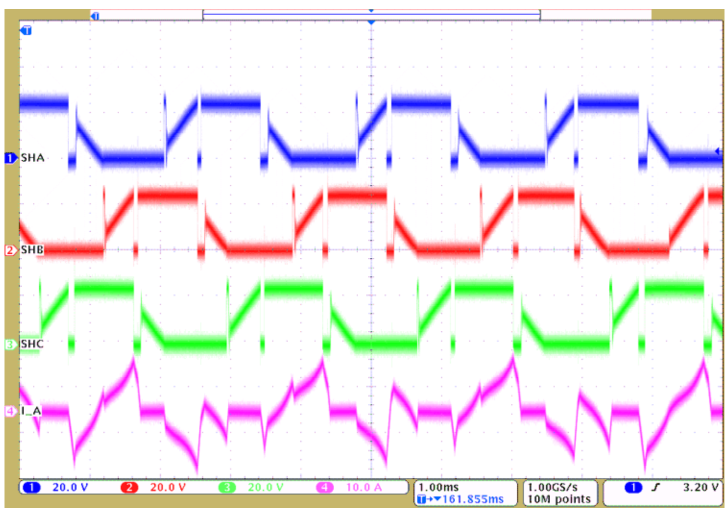


Figure 8-14. Driver operation at 100% duty cycle

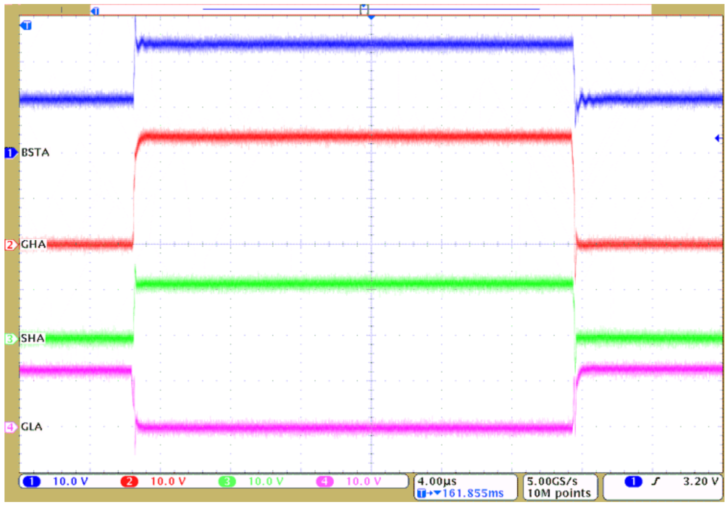


Figure 8-15. Driver PWM operation, 20 kHz, 50% duty cycle, zoomed

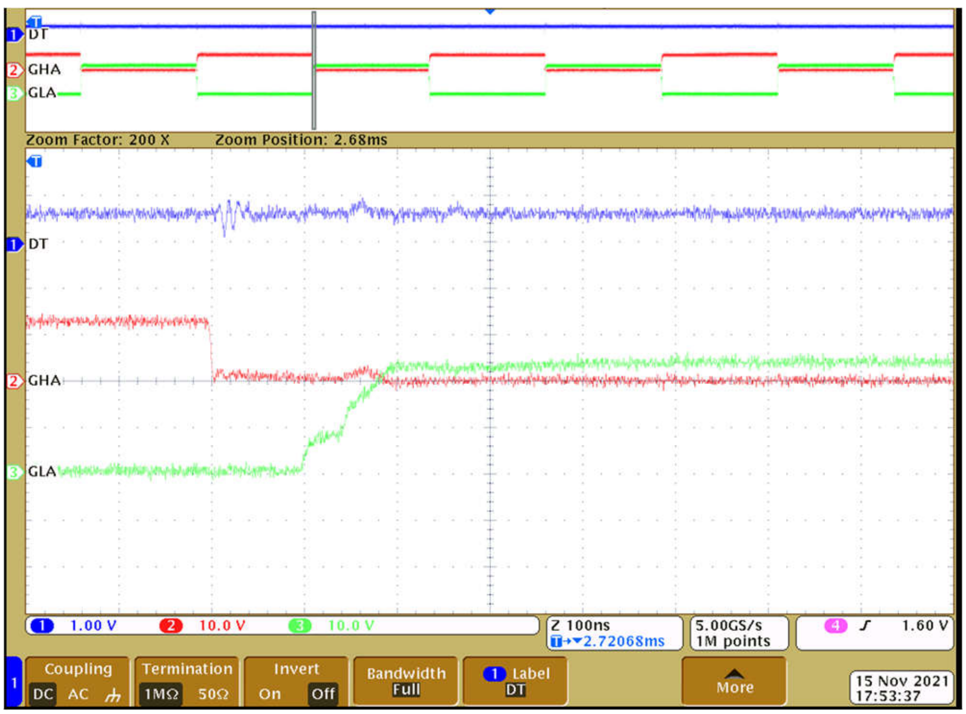


Figure 8-16. Driver dead time of 100 ns (DT = 10 kΩ to GND)

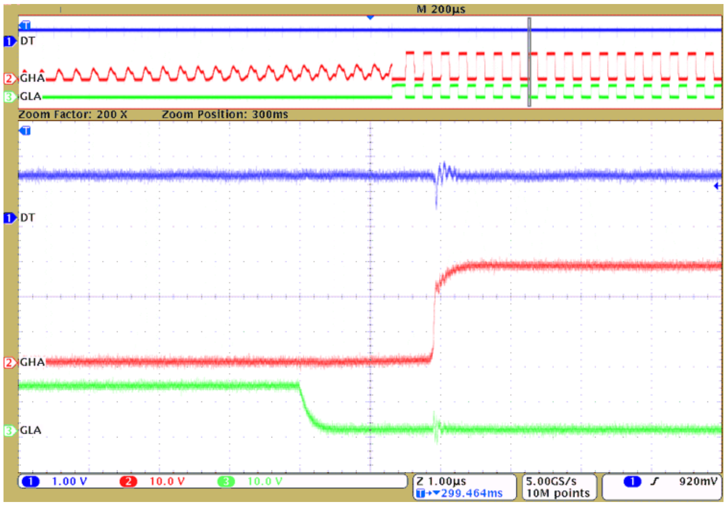


Figure 8-17. Driver dead time of 2000 ns (DT = 390 kΩ to GND)

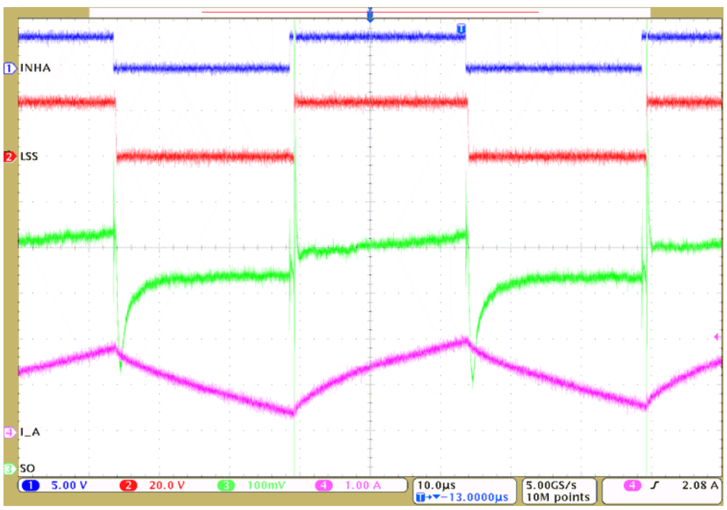


Figure 8-18. Current sense amplifier operation (GAIN = 40 V/V)

8.3 Power Supply Recommendations

The DRV8329-Q1 family of devices is designed to operate from an input voltage supply (PVDD) range from 4.5 V to 60 V. A 10-µF and 0.1-µF ceramic capacitor rated for PVDD must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the PVDD pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

8.3.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

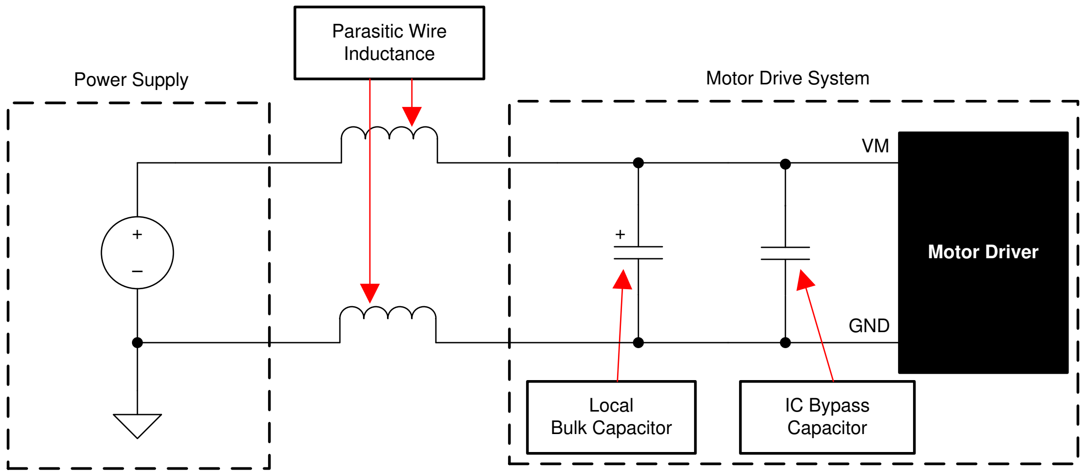


Figure 8-19. Motor Drive Supply Parasitics Example

8.4 Layout

8.4.1 Layout Guidelines

Bypass the PVDD pin to the PGND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for PVDD. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 470 nF, rated for PVDD, and be of type X5R or X7R.

The bootstrap capacitors (BSTx-SHx) should be placed closely to device pins to minimize loop inductance for the gate drive paths.

The dead time resistor (R_{DT}) should be placed as close as possible to the DT pin.

Bypass the AVDD pin to the AGND pin with a 1-µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

When designing higher power systems, physics in the PCB layout can cause parasitic inductances, capacitances, and impedances that deter the performance of the system as shown in Figure 8-20. Understanding the parasitics that are present in a higher power motor drive system can help designers mitigate their effects through good PCB layout. For more information, please visit the System Design Considerations for High-Power Motor Driver Applications and Best Practices for Board Layout of Motor Drivers application notes.

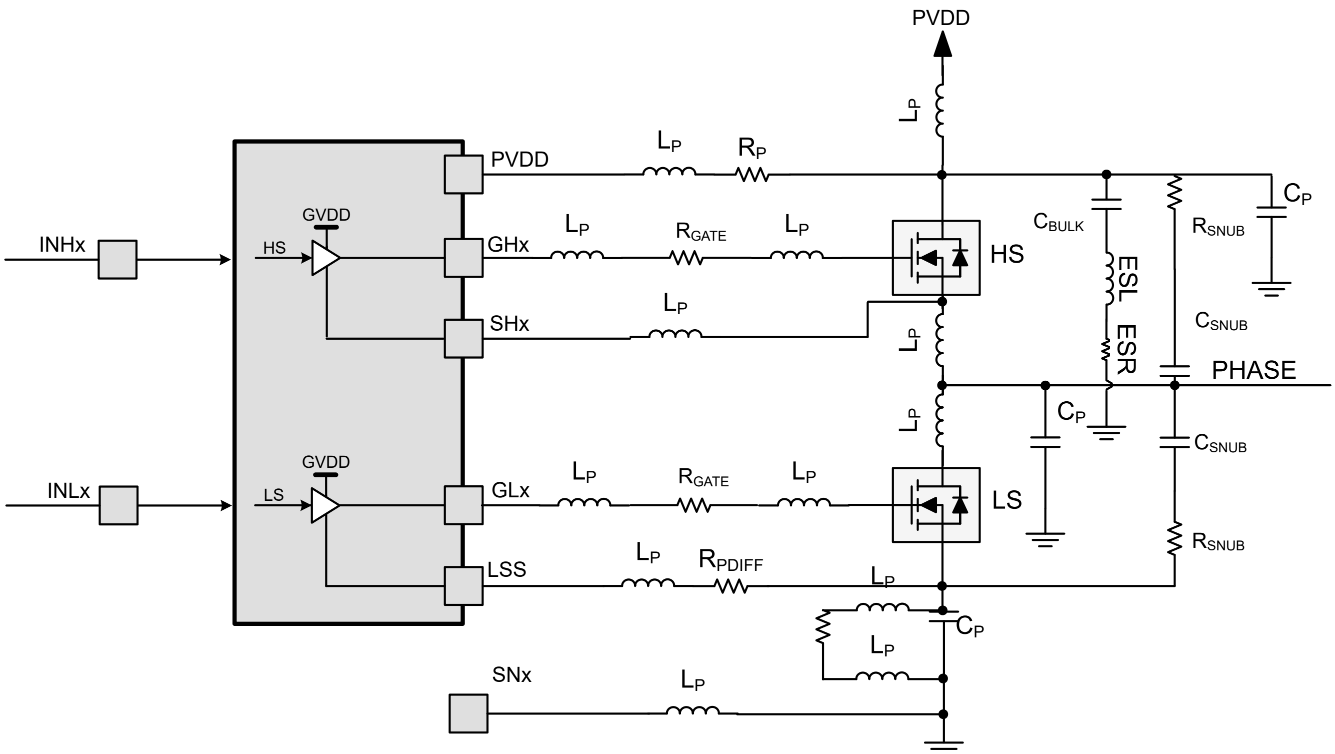


Figure 8-20. Parasitics in the PCB of a BLDC motor driver powerstage

Gate drive traces (BSTx, GHx, SHx, GLx, LSS) should be at least 15-20mil wide and as short as possible to the MOSFET gates to minimize parasitic inductances and impedances. This helps supply large gate drive currents, turn MOSFETs on efficiently, and improves VGS and VDS monitoring. If a shunt resistor is used to monitor the low-side current from LSS to GND, ensure the shunt resistor selected is wide to minimize inductance introduced at the low-side source LSS.

TI recommends connecting all non-power stage circuitry (including the thermal pad) to GND to reduce parasitic effects and improve power dissipation from the device. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

8.4.2 Thermal Considerations

The DRV8329-Q1 has thermal shutdown (TSD) to protect against overtemperature. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.4.2.1 Power Dissipation

The DRV8329-Q1 integrates a variety of circuits that contribute to total power losses. These power losses include standby power losses, GVDD power losses, and AVDD power losses.

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:

9.2 Documentation Support

9.2.1 Related Documentation

- Refer to the application note Power Delivery in Cordless Power Tools Using DRV8329
- Texas Instruments, DRV8329AEVM evaluation module
- Refer to the application note System Design Considerations for High-Power Motor Driver Applications
- Refer to the E2E FAQ How to Conduct a BLDC Schematic Review and Debug
- Refer to the application note Best Practices for Board Layout of Motor Drivers
- Refer to the application note QFN and SON PCB Attachment
- Refer to the application note Cut-Off Switch in High-Current Motor-Drive Applications
- Refer to the application note Hardware design considerations for an efficient vacuum cleaner using a BLDC motor
- Refer to the application note Hardware Design Considerations for an Electric Bicycle Using a BLDC Motor
- Refer to the application note Sensored 3-Phase BLDC Motor Control Using MSP430

9.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

9.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.5 Community Resources

9.6 Trademarks

All trademarks are the property of their respective owners.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2023) to Revision A (November 2024)	Page
• Updated device status to Production Data	1

11 Mechanical, Packaging, and Orderable Information

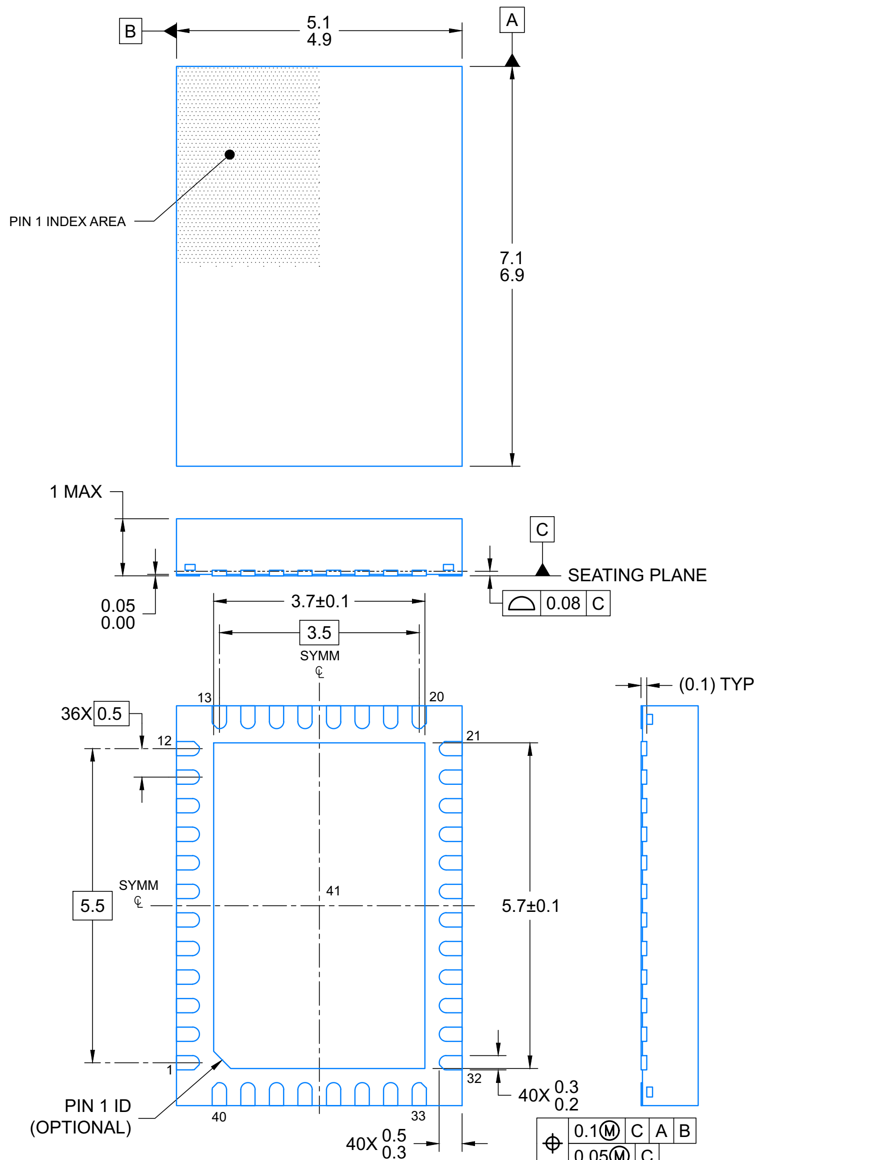
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGE OUTLINE

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

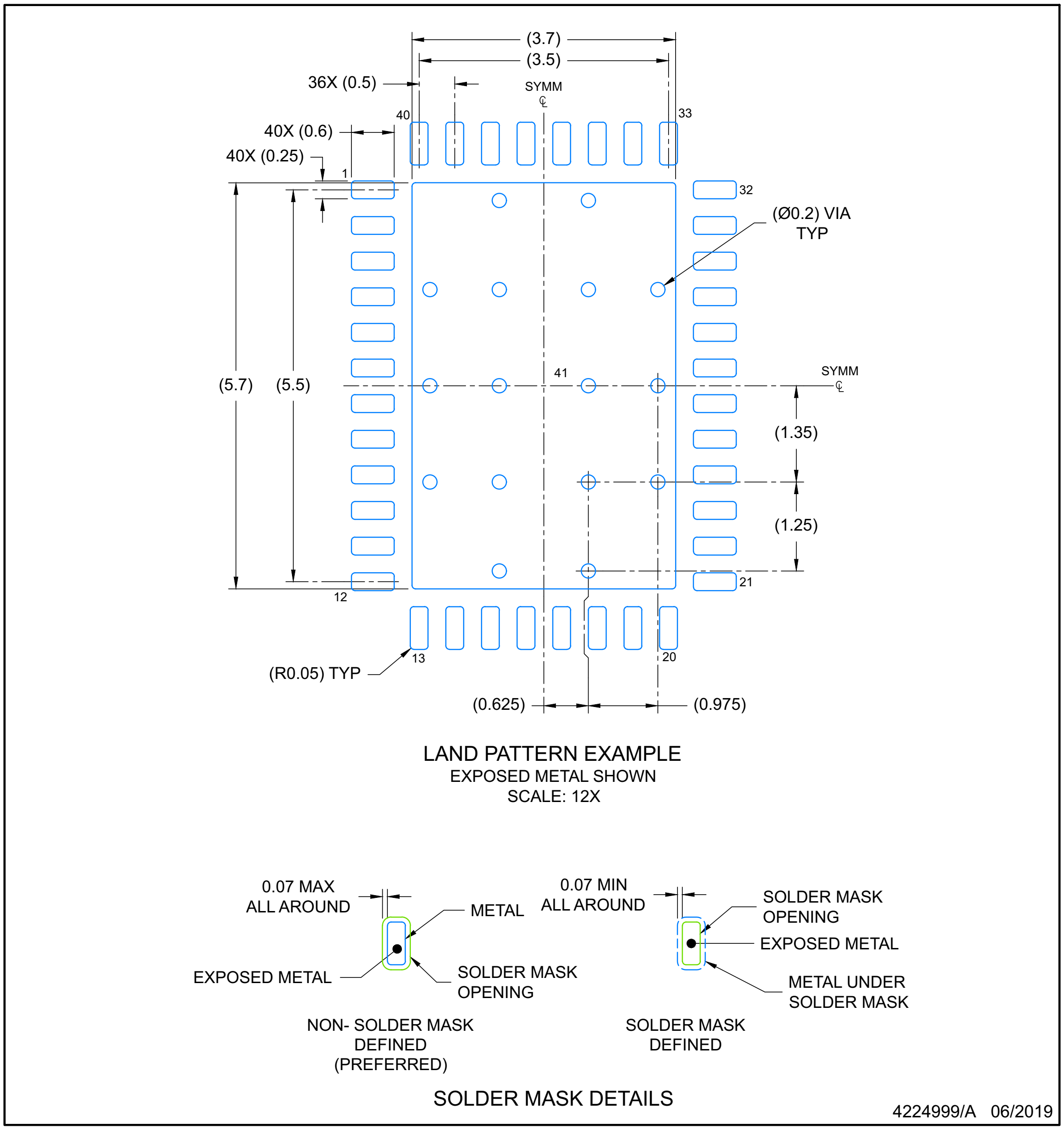
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

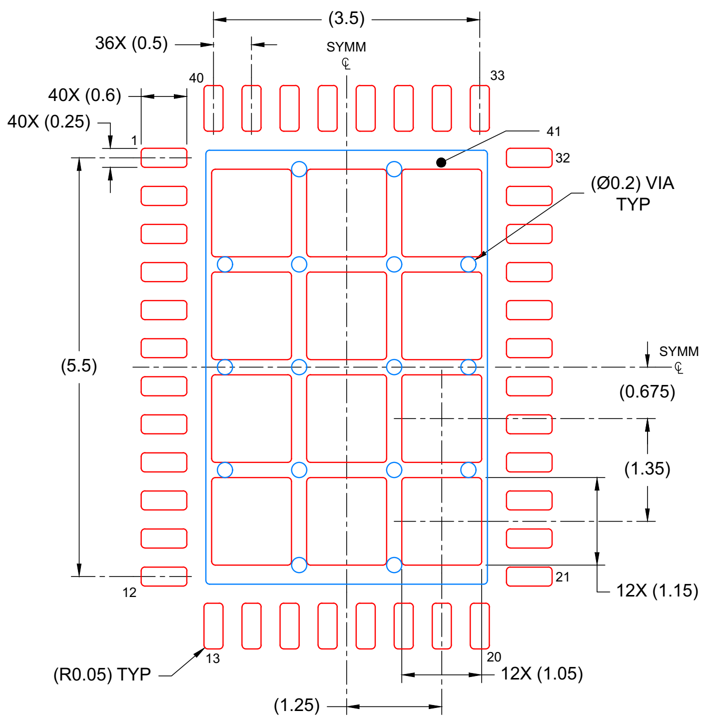
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE STENCIL DESIGN

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4224999/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8329AQRGFRQ1	ACTIVE	VQFN	RGF	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	D8329AQ	Samples
DRV8329BQRGFRQ1	ACTIVE	VQFN	RGF	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	D8329BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

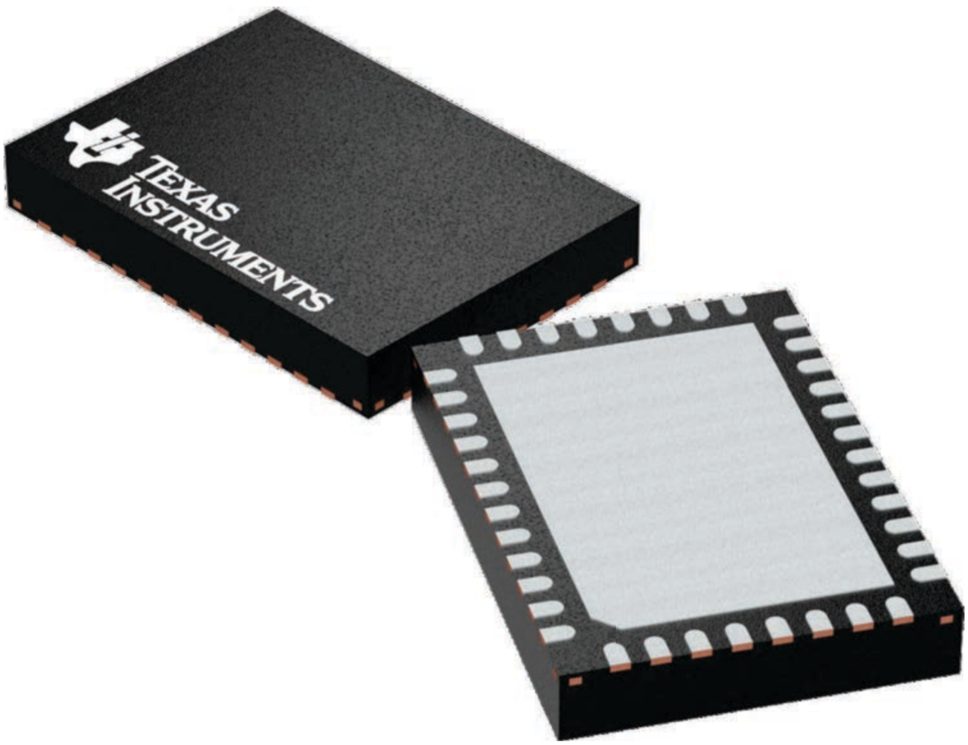
OTHER QUALIFIED VERSIONS OF DRV8329-Q1 :

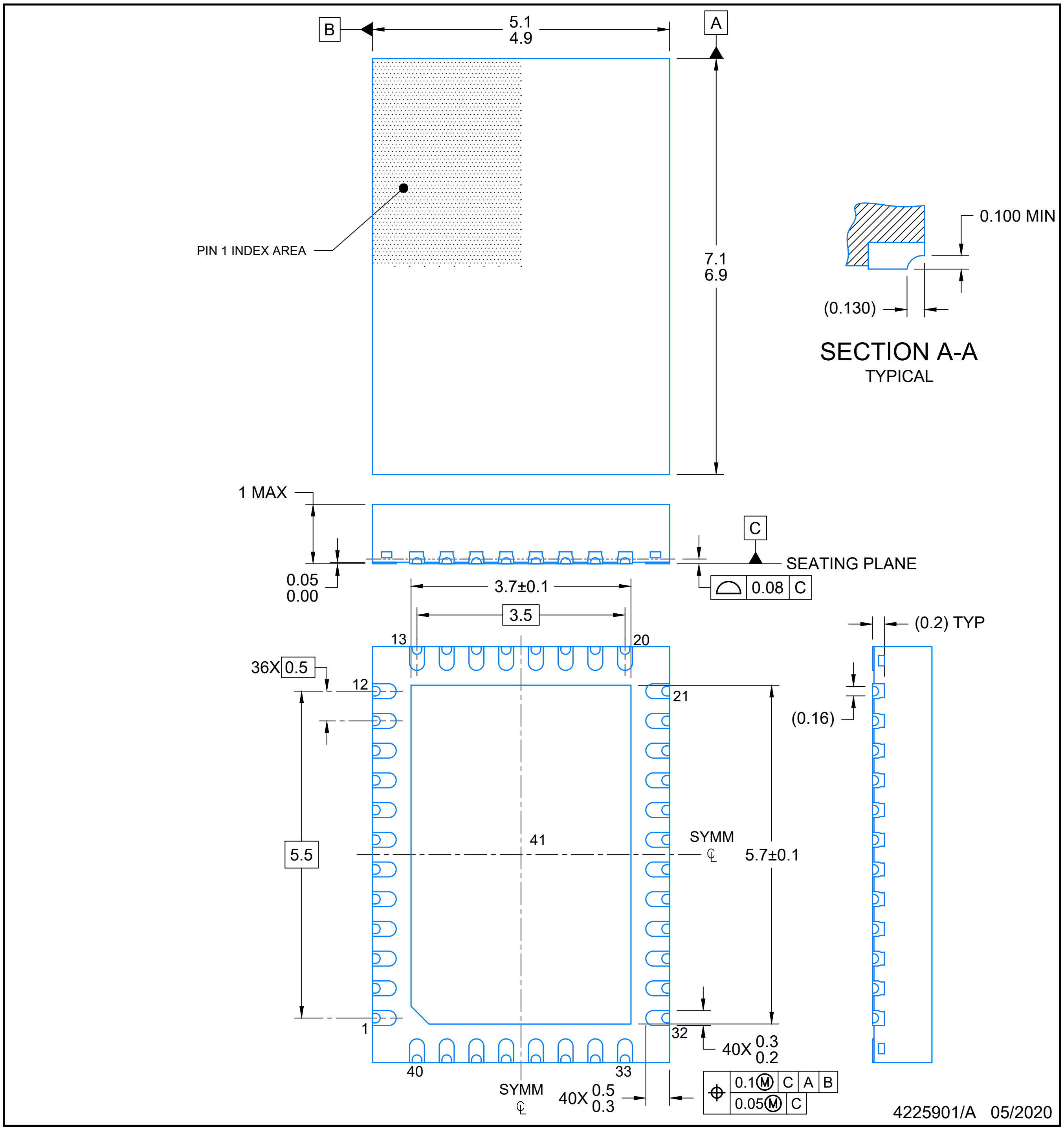
- Catalog : DRV8329

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

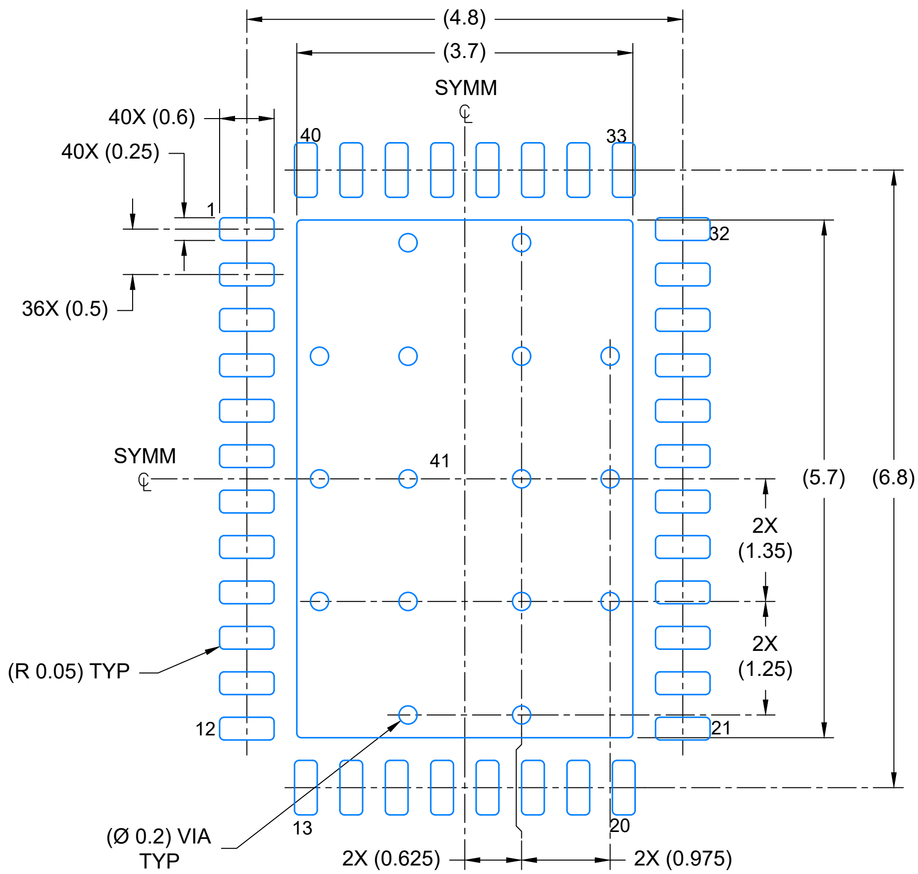
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



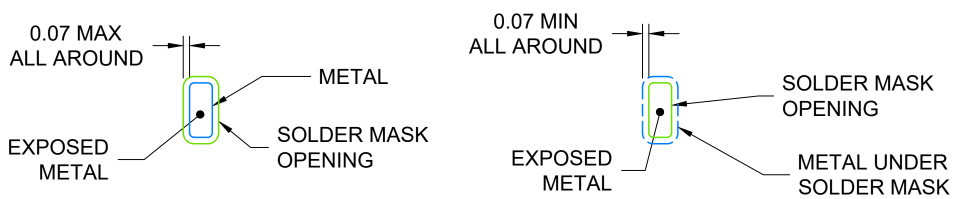


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



NON SOLDER MASK
DEFINED
(PREFERRED)

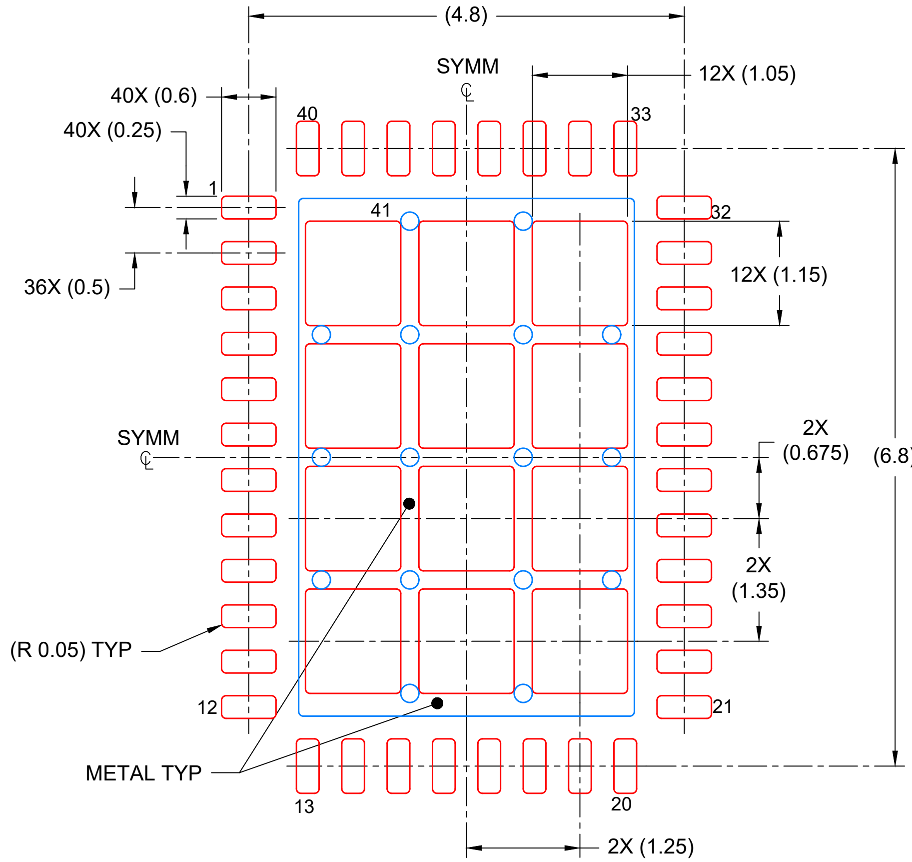
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225901/A 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.