F29H85x and F29P58x Real-Time Microcontrollers

1 Features

Real-time Processing

- Three C29x 64-bit CPUs (CPU1, CPU2, CPU3) running at 200MHz
  - 2x signal chain performance versus C28x with improved pipeline
  - Split lock and lockstep operating modes
- C29x CPU architecture
  - Byte addressability
  - High-performance real-time control with low latency
  - High-performance DSP and general-purpose processing capabilities
  - VLIW CPU executes 1 to 8 instructions in parallel
  - Fully protected pipeline
  - 8/16/32/64-bit single-cycle memory operations, up to two 64-bit memory reads and one 64-bit memory write in a single-cycle
  - IEEE 32-bit and 64-bit floating operations
  - 32-bit and 64-bit trigonometric operations
  - HW interrupt prioritization and nesting
  - 11-cycle real-time interrupt response
  - Atomic operations with memory protection
  - Multi safe island code execution managed in hardware

Memory

- 4MB of CPU-mappable flash (ECC-protected) capable of supporting Firmware Over the Air (FOTA) with A/B swap and LFU
- 256KB of Data-only Flash (ECC-protected)
- 452KB of RAM (ECC-protected)
- Dedicated 512KB Flash and 36KB RAM memories for HSM (ECC-protected)
- Built in ECC logic for system-wide safety

Safety Peripherals

- CPU1 and CPU2 splitlock and lockstep support
- Logic Power-On Self-Test (LPOST)
- Memory Power-On Self-Test (MPOST)
- Error and Signaling Module (ESM)
- Dual-clock Comparator (DCC)
- Waveform Analyzer and Diagnostics (WADI)
- Context-sensitive Memory and Peripheral Protection with SSU
- Safety Interconnect (SIC)
- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 and IEC 61508; system design will be available upon production release
  - Systematic capability up to ASIL D and SIL 3 targeted
  - Hardware capability up to ASIL D and SIL 3 targeted
- Safety-related certification
  - ISO 26262 certification up to ASIL D and IEC 61508 SIL 3 by TÜV SÜD planned

Security

- Hardware Security Module (HSM)
  - Independently running Arm® Cortex®-M4 based security controller subsystem at 100MHz
  - 512KB of flash (ECC-protected)
  - 36KB of RAM (ECC-protected)
  - Secure key storage
  - Secure BOOT
  - Secure Debug
  - Dedicated 8-channel Real-Time Direct Memory Access (RTDMA) controller
  - EVITA-full support
  - FOTA with A/B swap
  - Hardware cryptographic accelerators
    - Asymmetric cryptography - RSA, ECC, SM2
    - Symmetric cryptography - AES, SM4
    - Hash operations - SHA2, HMAC, SM3
    - True Random Number Generator
- Safety and Security Unit (SSU)
  - Advanced Real-Time Safety and Security
    - 64 Memory Access Protection Ranges per CPU
    - Up to 15 user LINKs and 7 stack pointers per CPU for hardware code isolation
    - Power-on Self-test (POST) capability
    - FOTA and LFU support with rollback control

Analog Subsystem

- Five Analog-to-Digital Converters (ADCs)
  - Two 16-bit ADCs, 1.19MSPS each
  - Three 12-bit ADCs, 3.92MSPS each
  - Up to 80 single-ended or 16 differential inputs
  - 40 redundant input channels for flexibility
  - Separate sample-and-hold (S/H) on each ADC for simultaneous sampling
  - Hardware post-processing of conversions
  - Hardware oversampling (up to 128x) and undersampling modes, with accumulation, averaging and outlier rejection

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  - Programmable delay from SOC trigger to start of conversion
  - Automatic comparison of conversion results for functional safety applications
- 12 windowed comparators with 12-bit Digital-to-Analog Converter (DAC) references
  - Connection options for internal temperature sensor and ADC reference
- Two 12-bit buffered DAC outputs

Control Peripherals

- 36 Pulse Width Modulator (PWM) channels, all with high-resolution capability (HRPWM)
  - Minimum Dead-Band Logic (MINDB)
  - Illegal Combo Logic (ICL) for standard and high resolution
  - Diode Emulation (DE) support
  - Multilevel shadowing on XCMP
- Six Enhanced Capture (eCAP) modules
  - High-resolution Capture (HRCAP) available on two of the six eCAP modules
  - Two new monitor units for edge, pulse width and period that can be coupled with ePWM strobes and trip events
  - Increased 256 multiplexed capture inputs
  - New ADC SOC generation capability
- Six Enhanced Quadrature Encoder Pulse (eQEP) modules
- 16 Sigma-Delta Filter Module (SDFM) input channels, 2 independent filters per channel
- Embedded Pattern Generator (EPG)
- Configurable Logic Block (CLB)
  - Six tiles
  - Augments existing peripheral capability
  - Supports position manager solutions

Communications Peripherals

- EtherCAT® SubordinateDevice (or SubDevice) Controller (ESC)
- Fast Serial Interface (FSI) with four transmitters and four receivers
- Five high-speed (up to 50MHz) SPI ports (pin-bootable)
- Six High-Speed Universal Asynchronous Receiver/Transmitters (UARTs) (pin-bootable)
- Two I2C interfaces (pin-bootable)
- Two Local Interconnect Network (LIN) (supports SCI)
- Power-Management Bus (PMBus) interface (supports I2C)
- Six Single Edge Nibble Transmission interface (SENT)
- Six Controller Area Networks with Flexible Data Rate (CAN FD/MCAN) (pin-bootable)

Systems Peripherals

- External Memory Interface (EMIF) with ASRAM and SDRAM support
- Two 10-channel Real-Time Direct Memory Access (RTDMA) controllers with MPU
- Up to 190 usable signal pins
  - 136 General-Purpose Input/Output (GPIO) pins
  - 80 analog pins (26 AGPIOs included in GPIOs)
- Peripheral Interrupt Priority and Expansion (PIPE)
- Low-power mode (LPM) support
- Embedded Real-time Analysis and Diagnostic (ERAD)

Clock and System Control

- On-chip crystal oscillator
- Windowed watchdog timer module
- Missing clock detection circuitry
- 1.2V core, 3.3V I/O design
  - Internal VREG for 1.2V generation
  - Brownout reset (BOR) circuit

Package Options:

- Lead-free, green packaging
- 256-ball New Fine Pitch Ball Grid Array (nFBGA) [ZEX suffix], 13mm x 13mm/0.8mm pitch
- 176-pin Thermally Enhanced Thin Quad Flatpack (HTQFP) [PTS suffix], 22mm x 22mm/0.4mm pitch
- 144-pin HTQFP [RFS suffix], 18mm x 18mm/0.4mm pitch
- 100-pin HTQFP [PZS suffix], 14mm x 14mm/0.4mm pitch

Temperature

- Ambient (T_A): –40°C to 125°C

2 Applications

- On-board charger (OBC) with or without Host Integration
- HEV/EV DC/DC converter
- Electric power steering (EPS)
- Traction Inverter
- Medium/short range radar
- HVAC large commercial motor control
- Automated sorting equipment
- CNC control
- Central inverter
- String inverter
- Inverter & motor control
- Linear motor segment controller
- Servo drive control module
- Industrial AC-DC
- Three phase UPS
- Merchant network and server PSU

3 Description

The F29H85x and F29P58x are members of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- Electrical vehicles and transportation
- Motor control
  - Traction inverter motor control
  - HVAC motor control
  - Mobile robot motor control
- Solar inverters
  - Central inverter
  - Micro inverter
  - String inverter
- Digital power
- Industrial motor drives
- EV charging infrastructure

The real-time control subsystem has up to three 200MHz C29x DSP cores. The C29x supports 32-bit and 64-bit floating- and fixed-point signal-processing running from on-chip flash or RAM. The C29x CPU is boosted by trigonometric math instructions, speeding up common algorithms key to real-time control systems.

Many features are included to support a system-level ASIL-D functional safety solution. The C29x CPU1 and CPU2 cores can be put in lockstep for detection of permanent and transient faults. Logic Power-On Self-Test (LPOST) and Memory Power-On Self-Test (MPOST) provide start-up detection of latent faults. Safe interconnects provide fault detection between the CPU and the peripherals. The ADC safety checker compares ADC conversion results from multiple ADC modules without additional CPU cycles. The Waveform Analyzer and Diagnostic (WADI) can monitor multiple signals for proper operation and take action to ensure a safe state is maintained. The device architecture features a Safe Interconnect (SIC) for end-to-end code and data safety, with CPU-based ECC protection for all memories and peripheral endpoints.

Hardware Security Manager (HSM) provides EVITA-full security support. Features include Secure Boot, secure storage and keyring support, secure debug authentication, and cryptographic accelerator engines. The HSM enables secure key and code provisioning in untrusted factory environments, and supports Firmware-Over-The-Air updates of HSM and host application firmware, with A/B swap capability and rollback control.

SSU (Safety and Security unit) enables superior run-time safety and security features. This feature can be used create safety isolation (Freedom From Interference) among the threads running on same CPU or different CPUs. The SSU features a context-sensitive MPU mechanism that automatically switches access permissions in hardware based on currently executing thread or task. This eliminates software overhead, enabling real-time code performance without compromising system safety. The SSU provides multi-user debug authentication, and also supports Live Firmware Update (LFU) and FOTA fpr application firmware updates with A/B swap and rollback control.

High-performance analog blocks are tightly integrated with the processing and control units to provide optimal real-time signal chain performance. Two 16-bit Analog-to-Digital Converters (ADC) and three 12-bit ADCs have up to 80 analog channels as well as an integrated post-processing block and hardware oversampling. Two 12-bit buffered DACs and twenty-four comparator channels are available.

Thirty-six frequency-independent PWMs, all with high-resolution capability, enable control of multiple power stages, from 3-phase inverters to advanced multilevel power topologies. The PWMs have been enhanced with Minimum Dead-Band Logic (MINDL), Diode Emulation (DE), and Illegal Combo Logic (ICL) features.

The Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

An EtherCAT SubDevice Controller, Ethernet MAC, and other industry-standard protocols like CAN FD are available on this device. The Fast Serial Interface (FSI) enables up to 200Mbps of robust communications across an isolation boundary.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000 real-time microcontrollers page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the F29H85X-SOM-EVM evaluation board, and download the MCU-SDK-F29H85x software development kit.

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Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)	PITCH
F29H85xTxx	ZEX (nFBGA, 256)	13mm × 13mm	13mm × 13mm	0.8mm
	PTS (HTQFP, 176)	22mm × 22mm	20mm × 20mm	0.4mm
	RFS (HTQFP, 144)	18mm × 18mm	16mm × 16mm	0.4mm
	PZS (HTQFP, 100)	14mm × 14mm	12mm × 12mm	0.4mm
F29H85xDxx	ZEX (nFBGA, 256)	13mm × 13mm	13mm × 13mm	0.8mm
	PTS (HTQFP, 176)	22mm × 22mm	20mm × 20mm	0.4mm
	RFS (HTQFP, 144)	18mm × 18mm	16mm × 16mm	0.4mm
	PZS (HTQFP, 100)	14mm × 14mm	12mm × 12mm	0.4mm
F29P58xDxx	ZEX (nFBGA, 256)	13mm × 13mm	13mm × 13mm	0.8mm
	PTS (HTQFP, 176)	22mm × 22mm	20mm × 20mm	0.4mm
	RFS (HTQFP, 144)	18mm × 18mm	16mm × 16mm	0.4mm
	PZS (HTQFP, 100)	14mm × 14mm	12mm × 12mm	0.4mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER(1)	CPU	FREQUENCY	FLASH	ADC	EMIF ETHERCAT
F29H85xTU9	CPU1 CPU2 CPU3	200MHz	4MB	2 – 16-bit/12-bit 3 – 12-bit	Yes
F29H85xTU8					–
F29H85xTM8			2MB		–
F29H85xDU7	CPU1 CPU3	200MHz	4MB	2 – 16-bit/12-bit 3 – 12-bit	Yes
F29H85xDU6					–
F29H85xDM7			2MB		Yes
F29H85xDM6					–
F29P58xDU5	CPU1 CPU2	200MHz	4MB	2 – 16-bit/12-bit 3 – 12-bit	–
F29P58xDM5			2MB		–

(1) For more information on these devices, see the *Device Comparison* table.

3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

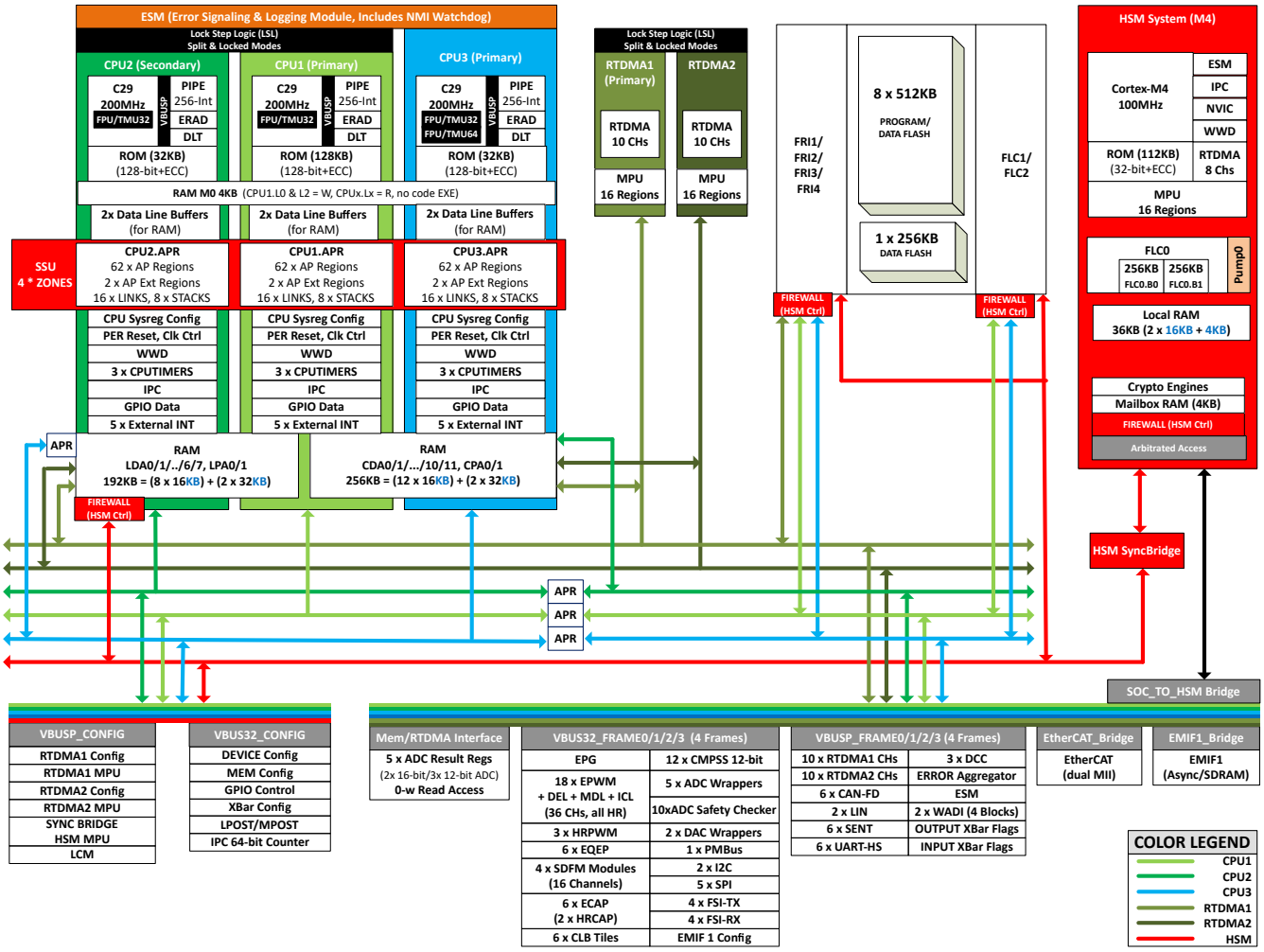

Figure 3-1. Functional Block Diagram

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Device Comparison

Table 4-1. Device Comparison

FEATURE[1]		F29H85xTxx			F29H85xDxx				F29P58xDxx	
		850TU9	859TU8	859TM8	850DU7	859DU6	850DM7	859DM6	589DU5	580DM5 589DM5
C29x CPU Subsystem										
C29x – CPU1	32-bit Floating Point and Trig Instructions	200MHz								
C29x – CPU2	32-bit Floating Point and Trig Instructions	200MHz			–				200MHz	
C29x – CPU3	64-bit Floating Point and Trig Instructions	200MHz							–	
Lockstep capable (CPU1 can lockstep with CPU2)		Yes			–				Yes	
RAM (ECC)	M0 (Shared CPU1 / CPU2 / CPU3)	4KB							4KB	
	LPAx (Program optimized CPU1 / CPU2)	64KB							64KB	
	LDAx (Data optimized CPU1 / CPU2, shared with HSM)	128KB							128KB	
	CPAx (Program optimized CPU1 / CPU3)	64KB							64KB	
	CDAx (Data optimized CPU1 / CPU3)	192KB							–	
	Total	452KB							260KB	
Flash (ECC)	C29x – CPU1 / CPU3	4MB		2MB	4MB		2MB		4MB	2MB
	Data Bank (Supports Software EEPROM Emulation)	256KB								
	Firmware Over the Air (FOTA) support	Yes								
	Live Firmware Update (LFU) support	Yes								
C29x System										
Data-log and Trace (DLT) – Type 0		1 per CPU								
Embedded Pattern Generator (EPG)		Yes								
Enhanced Real-time Analysis and Diagnostic (ERAD) – Type 5		1 per CPU								
External Memory Interface (EMIF)[2]		1	–	–	1	–	1	–	–	
Real-Time DMA (RTDMA) – 10 Channels Each		2 (Lockstep capable)								
Waveform Analysis and Diagnostic IP (WADI)		2 Instances with 4 blocks								
CPU timers		3 per CPU								
Windowed Watchdog Timer (WWD)		1 per CPU								
Dual-clock Comparator (DCC)		3								
Safety and Security										
Functional Safety Capability		ASIL D/SIL 3 (targeted)			ASIL B/SIL 2 (targeted)				ASIL D/SIL 3 (targeted)[3]	
Error Signaling Module (ESM)		Yes								
Hardware Security Module (HSM) with EVITA-full		Yes [see the *Hardware Security Module (HSM)* section]								
JTAG Lock		Yes								
Logic Power-on Self-test (LPOST)		Yes								
Memory Power-on Self-test (MPOST)		Yes								
Safety and Security (SSU) module		Yes								
SSU Access Protection Regions (APR)		64 per CPU								
Hardware Security Manager (HSM) Subsystem										
Cortex-M4		100 MHz								
Nested Vectored Interrupt Controller (NVIC)		64 Interrupts								
HSM Real-Time DMA (RTDMA) – 8 Channels		1								
HSM Error Signaling Module (HSM-ESM)		Yes								
Dual-clock Comparator (DCC)		1								
Dual Mode Timer (DMTimer)		2								
Real-time Clock (RTC) Counter		1								
Real-time Interrupt (RTI) Timer		1								
Secure Boot		Yes								
HSM Windowed Watchdog Timer		1								
Security Manager		Yes								
Flash	HSM	512KB								
	Firmware Over the Air (FOTA) support	Yes								

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 4-1. Device Comparison (continued)

FEATURE[1]		F29H85xTxx			F29H85xDxx				F29P58xDxx	
		850TU9	859TU8	859TM8	850DU7	859DU6	850DM7	859DM6	589DU5	580DM5 589DM5
RAM	Local	36KB								
	LDAx (Shared with C29x)	128KB								
	Mailbox	4KB								
Cryptographic Accelerators (Mappable to HSM or C29x)										
True Random Number Generator (TRNG)		Yes								
Deterministic Random Bit Generator (DRBG)		Yes								
CRC Engine		Yes								
Symmetric Cryptography	Advance Encryption Standard (AES)	Yes								
	SM4	Yes								
Asymmetric Cryptography	Public Key Accelerator (PKA): ECC, RSA	Yes								
	SM2	Yes								
Hashing Function	Hash-based Message Authentication Codes (HMAC)	Yes								
	Secure Hash Algorithm (SHA)	Yes								
	MD5	Yes								
	SM3	Yes								
GPIO Pins, Analog Pins, and Power Supply										
Internal 3.3-V to 1.2-V Voltage Regulator		–							100-pin (100MHz) only[4]	
Digital GPIO	256-ball ZEX BGA	110								
	176-pin PTS HTQFP	86								
	144-pin RFS HTQFP	65								
	100-pin PZS HTQFP	–	46		–	46	–	46		
Analog or Digital Bi-directional (AGPIO)	256-ball ZEX BGA	26								
	176-pin PTS HTQFP	26								
	144-pin RFS HTQFP	16								
	100-pin PZS HTQFP	–	8		–	8	–	8		
Analog or Digital Input (AIO)	256-ball ZEX BGA	54								
	176-pin PTS HTQFP	28								
	144-pin RFS HTQFP	28								
	100-pin PZS HTQFP	–	16		–	16	–	16		
Total Signal pins (GPIO, AGPIO and AIO)	256-ball ZEX BGA	190								
	176-pin PTS HTQFP	140								
	144-pin RFS HTQFP	109								
	100-pin PZS HTQFP	–	70		–	70	–	70		
Analog Peripherals										
ADC 16-/12-bit Modules ADC AB – Type 5	Number	2							2	
	16-bit mode Throughput	1.19 MSPS								
	16-bit mode Conversion Time[5]	840 ns								
	12-bit mode Throughput	3.92 MSPS								
	12-bit mode Conversion Time[5]	255 ns								
ADC 12-bit Modules ADC CDE – Type 5	Number	3								
	Throughput	3.92 MSPS								
	Conversion Time[5]	255 ns								
ADC channels (16-bit single-ended mode) Modules ADC AB	256-ball ZEX BGA	32								
	176-pin PTS HTQFP	26								
	144-pin RFS HTQFP	21								
	100-pin PZS HTQFP	–	12		–	12	–	12		
ADC channels (differential mode) Modules ADC AB	256-ball ZEX BGA	16								
	176-pin PTS HTQFP	13								
	144-pin RFS HTQFP	10								
	100-pin PZS HTQFP	–	6		–	6	–	6		

Table 4-1. Device Comparison (continued)

FEATURE[1]		F29H85xTxx			F29H85xDxx				F29P58xDxx	
		850TU9	859TU8	859TM8	850DU7	859DU6	850DM7	859DM6	589DU5	580DM5 589DM5
ADC channels (12-bit single-ended mode) All ADC modules	256-ball ZEX BGA	80								
	176-pin PTS HTQFP	54								
	144-pin RFS HTQFP	44								
	100-pin PZS HTQFP	–	24		–	24	–	24		
Temperature sensor		2								
Buffered DAC – Type 1		2							2	
CMPSS (two comparators and two internal DACs) – Type 6		12							12	
Control Peripherals										
Configurable Logic Block (CLB) – Type 3		6 Tiles							4 Tiles	
ePWM – Type 5	Total Channels	36							24	
	HRPWM Capable	36							24	
eCAP – Type 3	Total Modules	6							6	
	HRCAP Capable	2 (eCAP5, eCAP6)							–	
eQEP modules – Type 2		6							4	
Sigma-Delta Filter Module (SDFM) Channels – Type 2		16 Channels (4 SDFM modules)							16 Channels (4 SDFM modules)	
Communication Peripherals										
CAN with Flexible Data-Rate (CAN FD) – Type 2		6							4	
Ethernet for Control Automation Technology (EtherCAT)[2]		1	–	–	1	–	1	–	–	
Fast Serial Interface (FSI) RX – Type 2		4							3	
Fast Serial Interface (FSI) TX – Type 2		4							3	
Inter-Integrated Circuit (I2C) – Type 2		2								
LIN – Type 1 (UART-Compatible)		2							2	
Power Management Bus (PMBus) 1.1 – Type 0		1								
High Speed UART (HS-UART) – Type 1		6							4	
Single Edge Nibble Transmission (SENT) – Type 1		6								
SPI – Type 2		5								
Package Options, Temperature, and Qualification										
Maximum Junction temperature (T_J)	859xxx, 589xxx – all packages 850xxx, 580xxx – PTS, RFS, PZS packages	150°C	150°C	150°C	150°C	150°C	150°C	150°C	150°C	150°C
	850xxx, 580xxx – ZEX package	125°C	–	–	125°C	–	125°C	–	–	125°C
Maximum Free-Air temperature (T_A)	859xxx, 589xxx – all packages 850xxx, 580xxx – PTS, RFS, PZS packages	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C
	850xxx, 580xxx – ZEX package	105°C	–	–	105°C	–	105°C	–	–	105°C
Minimum temperature (T_J and T_A)		–40°C								
Package Options	256-ball ZEX BGA	850TU9	859TU8	859TM8	850DU7	859DU6	850DM7	859DM6	589DU5	580DM5 589DM5
	176-pin PTS HTQFP	850TU9	859TU8	859TM8	850DU7	859DU6	850DM7	859DM6	589DU5	580DM5 589DM5
	144-pin RFS HTQFP	850TU9	859TU8	859TM8	850DU7	859DU6	850DM7	859DM6	589DU5	580DM5 589DM5
	100-pin PZS HTQFP	–	859TU8	859TM8	–	859DU6	–	859DM6	589DU5	580DM5 589DM5

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the *C2000 Real-Time Microcontrollers Peripherals Reference Guide*.
(2) In the 144-pin package, EMIF and EtherCAT cannot be used concurrently.
(3) Supported only with external VREG.
(4) VREG is supported only on 100-pin devices, but the CPU has to run at 100MHz with no LPOST execution due to current limitations.
(5) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.

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4.1 Related Products

TMS320F2837xD Real-Time Dual-Core Microcontrollers

The F2837xD series sets a standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU accelerators. Capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

TMS320F2837xS Real-Time Microcontrollers

The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the TMS320F2807x series.

TMS320F2838x Real-Time Microcontrollers

The F2838x series offers more performance, larger pin counts, flash memory sizes, peripheral and wide variety of connectivity options. The F2838x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

TMS320F28P65x Real-Time Microcontrollers

The F28P65x series is built for efficient control of power electronics. The family of devices includes more ADC channels for further integration and hardware ADC oversampling to save CPU bandwidth. It's new EPWM type has 36 high resolution PWMs with enhanced flexibility to enable new power topologies like multiphase and multilevel power architectures. Other capabilities include up to 1.28MB of flash, 11 windowed comparators with dual-ramp generators, lockstep capability and a CLA module running at 200MHz. The F28P65x family of devices has 100-pin QFP, 169-pin BGA, 176-pin QFP and 256-pin BGA package variants.

5 Pin Configuration and Functions

5.1 Pin Diagrams

Figure 5-1 shows the ball assignments on the 256-ball ZEX New Fine Pitch Ball Grid Array (nFBGA). Figure 5-2 to Figure 5-5 show the ball assignments on the 256-ball ZEX nFBGA in quadrants.

Figure 5-6 shows the pin assignments on the 176-pin PTS Thermally Enhanced Thin Quad Flatpack.

Figure 5-7 shows the pin assignments on the 144-pin RFS Thermally Enhanced Thin Quad Flatpack.

Figure 5-8 shows the pin assignments on the 100-pin PZS Thermally Enhanced Thin Quad Flatpack.

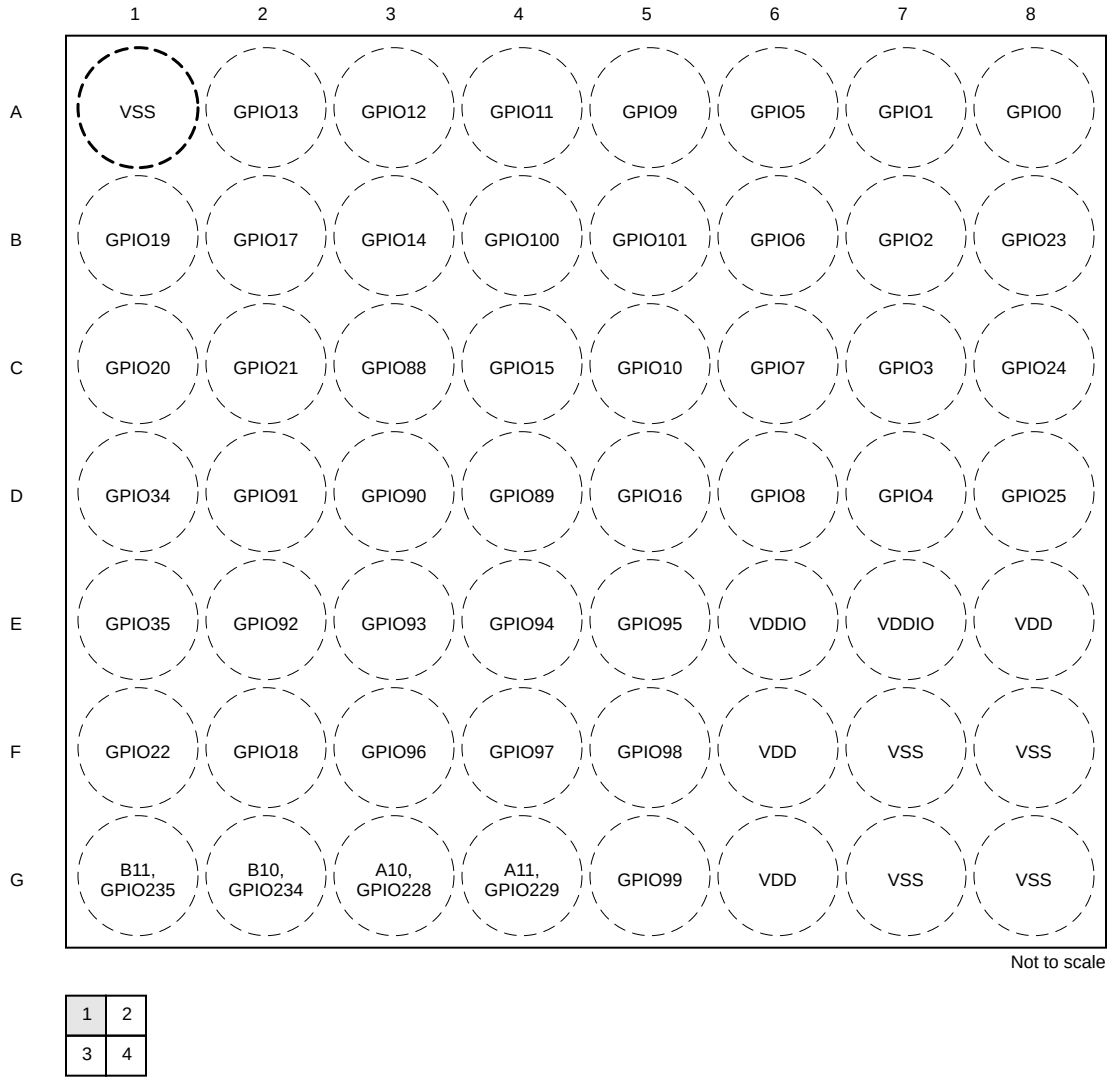
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	GPIO13	GPIO12	GPIO11	GPIO9	GPIO5	GPIO1	GPIO0	GPIO29	GPIO30	GPIO83	GPIO81	GPIO77	GPIO72	GPIO69	VSS
B	GPIO19	GPIO17	GPIO14	GPIO100	GPIO101	GPIO6	GPIO2	GPIO23	GPIO26	GPIO31	GPIO85	GPIO80	GPIO76	GPIO71	GPIO68	GPIO67
C	GPIO20	GPIO21	GPIO88	GPIO15	GPIO10	GPIO7	GPIO3	GPIO24	GPIO27	GPIO87	GPIO86	GPIO79	GPIO75	GPIO70	GPIO43	GPIO42
D	GPIO34	GPIO91	GPIO90	GPIO89	GPIO16	GPIO8	GPIO4	GPIO25	GPIO28	GPIO82	GPIO84	GPIO78	GPIO74	GPIO46	GPIO47	GPIO103
E	GPIO35	GPIO92	GPIO93	GPIO94	GPIO95	VDDIO	VDDIO	VDD	VDD	VDDIO	VDDIO	VDD	GPIO73	GPIO38	VSSOSC	GPIO220, X1
F	GPIO22	GPIO18	GPIO96	GPIO97	GPIO98	VDD	VSS	VSS	VSS	VSS	VSS	VDD	GPIO127	XRSn	VDDIO	GPIO221, X2
G	B11, GPIO235	B10, GPIO234	A10, GPIO228	A11, GPIO229	GPIO99	VDD	VSS	VSS	VSS	VSS	VSS	VDDIO	GPIO66	GPIO44	GPIO45	GPIO32
H	B9, GPIO233	B8, GPIO232	A9, GPIO227	A8, GPIO226	B7/E27, GPIO231	VDDIO	VSS	VSS	VSS	VSS	VSS	VDDIO	GPIO62	GPIO63	GPIO64	GPIO65
J	B13	B12	B17	B16	B6/E26, GPIO230	VDDIO	VSS	VSS	VSS	VSS	VSS	VDDIO	GPIO61	GPIO105	GPIO60	GPIO59
K	A13	A12	B5/D31	B4/D30	A7/E25, GPIO225	VDDA	VSSA	VSS	VSS	VSS	VSS	VDDIO	GPIO55	GPIO56	GPIO57	GPIO58
L	A5/D29	A4/D28	B3/D27	B2/D26	A6/E24, GPIO224	VDDA	VSSA	VDDIO	VDDIO	VDDIO	VDD	VDD	VDDIO	GPIO52	GPIO53	GPIO54
M	A2/D24	A3/D25	A14/B14 /C14/D14 /E14	A15/B15 /C15/D15 /E15	C3/E31	D13	D12	C6, GPIO236	C7, GPIO237	VDDIO	VDDIO	FLT3	GPIO51	GPIO50	GPIO49	GPIO219 /ERRORSTS
N	VREFLOAB	VREFHIAB	B1/C27	C2/E30	C5	D10	C16	C10	E13	D4/B28, GPIO240	D5/B29, GPIO241	C8, GPIO238	E7/A31, GPIO249	GPIO36	GPIO41	GPIO48
P	A1/C25	B0/C26 /VDAC	E0/A24 /DACB_OUT	E1/A25	C4	D11	C17	C11	E12	E16	E4/A28, GPIO246	C9, GPIO239	E6/A30, GPIO248	GPIO33	GPIO39	GPIO40
R	A0/C24 /DACA_OUT	C0/E28	D0/B24	VREFHICDE	D2/B26	D3/B27	D16	C12	E11	E10	E5/A29, GPIO247	D7/B31, GPIO243	D8/C28, GPIO244	GPIO223 /TDO	TCK	GPIO37
T	VSSA	C1/E29	D1/B25	VREFLOCDE	E2/A26	E3/A27	D17	C13	E9/C31	E8/C30	E17	D6/B30, GPIO242	D9/C29, GPIO245	GPIO222 /TDI	TMS	VSS

Not to scale

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

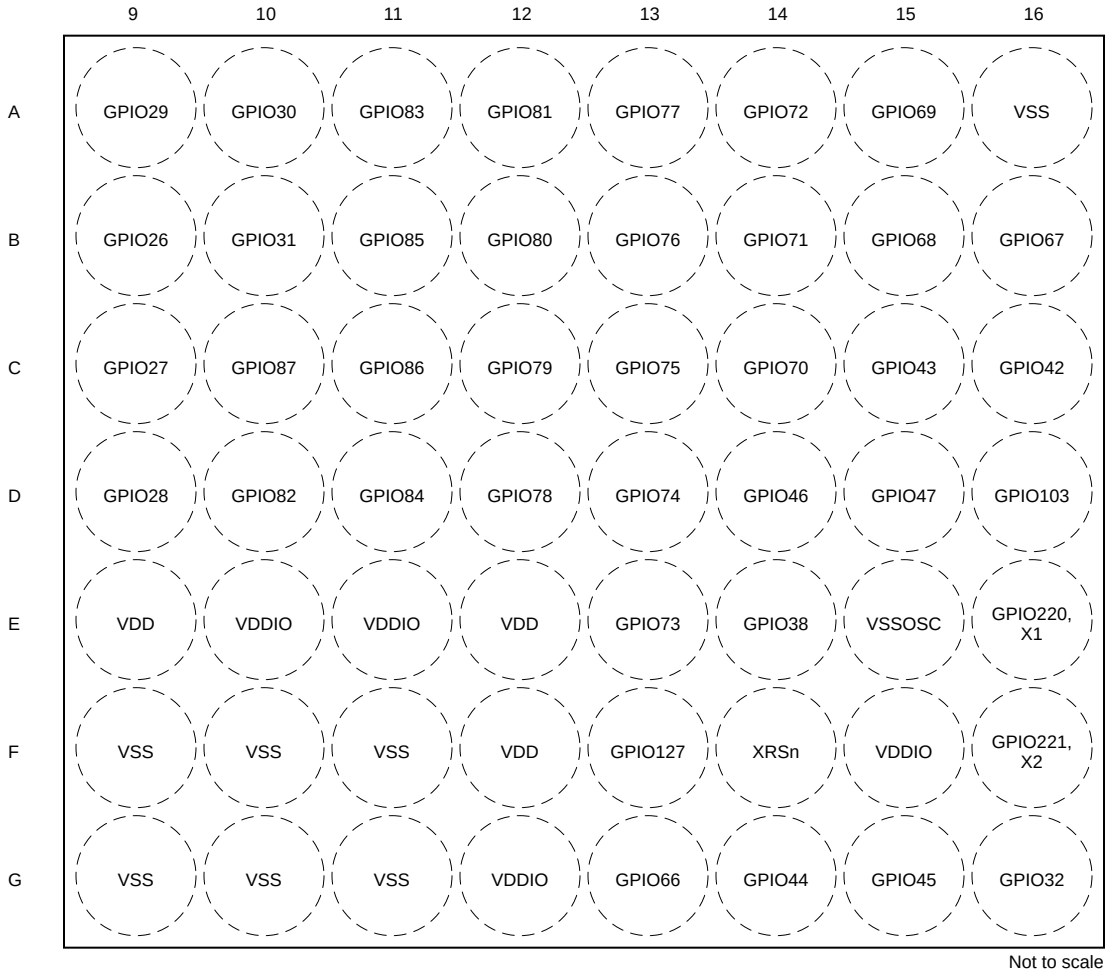
Figure 5-1. 256-Ball ZEX New Fine Pitch Ball Grid Array (Bottom View)

ADVANCE INFORMATION



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

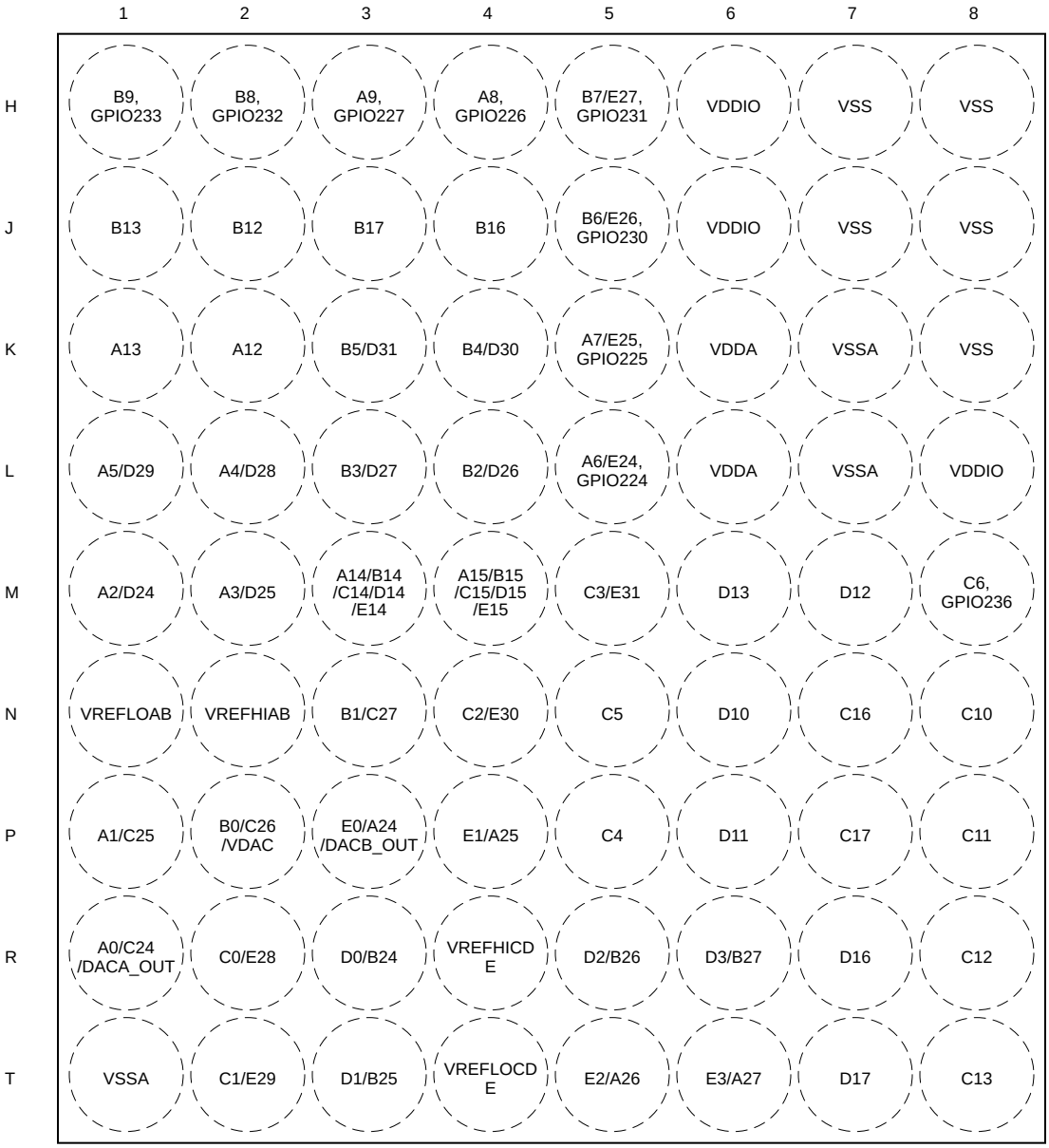
Figure 5-2. 256-Ball ZEX New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 1]



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

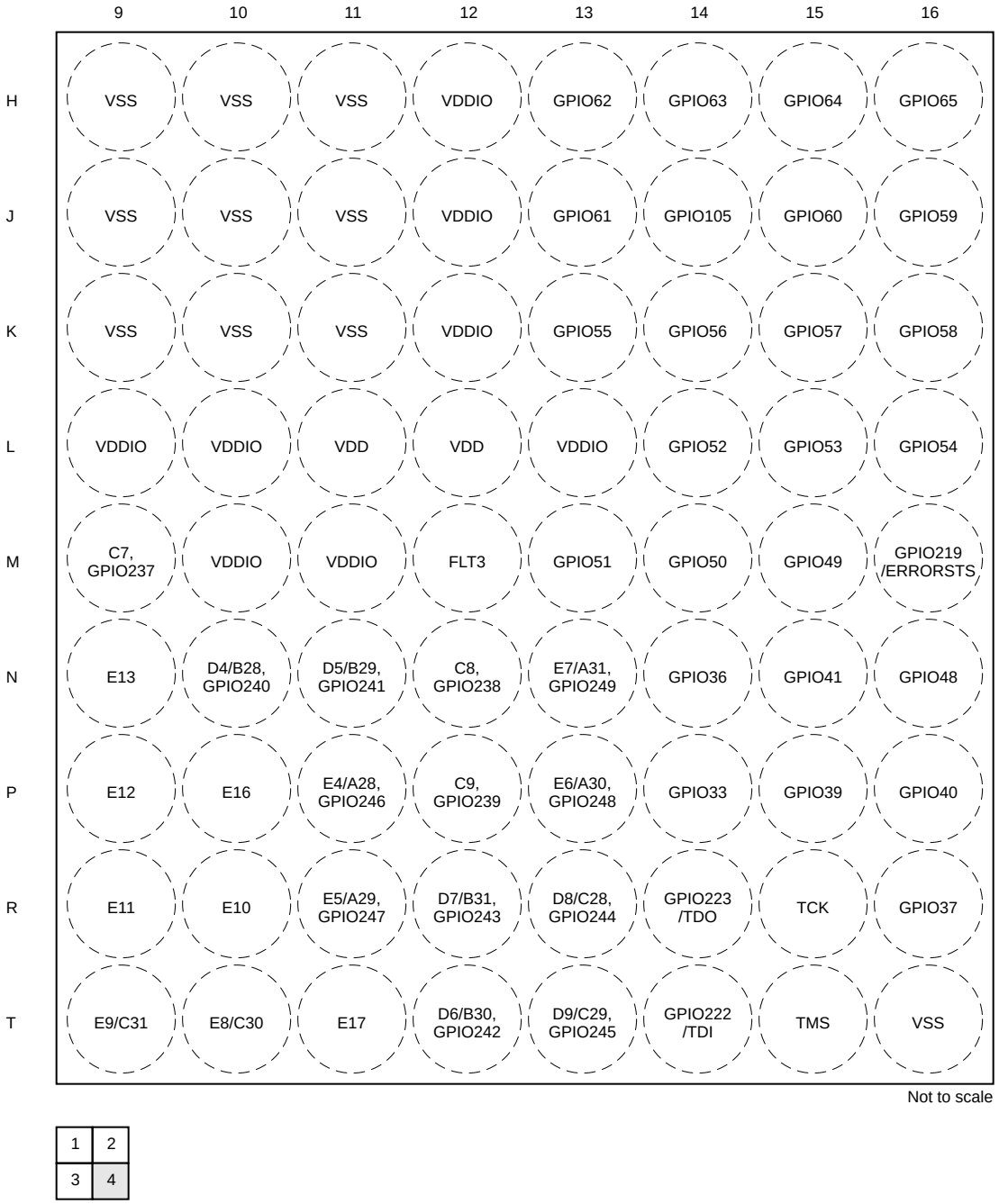
Figure 5-3. 256-Ball ZEX New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 2]

ADVANCE INFORMATION



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

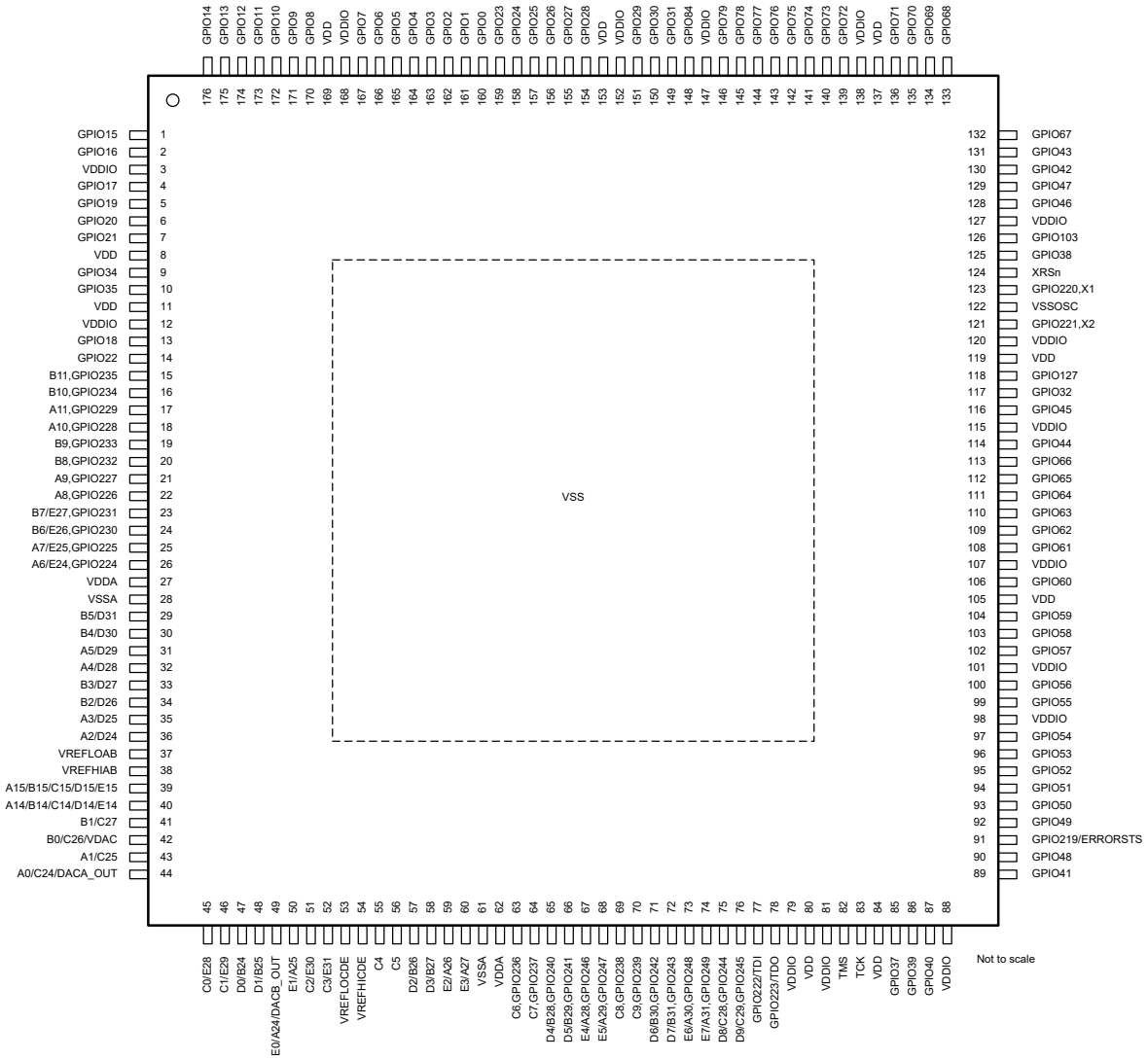
Figure 5-4. 256-Ball ZEX New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 3]



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

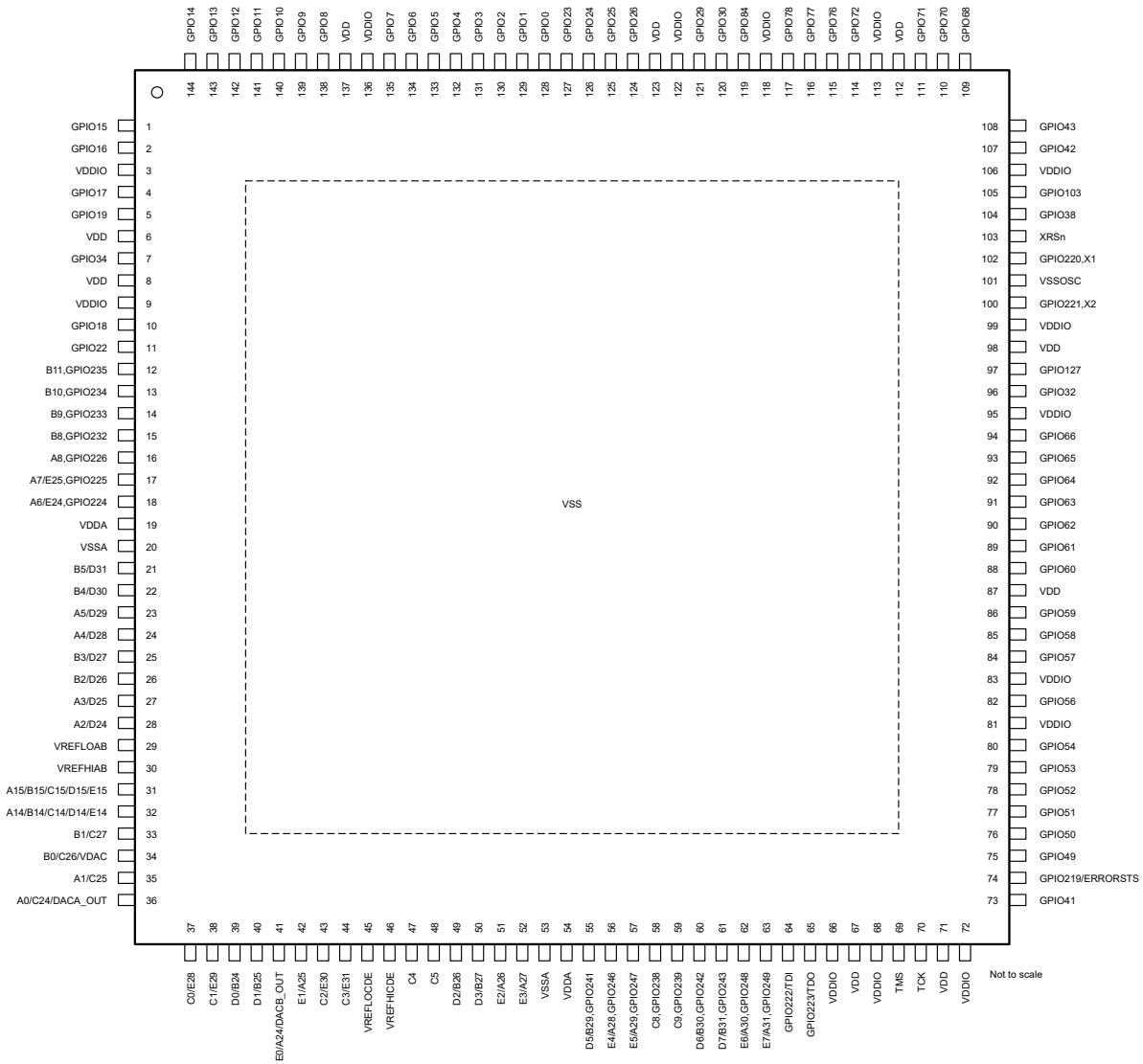
Figure 5-5. 256-Ball ZEX New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 4]

ADVANCE INFORMATION



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

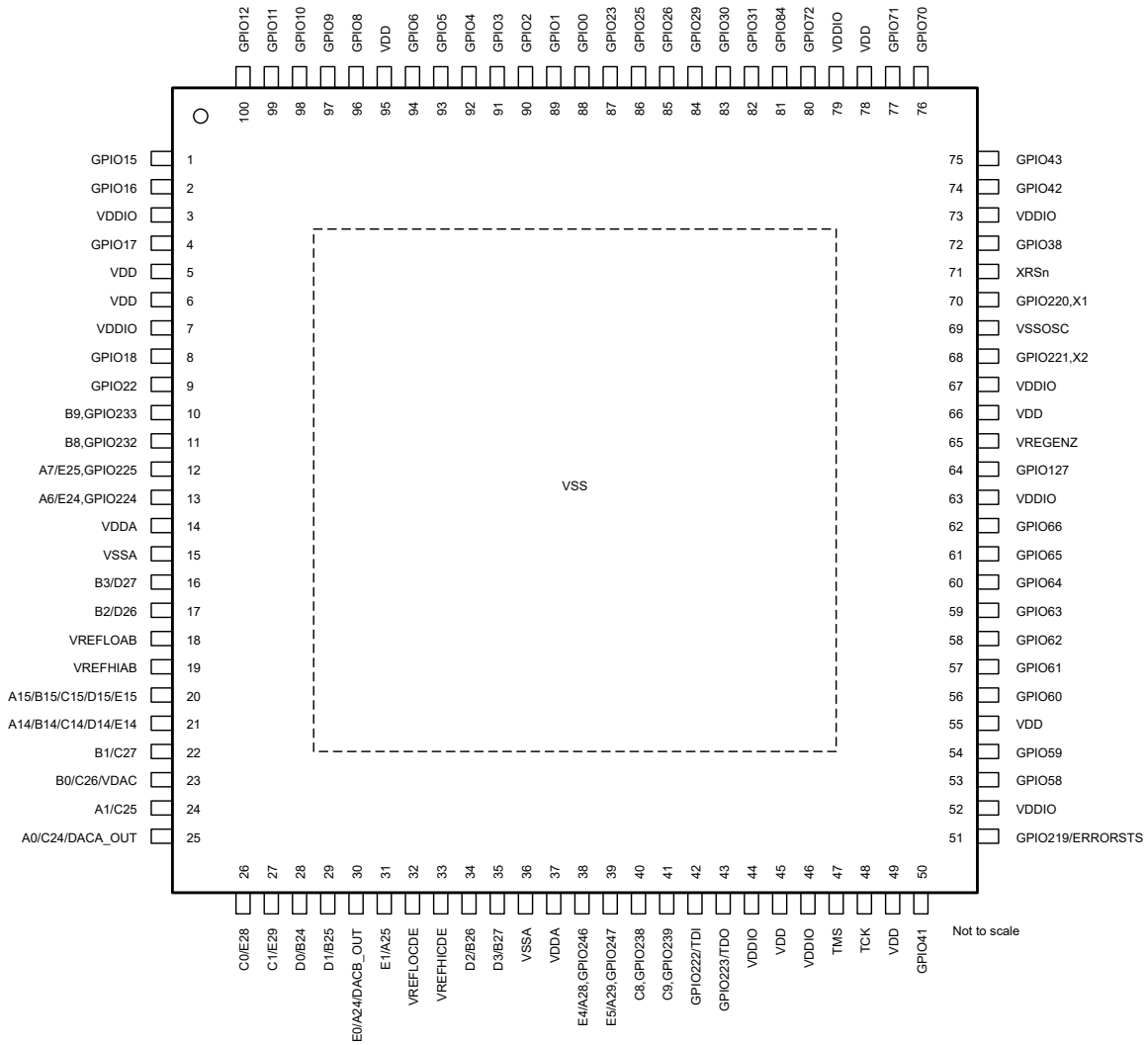
Figure 5-6. 176-Pin PTS Thermally Enhanced Thin Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-7. 144-Pin RFS Thermally Enhanced Thin Quad Flatpack (Top View)

ADVANCE INFORMATION



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-8. 100-Pin PZS Thermally Enhanced Thin Quad Flatpack (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
ANALOG							
A0						I	ADC-A Input 0
C24						I	ADC-C Input 24
DACA_OUT		R1	44	36	25	O	Buffered DAC-A Output.
AIO160	0, 4, 8, 12					I	Analog Pin Used For Digital Input 160 This pin also has digital mux functions which are described in the GPIO section of this table.
A1						I	ADC-A Input 1
C25						I	ADC-C Input 25
CMP4_HN0						I	CMPSS-4 High Comparator Negative Input 0
CMP4_LN0		P1	43	35	24	I	CMPSS-4 Low Comparator Negative Input 0
AIO161	0, 4, 8, 12					I	Analog Pin Used For Digital Input 161 This pin also has digital mux functions which are described in the GPIO section of this table.
A2						I	ADC-A Input 2
CMP1_HP1						I	CMPSS-1 High Comparator Positive Input 1
CMP1_LP1						I	CMPSS-1 Low Comparator Positive Input 1
CMP9_HN0						I	CMPSS-9 High Comparator Negative Input 0
CMP9_LN0		M1	36	28		I	CMPSS-9 Low Comparator Negative Input 0
D24						I	ADC-D Input 24
AIO162	0, 4, 8, 12					I	Analog Pin Used For Digital Input 162 This pin also has digital mux functions which are described in the GPIO section of this table.
A3						I	ADC-A Input 3
CMP1_HN1						I	CMPSS-1 High Comparator Negative Input 1
CMP1_HP2						I	CMPSS-1 High Comparator Positive Input 2
CMP1_LN1						I	CMPSS-1 Low Comparator Negative Input 1
CMP1_LP2		M2	35	27		I	CMPSS-1 Low Comparator Positive Input 2
D25						I	ADC-D Input 25
AIO163	0, 4, 8, 12					I	Analog Pin Used For Digital Input 163 This pin also has digital mux functions which are described in the GPIO section of this table.
A4						I	ADC-A Input 4
CMP1_HP0						I	CMPSS-1 High Comparator Positive Input 0
CMP1_LP0						I	CMPSS-1 Low Comparator Positive Input 0
CMP2_HN1						I	CMPSS-2 High Comparator Negative Input 1
CMP2_LN1		L2	32	24		I	CMPSS-2 Low Comparator Negative Input 1
D28						I	ADC-D Input 28
AIO164	0, 4, 8, 12					I	Analog Pin Used For Digital Input 164 This pin also has digital mux functions which are described in the GPIO section of this table.
A5						I	ADC-A Input 5
CMP1_HN0						I	CMPSS-1 High Comparator Negative Input 0
CMP1_LN0						I	CMPSS-1 Low Comparator Negative Input 0
D29		L1	31	23		I	ADC-D Input 29
AIO165	0, 4, 8, 12					I	Analog Pin Used For Digital Input 165 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
A6						I	ADC-A Input 6
CMP2_HP0						I	CMPSS-2 High Comparator Positive Input 0
CMP2_LP0						I	CMPSS-2 Low Comparator Positive Input 0
CMP12_HN0						I	CMPSS-12 High Comparator Negative Input 0
CMP12_LN0		L5	26	18	13	I	CMPSS-12 Low Comparator Negative Input 0
E24						I	ADC-E Input 24
GPIO224	0, 4, 8, 12					I/O	General-Purpose Input Output 224 This pin also has digital mux functions which are described in the GPIO section of this table.
A7						I	ADC-A Input 7
CMP2_HN0						I	CMPSS-2 High Comparator Negative Input 0
CMP2_LN0						I	CMPSS-2 Low Comparator Negative Input 0
CMP9_HP2						I	CMPSS-9 High Comparator Positive Input 2
CMP9_LP2		K5	25	17	12	I	CMPSS-9 Low Comparator Positive Input 2
E25						I	ADC-E Input 25
GPIO225	0, 4, 8, 12					I/O	General-Purpose Input Output 225 This pin also has digital mux functions which are described in the GPIO section of this table.
A8						I	ADC-A Input 8
CMP8_LP3						I	CMPSS-8 Low Comparator Positive Input 3
GPIO226	0, 4, 8, 12	H4	22	16		I/O	General-Purpose Input Output 226 This pin also has digital mux functions which are described in the GPIO section of this table.
A9						I	ADC-A Input 9
CMP6_HP4						I	CMPSS-6 High Comparator Positive Input 4
GPIO227	0, 4, 8, 12	H3	21			I/O	General-Purpose Input Output 227 This pin also has digital mux functions which are described in the GPIO section of this table.
A10						I	ADC-A Input 10
CMP7_HP4						I	CMPSS-7 High Comparator Positive Input 4
GPIO228	0, 4, 8, 12	G3	18			I/O	General-Purpose Input Output 228 This pin also has digital mux functions which are described in the GPIO section of this table.
A11						I	ADC-A Input 11
CMP8_HP4						I	CMPSS-8 High Comparator Positive Input 4
GPIO229	0, 4, 8, 12	G4	17			I/O	General-Purpose Input Output 229 This pin also has digital mux functions which are described in the GPIO section of this table.
A12						I	ADC-A Input 12
CMP1_HP5						I	CMPSS-1 High Comparator Positive Input 5
CMP1_LP5		K2				I	CMPSS-1 Low Comparator Positive Input 5
AIO166	0, 4, 8, 12					I	Analog Pin Used For Digital Input 166 This pin also has digital mux functions which are described in the GPIO section of this table.
A13						I	ADC-A Input 13
CMP2_HP5						I	CMPSS-2 High Comparator Positive Input 5
CMP2_LP5		K1				I	CMPSS-2 Low Comparator Positive Input 5
AIO167	0, 4, 8, 12					I	Analog Pin Used For Digital Input 167 This pin also has digital mux functions which are described in the GPIO section of this table.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
A14						I	ADC-A Input 14
B14						I	ADC-B Input 14
C14						I	ADC-C Input 14
D14		M3	40	32	21	I	ADC-D Input 14
E14						I	ADC-E Input 14
AIO168	0, 4, 8, 12					I	Analog Pin Used For Digital Input 168 This pin also has digital mux functions which are described in the GPIO section of this table.
A15						I	ADC-A Input 15
B15						I	ADC-B Input 15
C15						I	ADC-C Input 15
D15		M4	39	31	20	I	ADC-D Input 15
E15						I	ADC-E Input 15
AIO169	0, 4, 8, 12					I	Analog Pin Used For Digital Input 169 This pin also has digital mux functions which are described in the GPIO section of this table.
B0						I	ADC-B Input 0
C26						I	ADC-C Input 26
VDAC		P2	42	34	23	I	Optional external reference voltage for on-chip DACs.
AIO170	0, 4, 8, 12					I	Analog Pin Used For Digital Input 170 This pin also has digital mux functions which are described in the GPIO section of this table.
B1						I	ADC-B Input 1
C27						I	ADC-C Input 27
CMP3_HP2						I	CMPSS-3 High Comparator Positive Input 2
CMP3_LP2		N3	41	33	22	I	CMPSS-3 Low Comparator Positive Input 2
AIO171	0, 4, 8, 12					I	Analog Pin Used For Digital Input 171 This pin also has digital mux functions which are described in the GPIO section of this table.
B2						I	ADC-B Input 2
D26						I	ADC-D Input 26
AIO172	0, 4, 8, 12	L4	34	26	17	I	Analog Pin Used For Digital Input 172 This pin also has digital mux functions which are described in the GPIO section of this table.
B3						I	ADC-B Input 3
CMP1_HP3						I	CMPSS-1 High Comparator Positive Input 3
CMP1_LP3						I	CMPSS-1 Low Comparator Positive Input 3
CMP3_HN0						I	CMPSS-3 High Comparator Negative Input 0
CMP3_LN0		L3	33	25	16	I	CMPSS-3 Low Comparator Negative Input 0
D27						I	ADC-D Input 27
AIO173	0, 4, 8, 12					I	Analog Pin Used For Digital Input 173 This pin also has digital mux functions which are described in the GPIO section of this table.
B4						I	ADC-B Input 4
CMP7_HN1						I	CMPSS-7 High Comparator Negative Input 1
CMP7_HP1						I	CMPSS-7 High Comparator Positive Input 1
CMP7_LN1						I	CMPSS-7 Low Comparator Negative Input 1
CMP7_LP1		K4	30	22		I	CMPSS-7 Low Comparator Positive Input 1
D30						I	ADC-D Input 30
AIO174	0, 4, 8, 12					I	Analog Pin Used For Digital Input 174 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
B5						I	ADC-B Input 5
CMP3_HN1						I	CMPSS-3 High Comparator Negative Input 1
CMP3_LN1						I	CMPSS-3 Low Comparator Negative Input 1
CMP7_HP2						I	CMPSS-7 High Comparator Positive Input 2
CMP7_LP2		K3	29	21		I	CMPSS-7 Low Comparator Positive Input 2
D31						I	ADC-D Input 31
AIO175	0, 4, 8, 12					I	Analog Pin Used For Digital Input 175 This pin also has digital mux functions which are described in the GPIO section of this table.
B6						I	ADC-B Input 6
CMP9_HP4						I	CMPSS-9 High Comparator Positive Input 4
CMP11_HN0						I	CMPSS-11 High Comparator Negative Input 0
CMP11_LN0		J5	24			I	CMPSS-11 Low Comparator Negative Input 0
E26						I	ADC-E Input 26
GPIO230	0, 4, 8, 12					I/O	General-Purpose Input Output 230 This pin also has digital mux functions which are described in the GPIO section of this table.
B7						I	ADC-B Input 7
CMP10_HP4						I	CMPSS-10 High Comparator Positive Input 4
E27		H5	23			I	ADC-E Input 27
GPIO231	0, 4, 8, 12					I/O	General-Purpose Input Output 231 This pin also has digital mux functions which are described in the GPIO section of this table.
B8						I	ADC-B Input 8
GPIO232	0, 4, 8, 12	H2	20	15	11	I/O	General-Purpose Input Output 232 This pin also has digital mux functions which are described in the GPIO section of this table.
B9						I	ADC-B Input 9
GPIO233	0, 4, 8, 12	H1	19	14	10	I/O	General-Purpose Input Output 233 This pin also has digital mux functions which are described in the GPIO section of this table.
B10						I	ADC-B Input 10
CMP5_LP4		G2	16	13		I	CMPSS-5 Low Comparator Positive Input 4
GPIO234	0, 4, 8, 12					I/O	General-Purpose Input Output 234 This pin also has digital mux functions which are described in the GPIO section of this table.
B11						I	ADC-B Input 11
CMP6_LP4		G1	15	12		I	CMPSS-6 Low Comparator Positive Input 4
GPIO235	0, 4, 8, 12					I/O	General-Purpose Input Output 235 This pin also has digital mux functions which are described in the GPIO section of this table.
B12						I	ADC-B Input 12
CMP7_LP4		J2				I	CMPSS-7 Low Comparator Positive Input 4
AIO176	0, 4, 8, 12					I	Analog Pin Used For Digital Input 176 This pin also has digital mux functions which are described in the GPIO section of this table.
B13						I	ADC-B Input 13
CMP8_LP4		J1				I	CMPSS-8 Low Comparator Positive Input 4
AIO177	0, 4, 8, 12					I	Analog Pin Used For Digital Input 177 This pin also has digital mux functions which are described in the GPIO section of this table.
B16						I	ADC-B Input 16
CMP9_HP5		J4				I	CMPSS-9 High Comparator Positive Input 5
AIO178	0, 4, 8, 12					I	Analog Pin Used For Digital Input 178 This pin also has digital mux functions which are described in the GPIO section of this table.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
B17						I	ADC-B Input 17
CMP10_HP5		J3				I	CMPSS-10 High Comparator Positive Input 5
AIO179	0, 4, 8, 12					I	Analog Pin Used For Digital Input 179 This pin also has digital mux functions which are described in the GPIO section of this table.
C0						I	ADC-C Input 0
E28		R2	45	37	26	I	ADC-E Input 28
AIO180	0, 4, 8, 12					I	Analog Pin Used For Digital Input 180 This pin also has digital mux functions which are described in the GPIO section of this table.
C1						I	ADC-C Input 1
E29		T2	46	38	27	I	ADC-E Input 29
AIO181	0, 4, 8, 12					I	Analog Pin Used For Digital Input 181 This pin also has digital mux functions which are described in the GPIO section of this table.
C2						I	ADC-C Input 2
CMP9_HP1						I	CMPSS-9 High Comparator Positive Input 1
CMP9_LP1						I	CMPSS-9 Low Comparator Positive Input 1
CMP11_HN1						I	CMPSS-11 High Comparator Negative Input 1
CMP11_LN1		N4	51	43		I	CMPSS-11 Low Comparator Negative Input 1
E30						I	ADC-E Input 30
AIO182	0, 4, 8, 12					I	Analog Pin Used For Digital Input 182 This pin also has digital mux functions which are described in the GPIO section of this table.
C3						I	ADC-C Input 3
CMP9_LP4						I	CMPSS-9 Low Comparator Positive Input 4
E31		M5	52	44		I	ADC-E Input 31
AIO183	0, 4, 8, 12					I	Analog Pin Used For Digital Input 183 This pin also has digital mux functions which are described in the GPIO section of this table.
C4						I	ADC-C Input 4
CMP10_LP4		P5	55	47		I	CMPSS-10 Low Comparator Positive Input 4
AIO184	0, 4, 8, 12					I	Analog Pin Used For Digital Input 184 This pin also has digital mux functions which are described in the GPIO section of this table.
C5						I	ADC-C Input 5
CMP11_LP4		N5	56	48		I	CMPSS-11 Low Comparator Positive Input 4
AIO185	0, 4, 8, 12					I	Analog Pin Used For Digital Input 185 This pin also has digital mux functions which are described in the GPIO section of this table.
C6						I	ADC-C Input 6
CMP12_LP4		M8	63			I	CMPSS-12 Low Comparator Positive Input 4
GPIO236	0, 4, 8, 12					I/O	General-Purpose Input Output 236 This pin also has digital mux functions which are described in the GPIO section of this table.
C7						I	ADC-C Input 7
CMP5_HP5		M9	64			I	CMPSS-5 High Comparator Positive Input 5
GPIO237	0, 4, 8, 12					I/O	General-Purpose Input Output 237 This pin also has digital mux functions which are described in the GPIO section of this table.
C8						I	ADC-C Input 8
CMP12_LP0		N12	69	58	40	I	CMPSS-12 Low Comparator Positive Input 0
GPIO238	0, 4, 8, 12					I/O	General-Purpose Input Output 238 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
C9						I	ADC-C Input 9
CMP9_LP3		P12	70	59	41	I	CMPSS-9 Low Comparator Positive Input 3
GPIO239	0, 4, 8, 12					I/O	General-Purpose Input Output 239 This pin also has digital mux functions which are described in the GPIO section of this table.
C10						I	ADC-C Input 10
CMP8_HP5		N8				I	CMPSS-8 High Comparator Positive Input 5
AIO186	0, 4, 8, 12					I	Analog Pin Used For Digital Input 186 This pin also has digital mux functions which are described in the GPIO section of this table.
C11						I	ADC-C Input 11
CMP11_HP5		P8				I	CMPSS-11 High Comparator Positive Input 5
AIO187	0, 4, 8, 12					I	Analog Pin Used For Digital Input 187 This pin also has digital mux functions which are described in the GPIO section of this table.
C12						I	ADC-C Input 12
CMP12_HP5		R8				I	CMPSS-12 High Comparator Positive Input 5
AIO188	0, 4, 8, 12					I	Analog Pin Used For Digital Input 188 This pin also has digital mux functions which are described in the GPIO section of this table.
C13						I	ADC-C Input 13
CMP5_LP5		T8				I	CMPSS-5 Low Comparator Positive Input 5
AIO189	0, 4, 8, 12					I	Analog Pin Used For Digital Input 189 This pin also has digital mux functions which are described in the GPIO section of this table.
C16						I	ADC-C Input 16
CMP6_LP5		N7				I	CMPSS-6 Low Comparator Positive Input 5
AIO190	0, 4, 8, 12					I	Analog Pin Used For Digital Input 190 This pin also has digital mux functions which are described in the GPIO section of this table.
C17						I	ADC-C Input 17
CMP7_LP5		P7				I	CMPSS-7 Low Comparator Positive Input 5
AIO191	0, 4, 8, 12					I	Analog Pin Used For Digital Input 191 This pin also has digital mux functions which are described in the GPIO section of this table.
B24						I	ADC-B Input 24
D0		R3	47	39	28	I	ADC-D Input 0
AIO192	0, 4, 8, 12					I	Analog Pin Used For Digital Input 192 This pin also has digital mux functions which are described in the GPIO section of this table.
B25						I	ADC-B Input 25
D1		T3	48	40	29	I	ADC-D Input 1
AIO193	0, 4, 8, 12					I	Analog Pin Used For Digital Input 193 This pin also has digital mux functions which are described in the GPIO section of this table.
B26						I	ADC-B Input 26
CMP4_HP3						I	CMPSS-4 High Comparator Positive Input 3
CMP4_LP3						I	CMPSS-4 Low Comparator Positive Input 3
CMP7_HN0						I	CMPSS-7 High Comparator Negative Input 0
CMP7_LN0		R5	57	49	34	I	CMPSS-7 Low Comparator Negative Input 0
D2						I	ADC-D Input 2
AIO194	0, 4, 8, 12					I	Analog Pin Used For Digital Input 194 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
B27						I	ADC-B Input 27
D3		R6	58	50	35	I	ADC-D Input 3
AIO195	0, 4, 8, 12					I	Analog Pin Used For Digital Input 195 This pin also has digital mux functions which are described in the GPIO section of this table.
B28						I	ADC-B Input 28
CMP5_LP3						I	CMPSS-5 Low Comparator Positive Input 3
CMP8_HN0						I	CMPSS-8 High Comparator Negative Input 0
CMP8_LN0		N10	65			I	CMPSS-8 Low Comparator Negative Input 0
D4						I	ADC-D Input 4
GPIO240	0, 4, 8, 12					I/O	General-Purpose Input Output 240 This pin also has digital mux functions which are described in the GPIO section of this table.
B29						I	ADC-B Input 29
CMP4_HN1						I	CMPSS-4 High Comparator Negative Input 1
CMP4_HP1						I	CMPSS-4 High Comparator Positive Input 1
CMP4_LN1						I	CMPSS-4 Low Comparator Negative Input 1
CMP4_LP1		N11	66	55		I	CMPSS-4 Low Comparator Positive Input 1
D5						I	ADC-D Input 5
GPIO241	0, 4, 8, 12					I/O	General-Purpose Input Output 241 This pin also has digital mux functions which are described in the GPIO section of this table.
B30						I	ADC-B Input 30
CMP1_HP4						I	CMPSS-1 High Comparator Positive Input 4
CMP1_LP4						I	CMPSS-1 Low Comparator Positive Input 4
D6		T12	71	60		I	ADC-D Input 6
GPIO242	0, 4, 8, 12					I/O	General-Purpose Input Output 242 This pin also has digital mux functions which are described in the GPIO section of this table.
B31						I	ADC-B Input 31
CMP2_HP4						I	CMPSS-2 High Comparator Positive Input 4
CMP2_LP4						I	CMPSS-2 Low Comparator Positive Input 4
D7		R12	72	61		I	ADC-D Input 7
GPIO243	0, 4, 8, 12					I/O	General-Purpose Input Output 243 This pin also has digital mux functions which are described in the GPIO section of this table.
C28						I	ADC-C Input 28
CMP6_HP0						I	CMPSS-6 High Comparator Positive Input 0
CMP6_LP0						I	CMPSS-6 Low Comparator Positive Input 0
D8		R13	75			I	ADC-D Input 8
GPIO244	0, 4, 8, 12					I/O	General-Purpose Input Output 244 This pin also has digital mux functions which are described in the GPIO section of this table.
C29						I	ADC-C Input 29
CMP3_LP3						I	CMPSS-3 Low Comparator Positive Input 3
CMP6_HN0						I	CMPSS-6 High Comparator Negative Input 0
CMP6_LN0		T13	76			I	CMPSS-6 Low Comparator Negative Input 0
D9						I	ADC-D Input 9
GPIO245	0, 4, 8, 12					I/O	General-Purpose Input Output 245 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
CMP8_LP5						I	CMPSS-8 Low Comparator Positive Input 5
D10		N6				I	ADC-D Input 10
AIO196	0, 4, 8, 12					I	Analog Pin Used For Digital Input 196 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP9_LP5						I	CMPSS-9 Low Comparator Positive Input 5
D11		P6				I	ADC-D Input 11
AIO197	0, 4, 8, 12					I	Analog Pin Used For Digital Input 197 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP5_HP0						I	CMPSS-5 High Comparator Positive Input 0
CMP5_LP0						I	CMPSS-5 Low Comparator Positive Input 0
CMP10_HN1						I	CMPSS-10 High Comparator Negative Input 1
CMP10_LN1		M7				I	CMPSS-10 Low Comparator Negative Input 1
D12						I	ADC-D Input 12
AIO198	0, 4, 8, 12					I	Analog Pin Used For Digital Input 198 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP2_HP3						I	CMPSS-2 High Comparator Positive Input 3
CMP2_LP3						I	CMPSS-2 Low Comparator Positive Input 3
CMP5_HN0						I	CMPSS-5 High Comparator Negative Input 0
CMP5_LN0		M6				I	CMPSS-5 Low Comparator Negative Input 0
D13						I	ADC-D Input 13
AIO199	0, 4, 8, 12					I	Analog Pin Used For Digital Input 199 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP10_LP5						I	CMPSS-10 Low Comparator Positive Input 5
D16		R7				I	ADC-D Input 16
AIO200	0, 4, 8, 12					I	Analog Pin Used For Digital Input 200 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP11_LP5						I	CMPSS-11 Low Comparator Positive Input 5
D17		T7				I	ADC-D Input 17
AIO201	0, 4, 8, 12					I	Analog Pin Used For Digital Input 201 This pin also has digital mux functions which are described in the GPIO section of this table.
A24						I	ADC-A Input 24
DACB_OUT						O	Buffered DAC-B Output.
E0		P3	49	41	30	I	ADC-E Input 0
AIO202	0, 4, 8, 12					I	Analog Pin Used For Digital Input 202 This pin also has digital mux functions which are described in the GPIO section of this table.
A25						I	ADC-A Input 25
E1		P4	50	42	31	I	ADC-E Input 1
AIO203	0, 4, 8, 12					I	Analog Pin Used For Digital Input 203 This pin also has digital mux functions which are described in the GPIO section of this table.
A26						I	ADC-A Input 26
CMP3_HP4						I	CMPSS-3 High Comparator Positive Input 4
CMP3_LP4						I	CMPSS-3 Low Comparator Positive Input 4
E2		T5	59	51		I	ADC-E Input 2
AIO204	0, 4, 8, 12					I	Analog Pin Used For Digital Input 204 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
A27						I	ADC-A Input 27
CMP4_HP4						I	CMPSS-4 High Comparator Positive Input 4
CMP4_LP4						I	CMPSS-4 Low Comparator Positive Input 4
E3		T6	60	52		I	ADC-E Input 3
AIO205	0, 4, 8, 12					I	Analog Pin Used For Digital Input 205 This pin also has digital mux functions which are described in the GPIO section of this table.
A28						I	ADC-A Input 28
CMP8_HN1						I	CMPSS-8 High Comparator Negative Input 1
CMP8_HP1						I	CMPSS-8 High Comparator Positive Input 1
CMP8_LN1						I	CMPSS-8 Low Comparator Negative Input 1
CMP8_LP1		P11	67	56	38	I	CMPSS-8 Low Comparator Positive Input 1
E4						I	ADC-E Input 4
GPIO246	0, 4, 8, 12					I/O	General-Purpose Input Output 246 This pin also has digital mux functions which are described in the GPIO section of this table.
A29						I	ADC-A Input 29
CMP8_HP2						I	CMPSS-8 High Comparator Positive Input 2
CMP8_LP2						I	CMPSS-8 Low Comparator Positive Input 2
E5		R11	68	57	39	I	ADC-E Input 5
GPIO247	0, 4, 8, 12					I/O	General-Purpose Input Output 247 This pin also has digital mux functions which are described in the GPIO section of this table.
A30						I	ADC-A Input 30
CMP5_HN1						I	CMPSS-5 High Comparator Negative Input 1
CMP5_HP1						I	CMPSS-5 High Comparator Positive Input 1
CMP5_LN1						I	CMPSS-5 Low Comparator Negative Input 1
CMP5_LP1		P13	73	62		I	CMPSS-5 Low Comparator Positive Input 1
E6						I	ADC-E Input 6
GPIO248	0, 4, 8, 12					I/O	General-Purpose Input Output 248 This pin also has digital mux functions which are described in the GPIO section of this table.
A31						I	ADC-A Input 31
CMP5_HP2						I	CMPSS-5 High Comparator Positive Input 2
CMP5_LP2						I	CMPSS-5 Low Comparator Positive Input 2
E7		N13	74	63		I	ADC-E Input 7
GPIO249	0, 4, 8, 12					I/O	General-Purpose Input Output 249 This pin also has digital mux functions which are described in the GPIO section of this table.
C30						I	ADC-C Input 30
CMP2_HP1						I	CMPSS-2 High Comparator Positive Input 1
CMP2_LP1						I	CMPSS-2 Low Comparator Positive Input 1
CMP10_HN0						I	CMPSS-10 High Comparator Negative Input 0
CMP10_LN0		T10				I	CMPSS-10 Low Comparator Negative Input 0
E8						I	ADC-E Input 8
AIO206	0, 4, 8, 12					I	Analog Pin Used For Digital Input 206 This pin also has digital mux functions which are described in the GPIO section of this table.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
C31						I	ADC-C Input 31
CMP2_HP2						I	CMPSS-2 High Comparator Positive Input 2
CMP2_LP2						I	CMPSS-2 Low Comparator Positive Input 2
CMP9_HN1						I	CMPSS-9 High Comparator Negative Input 1
CMP9_LN1		T9				I	CMPSS-9 Low Comparator Negative Input 1
E9						I	ADC-E Input 9
AIO207	0, 4, 8, 12					I	Analog Pin Used For Digital Input 207 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP10_HP1						I	CMPSS-10 High Comparator Positive Input 1
CMP10_LP1						I	CMPSS-10 Low Comparator Positive Input 1
E10		R10				I	ADC-E Input 10
AIO208	0, 4, 8, 12					I	Analog Pin Used For Digital Input 208 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP11_HP1						I	CMPSS-11 High Comparator Positive Input 1
CMP11_LP1						I	CMPSS-11 Low Comparator Positive Input 1
E11		R9				I	ADC-E Input 11
AIO209	0, 4, 8, 12					I	Analog Pin Used For Digital Input 209 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP10_HP2						I	CMPSS-10 High Comparator Positive Input 2
CMP10_LP2						I	CMPSS-10 Low Comparator Positive Input 2
E12		P9				I	ADC-E Input 12
AIO210	0, 4, 8, 12					I	Analog Pin Used For Digital Input 210 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP11_HP2						I	CMPSS-11 High Comparator Positive Input 2
CMP11_LP2						I	CMPSS-11 Low Comparator Positive Input 2
E13		N9				I	ADC-E Input 13
AIO211	0, 4, 8, 12					I	Analog Pin Used For Digital Input 211 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP6_HP2						I	CMPSS-6 High Comparator Positive Input 2
CMP6_LP2						I	CMPSS-6 Low Comparator Positive Input 2
E16		P10				I	ADC-E Input 16
AIO212	0, 4, 8, 12					I	Analog Pin Used For Digital Input 212 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP6_HN1						I	CMPSS-6 High Comparator Negative Input 1
CMP6_HP1						I	CMPSS-6 High Comparator Positive Input 1
CMP6_LN1						I	CMPSS-6 Low Comparator Negative Input 1
CMP6_LP1		T11				I	CMPSS-6 Low Comparator Positive Input 1
E17						I	ADC-E Input 17
AIO213	0, 4, 8, 12					I	Analog Pin Used For Digital Input 213 This pin also has digital mux functions which are described in the GPIO section of this table.
VREFHIAB		N2	38	30	19	I	ADC-AB high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. NOTE: Do not load this pin externally

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
VREFHICDE		R4	54	46	33	I	ADC-CDE high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. NOTE: Do not load this pin externally
VREFLOAB		N1	37	29	18	I	ADC-AB Low Reference
VREFLOCDE		T4	53	45	32	I	ADC-CDE Low Reference
GPIO							
AIO160	0, 4, 8, 12	R1	44	36	25	I	Analog Pin Used For Digital Input 160 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C2	11					I	SDFM-3 Channel 2 Clock Input
AIO161	0, 4, 8, 12	P1	43	35	24	I	Analog Pin Used For Digital Input 161 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D2	11					I	SDFM-3 Channel 2 Data Input
AIO162	0, 4, 8, 12	M1	36	28		I	Analog Pin Used For Digital Input 162 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C2	11					I	SDFM-2 Channel 2 Clock Input
AIO163	0, 4, 8, 12	M2	35	27		I	Analog Pin Used For Digital Input 163 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D2	11					I	SDFM-2 Channel 2 Data Input
AIO164	0, 4, 8, 12	L2	32	24		I	Analog Pin Used For Digital Input 164 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C3	11					I	SDFM-2 Channel 3 Clock Input
AIO165	0, 4, 8, 12	L1	31	23		I	Analog Pin Used For Digital Input 165 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D3	11					I	SDFM-2 Channel 3 Data Input
GPIO224	0, 4, 8, 12	L5	26	18	13	I/O	General-Purpose Input Output 224 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM12_A	1					O	ePWM-12 Output A
EPWM12_B	2					O	ePWM-12 Output B
SPIB_POCI	5					I/O	SPI-B Peripheral Out, Controller In (POCI)
MCAND_RX	6					I	MCAN-D Receive
OUTPUTXBAR5	9					O	Output X-BAR Output 5
SD4_D2	11					I	SDFM-4 Channel 2 Data Input
ADCA_EXTMUXSEL0	14					O	External ADC selection Mux output
ESC_GPO8	15					O	EtherCAT General-Purpose Output 8
GPIO225	0, 4, 8, 12	K5	25	17	12	I/O	General-Purpose Input Output 225 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM11_B	1					O	ePWM-11 Output B
SPIB_PICO	5					I/O	SPI-B Peripheral In, Controller Out (PICO)
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
UARTF_TX	7					I/O	UART-F Serial Data Transmit
OUTPUTXBAR4	9					O	Output X-BAR Output 4
SD4_C1	11					I	SDFM-4 Channel 1 Clock Input
ADCA_EXTMUXSEL1	14					O	External ADC selection Mux output
ESC_GPO9	15					O	EtherCAT General-Purpose Output 9

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO226	0, 4, 8, 12					I/O	General-Purpose Input Output 226 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM10_A	1					O	ePWM-10 Output A
SPIA_PTE	5					I/O	SPI-A Peripheral Transmit Enable (PTE)
MCAND_TX	6					O	MCAN-D Transmit
UARTF_RX	7	H4	22	16		I/O	UART-F Serial Data Receive
OUTPUTXBAR1	9					O	Output X-BAR Output 1
SD1_C3	10					I	SDFM-1 Channel 3 Clock Input
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
ADCA_EXTMUXSEL2	14					O	External ADC selection Mux output
ESC_GPO10	15					O	EtherCAT General-Purpose Output 10
GPIO227	0, 4, 8, 12					I/O	General-Purpose Input Output 227 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM14_B	1					O	ePWM-14 Output B
SPIA_CLK	5	H3	21			I/O	SPI-A Clock
OUTPUTXBAR4	9					O	Output X-BAR Output 4
SD2_C2	11					I	SDFM-2 Channel 2 Clock Input
ADCA_EXTMUXSEL3	14					O	External ADC selection Mux output
GPIO228	0, 4, 8, 12					I/O	General-Purpose Input Output 228 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM18_A	1					O	ePWM-18 Output A
EPWM13_A	2					O	ePWM-13 Output A
SPIB_POCI	5	G3	18			I/O	SPI-B Peripheral Out, Controller In (POCI)
LINB_TX	6					O	LIN-B Transmit
OUTPUTXBAR1	9					O	Output X-BAR Output 1
SENT4	10					I/O	SENT Input Pin 4
SD2_D1	11					I	SDFM-2 Channel 1 Data Input
GPIO229	0, 4, 8, 12					I/O	General-Purpose Input Output 229 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM17_B	1					O	ePWM-17 Output B
EPWM12_B	2	G4	17			O	ePWM-12 Output B
SPIB_PICO	5					I/O	SPI-B Peripheral In, Controller Out (PICO)
MCANA_RX	6					I	MCAN-A Receive
SENT3	10					I/O	SENT Input Pin 3
SD1_C4	11					I	SDFM-1 Channel 4 Clock Input
AIO166	0, 4, 8, 12	K2				I	Analog Pin Used For Digital Input 166 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_C1	11					I	SDFM-4 Channel 1 Clock Input
AIO167	0, 4, 8, 12	K1				I	Analog Pin Used For Digital Input 167 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_D1	11					I	SDFM-4 Channel 1 Data Input
AIO168	0, 4, 8, 12	M3	40	32	21	I	Analog Pin Used For Digital Input 168 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C3	11					I	SDFM-3 Channel 3 Clock Input
AIO169	0, 4, 8, 12	M4	39	31	20	I	Analog Pin Used For Digital Input 169 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D3	11					I	SDFM-3 Channel 3 Data Input

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
AIO170	0, 4, 8, 12	P2	42	34	23	I	Analog Pin Used For Digital Input 170 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C4	11					I	SDFM-3 Channel 4 Clock Input
AIO171	0, 4, 8, 12	N3	41	33	22	I	Analog Pin Used For Digital Input 171 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D4	11					I	SDFM-3 Channel 4 Data Input
AIO172	0, 4, 8, 12	L4	34	26	17	I	Analog Pin Used For Digital Input 172 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
AIO173	0, 4, 8, 12	L3	33	25	16	I	Analog Pin Used For Digital Input 173 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
AIO174	0, 4, 8, 12	K4	30	22		I	Analog Pin Used For Digital Input 174 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C4	11					I	SDFM-2 Channel 4 Clock Input
AIO175	0, 4, 8, 12	K3	29	21		I	Analog Pin Used For Digital Input 175 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D4	11					I	SDFM-2 Channel 4 Data Input
GPIO230	0, 4, 8, 12	J5	24			I/O	General-Purpose Input Output 230 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM11_A	1					O	ePWM-11 Output A
SYNCOUT	3					O	External ePWM Synchronization Pulse
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
OUTPUTXBAR3	9					O	Output X-BAR Output 3
SD4_D1	11					I	SDFM-4 Channel 1 Data Input
ADCB_EXTMUXSEL0	14					O	External ADC selection Mux output
GPIO231	0, 4, 8, 12	H5	23			I/O	General-Purpose Input Output 231 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM10_B	1					O	ePWM-10 Output B
SPIA_PICO	5					I/O	SPI-A Peripheral In, Controller Out (PICO)
MCAND_RX	6					I	MCAN-D Receive
OUTPUTXBAR2	9					O	Output X-BAR Output 2
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
ADCB_EXTMUXSEL1	14					O	External ADC selection Mux output
GPIO232	0, 4, 8, 12	H2	20	15	11	I/O	General-Purpose Input Output 232 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM14_A	1					O	ePWM-14 Output A
EPWM8_B	2					O	ePWM-8 Output B
SPIA_POCI	5					I/O	SPI-A Peripheral Out, Controller In (POCI)
OUTPUTXBAR3	9					O	Output X-BAR Output 3
SENT6	10					I/O	SENT Input Pin 6
SD3_D1	11					I	SDFM-3 Channel 1 Data Input
ESC_PHY0_LINKSTATUS	13					I	EtherCAT PHY-0 Link Status
ADCB_EXTMUXSEL2	14					O	External ADC selection Mux output
ESC_GPO11	15					O	EtherCAT General-Purpose Output 11

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO233	0, 4, 8, 12	H1	19	14	10	I/O	General-Purpose Input Output 233 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM18_B	1					O	ePWM-18 Output B
EPWM13_B	2					O	ePWM-13 Output B
LINB_RX	6					I	LIN-B Receive
OUTPUTXBAR2	9					O	Output X-BAR Output 2
SENT5	10					I/O	SENT Input Pin 5
SD2_C1	11					I	SDFM-2 Channel 1 Clock Input
ESC_PHY1_LINKSTATUS	13					I	EtherCAT PHY-1 Link Status
ADCB_EXTMUXSEL3	14					O	External ADC selection Mux output
ESC_GPO12	15					O	EtherCAT General-Purpose Output 12
GPIO234	0, 4, 8, 12	G2	16	13		I/O	General-Purpose Input Output 234 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM17_A	1					O	ePWM-17 Output A
EPWM12_A	2					O	ePWM-12 Output A
SPIB_PTE	5					I/O	SPI-B Peripheral Transmit Enable (PTE)
MCANA_TX	6					O	MCAN-A Transmit
SENT2	10					I/O	SENT Input Pin 2
SD1_D4	11					I	SDFM-1 Channel 4 Data Input
ESC_GPO13	15					O	EtherCAT General-Purpose Output 13
GPIO235	0, 4, 8, 12	G1	15	12		I/O	General-Purpose Input Output 235 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM9_B	1					O	ePWM-9 Output B
SPIB_CLK	5					I/O	SPI-B Clock
MCANA_RX	6					I	MCAN-A Receive
SENT1	10					I/O	SENT Input Pin 1
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
ESC_GPO14	15					O	EtherCAT General-Purpose Output 14
AIO176	0, 4, 8, 12	J2				I	Analog Pin Used For Digital Input 176 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_C2	11					I	SDFM-4 Channel 2 Clock Input
AIO177	0, 4, 8, 12	J1				I	Analog Pin Used For Digital Input 177 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_D2	11					I	SDFM-4 Channel 2 Data Input
AIO178	0, 4, 8, 12	J4				I	Analog Pin Used For Digital Input 178 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_C3	11					I	SDFM-4 Channel 3 Clock Input
AIO179	0, 4, 8, 12	J3				I	Analog Pin Used For Digital Input 179 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_D3	11					I	SDFM-4 Channel 3 Data Input
AIO180	0, 4, 8, 12	R2	45	37	26	I	Analog Pin Used For Digital Input 180 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
AIO181	0, 4, 8, 12	T2	46	38	27	I	Analog Pin Used For Digital Input 181 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D2	11					I	SDFM-1 Channel 2 Data Input

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
AIO182	0, 4, 8, 12	N4	51	43		I	Analog Pin Used For Digital Input 182 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C1	11					I	SDFM-3 Channel 1 Clock Input
AIO183	0, 4, 8, 12	M5	52	44		I	Analog Pin Used For Digital Input 183 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D1	11					I	SDFM-3 Channel 1 Data Input
AIO184	0, 4, 8, 12	P5	55	47		I	Analog Pin Used For Digital Input 184 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C2	11					I	SDFM-3 Channel 2 Clock Input
AIO185	0, 4, 8, 12	N5	56	48		I	Analog Pin Used For Digital Input 185 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D2	11					I	SDFM-3 Channel 2 Data Input
GPIO236	0, 4, 8, 12	M8	63			I/O	General-Purpose Input Output 236 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM12_B	1					O	ePWM-12 Output B
EPWM8_A	2					O	ePWM-8 Output A
LINA_RX	6					I	LIN-A Receive
OUTPUTXBAR6	9					O	Output X-BAR Output 6
SD4_C2	11					I	SDFM-4 Channel 2 Clock Input
ESC_I2C_SDA	13					I/OC	EtherCAT I2C Data
ADCC_EXTMUXSEL0	14					O	External ADC selection Mux output
GPIO237	0, 4, 8, 12	M9	64			I/O	General-Purpose Input Output 237 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM14_A	1					O	ePWM-14 Output A
EPWM8_B	2					O	ePWM-8 Output B
EPWM17_B	3					O	ePWM-17 Output B
LINA_TX	6					O	LIN-A Transmit
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
OUTPUTXBAR7	9					O	Output X-BAR Output 7
SD4_D3	11					I	SDFM-4 Channel 3 Data Input
ESC_I2C_SCL	13					I/OC	EtherCAT I2C Clock
ADCC_EXTMUXSEL1	14					O	External ADC selection Mux output
GPIO238	0, 4, 8, 12	N12	69	58	40	I/O	General-Purpose Input Output 238 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM15_B	1					O	ePWM-15 Output B
OUTPUTXBAR6	9					O	Output X-BAR Output 6
SD1_D3	10					I	SDFM-1 Channel 3 Data Input
SD2_C3	11					I	SDFM-2 Channel 3 Clock Input
ESC_SYNC0	13					O	EtherCAT SyncSignal Output 0
ADCC_EXTMUXSEL2	14					O	External ADC selection Mux output
ESC_GPO15	15					O	EtherCAT General-Purpose Output 15

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO239	0, 4, 8, 12	P12	70	59	41	I/O	General-Purpose Input Output 239 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM16_B	1					O	ePWM-16 Output B
LINB_TX	6					O	LIN-B Transmit
I2CA_SCL	7					I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR8	9					O	Output X-BAR Output 8
SD2_C4	11					I	SDFM-2 Channel 4 Clock Input
ESC_SYNC1	13					O	EtherCAT SyncSignal Output 1
ADCC_EXTMUXSEL3	14					O	External ADC selection Mux output
ESC_GPO16	15					O	EtherCAT General-Purpose Output 16
AIO186	0, 4, 8, 12	N8				I	Analog Pin Used For Digital Input 186 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
AIO187	0, 4, 8, 12	P8				I	Analog Pin Used For Digital Input 187 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
AIO188	0, 4, 8, 12	R8				I	Analog Pin Used For Digital Input 188 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
AIO189	0, 4, 8, 12	T8				I	Analog Pin Used For Digital Input 189 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D2	11					I	SDFM-1 Channel 2 Data Input
AIO190	0, 4, 8, 12	N7				I	Analog Pin Used For Digital Input 190 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
AIO191	0, 4, 8, 12	P7				I	Analog Pin Used For Digital Input 191 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
AIO192	0, 4, 8, 12	R3	47	39	28	I	Analog Pin Used For Digital Input 192 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
AIO193	0, 4, 8, 12	T3	48	40	29	I	Analog Pin Used For Digital Input 193 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
AIO194	0, 4, 8, 12	R5	57	49	34	I	Analog Pin Used For Digital Input 194 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C4	11					I	SDFM-1 Channel 4 Clock Input
AIO195	0, 4, 8, 12	R6	58	50	35	I	Analog Pin Used For Digital Input 195 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D4	11					I	SDFM-1 Channel 4 Data Input

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO240	0, 4, 8, 12	N10	65			I/O	General-Purpose Input Output 240 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM14_B	1					O	ePWM-14 Output B
SPID_PICO	5					I/O	SPI-D Peripheral In, Controller Out (PICO)
SD4_C3	11					I	SDFM-4 Channel 3 Clock Input
ESC_LED_RUN	13					O	
ADCD_EXTMUXSEL0	14					O	External ADC selection Mux output
GPIO241	0, 4, 8, 12	N11	66	55		I/O	General-Purpose Input Output 241 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM8_A	1					O	ePWM-8 Output A
SPID_CLK	5					I/O	SPI-D Clock
SD4_D4	11					I	SDFM-4 Channel 4 Data Input
ESC_LED_ERR	13					O	
ADCD_EXTMUXSEL1	14					O	External ADC selection Mux output
ESC_GPO17	15					O	EtherCAT General-Purpose Output 17
GPIO242	0, 4, 8, 12	T12	71	60		I/O	General-Purpose Input Output 242 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D4	6					I	SDFM-1 Channel 4 Data Input
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
OUTPUTXBAR9	9					O	Output X-BAR Output 9
SENT1	10					I/O	SENT Input Pin 1
SD2_D2	11					I	SDFM-2 Channel 2 Data Input
ESC_LED_STATE_RUN	13					O	
ADCD_EXTMUXSEL2	14					O	External ADC selection Mux output
ESC_GPO18	15					O	EtherCAT General-Purpose Output 18
GPIO243	0, 4, 8, 12	R12	72	61		I/O	General-Purpose Input Output 243 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM8_B	1					O	ePWM-8 Output B
SENT2	10					I/O	SENT Input Pin 2
SD2_D4	11					I	SDFM-2 Channel 4 Data Input
ESC_LED_LINK0_ACTIVE	13					O	EtherCAT Link-0 Active
ADCD_EXTMUXSEL3	14					O	External ADC selection Mux output
ESC_GPO19	15					O	EtherCAT General-Purpose Output 19
GPIO244	0, 4, 8, 12	R13	75			I/O	General-Purpose Input Output 244 This pin also has analog functions which are described in the ANALOG section of this table.
SPIC_PTE	5					I/O	SPI-C Peripheral Transmit Enable (PTE)
SENT5	10					I/O	SENT Input Pin 5
SD4_C4	11					I	SDFM-4 Channel 4 Clock Input
ESC_LED_LINK1_ACTIVE	13					O	EtherCAT Link-1 Active
GPIO245	0, 4, 8, 12	T13	76			I/O	General-Purpose Input Output 245 This pin also has analog functions which are described in the ANALOG section of this table.
SPIC_POCI	5					I/O	SPI-C Peripheral Out, Controller In (POCI)
SENT6	10					I/O	SENT Input Pin 6
SD3_C1	11					I	SDFM-3 Channel 1 Clock Input
ESC_PHY_RESETn	13					O	EtherCAT PHY Active Low Reset
AIO196	0, 4, 8, 12	N6				I	Analog Pin Used For Digital Input 196 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_C4	11					I	SDFM-4 Channel 4 Clock Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
AIO197	0, 4, 8, 12	P6				I	Analog Pin Used For Digital Input 197 This pin also has analog functions which are described in the ANALOG section of this table.
SD4_D4	11					I	SDFM-4 Channel 4 Data Input
AIO198	0, 4, 8, 12	M7				I	Analog Pin Used For Digital Input 198 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_C4	11					I	SDFM-1 Channel 4 Clock Input
AIO199	0, 4, 8, 12	M6				I	Analog Pin Used For Digital Input 199 This pin also has analog functions which are described in the ANALOG section of this table.
SD1_D4	11					I	SDFM-1 Channel 4 Data Input
AIO200	0, 4, 8, 12	R7				I	Analog Pin Used For Digital Input 200 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C1	11					I	SDFM-2 Channel 1 Clock Input
AIO201	0, 4, 8, 12	T7				I	Analog Pin Used For Digital Input 201 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D1	11					I	SDFM-2 Channel 1 Data Input
AIO202	0, 4, 8, 12	P3	49	41	30	I	Analog Pin Used For Digital Input 202 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C1	11					I	SDFM-2 Channel 1 Clock Input
AIO203	0, 4, 8, 12	P4	50	42	31	I	Analog Pin Used For Digital Input 203 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D1	11					I	SDFM-2 Channel 1 Data Input
AIO204	0, 4, 8, 12	T5	59	51		I	Analog Pin Used For Digital Input 204 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C3	11					I	SDFM-3 Channel 3 Clock Input
AIO205	0, 4, 8, 12	T6	60	52		I	Analog Pin Used For Digital Input 205 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D3	11					I	SDFM-3 Channel 3 Data Input
GPIO246	0, 4, 8, 12	P11	67	56	38	I/O	General-Purpose Input Output 246 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM16_A	1					O	ePWM-16 Output A
SPID_PTE	5					I/O	SPI-D Peripheral Transmit Enable (PTE)
MCANC_RX	6					I	MCAN-C Receive
OUTPUTXBAR7	9					O	Output X-BAR Output 7
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
ADCE_EXTMUXSEL0	14					O	External ADC selection Mux output
ESC_GPO20	15					O	EtherCAT General-Purpose Output 20

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO247	0, 4, 8, 12	R11	68	57	39	I/O	General-Purpose Input Output 247 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM15_A	1					O	ePWM-15 Output A
ERRORSTS	2					O	Error Status Output. This signal requires an external pulldown.
SPID_POCI	5					I/O	SPI-D Peripheral Out, Controller In (POCI)
MCANC_RX	6					I	MCAN-C Receive
LINA_TX	7					O	LIN-A Transmit
OUTPUTXBAR5	9					O	Output X-BAR Output 5
SD2_D3	11					I	SDFM-2 Channel 3 Data Input
ADCE_EXTMUXSEL1	14					O	External ADC selection Mux output
ESC_GPO21	15					O	EtherCAT General-Purpose Output 21
GPIO248	0, 4, 8, 12	P13	73	62		I/O	General-Purpose Input Output 248 This pin also has analog functions which are described in the ANALOG section of this table.
EMIF1_SDCKE	2					O	External memory interface 1 SDRAM clock enable
SPIC_PICO	5					I/O	SPI-C Peripheral In, Controller Out (PICO)
SENT3	10					I/O	SENT Input Pin 3
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
ESC_LED_RUN	13					O	
ADCE_EXTMUXSEL2	14					O	External ADC selection Mux output
ESC_GPO22	15					O	EtherCAT General-Purpose Output 22
GPIO249	0, 4, 8, 12	N13	74	63		I/O	General-Purpose Input Output 249 This pin also has analog functions which are described in the ANALOG section of this table.
SPIC_CLK	5					I/O	SPI-C Clock
SENT4	10					I/O	SENT Input Pin 4
SD1_D2	11					I	SDFM-1 Channel 2 Data Input
ESC_PHY0_LINKSTATUS	13					I	EtherCAT PHY-0 Link Status
ADCE_EXTMUXSEL3	14					O	External ADC selection Mux output
ESC_GPO23	15					O	EtherCAT General-Purpose Output 23
AIO206	0, 4, 8, 12	T10				I	Analog Pin Used For Digital Input 206 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_C4	11					I	SDFM-3 Channel 4 Clock Input
AIO207	0, 4, 8, 12	T9				I	Analog Pin Used For Digital Input 207 This pin also has analog functions which are described in the ANALOG section of this table.
SD3_D4	11					I	SDFM-3 Channel 4 Data Input
AIO208	0, 4, 8, 12	R10				I	Analog Pin Used For Digital Input 208 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C2	11					I	SDFM-2 Channel 2 Clock Input
AIO209	0, 4, 8, 12	R9				I	Analog Pin Used For Digital Input 209 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D2	11					I	SDFM-2 Channel 2 Data Input
AIO210	0, 4, 8, 12	P9				I	Analog Pin Used For Digital Input 210 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C3	11					I	SDFM-2 Channel 3 Clock Input
AIO211	0, 4, 8, 12	N9				I	Analog Pin Used For Digital Input 211 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D3	11					I	SDFM-2 Channel 3 Data Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
AIO212	0, 4, 8, 12	P10				I	Analog Pin Used For Digital Input 212 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_C4	11					I	SDFM-2 Channel 4 Clock Input
AIO213	0, 4, 8, 12	T11				I	Analog Pin Used For Digital Input 213 This pin also has analog functions which are described in the ANALOG section of this table.
SD2_D4	11					I	SDFM-2 Channel 4 Data Input
GPIO0	0, 4, 8, 12	A8	160	128	88	I/O	General-Purpose Input Output 0
EPWM1_A	1					O	ePWM-1 Output A
EMIF1_A13	2					O	External memory interface 1 address line 13
EMIF1_D0	3					I/O	External memory interface 1 data line 0
MCAND_TX	5					O	MCAN-D Transmit
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
UARTE_TX	7					I/O	UART-E Serial Data Transmit
OUTPUTXBAR9	9					O	Output X-BAR Output 9
ESC_TX0_DATA0	10					O	EtherCAT MII Transmit-0 Data-0
ESC_GPI0	11					I	EtherCAT General-Purpose Input 0
FSITXA_D0	13					O	FSITX-A Primary Data Output
GPIO1	0, 4, 8, 12	A7	161	129	89	I/O	General-Purpose Input Output 1
EPWM1_B	1					O	ePWM-1 Output B
EMIF1_A14	2					O	External memory interface 1 address line 14
EMIF1_D3	3					I/O	External memory interface 1 data line 3
MCAND_RX	5					I	MCAN-D Receive
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
UARTE_RX	7					I/O	UART-E Serial Data Receive
OUTPUTXBAR10	9					O	Output X-BAR Output 10
ESC_TX1_DATA0	10					O	EtherCAT MII Transmit-1 Data-0
ESC_GPI1	11					I	EtherCAT General-Purpose Input 1
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output
GPIO2	0, 4, 8, 12	B7	162	130	90	I/O	General-Purpose Input Output 2
EPWM2_A	1					O	ePWM-2 Output A
EMIF1_A15	2					O	External memory interface 1 address line 15
EMIF1_D4	3					I/O	External memory interface 1 data line 4
UARTA_TX	5					I/O	UART-A Serial Data Transmit
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
MCANF_TX	7					O	MCAN-F Transmit
OUTPUTXBAR1	9					O	Output X-BAR Output 1
ESC_RX1_ERR	10					I	EtherCAT MII Receive-1 Error
ESC_GPI2	11					I	EtherCAT General-Purpose Input 2
FSITXA_CLK	13					O	FSITX-A Output Clock
GPIO3	0, 4, 8, 12	C7	163	131	91	I/O	General-Purpose Input Output 3
EPWM2_B	1					O	ePWM-2 Output B
EMIF1_A16	2					O	External memory interface 1 address line 16
EMIF1_D5	3					I/O	External memory interface 1 data line 5
UARTA_RX	5					I/O	UART-A Serial Data Receive
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
MCANF_RX	7					I	MCAN-F Receive
OUTPUTXBAR2	9					O	Output X-BAR Output 2
ESC_GPI3	11					I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13					I	FSIRX-A Primary Data Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO4	0, 4, 8, 12	D7	164	132	92	I/O	General-Purpose Input Output 4
EPWM3_A	1					O	ePWM-3 Output A
EMIF1_A17	2					O	External memory interface 1 address line 17
EMIF1_D9	3					I/O	External memory interface 1 data line 9
MCANC_TX	5					O	MCAN-C Transmit
UARTF_TX	7					I/O	UART-F Serial Data Transmit
OUTPUTXBAR3	9					O	Output X-BAR Output 3
ESC_GPI4	11					I	EtherCAT General-Purpose Input 4
FSIRXA_D1	13					I	FSIRX-A Optional Additional Data Input
ERRORSTS	15					O	Error Status Output. This signal requires an external pulldown.
GPIO5	0, 4, 8, 12	A6	165	133	93	I/O	General-Purpose Input Output 5
EPWM3_B	1					O	ePWM-3 Output B
EMIF1_A18	2					O	External memory interface 1 address line 18
EMIF1_D10	3					I/O	External memory interface 1 data line 10
MCANC_RX	5					I	MCAN-C Receive
UARTF_RX	7					I/O	UART-F Serial Data Receive
OUTPUTXBAR11	9					O	Output X-BAR Output 11
OUTPUTXBAR3	10					O	Output X-BAR Output 3
ESC_GPI5	11					I	EtherCAT General-Purpose Input 5
FSIRXA_CLK	13					I	FSIRX-A Input Clock
GPIO6	0, 4, 8, 12	B6	166	134	94	I/O	General-Purpose Input Output 6
EPWM4_A	1					O	ePWM-4 Output A
EMIF1_DQM0	2					O	External memory interface 1 Input/output mask for byte 0
EMIF1_CLK	3					O	External memory interface 1 clock
MCANB_TX	5					O	MCAN-B Transmit
LINA_TX	6					O	LIN-A Transmit
OUTPUTXBAR4	9					O	Output X-BAR Output 4
SYNCOUT	10					O	External ePWM Synchronization Pulse
ESC_GPI6	11					I	EtherCAT General-Purpose Input 6
FSITXB_D0	13					O	FSITX-B Primary Data Output
GPIO7	0, 4, 8, 12	C6	167	135		I/O	General-Purpose Input Output 7
EPWM4_B	1					O	ePWM-4 Output B
EMIF1_DQM1	2					O	External memory interface 1 Input/output mask for byte 1
EMIF1_CAS	3					O	External memory interface 1 column address strobe
MCANB_RX	5					I	MCAN-B Receive
LINA_RX	6					I	LIN-A Receive
OUTPUTXBAR5	9					O	Output X-BAR Output 5
ESC_GPI7	11					I	EtherCAT General-Purpose Input 7
FSITXB_D1	13					O	FSITX-B Optional Additional Data Output

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO8	0, 4, 8, 12	D6	170	138	96	I/O	General-Purpose Input Output 8
EPWM5_A	1					O	ePWM-5 Output A
EMIF1_RAS	2					O	External memory interface 1 row address strobe
EPWM4_B	3					O	ePWM-4 Output B
MCANC_TX	5					O	MCAN-C Transmit
SPIE_PICO	6					I/O	SPI-E Peripheral In, Controller Out (PICO)
UARTD_TX	7					I/O	UART-D Serial Data Transmit
OUTPUTXBAR12	9					O	Output X-BAR Output 12
ADCSOCAO	10					O	ADC Start of Conversion A Output for External ADC (from ePWM modules)
ESC_GPO0	11					O	EtherCAT General-Purpose Output 0
FSITXB_CLK	13					O	FSITX-B Output Clock
FSITXA_D1	14					O	FSITX-A Optional Additional Data Output
FSIRXA_D0	15					I	FSIRX-A Primary Data Input
GPIO9	0, 4, 8, 12	A5	171	139	97	I/O	General-Purpose Input Output 9
EPWM5_B	1					O	ePWM-5 Output B
EMIF1_D11	2					I/O	External memory interface 1 data line 11
SPIE_POCI	6					I/O	SPI-E Peripheral Out, Controller In (POCI)
UARTD_RX	7					I/O	UART-D Serial Data Receive
OUTPUTXBAR6	9					O	Output X-BAR Output 6
ESC_TX0_CLK	10					I	EtherCAT MII Transmit-0 Clock
ESC_GPO1	11					O	EtherCAT General-Purpose Output 1
FSIRXB_D0	13					I	FSIRX-B Primary Data Input
FSITXA_D0	14					O	FSITX-A Primary Data Output
FSIRXA_CLK	15					I	FSIRX-A Input Clock
GPIO10	0, 4, 8, 12	C5	172	140	98	I/O	General-Purpose Input Output 10
EPWM8_A	1					O	ePWM-8 Output A
PMBUSA_SCL	2					I/OD	PMBus-A Open-Drain Bidirectional Clock
ADCSOCBO	3					O	ADC Start of Conversion B Output for External ADC (from ePWM modules)
MCANC_RX	5					I	MCAN-C Receive
UARTC_TX	6					I/O	UART-C Serial Data Transmit
I2CA_SCL	7					I/OD	I2C-A Open-Drain Bidirectional Clock
SENT2	9					I/O	SENT Input Pin 2
ESC_GPI19	13					I	EtherCAT General-Purpose Input 19
ADCA_EXTMUXSEL2	14					O	External ADC selection Mux output
OUTPUTXBAR13	15					O	Output X-BAR Output 13
GPIO11	0, 4, 8, 12	A4	173	141	99	I/O	General-Purpose Input Output 11
EPWM6_B	1					O	ePWM-6 Output B
EMIF1_D15	2					I/O	External memory interface 1 data line 15
EPWM7_B	3					O	ePWM-7 Output B
SPIE_PTE	6					I/O	SPI-E Peripheral Transmit Enable (PTE)
SD4_D1	7					I	SDFM-4 Channel 1 Data Input
PMBUSA_ALERT	9					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
ESC_TX0_DATA1	10					O	EtherCAT MII Transmit-0 Data-1
ESC_GPO3	11					O	EtherCAT General-Purpose Output 3
FSIRXB_CLK	13					I	FSIRX-B Input Clock
FSIRXA_D1	14					I	FSIRX-A Optional Additional Data Input
OUTPUTXBAR7	15					O	Output X-BAR Output 7

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO12	0, 4, 8, 12	A3	174	142	100	I/O	General-Purpose Input Output 12
EPWM7_A	1					O	ePWM-7 Output A
EMIF1_A1	2					O	External memory interface 1 address line 1
ADCSOCAO	3					O	ADC Start of Conversion A Output for External ADC (from ePWM modules)
SPIE_CLK	6					I/O	SPI-E Clock
SD4_C2	7					I	SDFM-4 Channel 2 Clock Input
PMBUSA_CTL	9					I/O	PMBus-A Control Signal - Target Input/Controller Output
ESC_TX0_DATA2	10					O	EtherCAT MII Transmit-0 Data-2
ESC_GPO4	11					O	EtherCAT General-Purpose Output 4
FSIRXC_D0	13					I	FSIRX-C Primary Data Input
FSIRXA_D0	14					I	FSIRX-A Primary Data Input
OUTPUTXBAR14	15					O	Output X-BAR Output 14
GPIO13	0, 4, 8, 12	A2	175	143		I/O	General-Purpose Input Output 13
EPWM7_B	1					O	ePWM-7 Output B
EMIF1_CS0n	2					O	External memory interface 1 chip select 0
EMIF1_D9	3					I/O	External memory interface 1 data line 9
UARTC_RX	6					I/O	UART-C Serial Data Receive
SD4_D2	7					I	SDFM-4 Channel 2 Data Input
PMBUSA_SDA	9					I/OD	PMBus-A Open-Drain Bidirectional Data
ESC_TX0_DATA3	10					O	EtherCAT MII Transmit-0 Data-3
ESC_GPO5	11					O	EtherCAT General-Purpose Output 5
FSIRXC_D1	13					I	FSIRX-C Optional Additional Data Input
FSIRXA_CLK	14					I	FSIRX-A Input Clock
OUTPUTXBAR15	15					O	Output X-BAR Output 15
GPIO14	0, 4, 8, 12	B3	176	144		I/O	General-Purpose Input Output 14
EPWM6_A	1					O	ePWM-6 Output A
EMIF1_D17	2					I/O	External memory interface 1 data line 17
EPWM18_A	3					O	ePWM-18 Output A
EMIF1_D13	5					I/O	External memory interface 1 data line 13
LINA_TX	6					O	LIN-A Transmit
OUTPUTXBAR3	7					O	Output X-BAR Output 3
PMBUSA_SCL	9					I/OD	PMBus-A Open-Drain Bidirectional Clock
ESC_PHY1_LINKSTATUS	10					I	EtherCAT PHY-1 Link Status
ESC_GPO6	11					O	EtherCAT General-Purpose Output 6
FSIRXC_CLK	13					I	FSIRX-C Input Clock
SD4_C1	14					I	SDFM-4 Channel 1 Clock Input
OUTPUTXBAR8	15					O	Output X-BAR Output 8
GPIO15	0, 4, 8, 12	C4	1	1	1	I/O	General-Purpose Input Output 15
EPWM8_B	1					O	ePWM-8 Output B
PMBUSA_CTL	3					I/O	PMBus-A Control Signal - Target Input/Controller Output
I2CA_SDA	5					I/OD	I2C-A Open-Drain Bidirectional Data
LINA_RX	6					I	LIN-A Receive
OUTPUTXBAR4	7					O	Output X-BAR Output 4
SENT1	9					I/O	SENT Input Pin 1
ESC_GPO7	10					O	EtherCAT General-Purpose Output 7
ESC_GPI20	13					I	EtherCAT General-Purpose Input 20
ADCA_EXTMUXSEL3	14					O	External ADC selection Mux output
OUTPUTXBAR16	15					O	Output X-BAR Output 16

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO16	0, 4, 8, 12	D5	2	2	2	I/O	General-Purpose Input Output 16
EPWM9_A	1					O	ePWM-9 Output A
EMIF1_D29	2					I/O	External memory interface 1 data line 29
EMIF1_BA0	3					O	External memory interface 1 bank address 0
SPIA_PICO	5					I/O	SPI-A Peripheral In, Controller Out (PICO)
MCAND_TX	7					O	MCAN-D Transmit
ESC_RX1_CLK	10					I	EtherCAT MII Receive-1 Clock
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
FSIRXD_D1	13					I	FSIRX-D Optional Additional Data Input
FSIRXC_CLK	14					I	FSIRX-C Input Clock
OUTPUTXBAR7	15					O	Output X-BAR Output 7
GPIO17	0, 4, 8, 12	B2	4	4	4	I/O	General-Purpose Input Output 17
EPWM9_B	1					O	ePWM-9 Output B
EMIF1_DQM3	2					O	External memory interface 1 Input/output mask for byte 3
EMIF1_BA1	3					O	External memory interface 1 bank address 1
SPIA_POCI	5					I/O	SPI-A Peripheral Out, Controller In (POCI)
MCAND_RX	7					I	MCAN-D Receive
ESC_RX1_DV	10					I	EtherCAT MII Receive-1 Data Valid
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
FSIRXD_CLK	13					I	FSIRX-D Input Clock
UARTC_TX	14					I/O	UART-C Serial Data Transmit
OUTPUTXBAR8	15					O	Output X-BAR Output 8
GPIO18	0, 4, 8, 12	F2	13	10	8	I/O	General-Purpose Input Output 18
EPWM15_A	1					O	ePWM-15 Output A
PMBUSA_ALERT	3					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
I2CA_SCL	5					I/OD	I2C-A Open-Drain Bidirectional Clock
UARTC_RX	6					I/O	UART-C Serial Data Receive
SENT4	9					I/O	SENT Input Pin 4
ESC_GPI21	13					I	EtherCAT General-Purpose Input 21
ADCB_EXTMUXSEL0	14					O	External ADC selection Mux output
GPIO19	0, 4, 8, 12	B1	5	5		I/O	General-Purpose Input Output 19
EPWM10_B	1					O	ePWM-10 Output B
EMIF1_CS3n	2					O	External memory interface 1 chip select 3
ADCSOCBO	3					O	ADC Start of Conversion B Output for External ADC (from ePWM modules)
SPIA_PTE	5					I/O	SPI-A Peripheral Transmit Enable (PTE)
UARTE_RX	6					I/O	UART-E Serial Data Receive
MCANC_TX	7					O	MCAN-C Transmit
PMBUSA_ALERT	9					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
ESC_TX1_DATA3	10					O	EtherCAT MII Transmit-1 Data-3
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
GPIO20	0, 4, 8, 12	C1	6			I/O	General-Purpose Input Output 20
EPWM11_A	1					O	ePWM-11 Output A
EMIF1_BA0	2					O	External memory interface 1 bank address 0
EMIF1_DQM2	3					O	External memory interface 1 Input/output mask for byte 2
SPIC_PICO	6					I/O	SPI-C Peripheral In, Controller Out (PICO)
MCANB_RX	7					I	MCAN-B Receive
ESC_TX1_DATA2	10					O	EtherCAT MII Transmit-1 Data-2
SD1_D3	11					I	SDFM-1 Channel 3 Data Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO21	0, 4, 8, 12					I/O	General-Purpose Input Output 21
EPWM11_B	1					O	ePWM-11 Output B
EMIF1_BA1	2					O	External memory interface 1 bank address 1
SPIC_POCI	6	C2	7			I/O	SPI-C Peripheral Out, Controller In (POCI)
MCANB_TX	7					O	MCAN-B Transmit
ESC_TX1_DATA1	10					O	EtherCAT MII Transmit-1 Data-1
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
GPIO22	0, 4, 8, 12					I/O	General-Purpose Input Output 22
EPWM12_A	1					O	ePWM-12 Output A
PMBUSA_SDA	3					I/OD	PMBus-A Open-Drain Bidirectional Data
I2CB_SDA	5					I/OD	I2C-B Open-Drain Bidirectional Data
UARTB_TX	6					I/O	UART-B Serial Data Transmit
MCANC_TX	7	F1	14	11	9	O	MCAN-C Transmit
SENT5	9					I/O	SENT Input Pin 5
ESC_GPO2	10					O	EtherCAT General-Purpose Output 2
ESC_GPI22	13					I	EtherCAT General-Purpose Input 22
ADCB_EXTMUXSEL1	14					O	External ADC selection Mux output
GPIO23	0, 4, 8, 12					I/O	General-Purpose Input Output 23
EPWM12_B	1					O	ePWM-12 Output B
PMBUSA_SCL	3					I/OD	PMBus-A Open-Drain Bidirectional Clock
I2CB_SCL	5					I/OD	I2C-B Open-Drain Bidirectional Clock
UARTB_RX	6					I/O	UART-B Serial Data Receive
MCANC_RX	7	B8	159	127	87	I	MCAN-C Receive
SENT6	9					I/O	SENT Input Pin 6
ESC_PHY_RESETn	10					O	EtherCAT PHY Active Low Reset
ESC_GPI23	13					I	EtherCAT General-Purpose Input 23
ADCC_EXTMUXSEL0	14					O	External ADC selection Mux output
GPIO24	0, 4, 8, 12					I/O	General-Purpose Input Output 24
EPWM13_A	1					O	ePWM-13 Output A
EMIF1_DQM0	2					O	External memory interface 1 Input/output mask for byte 0
SPIB_PICO	5					I/O	SPI-B Peripheral In, Controller Out (PICO)
LINB_TX	6					O	LIN-B Transmit
MCANE_TX	7	C8	158	126		O	MCAN-E Transmit
ESC_RX0_CLK	10					I	EtherCAT MII Receive-0 Clock
SD2_D1	11					I	SDFM-2 Channel 1 Data Input
ESC_GPI24	13					I	EtherCAT General-Purpose Input 24
EPWM2_A	14					O	ePWM-2 Output A
OUTPUTXBAR1	15					O	Output X-BAR Output 1

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO25	0, 4, 8, 12	D8	157	125	86	I/O	General-Purpose Input Output 25
EPWM13_B	1					O	ePWM-13 Output B
EMIF1_DQM1	2					O	External memory interface 1 Input/output mask for byte 1
SPIB_POCI	5					I/O	SPI-B Peripheral Out, Controller In (POCI)
LINB_RX	6					I	LIN-B Receive
MCANE_RX	7					I	MCAN-E Receive
PMBUSA_SDA	9					I/OD	PMBus-A Open-Drain Bidirectional Data
ESC_RX0_DV	10					I	EtherCAT MII Receive-0 Data Valid
SD2_C1	11					I	SDFM-2 Channel 1 Clock Input
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output
EPWM2_B	14					O	ePWM-2 Output B
OUTPUTXBAR2	15					O	Output X-BAR Output 2
GPIO26	0, 4, 8, 12	B9	156	124	85	I/O	General-Purpose Input Output 26
EPWM14_A	1					O	ePWM-14 Output A
EMIF1_DQM2	2					O	External memory interface 1 Input/output mask for byte 2
SPIB_CLK	5					I/O	SPI-B Clock
UARTE_TX	6					I/O	UART-E Serial Data Transmit
MCANE_TX	7					O	MCAN-E Transmit
PMBUSA_CTL	9					I/O	PMBus-A Control Signal - Target Input/Controller Output
ESC_RX0_ERR	10					I	EtherCAT MII Receive-0 Error
SD2_D2	11					I	SDFM-2 Channel 2 Data Input
FSITXA_D0	13					O	FSITX-A Primary Data Output
ESC_MDIO_CLK	14					O	EtherCAT MDIO Clock
OUTPUTXBAR3	15					O	Output X-BAR Output 3
GPIO27	0, 4, 8, 12	C9	155			I/O	General-Purpose Input Output 27
EPWM14_B	1					O	ePWM-14 Output B
EMIF1_DQM3	2					O	External memory interface 1 Input/output mask for byte 3
SPIB_PTE	5					I/O	SPI-B Peripheral Transmit Enable (PTE)
UARTA_TX	6					I/O	UART-A Serial Data Transmit
EPWM4_A	9					O	ePWM-4 Output A
ESC_RX0_DATA0	10					I	EtherCAT MII Receive-0 Data-0
SD2_C2	11					I	SDFM-2 Channel 2 Clock Input
FSITXA_CLK	13					O	FSITX-A Output Clock
ESC_MDIO_DATA	14					I/O	EtherCAT MDIO Data
OUTPUTXBAR4	15					O	Output X-BAR Output 4
GPIO28	0, 4, 8, 12	D9	154			I/O	General-Purpose Input Output 28
EPWM15_A	1					O	ePWM-15 Output A
EMIF1_CS4n	2					O	External memory interface 1 chip select 4
EMIF1_CS2n	3					O	External memory interface 1 chip select 2
UARTA_RX	6					I/O	UART-A Serial Data Receive
EPWM4_B	9					O	ePWM-4 Output B
ESC_RX0_DATA1	10					I	EtherCAT MII Receive-0 Data-1
SD2_D3	11					I	SDFM-2 Channel 3 Data Input
OUTPUTXBAR5	15					O	Output X-BAR Output 5

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO29	0, 4, 8, 12	A9	151	121	84	I/O	General-Purpose Input Output 29
EPWM15_B	1					O	ePWM-15 Output B
PMBUSA_SDA	2					I/OD	PMBus-A Open-Drain Bidirectional Data
UARTE_RX	6					I/O	UART-E Serial Data Receive
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
SENT3	9					I/O	SENT Input Pin 3
ESC_LATCH0	10					I	EtherCAT LatchSignal Input 0
ESC_I2C_SDA	13					I/OC	EtherCAT I2C Data
ADCC_EXTMUXSEL1	14					O	External ADC selection Mux output
OUTPUTXBAR6	15					O	Output X-BAR Output 6
GPIO30	0, 4, 8, 12	A10	150	120	83	I/O	General-Purpose Input Output 30
EPWM16_A	1					O	ePWM-16 Output A
EMIF1_CLK	2					O	External memory interface 1 clock
EMIF1_CS4n	3					O	External memory interface 1 chip select 4
MCANC_RX	5					I	MCAN-C Receive
SPID_PICO	6					I/O	SPI-D Peripheral In, Controller Out (PICO)
EMIF1_A12	7					O	External memory interface 1 address line 12
ESC_LATCH1	10					I	EtherCAT LatchSignal Input 1
SD2_D4	11					I	SDFM-2 Channel 4 Data Input
ESC_I2C_SCL	13					I/OC	EtherCAT I2C Clock
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
OUTPUTXBAR7	15					O	Output X-BAR Output 7
GPIO31	0, 4, 8, 12	B10	149		82	I/O	General-Purpose Input Output 31
EPWM16_B	1					O	ePWM-16 Output B
EMIF1_WEn	2					O	External memory interface 1 write enable
EMIF1_RNW	3					O	External memory interface 1 read not write
MCANC_TX	5					O	MCAN-C Transmit
SPID_POCI	6					I/O	SPI-D Peripheral Out, Controller In (POCI)
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
ESC_RX1_DATA0	10					I	EtherCAT MII Receive-1 Data-0
SD2_C4	11					I	SDFM-2 Channel 4 Clock Input
FSITXD_D0	13					O	FSITX-D Primary Data Output
OUTPUTXBAR8	15					O	Output X-BAR Output 8
GPIO32	0, 4, 8, 12	G16	117	96		I/O	General-Purpose Input Output 32
EMIF1_CS0n	2					O	External memory interface 1 chip select 0
EMIF1_OEn	3					O	External memory interface 1 output enable
SPIA_PICO	5					I/O	SPI-A Peripheral In, Controller Out (PICO)
SPID_CLK	6					I/O	SPI-D Clock
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
OUTPUTXBAR9	9					O	Output X-BAR Output 9
ESC_RX0_DATA0	10					I	EtherCAT MII Receive-0 Data-0
GPIO33	0, 4, 8, 12	P14				I/O	General-Purpose Input Output 33
EMIF1_RNW	2					O	External memory interface 1 read not write
EMIF1_BA0	3					O	External memory interface 1 bank address 0
SPIA_POCI	5					I/O	SPI-A Peripheral Out, Controller In (POCI)
SPID_PTE	6					I/O	SPI-D Peripheral Transmit Enable (PTE)
I2CA_SCL	7					I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR10	9					O	Output X-BAR Output 10
ESC_LED_ERR	10					O	

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO34	0, 4, 8, 12	D1	9	7		I/O	General-Purpose Input Output 34
EPWM18_A	1					O	ePWM-18 Output A
EMIF1_CS2n	2					O	External memory interface 1 chip select 2
EMIF1_BA1	3					O	External memory interface 1 bank address 1
SPIA_CLK	5					I/O	SPI-A Clock
UARTF_TX	6					I/O	UART-F Serial Data Transmit
I2CB_SDA	7					I/OD	I2C-B Open-Drain Bidirectional Data
OUTPUTXBAR11	9					O	Output X-BAR Output 11
ESC_LATCH0	10					I	EtherCAT LatchSignal Input 0
EPWM3_B	13					O	ePWM-3 Output B
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
OUTPUTXBAR1	15					O	Output X-BAR Output 1
GPIO35	0, 4, 8, 12	E1	10			I/O	General-Purpose Input Output 35
EPWM18_B	1					O	ePWM-18 Output B
EMIF1_CS3n	2					O	External memory interface 1 chip select 3
EMIF1_A0	3					O	External memory interface 1 address line 0
SPIA_PTE	5					I/O	SPI-A Peripheral Transmit Enable (PTE)
UARTF_RX	6					I/O	UART-F Serial Data Receive
I2CB_SCL	7					I/OD	I2C-B Open-Drain Bidirectional Clock
OUTPUTXBAR12	9					O	Output X-BAR Output 12
ESC_LATCH1	10					I	EtherCAT LatchSignal Input 1
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
GPIO36	0, 4, 8, 12	N14				I/O	General-Purpose Input Output 36
EMIF1_WAIT	2					I	External memory interface 1 Asynchronous SRAM WAIT
EMIF1_A1	3					O	External memory interface 1 address line 1
UARTC_TX	5					I/O	UART-C Serial Data Transmit
MCANC_RX	6					I	MCAN-C Receive
OUTPUTXBAR13	9					O	Output X-BAR Output 13
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
EMIF1_WEn	14					O	External memory interface 1 write enable
GPIO37	0, 4, 8, 12	R16	85			I/O	General-Purpose Input Output 37
EPWM18_A	1					O	ePWM-18 Output A
EMIF1_OEn	2					O	External memory interface 1 output enable
EMIF1_A2	3					O	External memory interface 1 address line 2
UARTC_RX	5					I/O	UART-C Serial Data Receive
MCANC_TX	6					O	MCAN-C Transmit
OUTPUTXBAR14	9					O	Output X-BAR Output 14
ESC_RX1_DATA1	10					I	EtherCAT MII Receive-1 Data-1
SD1_D2	11					I	SDFM-1 Channel 2 Data Input
EMIF1_D24	14					I/O	External memory interface 1 data line 24
OUTPUTXBAR2	15					O	Output X-BAR Output 2

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO38	0, 4, 8, 12					I/O	General-Purpose Input Output 38
EPWM18_B	1					O	ePWM-18 Output B
EMIF1_A0	2					O	External memory interface 1 address line 0
EMIF1_A3	3					O	External memory interface 1 address line 3
UARTA_TX	5					I/O	UART-A Serial Data Transmit
SPIE_PICO	6	E14	125	104	72	I/O	SPI-E Peripheral In, Controller Out (PICO)
OUTPUTXBAR15	9					O	Output X-BAR Output 15
ESC_RX0_DATA1	10					I	EtherCAT MII Receive-0 Data-1
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
FSITXD_D1	13					O	FSITX-D Optional Additional Data Output
EMIF1_CS2n	14					O	External memory interface 1 chip select 2
GPIO39	0, 4, 8, 12					I/O	General-Purpose Input Output 39
EMIF1_A1	2					O	External memory interface 1 address line 1
EMIF1_A4	3					O	External memory interface 1 address line 4
UARTA_RX	5					I/O	UART-A Serial Data Receive
OUTPUTXBAR16	9	P15	86			O	Output X-BAR Output 16
ESC_MDIO_DATA	10					I/O	EtherCAT MDIO Data
SD1_D4	11					I	SDFM-1 Channel 4 Data Input
FSIRXD_CLK	13					I	FSIRX-D Input Clock
ESC_LED_RUN	15					O	
GPIO40	0, 4, 8, 12					I/O	General-Purpose Input Output 40
EPWM13_A	1					O	ePWM-13 Output A
EMIF1_A2	2					O	External memory interface 1 address line 2
MCANB_RX	5					I	MCAN-B Receive
I2CB_SDA	6	P16	87			I/OD	I2C-B Open-Drain Bidirectional Data
OUTPUTXBAR9	9					O	Output X-BAR Output 9
ESC_GPO2	10					O	EtherCAT General-Purpose Output 2
SD4_C3	11					I	SDFM-4 Channel 3 Clock Input
EPWM1_A	14					O	ePWM-1 Output A
SD2_C1	15					I	SDFM-2 Channel 1 Clock Input
GPIO41	0, 4, 8, 12					I/O	General-Purpose Input Output 41
EPWM13_B	1					O	ePWM-13 Output B
EMIF1_A3	2					O	External memory interface 1 address line 3
EPWM18_A	3					O	ePWM-18 Output A
MCANB_TX	5					O	MCAN-B Transmit
SPIE_POCI	6					I/O	SPI-E Peripheral Out, Controller In (POCI)
I2CB_SCL	7	N15	89	73	50	I/OD	I2C-B Open-Drain Bidirectional Clock
OUTPUTXBAR10	9					O	Output X-BAR Output 10
ESC_RX0_DATA2	10					I	EtherCAT MII Receive-0 Data-2
SD4_D3	11					I	SDFM-4 Channel 3 Data Input
FSIRXD_CLK	13					I	FSIRX-D Input Clock
EPWM1_B	14					O	ePWM-1 Output B
SD2_D1	15					I	SDFM-2 Channel 1 Data Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO42	0, 4, 8, 12	C16	130	107	74	I/O	General-Purpose Input Output 42
EPWM14_A	1					O	ePWM-14 Output A
EMIF1_A2	2					O	External memory interface 1 address line 2
EMIF1_A13	3					O	External memory interface 1 address line 13
UARTA_TX	5					I/O	UART-A Serial Data Transmit
SPIE_CLK	6					I/O	SPI-E Clock
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
OUTPUTXBAR13	9					O	Output X-BAR Output 13
SD4_C3	10					I	SDFM-4 Channel 3 Clock Input
SD4_C4	11					I	SDFM-4 Channel 4 Clock Input
FSIRXD_D0	13					I	FSIRX-D Primary Data Input
ADCE_EXTMUXSEL2	14					O	External ADC selection Mux output
GPIO43	0, 4, 8, 12	C15	131	108	75	I/O	General-Purpose Input Output 43
EPWM14_B	1					O	ePWM-14 Output B
EMIF1_A4	2					O	External memory interface 1 address line 4
EMIF1_D13	3					I/O	External memory interface 1 data line 13
UARTA_RX	5					I/O	UART-A Serial Data Receive
SPIE_PTE	6					I/O	SPI-E Peripheral Transmit Enable (PTE)
I2CA_SCL	7					I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR14	9					O	Output X-BAR Output 14
SD4_D4	11					I	SDFM-4 Channel 4 Data Input
FSIRXD_D1	13					I	FSIRX-D Optional Additional Data Input
ADCE_EXTMUXSEL3	14					O	External ADC selection Mux output
GPIO44	0, 4, 8, 12	G14	114			I/O	General-Purpose Input Output 44
EMIF1_A4	2					O	External memory interface 1 address line 4
SPID_POCI	5					I/O	SPI-D Peripheral Out, Controller In (POCI)
MCANB_RX	6					I	MCAN-B Receive
UARTB_TX	7					I/O	UART-B Serial Data Transmit
OUTPUTXBAR14	9					O	Output X-BAR Output 14
ESC_TX1_CLK	10					I	EtherCAT MII Transmit-1 Clock
SD3_C4	11					I	SDFM-3 Channel 4 Clock Input
FSIRXD_CLK	13					I	FSIRX-D Input Clock
GPIO45	0, 4, 8, 12	G15	116			I/O	General-Purpose Input Output 45
EMIF1_A5	2					O	External memory interface 1 address line 5
SPID_PTE	5					I/O	SPI-D Peripheral Transmit Enable (PTE)
MCANB_TX	6					O	MCAN-B Transmit
UARTB_RX	7					I/O	UART-B Serial Data Receive
OUTPUTXBAR15	9					O	Output X-BAR Output 15
ESC_TX1_ENA	10					I/O	EtherCAT MII Transmit-1 Enable
SD3_D4	11					I	SDFM-3 Channel 4 Data Input
FSIRXD_D0	13					I	FSIRX-D Primary Data Input
GPIO46	0, 4, 8, 12	D14	128			I/O	General-Purpose Input Output 46
EPWM4_A	1					O	ePWM-4 Output A
EMIF1_A6	2					O	External memory interface 1 address line 6
EPWM14_A	3					O	ePWM-14 Output A
UARTC_TX	5					I/O	UART-C Serial Data Transmit
MCANE_TX	7					O	MCAN-E Transmit
ESC_MDIO_CLK	10					O	EtherCAT MDIO Clock
SD3_C4	11					I	SDFM-3 Channel 4 Clock Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO47	0, 4, 8, 12	D15	129			I/O	General-Purpose Input Output 47
EPWM4_B	1					O	ePWM-4 Output B
EMIF1_A7	2					O	External memory interface 1 address line 7
EPWM14_B	3					O	ePWM-14 Output B
UARTC_RX	5					I/O	UART-C Serial Data Receive
MCANE_RX	7					I	MCAN-E Receive
ESC_MDIO_DATA	10					I/O	EtherCAT MDIO Data
SD4_C3	11					I	SDFM-4 Channel 3 Clock Input
GPIO48	0, 4, 8, 12	N16	90			I/O	General-Purpose Input Output 48
EMIF1_A8	2					O	External memory interface 1 address line 8
UARTD_TX	5					I/O	UART-D Serial Data Transmit
OUTPUTXBAR3	9					O	Output X-BAR Output 3
ESC_PHY_CLK	10					O	EtherCAT PHY Clock
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
EPWM3_A	13					O	ePWM-3 Output A
SD2_C2	15					I	SDFM-2 Channel 2 Clock Input
GPIO49	0, 4, 8, 12	M15	92	75		I/O	General-Purpose Input Output 49
EMIF1_A9	2					O	External memory interface 1 address line 9
EMIF1_A5	3					O	External memory interface 1 address line 5
UARTD_RX	5					I/O	UART-D Serial Data Receive
OUTPUTXBAR4	9					O	Output X-BAR Output 4
ESC_TX1_DATA2	10					O	EtherCAT MII Transmit-1 Data-2
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
FSITXA_D0	13					O	FSITX-A Primary Data Output
SD2_D1	15					I	SDFM-2 Channel 1 Data Input
GPIO50	0, 4, 8, 12	M14	93	76		I/O	General-Purpose Input Output 50
EPWM15_A	1					O	ePWM-15 Output A
EMIF1_A10	2					O	External memory interface 1 address line 10
EMIF1_A6	3					O	External memory interface 1 address line 6
SPIC_PICO	6					I/O	SPI-C Peripheral In, Controller Out (PICO)
MCANF_TX	7					O	MCAN-F Transmit
ESC_TX1_DATA1	10					O	EtherCAT MII Transmit-1 Data-1
SD1_D2	11					I	SDFM-1 Channel 2 Data Input
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output
ESC_GPI25	14					I	EtherCAT General-Purpose Input 25
SD2_D2	15					I	SDFM-2 Channel 2 Data Input
GPIO51	0, 4, 8, 12	M13	94	77		I/O	General-Purpose Input Output 51
EPWM15_B	1					O	ePWM-15 Output B
EMIF1_A11	2					O	External memory interface 1 address line 11
EMIF1_A7	3					O	External memory interface 1 address line 7
SPIC_POCI	6					I/O	SPI-C Peripheral Out, Controller In (POCI)
MCANF_RX	7					I	MCAN-F Receive
ESC_TX1_CLK	10					I	EtherCAT MII Transmit-1 Clock
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
FSITXA_CLK	13					O	FSITX-A Output Clock
ESC_GPI26	14					I	EtherCAT General-Purpose Input 26
SD2_D3	15					I	SDFM-2 Channel 3 Data Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO52	0, 4, 8, 12	L14	95	78		I/O	General-Purpose Input Output 52
EPWM16_A	1					O	ePWM-16 Output A
EMIF1_A12	2					O	External memory interface 1 address line 12
EMIF1_A8	3					O	External memory interface 1 address line 8
UARTD_TX	5					I/O	UART-D Serial Data Transmit
SPIC_CLK	6					I/O	SPI-C Clock
ESC_TX1_ENA	10					I/O	EtherCAT MII Transmit-1 Enable
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
FSIRXA_D0	13					I	FSIRX-A Primary Data Input
SD2_D4	15					I	SDFM-2 Channel 4 Data Input
GPIO53	0, 4, 8, 12	L15	96	79		I/O	General-Purpose Input Output 53
EPWM16_B	1					O	ePWM-16 Output B
EMIF1_D31	2					I/O	External memory interface 1 data line 31
EMIF1_A9	3					O	External memory interface 1 address line 9
UARTD_RX	5					I/O	UART-D Serial Data Receive
SPIC_PTE	6					I/O	SPI-C Peripheral Transmit Enable (PTE)
ESC_PHY0_LINKSTATUS	10					I	EtherCAT PHY-0 Link Status
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
FSIRXA_D1	13					I	FSIRX-A Optional Additional Data Input
ESC_GPI28	14					I	EtherCAT General-Purpose Input 28
SD1_C1	15					I	SDFM-1 Channel 1 Clock Input
GPIO54	0, 4, 8, 12	L16	97	80		I/O	General-Purpose Input Output 54
EMIF1_D30	2					I/O	External memory interface 1 data line 30
EMIF1_A10	3					O	External memory interface 1 address line 10
SPIA_PICO	5					I/O	SPI-A Peripheral In, Controller Out (PICO)
ESC_PHY_CLK	10					O	EtherCAT PHY Clock
SD1_D4	11					I	SDFM-1 Channel 4 Data Input
FSIRXA_CLK	13					I	FSIRX-A Input Clock
ESC_GPI29	14					I	EtherCAT General-Purpose Input 29
SD1_C2	15					I	SDFM-1 Channel 2 Clock Input
GPIO55	0, 4, 8, 12	K13	99			I/O	General-Purpose Input Output 55
EPWM16_B	1					O	ePWM-16 Output B
EMIF1_D29	2					I/O	External memory interface 1 data line 29
EMIF1_D0	3					I/O	External memory interface 1 data line 0
SPIA_POCI	5					I/O	SPI-A Peripheral Out, Controller In (POCI)
EMIF1_WAIT	6					I	External memory interface 1 Asynchronous SRAM WAIT
ESC_PHY0_LINKSTATUS	10					I	EtherCAT PHY-0 Link Status
SD1_C4	11					I	SDFM-1 Channel 4 Clock Input
FSITXB_D0	13					O	FSITX-B Primary Data Output
SD1_C3	15					I	SDFM-1 Channel 3 Clock Input

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO56	0, 4, 8, 12	K14	100	82		I/O	General-Purpose Input Output 56
EPWM17_A	1					O	ePWM-17 Output A
EMIF1_D28	2					I/O	External memory interface 1 data line 28
EMIF1_D1	3					I/O	External memory interface 1 data line 1
SPIA_CLK	5					I/O	SPI-A Clock
MCAND_TX	6					O	MCAN-D Transmit
I2CA_SDA	7					I/OD	I2C-A Open-Drain Bidirectional Data
ESC_PDI_UC_IRQ	10					O	EtherCAT PDI IRQ Interrupt Line
SD2_D1	11					I	SDFM-2 Channel 1 Data Input
FSITXB_CLK	13					O	FSITX-B Output Clock
ESC_GPI30	14					I	EtherCAT General-Purpose Input 30
SD1_C4	15					I	SDFM-1 Channel 4 Clock Input
GPIO57	0, 4, 8, 12	K15	102	84		I/O	General-Purpose Input Output 57
EPWM17_B	1					O	ePWM-17 Output B
EMIF1_D27	2					I/O	External memory interface 1 data line 27
EMIF1_D2	3					I/O	External memory interface 1 data line 2
SPIA_PTE	5					I/O	SPI-A Peripheral Transmit Enable (PTE)
MCAND_RX	6					I	MCAN-D Receive
I2CA_SCL	7					I/OD	I2C-A Open-Drain Bidirectional Clock
ESC_MDIO_DATA	10					I/O	EtherCAT MDIO Data
SD2_C1	11					I	SDFM-2 Channel 1 Clock Input
FSITXB_D1	13					O	FSITX-B Optional Additional Data Output
ESC_GPI31	14					I	EtherCAT General-Purpose Input 31
SD3_D3	15					I	SDFM-3 Channel 3 Data Input
GPIO58	0, 4, 8, 12	K16	103	85	53	I/O	General-Purpose Input Output 58
EPWM13_A	1					O	ePWM-13 Output A
EMIF1_D26	2					I/O	External memory interface 1 data line 26
EPWM8_A	3					O	ePWM-8 Output A
SPIA_PICO	5					I/O	SPI-A Peripheral In, Controller Out (PICO)
MCANC_RX	7					I	MCAN-C Receive
SENT1	9					I/O	SENT Input Pin 1
ESC_LED_LINK0_ACTIVE	10					O	EtherCAT Link-0 Active
SD2_D2	11					I	SDFM-2 Channel 2 Data Input
FSIRXB_D0	13					I	FSIRX-B Primary Data Input
ESC_TX0_DATA3	14					O	EtherCAT MII Transmit-0 Data-3
SD2_C2	15					I	SDFM-2 Channel 2 Clock Input
GPIO59	0, 4, 8, 12	J16	104	86	54	I/O	General-Purpose Input Output 59
EPWM5_A	1					O	ePWM-5 Output A
EMIF1_D25	2					I/O	External memory interface 1 data line 25
EPWM8_B	3					O	ePWM-8 Output B
SPIA_POCI	5					I/O	SPI-A Peripheral Out, Controller In (POCI)
MCANC_TX	7					O	MCAN-C Transmit
SENT2	9					I/O	SENT Input Pin 2
ESC_LED_LINK1_ACTIVE	10					O	EtherCAT Link-1 Active
SD2_C2	11					I	SDFM-2 Channel 2 Clock Input
FSIRXB_D1	13					I	FSIRX-B Optional Additional Data Input
ESC_TX0_ENA	14					I/O	EtherCAT MII Transmit-0 Enable
SD2_C3	15					I	SDFM-2 Channel 3 Clock Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO60	0, 4, 8, 12					I/O	General-Purpose Input Output 60
EPWM3_B	1					O	ePWM-3 Output B
EMIF1_D24	2					I/O	External memory interface 1 data line 24
EMIF1_D0	3					I/O	External memory interface 1 data line 0
SPIA_CLK	5					I/O	SPI-A Clock
OUTPUTXBAR3	6	J15	106	88	56	O	Output X-BAR Output 3
SENT3	9					I/O	SENT Input Pin 3
ESC_LED_ERR	10					O	
ESC_LATCH0	11					I	EtherCAT LatchSignal Input 0
FSIRXB_CLK	13					I	FSIRX-B Input Clock
SD2_C4	15					I	SDFM-2 Channel 4 Clock Input
GPIO61	0, 4, 8, 12					I/O	General-Purpose Input Output 61
EPWM17_B	1					O	ePWM-17 Output B
EMIF1_D23	2					I/O	External memory interface 1 data line 23
EMIF1_D6	3					I/O	External memory interface 1 data line 6
SPIA_PTE	5					I/O	SPI-A Peripheral Transmit Enable (PTE)
MCANC_RX	7	J13	108	89	57	I	MCAN-C Receive
OUTPUTXBAR4	9					O	Output X-BAR Output 4
ESC_LED_RUN	10					O	
SD2_C3	11					I	SDFM-2 Channel 3 Clock Input
FSITXD_CLK	13					O	FSITX-D Output Clock
ESC_LATCH1	14					I	EtherCAT LatchSignal Input 1
GPIO62	0, 4, 8, 12					I/O	General-Purpose Input Output 62
EPWM17_A	1					O	ePWM-17 Output A
EMIF1_D22	2					I/O	External memory interface 1 data line 22
EMIF1_D7	3					I/O	External memory interface 1 data line 7
MCANC_RX	6					I	MCAN-C Receive
MCANC_TX	7	H13	109	90	58	O	MCAN-C Transmit
SENT4	9					I/O	SENT Input Pin 4
ESC_LED_STATE_RUN	10					O	
SD2_D4	11					I	SDFM-2 Channel 4 Data Input
FSITXD_D0	13					O	FSITX-D Primary Data Output
ESC_MDIO_CLK	14					O	EtherCAT MDIO Clock
GPIO63	0, 4, 8, 12					I/O	General-Purpose Input Output 63
EPWM9_A	1					O	ePWM-9 Output A
EMIF1_D21	2					I/O	External memory interface 1 data line 21
EMIF1_RNW	3					O	External memory interface 1 read not write
SPIB_PICO	5					I/O	SPI-B Peripheral In, Controller Out (PICO)
MCANC_TX	6	H14	110	91	59	O	MCAN-C Transmit
SENT5	9					I/O	SENT Input Pin 5
ESC_RX1_DATA0	10					I	EtherCAT MII Receive-1 Data-0
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
FSITXD_D1	13					O	FSITX-D Optional Additional Data Output
ADCD_EXTMUXSEL0	14					O	External ADC selection Mux output
SD2_C4	15					I	SDFM-2 Channel 4 Clock Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO64	0, 4, 8, 12	H15	111	92	60	I/O	General-Purpose Input Output 64
EPWM9_B	1					O	ePWM-9 Output B
EMIF1_D20	2					I/O	External memory interface 1 data line 20
EMIF1_WAIT	3					I	External memory interface 1 Asynchronous SRAM WAIT
SPIB_POCI	5					I/O	SPI-B Peripheral Out, Controller In (POCI)
MCANA_TX	6					O	MCAN-A Transmit
UARTF_TX	7					I/O	UART-F Serial Data Transmit
SENT6	9					I/O	SENT Input Pin 6
ESC_RX1_DATA1	10					I	EtherCAT MII Receive-1 Data-1
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
FSITXD_CLK	13					O	FSITX-D Output Clock
ADCD_EXTMUXSEL1	14					O	External ADC selection Mux output
GPIO65	0, 4, 8, 12	H16	112	93	61	I/O	General-Purpose Input Output 65
EPWM10_A	1					O	ePWM-10 Output A
EMIF1_D19	2					I/O	External memory interface 1 data line 19
EMIF1_WEn	3					O	External memory interface 1 write enable
SPIB_CLK	5					I/O	SPI-B Clock
MCANA_RX	6					I	MCAN-A Receive
UARTF_RX	7					I/O	UART-F Serial Data Receive
ESC_RX1_DATA2	10					I	EtherCAT MII Receive-1 Data-2
SD1_D2	11					I	SDFM-1 Channel 2 Data Input
FSITXB_CLK	13					O	FSITX-B Output Clock
ADCD_EXTMUXSEL2	14					O	External ADC selection Mux output
ESC_GPI13	15					I	EtherCAT General-Purpose Input 13
GPIO66	0, 4, 8, 12	G13	113	94	62	I/O	General-Purpose Input Output 66
EPWM10_B	1					O	ePWM-10 Output B
EMIF1_D18	2					I/O	External memory interface 1 data line 18
EMIF1_OEn	3					O	External memory interface 1 output enable
SPIB_PTE	5					I/O	SPI-B Peripheral Transmit Enable (PTE)
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
ESC_RX1_DATA3	10					I	EtherCAT MII Receive-1 Data-3
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
FSITXB_D1	13					O	FSITX-B Optional Additional Data Output
ADCD_EXTMUXSEL3	14					O	External ADC selection Mux output
ESC_GPI14	15					I	EtherCAT General-Purpose Input 14
GPIO67	0, 4, 8, 12	B16	132			I/O	General-Purpose Input Output 67
EPWM17_A	1					O	ePWM-17 Output A
EMIF1_D17	2					I/O	External memory interface 1 data line 17
LINB_TX	5					O	LIN-B Transmit
MCAND_TX	6					O	MCAN-D Transmit
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
FSITXB_CLK	13					O	FSITX-B Output Clock

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO68	0, 4, 8, 12	B15	133	109		I/O	General-Purpose Input Output 68
EPWM17_B	1					O	ePWM-17 Output B
EMIF1_D16	2					I/O	External memory interface 1 data line 16
EMIF1_D4	3					I/O	External memory interface 1 data line 4
LINB_RX	5					I	LIN-B Receive
MCAND_RX	6					I	MCAN-D Receive
EMIF1_D13	7					I/O	External memory interface 1 data line 13
ESC_PHY1_LINKSTATUS	10					I	EtherCAT PHY-1 Link Status
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
FSIRXB_D1	13					I	FSIRX-B Optional Additional Data Input
ESC_GPI15	15					I	EtherCAT General-Purpose Input 15
GPIO69	0, 4, 8, 12	A15	134			I/O	General-Purpose Input Output 69
EPWM11_A	1					O	ePWM-11 Output A
EMIF1_D15	2					I/O	External memory interface 1 data line 15
SPIC_PICO	5					I/O	SPI-C Peripheral In, Controller Out (PICO)
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
ESC_RX1_CLK	10					I	EtherCAT MII Receive-1 Clock
SD1_D4	11					I	SDFM-1 Channel 4 Data Input
FSITXB_D0	13					O	FSITX-B Primary Data Output
GPIO70	0, 4, 8, 12	C14	135	110	76	I/O	General-Purpose Input Output 70
EPWM11_B	1					O	ePWM-11 Output B
EMIF1_D14	2					I/O	External memory interface 1 data line 14
SPIC_POCI	5					I/O	SPI-C Peripheral Out, Controller In (POCI)
MCANC_RX	6					I	MCAN-C Receive
UARTB_TX	7					I/O	UART-B Serial Data Transmit
ESC_RX1_DV	10					I	EtherCAT MII Receive-1 Data Valid
SD1_C4	11					I	SDFM-1 Channel 4 Clock Input
FSIRXB_D0	13					I	FSIRX-B Primary Data Input
ESC_GPI16	15					I	EtherCAT General-Purpose Input 16
GPIO71	0, 4, 8, 12	B14	136	111	77	I/O	General-Purpose Input Output 71
EPWM12_A	1					O	ePWM-12 Output A
EPWM11_A	2					O	ePWM-11 Output A
EMIF1_D5	3					I/O	External memory interface 1 data line 5
SPIC_CLK	5					I/O	SPI-C Clock
MCANC_TX	6					O	MCAN-C Transmit
UARTB_RX	7					I/O	UART-B Serial Data Receive
EMIF1_D13	9					I/O	External memory interface 1 data line 13
ESC_RX1_ERR	10					I	EtherCAT MII Receive-1 Error
SD3_D1	11					I	SDFM-3 Channel 1 Data Input
FSITXC_CLK	13					O	FSITX-C Output Clock
FSITXB_D0	14					O	FSITX-B Primary Data Output

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO72	0, 4, 8, 12					I/O	General-Purpose Input Output 72
EPWM12_B	1					O	ePWM-12 Output B
EMIF1_D12	2					I/O	External memory interface 1 data line 12
SPIC_PTE	5					I/O	SPI-C Peripheral Transmit Enable (PTE)
MCANB_RX	6					I	MCAN-B Receive
UARTA_TX	7	A14	139	114	80	I/O	UART-A Serial Data Transmit
OUTPUTXBAR8	9					O	Output X-BAR Output 8
ESC_TX1_DATA3	10					O	EtherCAT MII Transmit-1 Data-3
SD3_D2	11					I	SDFM-3 Channel 2 Data Input
FSITXC_D0	13					O	FSITX-C Primary Data Output
SD3_C1	14					I	SDFM-3 Channel 1 Clock Input
GPIO73	0, 4, 8, 12					I/O	General-Purpose Input Output 73
EPWM5_B	1					O	ePWM-5 Output B
EMIF1_D11	2					I/O	External memory interface 1 data line 11
XCLKOUT	3					O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
MCANB_TX	6	E13	140			O	MCAN-B Transmit
UARTA_RX	7					I/O	UART-A Serial Data Receive
OUTPUTXBAR6	9					O	Output X-BAR Output 6
ESC_TX1_DATA2	10					O	EtherCAT MII Transmit-1 Data-2
SD4_D4	11					I	SDFM-4 Channel 4 Data Input
FSITXC_CLK	13					O	FSITX-C Output Clock
SD2_D2	14					I	SDFM-2 Channel 2 Data Input
GPIO74	0, 4, 8, 12					I/O	General-Purpose Input Output 74
EPWM8_A	1					O	ePWM-8 Output A
EMIF1_D10	2					I/O	External memory interface 1 data line 10
MCANC_TX	6	D13	141			O	MCAN-C Transmit
ESC_TX1_DATA1	10					O	EtherCAT MII Transmit-1 Data-1
SD1_D4	11					I	SDFM-1 Channel 4 Data Input
FSITXA_D0	13					O	FSITX-A Primary Data Output
SD2_C2	14					I	SDFM-2 Channel 2 Clock Input
GPIO75	0, 4, 8, 12					I/O	General-Purpose Input Output 75
EPWM8_B	1					O	ePWM-8 Output B
EMIF1_D9	2					I/O	External memory interface 1 data line 9
SPID_CLK	5	C13	142			I/O	SPI-D Clock
MCANC_RX	6					I	MCAN-C Receive
OUTPUTXBAR16	9					O	Output X-BAR Output 16
ESC_TX1_DATA0	10					O	EtherCAT MII Transmit-1 Data-0
SD2_D3	14					I	SDFM-2 Channel 3 Data Input
GPIO76	0, 4, 8, 12					I/O	General-Purpose Input Output 76
EPWM9_A	1					O	ePWM-9 Output A
EMIF1_D8	2					I/O	External memory interface 1 data line 8
UARTD_TX	5					I/O	UART-D Serial Data Transmit
MCANE_TX	7					O	MCAN-E Transmit
SD4_D4	9	B13	143	115		I	SDFM-4 Channel 4 Data Input
ESC_PHY_RESETn	10					O	EtherCAT PHY Active Low Reset
SD3_C1	11					I	SDFM-3 Channel 1 Clock Input
FSIRXC_D0	13					I	FSIRX-C Primary Data Input
SD2_C3	14					I	SDFM-2 Channel 3 Clock Input
ESC_GPI17	15					I	EtherCAT General-Purpose Input 17

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO77	0, 4, 8, 12	A13	144	116		I/O	General-Purpose Input Output 77
EPWM9_B	1					O	ePWM-9 Output B
EMIF1_D7	2					I/O	External memory interface 1 data line 7
UARTD_RX	5					I/O	UART-D Serial Data Receive
MCANE_RX	7					I	MCAN-E Receive
SD1_D4	9					I	SDFM-1 Channel 4 Data Input
ESC_RX0_CLK	10					I	EtherCAT MII Receive-0 Clock
SD3_D1	11					I	SDFM-3 Channel 1 Data Input
FSITXB_D0	13					O	FSITX-B Primary Data Output
SD2_D4	14					I	SDFM-2 Channel 4 Data Input
GPIO78	0, 4, 8, 12	D12	145	117		I/O	General-Purpose Input Output 78
EPWM10_A	1					O	ePWM-10 Output A
EMIF1_D6	2					I/O	External memory interface 1 data line 6
EPWM11_A	3					O	ePWM-11 Output A
MCANF_TX	7					O	MCAN-F Transmit
SD4_D4	9					I	SDFM-4 Channel 4 Data Input
ESC_RX0_DV	10					I	EtherCAT MII Receive-0 Data Valid
SD3_C2	11					I	SDFM-3 Channel 2 Clock Input
FSITXC_D1	13					O	FSITX-C Optional Additional Data Output
SD2_C4	14					I	SDFM-2 Channel 4 Clock Input
ESC_GPI18	15					I	EtherCAT General-Purpose Input 18
GPIO79	0, 4, 8, 12	C12	146			I/O	General-Purpose Input Output 79
EPWM10_B	1					O	ePWM-10 Output B
EMIF1_D5	2					I/O	External memory interface 1 data line 5
ERRORSTS	5					O	Error Status Output. This signal requires an external pulldown.
ESC_RX0_ERR	10					I	EtherCAT MII Receive-0 Error
SD3_D2	11					I	SDFM-3 Channel 2 Data Input
FSITXC_D0	13					O	FSITX-C Primary Data Output
SD2_D1	14					I	SDFM-2 Channel 1 Data Input
GPIO80	0, 4, 8, 12	B12				I/O	General-Purpose Input Output 80
EPWM11_A	1					O	ePWM-11 Output A
EMIF1_D4	2					I/O	External memory interface 1 data line 4
ERRORSTS	5					O	Error Status Output. This signal requires an external pulldown.
SD1_D4	9					I	SDFM-1 Channel 4 Data Input
ESC_RX0_DATA0	10					I	EtherCAT MII Receive-0 Data-0
SD3_C3	11					I	SDFM-3 Channel 3 Clock Input
SD2_C1	14					I	SDFM-2 Channel 1 Clock Input
GPIO81	0, 4, 8, 12	A12				I/O	General-Purpose Input Output 81
EPWM11_B	1					O	ePWM-11 Output B
EMIF1_D3	2					I/O	External memory interface 1 data line 3
ESC_RX0_DATA1	10					I	EtherCAT MII Receive-0 Data-1
SD3_D3	11					I	SDFM-3 Channel 3 Data Input
GPIO82	0, 4, 8, 12	D10				I/O	General-Purpose Input Output 82
EPWM12_A	1					O	ePWM-12 Output A
EMIF1_D2	2					I/O	External memory interface 1 data line 2
ESC_RX0_DATA2	10					I	EtherCAT MII Receive-0 Data-2
SD3_C2	11					I	SDFM-3 Channel 2 Clock Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO83	0, 4, 8, 12					I/O	General-Purpose Input Output 83
EPWM12_B	1					O	ePWM-12 Output B
EMIF1_D1	2	A11				I/O	External memory interface 1 data line 1
ESC_RX0_DATA3	10					I	EtherCAT MII Receive-0 Data-3
SD3_D2	11					I	SDFM-3 Channel 2 Data Input
GPIO84	0, 4, 8, 12					I/O	General-Purpose Input Output 84
EPWM12_B	1					O	ePWM-12 Output B
EMIF1_D1	2					I/O	External memory interface 1 data line 1
EMIF1_CS4n	3					O	External memory interface 1 chip select 4
SPIC_PICO	5					I/O	SPI-C Peripheral In, Controller Out (PICO)
UARTA_TX	6	D11	148	119	81	I/O	UART-A Serial Data Transmit
MCANF_RX	7					I	MCAN-F Receive
ESC_TX0_ENA	10					I/O	EtherCAT MII Transmit-0 Enable
SD3_C2	11					I	SDFM-3 Channel 2 Clock Input
FSITXC_D1	13					O	FSITX-C Optional Additional Data Output
ESC_RX0_DATA3	14					I	EtherCAT MII Receive-0 Data-3
ESC_GPO24	15					O	EtherCAT General-Purpose Output 24
GPIO85	0, 4, 8, 12					I/O	General-Purpose Input Output 85
EPWM13_A	1					O	ePWM-13 Output A
EMIF1_D0	2					I/O	External memory interface 1 data line 0
UARTA_RX	6	B11				I/O	UART-A Serial Data Receive
EMIF1_DQM2	9					O	External memory interface 1 Input/output mask for byte 2
ESC_TX0_CLK	10					I	EtherCAT MII Transmit-0 Clock
SD3_D3	11					I	SDFM-3 Channel 3 Data Input
GPIO86	0, 4, 8, 12					I/O	General-Purpose Input Output 86
EPWM13_B	1					O	ePWM-13 Output B
EMIF1_A13	2					O	External memory interface 1 address line 13
EMIF1_CAS	3	C11				O	External memory interface 1 column address strobe
UARTD_TX	6					I/O	UART-D Serial Data Transmit
ESC_PHY0_LINKSTATUS	10					I	EtherCAT PHY-0 Link Status
SD3_C3	11					I	SDFM-3 Channel 3 Clock Input
GPIO87	0, 4, 8, 12					I/O	General-Purpose Input Output 87
EPWM14_A	1					O	ePWM-14 Output A
EMIF1_A14	2					O	External memory interface 1 address line 14
EMIF1_RAS	3					O	External memory interface 1 row address strobe
UARTD_RX	6	C10				I/O	UART-D Serial Data Receive
EMIF1_DQM3	9					O	External memory interface 1 Input/output mask for byte 3
ESC_TX0_DATA0	10					O	EtherCAT MII Transmit-0 Data-0
SD3_D4	11					I	SDFM-3 Channel 4 Data Input
GPIO88	0, 4, 8, 12					I/O	General-Purpose Input Output 88
EPWM14_B	1					O	ePWM-14 Output B
EMIF1_A15	2					O	External memory interface 1 address line 15
EMIF1_DQM0	3	C3				O	External memory interface 1 Input/output mask for byte 0
EMIF1_DQM1	9					O	External memory interface 1 Input/output mask for byte 1
ESC_TX0_DATA1	10					O	EtherCAT MII Transmit-0 Data-1
SD3_C4	11					I	SDFM-3 Channel 4 Clock Input

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO89	0, 4, 8, 12	D4				I/O	General-Purpose Input Output 89
EPWM15_A	1					O	ePWM-15 Output A
EMIF1_A16	2					O	External memory interface 1 address line 16
EMIF1_DQM1	3					O	External memory interface 1 Input/output mask for byte 1
SPID_PTE	5					I/O	SPI-D Peripheral Transmit Enable (PTE)
EMIF1_CAS	9					O	External memory interface 1 column address strobe
ESC_TX0_DATA2	10					O	EtherCAT MII Transmit-0 Data-2
SD1_D3	11					I	SDFM-1 Channel 3 Data Input
SD4_D1	14					I	SDFM-4 Channel 1 Data Input
GPIO90	0, 4, 8, 12	D3				I/O	General-Purpose Input Output 90
EPWM15_B	1					O	ePWM-15 Output B
EMIF1_A17	2					O	External memory interface 1 address line 17
EMIF1_DQM2	3					O	External memory interface 1 Input/output mask for byte 2
SPID_CLK	5					I/O	SPI-D Clock
EMIF1_RAS	9					O	External memory interface 1 row address strobe
ESC_TX0_DATA3	10					O	EtherCAT MII Transmit-0 Data-3
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
SD4_C1	14					I	SDFM-4 Channel 1 Clock Input
GPIO91	0, 4, 8, 12	D2				I/O	General-Purpose Input Output 91
EPWM16_A	1					O	ePWM-16 Output A
EMIF1_A18	2					O	External memory interface 1 address line 18
EMIF1_DQM3	3					O	External memory interface 1 Input/output mask for byte 3
SPID_PICO	5					I/O	SPI-D Peripheral In, Controller Out (PICO)
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
MCAND_TX	7					O	MCAN-D Transmit
EMIF1_DQM2	9					O	External memory interface 1 Input/output mask for byte 2
SD4_D2	11					I	SDFM-4 Channel 2 Data Input
OUTPUTXBAR9	14					O	Output X-BAR Output 9
GPIO92	0, 4, 8, 12	E2				I/O	General-Purpose Input Output 92
EPWM16_B	1					O	ePWM-16 Output B
EMIF1_A19	2					O	External memory interface 1 address line 19
EMIF1_BA1	3					O	External memory interface 1 bank address 1
SPID_POCI	5					I/O	SPI-D Peripheral Out, Controller In (POCI)
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
MCAND_RX	7					I	MCAN-D Receive
EMIF1_DQM0	9					O	External memory interface 1 Input/output mask for byte 0
FSIRXD_CLK	10					I	FSIRX-D Input Clock
SD4_C2	11					I	SDFM-4 Channel 2 Clock Input
OUTPUTXBAR10	14					O	Output X-BAR Output 10
GPIO93	0, 4, 8, 12	E3				I/O	General-Purpose Input Output 93
EPWM17_A	1					O	ePWM-17 Output A
EMIF1_BA0	3					O	External memory interface 1 bank address 0
SPID_CLK	5					I/O	SPI-D Clock
ESC_TX1_CLK	10					I	EtherCAT MII Transmit-1 Clock
SD4_D3	11					I	SDFM-4 Channel 3 Data Input
OUTPUTXBAR11	14					O	Output X-BAR Output 11

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO94	0, 4, 8, 12					I/O	General-Purpose Input Output 94
EPWM17_B	1					O	ePWM-17 Output B
SPID_PTE	5					I/O	SPI-D Peripheral Transmit Enable (PTE)
EMIF1_BA1	9	E4				O	External memory interface 1 bank address 1
ESC_TX1_ENA	10					I/O	EtherCAT MII Transmit-1 Enable
SD4_C3	11					I	SDFM-4 Channel 3 Clock Input
OUTPUTXBAR12	14					O	Output X-BAR Output 12
GPIO95	0, 4, 8, 12					I/O	General-Purpose Input Output 95
EPWM18_A	1					O	ePWM-18 Output A
ESC_GPO10	10	E5				O	EtherCAT General-Purpose Output 10
SD1_D1	11					I	SDFM-1 Channel 1 Data Input
OUTPUTXBAR13	14					O	Output X-BAR Output 13
GPIO96	0, 4, 8, 12					I/O	General-Purpose Input Output 96
EPWM18_B	1					O	ePWM-18 Output B
ESC_GPO11	10	F3				O	EtherCAT General-Purpose Output 11
SD1_C1	11					I	SDFM-1 Channel 1 Clock Input
OUTPUTXBAR14	14					O	Output X-BAR Output 14
GPIO97	0, 4, 8, 12					I/O	General-Purpose Input Output 97
ESC_GPI17	10	F4				I	EtherCAT General-Purpose Input 17
SD1_D2	11					I	SDFM-1 Channel 2 Data Input
OUTPUTXBAR15	14					O	Output X-BAR Output 15
GPIO98	0, 4, 8, 12					I/O	General-Purpose Input Output 98
ESC_GPI18	10	F5				I	EtherCAT General-Purpose Input 18
SD1_C2	11					I	SDFM-1 Channel 2 Clock Input
OUTPUTXBAR16	14					O	Output X-BAR Output 16
GPIO99	0, 4, 8, 12					I/O	General-Purpose Input Output 99
EPWM8_A	1					O	ePWM-8 Output A
EMIF1_DQM3	2	G5				O	External memory interface 1 Input/output mask for byte 3
EMIF1_D17	3					I/O	External memory interface 1 data line 17
ESC_GPI21	10					I	EtherCAT General-Purpose Input 21
SD4_D4	11					I	SDFM-4 Channel 4 Data Input
GPIO100	0, 4, 8, 12					I/O	General-Purpose Input Output 100
EPWM9_A	1					O	ePWM-9 Output A
EMIF1_BA1	2					O	External memory interface 1 bank address 1
EMIF1_D24	3					I/O	External memory interface 1 data line 24
SPIC_PICO	5					I/O	SPI-C Peripheral In, Controller Out (PICO)
SPIA_PICO	6	B4				I/O	SPI-A Peripheral In, Controller Out (PICO)
SD1_D1	9					I	SDFM-1 Channel 1 Data Input
ESC_GPI0	10					I	EtherCAT General-Purpose Input 0
SD4_C4	11					I	SDFM-4 Channel 4 Clock Input
FSITXA_D0	13					O	FSITX-A Primary Data Output
FSIRXD_D1	14					I	FSIRX-D Optional Additional Data Input
GPIO101	0, 4, 8, 12					I/O	General-Purpose Input Output 101
EPWM18_A	1					O	ePWM-18 Output A
EMIF1_A5	2	B5				O	External memory interface 1 address line 5
SPIC_POCI	5					I/O	SPI-C Peripheral Out, Controller In (POCI)
ESC_GPI1	10					I	EtherCAT General-Purpose Input 1
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO103	0, 4, 8, 12					I/O	General-Purpose Input Output 103
EPWM8_B	1					O	ePWM-8 Output B
EMIF1_BA0	2					O	External memory interface 1 bank address 0
EMIF1_D3	3					I/O	External memory interface 1 data line 3
SPIC_PTE	5	D16	126	105		I/O	SPI-C Peripheral Transmit Enable (PTE)
ESC_GPI3	10					I	EtherCAT General-Purpose Input 3
SD4_C4	11					I	SDFM-4 Channel 4 Clock Input
FSIRXA_D0	13					I	FSIRX-A Primary Data Input
ESC_GPO25	15					O	EtherCAT General-Purpose Output 25
GPIO105	0, 4, 8, 12					I/O	General-Purpose Input Output 105
EPWM18_B	1					O	ePWM-18 Output B
I2CA_SCL	5	J14				I/OD	I2C-A Open-Drain Bidirectional Clock
ESC_GPI5	10					I	EtherCAT General-Purpose Input 5
SD3_C1	11					I	SDFM-3 Channel 1 Clock Input
FSIRXA_CLK	13					I	FSIRX-A Input Clock
GPIO127	0, 4, 8, 12					I/O	General-Purpose Input Output 127
EPWM18_A	1					O	ePWM-18 Output A
EMIF1_D18	2					I/O	External memory interface 1 data line 18
EMIF1_A11	3					O	External memory interface 1 address line 11
SPID_POCI	5	F13	118	97	64	I/O	SPI-D Peripheral Out, Controller In (POCI)
ESC_GPI27	10					I	EtherCAT General-Purpose Input 27
SD1_C3	11					I	SDFM-1 Channel 3 Clock Input
FSIRXC_D1	13					I	FSIRX-C Optional Additional Data Input
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
ESC_GPO26	15					O	EtherCAT General-Purpose Output 26
GPIO219	0, 4, 8, 12					I/O	General-Purpose Input Output 219
ERRORSTS	1					O	Error Status Output. This signal requires an external pulldown.
EMIF1_A19	2					O	External memory interface 1 address line 19
EPWM18_B	3					O	ePWM-18 Output B
OUTPUTXBAR1	9					O	Output X-BAR Output 1
XCLKOUT	10	M16	91	74	51	O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
SD2_C1	11					I	SDFM-2 Channel 1 Clock Input
ESC_GPI8	13					I	EtherCAT General-Purpose Input 8
ESC_TX0_ENA	14					I/O	EtherCAT MII Transmit-0 Enable
ESC_GPO27	15					O	EtherCAT General-Purpose Output 27
GPIO220	0, 4, 8, 12					I/O	General-Purpose Input Output 220
EPWM6_A	1					O	ePWM-6 Output A
SPID_POCI	5					I/O	SPI-D Peripheral Out, Controller In (POCI)
MCANC_TX	6					O	MCAN-C Transmit
OUTPUTXBAR2	9					O	Output X-BAR Output 2
SD3_D3	11					I	SDFM-3 Channel 3 Data Input
ESC_GPI9	13	E16	123	102	70	I	EtherCAT General-Purpose Input 9
ESC_GPO28	15					O	EtherCAT General-Purpose Output 28
X1	ALT					I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
GPIO221	0, 4, 8, 12	F16	121	100	68	I/O	General-Purpose Input Output 221
EPWM6_B	1					O	ePWM-6 Output B
EMIF1_CAS	3					O	External memory interface 1 column address strobe
SPID_PTE	5					I/O	SPI-D Peripheral Transmit Enable (PTE)
MCANC_RX	6					I	MCAN-C Receive
OUTPUTXBAR3	9					O	Output X-BAR Output 3
SD3_C3	11					I	SDFM-3 Channel 3 Clock Input
ESC_GPI10	13					I	EtherCAT General-Purpose Input 10
ESC_GPO29	15					O	EtherCAT General-Purpose Output 29
X2	ALT					I/O	Crystal oscillator output.
GPIO222	0, 4, 8, 12	T14	77	64	42	I/O	General-Purpose Input Output 222
TDI	1					I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
EPWM7_A	2					O	ePWM-7 Output A
SPID_PICO	5					I/O	SPI-D Peripheral In, Controller Out (PICO)
UARTB_TX	6					I/O	UART-B Serial Data Transmit
I2CB_SCL	7					I/OD	I2C-B Open-Drain Bidirectional Clock
OUTPUTXBAR4	9					O	Output X-BAR Output 4
SPIC_CLK	10					I/O	SPI-C Clock
SD3_D4	11					I	SDFM-3 Channel 4 Data Input
ESC_GPI11	13					I	EtherCAT General-Purpose Input 11
ESC_GPO30	15					O	EtherCAT General-Purpose Output 30
GPIO223	0, 4, 8, 12	R14	78	65	43	I/O	General-Purpose Input Output 223
TDO	1					O	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.
EPWM7_B	2					O	ePWM-7 Output B
SPID_CLK	5					I/O	SPI-D Clock
UARTB_RX	6					I/O	UART-B Serial Data Receive
I2CB_SDA	7					I/OD	I2C-B Open-Drain Bidirectional Data
OUTPUTXBAR5	9					O	Output X-BAR Output 5
SPIC_PTE	10					I/O	SPI-C Peripheral Transmit Enable (PTE)
SD3_C4	11					I	SDFM-3 Channel 4 Clock Input
ESC_GPI12	13					I	EtherCAT General-Purpose Input 12
ESC_GPO31	15					O	EtherCAT General-Purpose Output 31
TEST, JTAG, AND RESET							
FLT3		M12				I/O	Flash test pin 3. Reserved for TI. Must be left unconnected.
TCK		R15	83	70	48	I	JTAG test clock with internal pullup.
TMS		T15	82	69	47	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
VREGENZ					65	I	Internal voltage regulator enable with internal pullup. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
XRSn		F14	124	103	71	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.
POWER AND GROUND							
VDD		E8, E9, E12, F6, F12, G6, L11, L12	8, 11, 80, 84, 105, 119, 137, 153, 169	6, 8, 67, 71, 87, 98, 112, 123, 137	5, 6, 45, 49, 55, 66, 78, 95		1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.
VDDA		K6, L6	27, 62	19, 54	14, 37		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin. Connect this pin to 3.3-V supply.
VDDIO		E6, E7, E10, E11, F15, G12, H6, H12, J6, J12, K12, L8, L9, L10, L13, M10, M11	3, 12, 79, 81, 88, 98, 101, 107, 115, 120, 127, 138, 147, 152, 168	3, 9, 66, 68, 72, 81, 83, 95, 99, 106, 113, 118, 122, 136	3, 7, 44, 46, 52, 63, 67, 73, 79		3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin. Connect this pin to 3.3-V supply.
VSS		A1, A16, F7, F8, F9, F10, F11, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K8, K9, K10, K11, T16	PAD	PAD	PAD		Digital Ground
VSSA		K7, L7, T1	28, 61	20, 53	15, 36		Analog Ground

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEX	176 PTS	144 RFS	100 PZS	PIN TYPE	DESCRIPTION
VSSOSC		E15	122	101	69		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. Connect this pin to board ground.

ADVANCE INFORMATION

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
A0	I	ADC-A Input 0		R1	44	36	25
A1	I	ADC-A Input 1		P1	43	35	24
A2	I	ADC-A Input 2		M1	36	28	
A3	I	ADC-A Input 3		M2	35	27	
A4	I	ADC-A Input 4		L2	32	24	
A5	I	ADC-A Input 5		L1	31	23	
A6	I	ADC-A Input 6	224	L5	26	18	13
A7	I	ADC-A Input 7	225	K5	25	17	12
A8	I	ADC-A Input 8	226	H4	22	16	
A9	I	ADC-A Input 9	227	H3	21		
A10	I	ADC-A Input 10	228	G3	18		
A11	I	ADC-A Input 11	229	G4	17		
A12	I	ADC-A Input 12		K2			
A13	I	ADC-A Input 13		K1			
A14	I	ADC-A Input 14		M3	40	32	21
A15	I	ADC-A Input 15		M4	39	31	20
A24	I	ADC-A Input 24		P3	49	41	30
A25	I	ADC-A Input 25		P4	50	42	31
A26	I	ADC-A Input 26		T5	59	51	
A27	I	ADC-A Input 27		T6	60	52	
A28	I	ADC-A Input 28	246	P11	67	56	38
A29	I	ADC-A Input 29	247	R11	68	57	39
A30	I	ADC-A Input 30	248	P13	73	62	
A31	I	ADC-A Input 31	249	N13	74	63	
AIO160	I	Analog Pin Used For Digital Input 160		R1	44	36	25
AIO161	I	Analog Pin Used For Digital Input 161		P1	43	35	24
AIO162	I	Analog Pin Used For Digital Input 162		M1	36	28	
AIO163	I	Analog Pin Used For Digital Input 163		M2	35	27	
AIO164	I	Analog Pin Used For Digital Input 164		L2	32	24	
AIO165	I	Analog Pin Used For Digital Input 165		L1	31	23	
AIO166	I	Analog Pin Used For Digital Input 166		K2			
AIO167	I	Analog Pin Used For Digital Input 167		K1			
AIO168	I	Analog Pin Used For Digital Input 168		M3	40	32	21
AIO169	I	Analog Pin Used For Digital Input 169		M4	39	31	20
AIO170	I	Analog Pin Used For Digital Input 170		P2	42	34	23
AIO171	I	Analog Pin Used For Digital Input 171		N3	41	33	22
AIO172	I	Analog Pin Used For Digital Input 172		L4	34	26	17
AIO173	I	Analog Pin Used For Digital Input 173		L3	33	25	16
AIO174	I	Analog Pin Used For Digital Input 174		K4	30	22	
AIO175	I	Analog Pin Used For Digital Input 175		K3	29	21	
AIO176	I	Analog Pin Used For Digital Input 176		J2			
AIO177	I	Analog Pin Used For Digital Input 177		J1			

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
AIO178	I	Analog Pin Used For Digital Input 178		J4			
AIO179	I	Analog Pin Used For Digital Input 179		J3			
AIO180	I	Analog Pin Used For Digital Input 180		R2	45	37	26
AIO181	I	Analog Pin Used For Digital Input 181		T2	46	38	27
AIO182	I	Analog Pin Used For Digital Input 182		N4	51	43	
AIO183	I	Analog Pin Used For Digital Input 183		M5	52	44	
AIO184	I	Analog Pin Used For Digital Input 184		P5	55	47	
AIO185	I	Analog Pin Used For Digital Input 185		N5	56	48	
AIO186	I	Analog Pin Used For Digital Input 186		N8			
AIO187	I	Analog Pin Used For Digital Input 187		P8			
AIO188	I	Analog Pin Used For Digital Input 188		R8			
AIO189	I	Analog Pin Used For Digital Input 189		T8			
AIO190	I	Analog Pin Used For Digital Input 190		N7			
AIO191	I	Analog Pin Used For Digital Input 191		P7			
AIO192	I	Analog Pin Used For Digital Input 192		R3	47	39	28
AIO193	I	Analog Pin Used For Digital Input 193		T3	48	40	29
AIO194	I	Analog Pin Used For Digital Input 194		R5	57	49	34
AIO195	I	Analog Pin Used For Digital Input 195		R6	58	50	35
AIO196	I	Analog Pin Used For Digital Input 196		N6			
AIO197	I	Analog Pin Used For Digital Input 197		P6			
AIO198	I	Analog Pin Used For Digital Input 198		M7			
AIO199	I	Analog Pin Used For Digital Input 199		M6			
AIO200	I	Analog Pin Used For Digital Input 200		R7			
AIO201	I	Analog Pin Used For Digital Input 201		T7			
AIO202	I	Analog Pin Used For Digital Input 202		P3	49	41	30
AIO203	I	Analog Pin Used For Digital Input 203		P4	50	42	31
AIO204	I	Analog Pin Used For Digital Input 204		T5	59	51	
AIO205	I	Analog Pin Used For Digital Input 205		T6	60	52	
AIO206	I	Analog Pin Used For Digital Input 206		T10			
AIO207	I	Analog Pin Used For Digital Input 207		T9			
AIO208	I	Analog Pin Used For Digital Input 208		R10			
AIO209	I	Analog Pin Used For Digital Input 209		R9			
AIO210	I	Analog Pin Used For Digital Input 210		P9			
AIO211	I	Analog Pin Used For Digital Input 211		N9			
AIO212	I	Analog Pin Used For Digital Input 212		P10			
AIO213	I	Analog Pin Used For Digital Input 213		T11			
B0	I	ADC-B Input 0		P2	42	34	23
B1	I	ADC-B Input 1		N3	41	33	22
B2	I	ADC-B Input 2		L4	34	26	17
B3	I	ADC-B Input 3		L3	33	25	16
B4	I	ADC-B Input 4		K4	30	22	
B5	I	ADC-B Input 5		K3	29	21	
B6	I	ADC-B Input 6	230	J5	24		
B7	I	ADC-B Input 7	231	H5	23		

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
B8	I	ADC-B Input 8	232	H2	20	15	11
B9	I	ADC-B Input 9	233	H1	19	14	10
B10	I	ADC-B Input 10	234	G2	16	13	
B11	I	ADC-B Input 11	235	G1	15	12	
B12	I	ADC-B Input 12		J2			
B13	I	ADC-B Input 13		J1			
B14	I	ADC-B Input 14		M3	40	32	21
B15	I	ADC-B Input 15		M4	39	31	20
B16	I	ADC-B Input 16		J4			
B17	I	ADC-B Input 17		J3			
B24	I	ADC-B Input 24		R3	47	39	28
B25	I	ADC-B Input 25		T3	48	40	29
B26	I	ADC-B Input 26		R5	57	49	34
B27	I	ADC-B Input 27		R6	58	50	35
B28	I	ADC-B Input 28	240	N10	65		
B29	I	ADC-B Input 29	241	N11	66	55	
B30	I	ADC-B Input 30	242	T12	71	60	
B31	I	ADC-B Input 31	243	R12	72	61	
C0	I	ADC-C Input 0		R2	45	37	26
C1	I	ADC-C Input 1		T2	46	38	27
C2	I	ADC-C Input 2		N4	51	43	
C3	I	ADC-C Input 3		M5	52	44	
C4	I	ADC-C Input 4		P5	55	47	
C5	I	ADC-C Input 5		N5	56	48	
C6	I	ADC-C Input 6	236	M8	63		
C7	I	ADC-C Input 7	237	M9	64		
C8	I	ADC-C Input 8	238	N12	69	58	40
C9	I	ADC-C Input 9	239	P12	70	59	41
C10	I	ADC-C Input 10		N8			
C11	I	ADC-C Input 11		P8			
C12	I	ADC-C Input 12		R8			
C13	I	ADC-C Input 13		T8			
C14	I	ADC-C Input 14		M3	40	32	21
C15	I	ADC-C Input 15		M4	39	31	20
C16	I	ADC-C Input 16		N7			
C17	I	ADC-C Input 17		P7			
C24	I	ADC-C Input 24		R1	44	36	25
C25	I	ADC-C Input 25		P1	43	35	24
C26	I	ADC-C Input 26		P2	42	34	23
C27	I	ADC-C Input 27		N3	41	33	22
C28	I	ADC-C Input 28	244	R13	75		
C29	I	ADC-C Input 29	245	T13	76		
C30	I	ADC-C Input 30		T10			
C31	I	ADC-C Input 31		T9			

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
CMP1_HN0	I	CMPSS-1 High Comparator Negative Input 0		L1	31	23	
CMP1_HN1	I	CMPSS-1 High Comparator Negative Input 1		M2	35	27	
CMP1_HP0	I	CMPSS-1 High Comparator Positive Input 0		L2	32	24	
CMP1_HP1	I	CMPSS-1 High Comparator Positive Input 1		M1	36	28	
CMP1_HP2	I	CMPSS-1 High Comparator Positive Input 2		M2	35	27	
CMP1_HP3	I	CMPSS-1 High Comparator Positive Input 3		L3	33	25	16
CMP1_HP4	I	CMPSS-1 High Comparator Positive Input 4	242	T12	71	60	
CMP1_HP5	I	CMPSS-1 High Comparator Positive Input 5		K2			
CMP1_LN0	I	CMPSS-1 Low Comparator Negative Input 0		L1	31	23	
CMP1_LN1	I	CMPSS-1 Low Comparator Negative Input 1		M2	35	27	
CMP1_LP0	I	CMPSS-1 Low Comparator Positive Input 0		L2	32	24	
CMP1_LP1	I	CMPSS-1 Low Comparator Positive Input 1		M1	36	28	
CMP1_LP2	I	CMPSS-1 Low Comparator Positive Input 2		M2	35	27	
CMP1_LP3	I	CMPSS-1 Low Comparator Positive Input 3		L3	33	25	16
CMP1_LP4	I	CMPSS-1 Low Comparator Positive Input 4	242	T12	71	60	
CMP1_LP5	I	CMPSS-1 Low Comparator Positive Input 5		K2			
CMP2_HN0	I	CMPSS-2 High Comparator Negative Input 0	225	K5	25	17	12
CMP2_HN1	I	CMPSS-2 High Comparator Negative Input 1		L2	32	24	
CMP2_HP0	I	CMPSS-2 High Comparator Positive Input 0	224	L5	26	18	13
CMP2_HP1	I	CMPSS-2 High Comparator Positive Input 1		T10			
CMP2_HP2	I	CMPSS-2 High Comparator Positive Input 2		T9			
CMP2_HP3	I	CMPSS-2 High Comparator Positive Input 3		M6			
CMP2_HP4	I	CMPSS-2 High Comparator Positive Input 4	243	R12	72	61	
CMP2_HP5	I	CMPSS-2 High Comparator Positive Input 5		K1			
CMP2_LN0	I	CMPSS-2 Low Comparator Negative Input 0	225	K5	25	17	12
CMP2_LN1	I	CMPSS-2 Low Comparator Negative Input 1		L2	32	24	

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
CMP2_LP0	I	CMPSS-2 Low Comparator Positive Input 0	224	L5	26	18	13
CMP2_LP1	I	CMPSS-2 Low Comparator Positive Input 1		T10			
CMP2_LP2	I	CMPSS-2 Low Comparator Positive Input 2		T9			
CMP2_LP3	I	CMPSS-2 Low Comparator Positive Input 3		M6			
CMP2_LP4	I	CMPSS-2 Low Comparator Positive Input 4	243	R12	72	61	
CMP2_LP5	I	CMPSS-2 Low Comparator Positive Input 5		K1			
CMP3_HN0	I	CMPSS-3 High Comparator Negative Input 0		L3	33	25	16
CMP3_HN1	I	CMPSS-3 High Comparator Negative Input 1		K3	29	21	
CMP3_HP2	I	CMPSS-3 High Comparator Positive Input 2		N3	41	33	22
CMP3_HP4	I	CMPSS-3 High Comparator Positive Input 4		T5	59	51	
CMP3_LN0	I	CMPSS-3 Low Comparator Negative Input 0		L3	33	25	16
CMP3_LN1	I	CMPSS-3 Low Comparator Negative Input 1		K3	29	21	
CMP3_LP2	I	CMPSS-3 Low Comparator Positive Input 2		N3	41	33	22
CMP3_LP3	I	CMPSS-3 Low Comparator Positive Input 3	245	T13	76		
CMP3_LP4	I	CMPSS-3 Low Comparator Positive Input 4		T5	59	51	
CMP4_HN0	I	CMPSS-4 High Comparator Negative Input 0		P1	43	35	24
CMP4_HN1	I	CMPSS-4 High Comparator Negative Input 1	241	N11	66	55	
CMP4_HP1	I	CMPSS-4 High Comparator Positive Input 1	241	N11	66	55	
CMP4_HP3	I	CMPSS-4 High Comparator Positive Input 3		R5	57	49	34
CMP4_HP4	I	CMPSS-4 High Comparator Positive Input 4		T6	60	52	
CMP4_LN0	I	CMPSS-4 Low Comparator Negative Input 0		P1	43	35	24
CMP4_LN1	I	CMPSS-4 Low Comparator Negative Input 1	241	N11	66	55	
CMP4_LP1	I	CMPSS-4 Low Comparator Positive Input 1	241	N11	66	55	
CMP4_LP3	I	CMPSS-4 Low Comparator Positive Input 3		R5	57	49	34
CMP4_LP4	I	CMPSS-4 Low Comparator Positive Input 4		T6	60	52	
CMP5_HN0	I	CMPSS-5 High Comparator Negative Input 0		M6			

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
CMP5_HN1	I	CMPSS-5 High Comparator Negative Input 1	248	P13	73	62	
CMP5_HP0	I	CMPSS-5 High Comparator Positive Input 0		M7			
CMP5_HP1	I	CMPSS-5 High Comparator Positive Input 1	248	P13	73	62	
CMP5_HP2	I	CMPSS-5 High Comparator Positive Input 2	249	N13	74	63	
CMP5_HP5	I	CMPSS-5 High Comparator Positive Input 5	237	M9	64		
CMP5_LN0	I	CMPSS-5 Low Comparator Negative Input 0		M6			
CMP5_LN1	I	CMPSS-5 Low Comparator Negative Input 1	248	P13	73	62	
CMP5_LP0	I	CMPSS-5 Low Comparator Positive Input 0		M7			
CMP5_LP1	I	CMPSS-5 Low Comparator Positive Input 1	248	P13	73	62	
CMP5_LP2	I	CMPSS-5 Low Comparator Positive Input 2	249	N13	74	63	
CMP5_LP3	I	CMPSS-5 Low Comparator Positive Input 3	240	N10	65		
CMP5_LP4	I	CMPSS-5 Low Comparator Positive Input 4	234	G2	16	13	
CMP5_LP5	I	CMPSS-5 Low Comparator Positive Input 5		T8			
CMP6_HN0	I	CMPSS-6 High Comparator Negative Input 0	245	T13	76		
CMP6_HN1	I	CMPSS-6 High Comparator Negative Input 1		T11			
CMP6_HP0	I	CMPSS-6 High Comparator Positive Input 0	244	R13	75		
CMP6_HP1	I	CMPSS-6 High Comparator Positive Input 1		T11			
CMP6_HP2	I	CMPSS-6 High Comparator Positive Input 2		P10			
CMP6_HP4	I	CMPSS-6 High Comparator Positive Input 4	227	H3	21		
CMP6_LN0	I	CMPSS-6 Low Comparator Negative Input 0	245	T13	76		
CMP6_LN1	I	CMPSS-6 Low Comparator Negative Input 1		T11			
CMP6_LP0	I	CMPSS-6 Low Comparator Positive Input 0	244	R13	75		
CMP6_LP1	I	CMPSS-6 Low Comparator Positive Input 1		T11			
CMP6_LP2	I	CMPSS-6 Low Comparator Positive Input 2		P10			
CMP6_LP4	I	CMPSS-6 Low Comparator Positive Input 4	235	G1	15	12	
CMP6_LP5	I	CMPSS-6 Low Comparator Positive Input 5		N7			

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
CMP7_HN0	I	CMPSS-7 High Comparator Negative Input 0		R5	57	49	34
CMP7_HN1	I	CMPSS-7 High Comparator Negative Input 1		K4	30	22	
CMP7_HP1	I	CMPSS-7 High Comparator Positive Input 1		K4	30	22	
CMP7_HP2	I	CMPSS-7 High Comparator Positive Input 2		K3	29	21	
CMP7_HP4	I	CMPSS-7 High Comparator Positive Input 4	228	G3	18		
CMP7_LN0	I	CMPSS-7 Low Comparator Negative Input 0		R5	57	49	34
CMP7_LN1	I	CMPSS-7 Low Comparator Negative Input 1		K4	30	22	
CMP7_LP1	I	CMPSS-7 Low Comparator Positive Input 1		K4	30	22	
CMP7_LP2	I	CMPSS-7 Low Comparator Positive Input 2		K3	29	21	
CMP7_LP4	I	CMPSS-7 Low Comparator Positive Input 4		J2			
CMP7_LP5	I	CMPSS-7 Low Comparator Positive Input 5		P7			
CMP8_HN0	I	CMPSS-8 High Comparator Negative Input 0	240	N10	65		
CMP8_HN1	I	CMPSS-8 High Comparator Negative Input 1	246	P11	67	56	38
CMP8_HP1	I	CMPSS-8 High Comparator Positive Input 1	246	P11	67	56	38
CMP8_HP2	I	CMPSS-8 High Comparator Positive Input 2	247	R11	68	57	39
CMP8_HP4	I	CMPSS-8 High Comparator Positive Input 4	229	G4	17		
CMP8_HP5	I	CMPSS-8 High Comparator Positive Input 5		N8			
CMP8_LN0	I	CMPSS-8 Low Comparator Negative Input 0	240	N10	65		
CMP8_LN1	I	CMPSS-8 Low Comparator Negative Input 1	246	P11	67	56	38
CMP8_LP1	I	CMPSS-8 Low Comparator Positive Input 1	246	P11	67	56	38
CMP8_LP2	I	CMPSS-8 Low Comparator Positive Input 2	247	R11	68	57	39
CMP8_LP3	I	CMPSS-8 Low Comparator Positive Input 3	226	H4	22	16	
CMP8_LP4	I	CMPSS-8 Low Comparator Positive Input 4		J1			
CMP8_LP5	I	CMPSS-8 Low Comparator Positive Input 5		N6			
CMP9_HN0	I	CMPSS-9 High Comparator Negative Input 0		M1	36	28	
CMP9_HN1	I	CMPSS-9 High Comparator Negative Input 1		T9			

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
CMP9_HP1	I	CMPSS-9 High Comparator Positive Input 1		N4	51	43	
CMP9_HP2	I	CMPSS-9 High Comparator Positive Input 2	225	K5	25	17	12
CMP9_HP4	I	CMPSS-9 High Comparator Positive Input 4	230	J5	24		
CMP9_HP5	I	CMPSS-9 High Comparator Positive Input 5		J4			
CMP9_LN0	I	CMPSS-9 Low Comparator Negative Input 0		M1	36	28	
CMP9_LN1	I	CMPSS-9 Low Comparator Negative Input 1		T9			
CMP9_LP1	I	CMPSS-9 Low Comparator Positive Input 1		N4	51	43	
CMP9_LP2	I	CMPSS-9 Low Comparator Positive Input 2	225	K5	25	17	12
CMP9_LP3	I	CMPSS-9 Low Comparator Positive Input 3	239	P12	70	59	41
CMP9_LP4	I	CMPSS-9 Low Comparator Positive Input 4		M5	52	44	
CMP9_LP5	I	CMPSS-9 Low Comparator Positive Input 5		P6			
CMP10_HN0	I	CMPSS-10 High Comparator Negative Input 0		T10			
CMP10_HN1	I	CMPSS-10 High Comparator Negative Input 1		M7			
CMP10_HP1	I	CMPSS-10 High Comparator Positive Input 1		R10			
CMP10_HP2	I	CMPSS-10 High Comparator Positive Input 2		P9			
CMP10_HP4	I	CMPSS-10 High Comparator Positive Input 4	231	H5	23		
CMP10_HP5	I	CMPSS-10 High Comparator Positive Input 5		J3			
CMP10_LN0	I	CMPSS-10 Low Comparator Negative Input 0		T10			
CMP10_LN1	I	CMPSS-10 Low Comparator Negative Input 1		M7			
CMP10_LP1	I	CMPSS-10 Low Comparator Positive Input 1		R10			
CMP10_LP2	I	CMPSS-10 Low Comparator Positive Input 2		P9			
CMP10_LP4	I	CMPSS-10 Low Comparator Positive Input 4		P5	55	47	
CMP10_LP5	I	CMPSS-10 Low Comparator Positive Input 5		R7			
CMP11_HN0	I	CMPSS-11 High Comparator Negative Input 0	230	J5	24		
CMP11_HN1	I	CMPSS-11 High Comparator Negative Input 1		N4	51	43	
CMP11_HP1	I	CMPSS-11 High Comparator Positive Input 1		R9			

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
CMP11_HP2	I	CMPSS-11 High Comparator Positive Input 2		N9			
CMP11_HP5	I	CMPSS-11 High Comparator Positive Input 5		P8			
CMP11_LN0	I	CMPSS-11 Low Comparator Negative Input 0	230	J5	24		
CMP11_LN1	I	CMPSS-11 Low Comparator Negative Input 1		N4	51	43	
CMP11_LP1	I	CMPSS-11 Low Comparator Positive Input 1		R9			
CMP11_LP2	I	CMPSS-11 Low Comparator Positive Input 2		N9			
CMP11_LP4	I	CMPSS-11 Low Comparator Positive Input 4		N5	56	48	
CMP11_LP5	I	CMPSS-11 Low Comparator Positive Input 5		T7			
CMP12_HN0	I	CMPSS-12 High Comparator Negative Input 0	224	L5	26	18	13
CMP12_HP5	I	CMPSS-12 High Comparator Positive Input 5		R8			
CMP12_LN0	I	CMPSS-12 Low Comparator Negative Input 0	224	L5	26	18	13
CMP12_LP0	I	CMPSS-12 Low Comparator Positive Input 0	238	N12	69	58	40
CMP12_LP4	I	CMPSS-12 Low Comparator Positive Input 4	236	M8	63		
D0	I	ADC-D Input 0		R3	47	39	28
D1	I	ADC-D Input 1		T3	48	40	29
D2	I	ADC-D Input 2		R5	57	49	34
D3	I	ADC-D Input 3		R6	58	50	35
D4	I	ADC-D Input 4	240	N10	65		
D5	I	ADC-D Input 5	241	N11	66	55	
D6	I	ADC-D Input 6	242	T12	71	60	
D7	I	ADC-D Input 7	243	R12	72	61	
D8	I	ADC-D Input 8	244	R13	75		
D9	I	ADC-D Input 9	245	T13	76		
D10	I	ADC-D Input 10		N6			
D11	I	ADC-D Input 11		P6			
D12	I	ADC-D Input 12		M7			
D13	I	ADC-D Input 13		M6			
D14	I	ADC-D Input 14		M3	40	32	21
D15	I	ADC-D Input 15		M4	39	31	20
D16	I	ADC-D Input 16		R7			
D17	I	ADC-D Input 17		T7			
D24	I	ADC-D Input 24		M1	36	28	
D25	I	ADC-D Input 25		M2	35	27	
D26	I	ADC-D Input 26		L4	34	26	17
D27	I	ADC-D Input 27		L3	33	25	16
D28	I	ADC-D Input 28		L2	32	24	

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
D29	I	ADC-D Input 29		L1	31	23	
D30	I	ADC-D Input 30		K4	30	22	
D31	I	ADC-D Input 31		K3	29	21	
DACA_OUT	O	Buffered DAC-A Output.		R1	44	36	25
DACB_OUT	O	Buffered DAC-B Output.		P3	49	41	30
E0	I	ADC-E Input 0		P3	49	41	30
E1	I	ADC-E Input 1		P4	50	42	31
E2	I	ADC-E Input 2		T5	59	51	
E3	I	ADC-E Input 3		T6	60	52	
E4	I	ADC-E Input 4	246	P11	67	56	38
E5	I	ADC-E Input 5	247	R11	68	57	39
E6	I	ADC-E Input 6	248	P13	73	62	
E7	I	ADC-E Input 7	249	N13	74	63	
E8	I	ADC-E Input 8		T10			
E9	I	ADC-E Input 9		T9			
E10	I	ADC-E Input 10		R10			
E11	I	ADC-E Input 11		R9			
E12	I	ADC-E Input 12		P9			
E13	I	ADC-E Input 13		N9			
E14	I	ADC-E Input 14		M3	40	32	21
E15	I	ADC-E Input 15		M4	39	31	20
E16	I	ADC-E Input 16		P10			
E17	I	ADC-E Input 17		T11			
E24	I	ADC-E Input 24	224	L5	26	18	13
E25	I	ADC-E Input 25	225	K5	25	17	12
E26	I	ADC-E Input 26	230	J5	24		
E27	I	ADC-E Input 27	231	H5	23		
E28	I	ADC-E Input 28		R2	45	37	26
E29	I	ADC-E Input 29		T2	46	38	27
E30	I	ADC-E Input 30		N4	51	43	
E31	I	ADC-E Input 31		M5	52	44	
VDAC	I	Optional external reference voltage for on-chip DACs.		P2	42	34	23
VREFHIAB	I	ADC-AB high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. NOTE: Do not load this pin externally		N2	38	30	19

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
VREFHICDE	I	ADC-CDE high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. NOTE: Do not load this pin externally		R4	54	46	33
VREFLOAB	I	ADC-AB Low Reference		N1	37	29	18
VREFLOCDE	I	ADC-CDE Low Reference		T4	53	45	32

5.3.2 Digital Signals

Table 5-3. Digital Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
ADCA_EXTMUXSEL0	O	External ADC selection Mux output	224	L5	26	18	13
ADCA_EXTMUXSEL1	O	External ADC selection Mux output	225	K5	25	17	12
ADCA_EXTMUXSEL2	O	External ADC selection Mux output	10, 226	C5, H4	22, 172	16, 140	98
ADCA_EXTMUXSEL3	O	External ADC selection Mux output	15, 227	C4, H3	1, 21	1	1
ADCB_EXTMUXSEL0	O	External ADC selection Mux output	18, 230	F2, J5	13, 24	10	8
ADCB_EXTMUXSEL1	O	External ADC selection Mux output	22, 231	F1, H5	14, 23	11	9
ADCB_EXTMUXSEL2	O	External ADC selection Mux output	232	H2	20	15	11
ADCB_EXTMUXSEL3	O	External ADC selection Mux output	233	H1	19	14	10
ADCC_EXTMUXSEL0	O	External ADC selection Mux output	23, 236	B8, M8	63, 159	127	87
ADCC_EXTMUXSEL1	O	External ADC selection Mux output	29, 237	A9, M9	64, 151	121	84
ADCC_EXTMUXSEL2	O	External ADC selection Mux output	238	N12	69	58	40
ADCC_EXTMUXSEL3	O	External ADC selection Mux output	239	P12	70	59	41
ADCD_EXTMUXSEL0	O	External ADC selection Mux output	63, 240	H14, N10	65, 110	91	59
ADCD_EXTMUXSEL1	O	External ADC selection Mux output	64, 241	H15, N11	66, 111	55, 92	60
ADCD_EXTMUXSEL2	O	External ADC selection Mux output	65, 242	H16, T12	71, 112	60, 93	61
ADCD_EXTMUXSEL3	O	External ADC selection Mux output	66, 243	G13, R12	72, 113	61, 94	62
ADCE_EXTMUXSEL0	O	External ADC selection Mux output	246	P11	67	56	38
ADCE_EXTMUXSEL1	O	External ADC selection Mux output	247	R11	68	57	39
ADCE_EXTMUXSEL2	O	External ADC selection Mux output	42, 248	C16, P13	73, 130	62, 107	74
ADCE_EXTMUXSEL3	O	External ADC selection Mux output	43, 249	C15, N13	74, 131	63, 108	75
ADCSOCAO	O	ADC Start of Conversion A Output for External ADC (from ePWM modules)	8, 12	A3, D6	170, 174	138, 142	96, 100
ADCSOCBO	O	ADC Start of Conversion B Output for External ADC (from ePWM modules)	10, 19	B1, C5	5, 172	5, 140	98
EMIF1_A0	O	External memory interface 1 address line 0	35, 38	E1, E14	10, 125	104	72
EMIF1_A1	O	External memory interface 1 address line 1	12, 36, 39	A3, N14, P15	86, 174	142	100
EMIF1_A2	O	External memory interface 1 address line 2	37, 40, 42	C16, P16, R16	85, 87, 130	107	74
EMIF1_A3	O	External memory interface 1 address line 3	38, 41	E14, N15	89, 125	73, 104	50, 72
EMIF1_A4	O	External memory interface 1 address line 4	39, 43, 44	C15, G14, P15	86, 114, 131	108	75
EMIF1_A5	O	External memory interface 1 address line 5	45, 49, 101	B5, G15, M15	92, 116	75	
EMIF1_A6	O	External memory interface 1 address line 6	46, 50	D14, M14	93, 128	76	
EMIF1_A7	O	External memory interface 1 address line 7	47, 51	D15, M13	94, 129	77	
EMIF1_A8	O	External memory interface 1 address line 8	48, 52	L14, N16	90, 95	78	
EMIF1_A9	O	External memory interface 1 address line 9	49, 53	L15, M15	92, 96	75, 79	
EMIF1_A10	O	External memory interface 1 address line 10	50, 54	L16, M14	93, 97	76, 80	
EMIF1_A11	O	External memory interface 1 address line 11	51, 127	F13, M13	94, 118	77, 97	64
EMIF1_A12	O	External memory interface 1 address line 12	30, 52	A10, L14	95, 150	78, 120	83
EMIF1_A13	O	External memory interface 1 address line 13	0, 42, 86	A8, C11, C16	130, 160	107, 128	74, 88
EMIF1_A14	O	External memory interface 1 address line 14	1, 87	A7, C10	161	129	89
EMIF1_A15	O	External memory interface 1 address line 15	2, 88	B7, C3	162	130	90
EMIF1_A16	O	External memory interface 1 address line 16	3, 89	C7, D4	163	131	91
EMIF1_A17	O	External memory interface 1 address line 17	4, 90	D3, D7	164	132	92
EMIF1_A18	O	External memory interface 1 address line 18	5, 91	A6, D2	165	133	93
EMIF1_A19	O	External memory interface 1 address line 19	92, 219	E2, M16	91	74	51
EMIF1_BA0	O	External memory interface 1 bank address 0	16, 20, 33, 93, 103	C1, D5, D16, E3, P14	2, 6, 126	2, 105	2
EMIF1_BA1	O	External memory interface 1 bank address 1	17, 21, 34, 92, 94, 100	B2, B4, C2, D1, E2, E4	4, 7, 9	4, 7	4
EMIF1_CAS	O	External memory interface 1 column address strobe	7, 86, 89, 221	C6, C11, D4, F16	121, 167	100, 135	68
EMIF1_CLK	O	External memory interface 1 clock	6, 30	A10, B6	150, 166	120, 134	83, 94
EMIF1_CS0n	O	External memory interface 1 chip select 0	13, 32	A2, G16	117, 175	96, 143	
EMIF1_CS2n	O	External memory interface 1 chip select 2	28, 34, 38	D1, D9, E14	9, 125, 154	7, 104	72
EMIF1_CS3n	O	External memory interface 1 chip select 3	19, 35	B1, E1	5, 10	5	
EMIF1_CS4n	O	External memory interface 1 chip select 4	28, 30, 84	A10, D9, D11	148, 150, 154	119, 120	81, 83

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
EMIF1_D0	I/O	External memory interface 1 data line 0	0, 55, 60, 85	A8, B11, J15, K13	99, 106, 160	88, 128	56, 88
EMIF1_D1	I/O	External memory interface 1 data line 1	56, 83, 84	A11, D11, K14	100, 148	82, 119	81
EMIF1_D2	I/O	External memory interface 1 data line 2	57, 82	D10, K15	102	84	
EMIF1_D3	I/O	External memory interface 1 data line 3	1, 81, 103	A7, A12, D16	126, 161	105, 129	89
EMIF1_D4	I/O	External memory interface 1 data line 4	2, 68, 80	B7, B12, B15	133, 162	109, 130	90
EMIF1_D5	I/O	External memory interface 1 data line 5	3, 71, 79	B14, C7, C12	136, 146, 163	111, 131	77, 91
EMIF1_D6	I/O	External memory interface 1 data line 6	61, 78	D12, J13	108, 145	89, 117	57
EMIF1_D7	I/O	External memory interface 1 data line 7	62, 77	A13, H13	109, 144	90, 116	58
EMIF1_D8	I/O	External memory interface 1 data line 8	76	B13	143	115	
EMIF1_D9	I/O	External memory interface 1 data line 9	4, 13, 75	A2, C13, D7	142, 164, 175	132, 143	92
EMIF1_D10	I/O	External memory interface 1 data line 10	5, 74	A6, D13	141, 165	133	93
EMIF1_D11	I/O	External memory interface 1 data line 11	9, 73	A5, E13	140, 171	139	97
EMIF1_D12	I/O	External memory interface 1 data line 12	72	A14	139	114	80
EMIF1_D13	I/O	External memory interface 1 data line 13	14, 43, 68, 71	B3, B14, B15, C15	131, 133, 136, 176	108, 109, 111, 144	75, 77
EMIF1_D14	I/O	External memory interface 1 data line 14	70	C14	135	110	76
EMIF1_D15	I/O	External memory interface 1 data line 15	11, 69	A4, A15	134, 173	141	99
EMIF1_D16	I/O	External memory interface 1 data line 16	68	B15	133	109	
EMIF1_D17	I/O	External memory interface 1 data line 17	14, 67, 99	B3, B16, G5	132, 176	144	
EMIF1_D18	I/O	External memory interface 1 data line 18	66, 127	F13, G13	113, 118	94, 97	62, 64
EMIF1_D19	I/O	External memory interface 1 data line 19	65	H16	112	93	61
EMIF1_D20	I/O	External memory interface 1 data line 20	64	H15	111	92	60
EMIF1_D21	I/O	External memory interface 1 data line 21	63	H14	110	91	59
EMIF1_D22	I/O	External memory interface 1 data line 22	62	H13	109	90	58
EMIF1_D23	I/O	External memory interface 1 data line 23	61	J13	108	89	57
EMIF1_D24	I/O	External memory interface 1 data line 24	37, 60, 100	B4, J15, R16	85, 106	88	56
EMIF1_D25	I/O	External memory interface 1 data line 25	59	J16	104	86	54
EMIF1_D26	I/O	External memory interface 1 data line 26	58	K16	103	85	53
EMIF1_D27	I/O	External memory interface 1 data line 27	57	K15	102	84	
EMIF1_D28	I/O	External memory interface 1 data line 28	56	K14	100	82	
EMIF1_D29	I/O	External memory interface 1 data line 29	16, 55	D5, K13	2, 99	2	2
EMIF1_D30	I/O	External memory interface 1 data line 30	54	L16	97	80	
EMIF1_D31	I/O	External memory interface 1 data line 31	53	L15	96	79	
EMIF1_DQM0	O	External memory interface 1 Input/output mask for byte 0	6, 24, 88, 92	B6, C3, C8, E2	158, 166	126, 134	94
EMIF1_DQM1	O	External memory interface 1 Input/output mask for byte 1	7, 25, 88, 89	C3, C6, D4, D8	157, 167	125, 135	86
EMIF1_DQM2	O	External memory interface 1 Input/output mask for byte 2	20, 26, 85, 90, 91	B9, B11, C1, D2, D3	6, 156	124	85
EMIF1_DQM3	O	External memory interface 1 Input/output mask for byte 3	17, 27, 87, 91, 99	B2, C9, C10, D2, G5	4, 155	4	4
EMIF1_OEn	O	External memory interface 1 output enable	32, 37, 66	G13, G16, R16	85, 113, 117	94, 96	62
EMIF1_RAS	O	External memory interface 1 row address strobe	8, 87, 90	C10, D3, D6	170	138	96
EMIF1_RNW	O	External memory interface 1 read not write	31, 33, 63	B10, H14, P14	110, 149	91	59, 82
EMIF1_SDCKE	O	External memory interface 1 SDRAM clock enable	248	P13	73	62	
EMIF1_WAIT	I	External memory interface 1 Asynchronous SRAM WAIT	36, 55, 64	H15, K13, N14	99, 111	92	60
EMIF1_WEn	O	External memory interface 1 write enable	31, 36, 65	B10, H16, N14	112, 149	93	61, 82
EPWM1_A	O	ePWM-1 Output A	0, 40	A8, P16	87, 160	128	88
EPWM1_B	O	ePWM-1 Output B	1, 41	A7, N15	89, 161	73, 129	50, 89
EPWM2_A	O	ePWM-2 Output A	2, 24	B7, C8	158, 162	126, 130	90
EPWM2_B	O	ePWM-2 Output B	3, 25	C7, D8	157, 163	125, 131	86, 91
EPWM3_A	O	ePWM-3 Output A	4, 48	D7, N16	90, 164	132	92
EPWM3_B	O	ePWM-3 Output B	5, 34, 60	A6, D1, J15	9, 106, 165	7, 88, 133	56, 93
EPWM4_A	O	ePWM-4 Output A	6, 27, 46	B6, C9, D14	128, 155, 166	134	94
EPWM4_B	O	ePWM-4 Output B	7, 8, 28, 47	C6, D6, D9, D15	129, 154, 167, 170	135, 138	96

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
EPWM5_A	O	ePWM-5 Output A	8, 59	D6, J16	104, 170	86, 138	54, 96
EPWM5_B	O	ePWM-5 Output B	9, 73	A5, E13	140, 171	139	97
EPWM6_A	O	ePWM-6 Output A	14, 220	B3, E16	123, 176	102, 144	70
EPWM6_B	O	ePWM-6 Output B	11, 221	A4, F16	121, 173	100, 141	68, 99
EPWM7_A	O	ePWM-7 Output A	12, 222	A3, T14	77, 174	64, 142	42, 100
EPWM7_B	O	ePWM-7 Output B	11, 13, 223	A2, A4, R14	78, 173, 175	65, 141, 143	43, 99
EPWM8_A	O	ePWM-8 Output A	10, 58, 74, 99, 236, 241	C5, D13, G5, K16, M8, N11	63, 66, 103, 141, 172	55, 85, 140	53, 98
EPWM8_B	O	ePWM-8 Output B	15, 59, 75, 103, 232, 237, 243	C4, C13, D16, H2, J16, M9, R12	1, 20, 64, 72, 104, 126, 142	1, 15, 61, 86, 105	1, 11, 54
EPWM9_A	O	ePWM-9 Output A	16, 63, 76, 100	B4, B13, D5, H14	2, 110, 143	2, 91, 115	2, 59
EPWM9_B	O	ePWM-9 Output B	17, 64, 77, 235	A13, B2, G1, H15	4, 15, 111, 144	4, 12, 92, 116	4, 60
EPWM10_A	O	ePWM-10 Output A	65, 78, 226	D12, H4, H16	22, 112, 145	16, 93, 117	61
EPWM10_B	O	ePWM-10 Output B	19, 66, 79, 231	B1, C12, G13, H5	5, 23, 113, 146	5, 94	62
EPWM11_A	O	ePWM-11 Output A	20, 69, 71, 78, 80, 230	A15, B12, B14, C1, D12, J5	6, 24, 134, 136, 145	111, 117	77
EPWM11_B	O	ePWM-11 Output B	21, 70, 81, 225	A12, C2, C14, K5	7, 25, 135	17, 110	12, 76
EPWM12_A	O	ePWM-12 Output A	22, 71, 82, 224, 234	B14, D10, F1, G2, L5	14, 16, 26, 136	11, 13, 18, 111	9, 13, 77
EPWM12_B	O	ePWM-12 Output B	23, 72, 83, 84, 224, 229, 236	A11, A14, B8, D11, G4, L5, M8	17, 26, 63, 139, 148, 159	18, 114, 119, 127	13, 80, 81, 87
EPWM13_A	O	ePWM-13 Output A	24, 40, 58, 85, 228	B11, C8, G3, K16, P16	18, 87, 103, 158	85, 126	53
EPWM13_B	O	ePWM-13 Output B	25, 41, 86, 233	C11, D8, H1, N15	19, 89, 157	14, 73, 125	10, 50, 86
EPWM14_A	O	ePWM-14 Output A	26, 42, 46, 87, 232, 237	B9, C10, C16, D14, H2, M9	20, 64, 128, 130, 156	15, 107, 124	11, 74, 85
EPWM14_B	O	ePWM-14 Output B	27, 43, 47, 88, 227, 240	C3, C9, C15, D15, H3, N10	21, 65, 129, 131, 155	108	75
EPWM15_A	O	ePWM-15 Output A	18, 28, 50, 89, 247	D4, D9, F2, M14, R11	13, 68, 93, 154	10, 57, 76	8, 39
EPWM15_B	O	ePWM-15 Output B	29, 51, 90, 238	A9, D3, M13, N12	69, 94, 151	58, 77, 121	40, 84
EPWM16_A	O	ePWM-16 Output A	30, 52, 91, 246	A10, D2, L14, P11	67, 95, 150	56, 78, 120	38, 83
EPWM16_B	O	ePWM-16 Output B	31, 53, 55, 92, 239	B10, E2, K13, L15, P12	70, 96, 99, 149	59, 79	41, 82
EPWM17_A	O	ePWM-17 Output A	56, 62, 67, 93, 234	B16, E3, G2, H13, K14	16, 100, 109, 132	13, 82, 90	58
EPWM17_B	O	ePWM-17 Output B	57, 61, 68, 94, 229, 237	B15, E4, G4, J13, K15, M9	17, 64, 102, 108, 133	84, 89, 109	57
EPWM18_A	O	ePWM-18 Output A	14, 34, 37, 41, 95, 101, 127, 228	B3, B5, D1, E5, F13, G3, N15, R16	9, 18, 85, 89, 118, 176	7, 73, 97, 144	50, 64
EPWM18_B	O	ePWM-18 Output B	35, 38, 96, 105, 219, 233	E1, E14, F3, H1, J14, M16	10, 19, 91, 125	14, 74, 104	10, 51, 72
ERRORSTS	O	Error Status Output. This signal requires an external pulldown.	4, 79, 80, 219, 247	B12, C12, D7, M16, R11	68, 91, 146, 164	57, 74, 132	39, 51, 92
ESC_GPI0	I	EtherCAT General-Purpose Input 0	0, 100	A8, B4	160	128	88
ESC_GPI1	I	EtherCAT General-Purpose Input 1	1, 101	A7, B5	161	129	89
ESC_GPI2	I	EtherCAT General-Purpose Input 2	2	B7	162	130	90
ESC_GPI3	I	EtherCAT General-Purpose Input 3	3, 103	C7, D16	126, 163	105, 131	91
ESC_GPI4	I	EtherCAT General-Purpose Input 4	4	D7	164	132	92
ESC_GPI5	I	EtherCAT General-Purpose Input 5	5, 105	A6, J14	165	133	93
ESC_GPI6	I	EtherCAT General-Purpose Input 6	6	B6	166	134	94
ESC_GPI7	I	EtherCAT General-Purpose Input 7	7	C6	167	135	
ESC_GPI8	I	EtherCAT General-Purpose Input 8	219	M16	91	74	51
ESC_GPI9	I	EtherCAT General-Purpose Input 9	220	E16	123	102	70
ESC_GPI10	I	EtherCAT General-Purpose Input 10	221	F16	121	100	68
ESC_GPI11	I	EtherCAT General-Purpose Input 11	222	T14	77	64	42
ESC_GPI12	I	EtherCAT General-Purpose Input 12	223	R14	78	65	43
ESC_GPI13	I	EtherCAT General-Purpose Input 13	65	H16	112	93	61

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
ESC_GPI14	I	EtherCAT General-Purpose Input 14	66	G13	113	94	62
ESC_GPI15	I	EtherCAT General-Purpose Input 15	68	B15	133	109	
ESC_GPI16	I	EtherCAT General-Purpose Input 16	70	C14	135	110	76
ESC_GPI17	I	EtherCAT General-Purpose Input 17	76, 97	B13, F4	143	115	
ESC_GPI18	I	EtherCAT General-Purpose Input 18	78, 98	D12, F5	145	117	
ESC_GPI19	I	EtherCAT General-Purpose Input 19	10	C5	172	140	98
ESC_GPI20	I	EtherCAT General-Purpose Input 20	15	C4	1	1	1
ESC_GPI21	I	EtherCAT General-Purpose Input 21	18, 99	F2, G5	13	10	8
ESC_GPI22	I	EtherCAT General-Purpose Input 22	22	F1	14	11	9
ESC_GPI23	I	EtherCAT General-Purpose Input 23	23	B8	159	127	87
ESC_GPI24	I	EtherCAT General-Purpose Input 24	24	C8	158	126	
ESC_GPI25	I	EtherCAT General-Purpose Input 25	50	M14	93	76	
ESC_GPI26	I	EtherCAT General-Purpose Input 26	51	M13	94	77	
ESC_GPI27	I	EtherCAT General-Purpose Input 27	127	F13	118	97	64
ESC_GPI28	I	EtherCAT General-Purpose Input 28	53	L15	96	79	
ESC_GPI29	I	EtherCAT General-Purpose Input 29	54	L16	97	80	
ESC_GPI30	I	EtherCAT General-Purpose Input 30	56	K14	100	82	
ESC_GPI31	I	EtherCAT General-Purpose Input 31	57	K15	102	84	
ESC_GPO0	O	EtherCAT General-Purpose Output 0	8	D6	170	138	96
ESC_GPO1	O	EtherCAT General-Purpose Output 1	9	A5	171	139	97
ESC_GPO2	O	EtherCAT General-Purpose Output 2	22, 40	F1, P16	14, 87	11	9
ESC_GPO3	O	EtherCAT General-Purpose Output 3	11	A4	173	141	99
ESC_GPO4	O	EtherCAT General-Purpose Output 4	12	A3	174	142	100
ESC_GPO5	O	EtherCAT General-Purpose Output 5	13	A2	175	143	
ESC_GPO6	O	EtherCAT General-Purpose Output 6	14	B3	176	144	
ESC_GPO7	O	EtherCAT General-Purpose Output 7	15	C4	1	1	1
ESC_GPO8	O	EtherCAT General-Purpose Output 8	224	L5	26	18	13
ESC_GPO9	O	EtherCAT General-Purpose Output 9	225	K5	25	17	12
ESC_GPO10	O	EtherCAT General-Purpose Output 10	95, 226	E5, H4	22	16	
ESC_GPO11	O	EtherCAT General-Purpose Output 11	96, 232	F3, H2	20	15	11
ESC_GPO12	O	EtherCAT General-Purpose Output 12	233	H1	19	14	10
ESC_GPO13	O	EtherCAT General-Purpose Output 13	234	G2	16	13	
ESC_GPO14	O	EtherCAT General-Purpose Output 14	235	G1	15	12	
ESC_GPO15	O	EtherCAT General-Purpose Output 15	238	N12	69	58	40
ESC_GPO16	O	EtherCAT General-Purpose Output 16	239	P12	70	59	41
ESC_GPO17	O	EtherCAT General-Purpose Output 17	241	N11	66	55	
ESC_GPO18	O	EtherCAT General-Purpose Output 18	242	T12	71	60	
ESC_GPO19	O	EtherCAT General-Purpose Output 19	243	R12	72	61	
ESC_GPO20	O	EtherCAT General-Purpose Output 20	246	P11	67	56	38
ESC_GPO21	O	EtherCAT General-Purpose Output 21	247	R11	68	57	39
ESC_GPO22	O	EtherCAT General-Purpose Output 22	248	P13	73	62	
ESC_GPO23	O	EtherCAT General-Purpose Output 23	249	N13	74	63	
ESC_GPO24	O	EtherCAT General-Purpose Output 24	84	D11	148	119	81
ESC_GPO25	O	EtherCAT General-Purpose Output 25	103	D16	126	105	
ESC_GPO26	O	EtherCAT General-Purpose Output 26	127	F13	118	97	64
ESC_GPO27	O	EtherCAT General-Purpose Output 27	219	M16	91	74	51
ESC_GPO28	O	EtherCAT General-Purpose Output 28	220	E16	123	102	70
ESC_GPO29	O	EtherCAT General-Purpose Output 29	221	F16	121	100	68
ESC_GPO30	O	EtherCAT General-Purpose Output 30	222	T14	77	64	42
ESC_GPO31	O	EtherCAT General-Purpose Output 31	223	R14	78	65	43
ESC_I2C_SCL	I/OC	EtherCAT I2C Clock	30, 237	A10, M9	64, 150	120	83
ESC_I2C_SDA	I/OC	EtherCAT I2C Data	29, 236	A9, M8	63, 151	121	84
ESC_LATCH0	I	EtherCAT LatchSignal Input 0	29, 34, 60	A9, D1, J15	9, 106, 151	7, 88, 121	56, 84
ESC_LATCH1	I	EtherCAT LatchSignal Input 1	30, 35, 61	A10, E1, J13	10, 108, 150	89, 120	57, 83

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
ESC_LED_ERR	O		33, 60, 241	J15, N11, P14	66, 106	55, 88	56
ESC_LED_LINK0_ACTIVE	O	EtherCAT Link-0 Active	58, 243	K16, R12	72, 103	61, 85	53
ESC_LED_LINK1_ACTIVE	O	EtherCAT Link-1 Active	59, 244	J16, R13	75, 104	86	54
ESC_LED_RUN	O		39, 61, 240, 248	J13, N10, P13, P15	65, 73, 86, 108	62, 89	57
ESC_LED_STATE_RUN	O		62, 242	H13, T12	71, 109	60, 90	58
ESC_MDIO_CLK	O	EtherCAT MDIO Clock	26, 46, 62	B9, D14, H13	109, 128, 156	90, 124	58, 85
ESC_MDIO_DATA	I/O	EtherCAT MDIO Data	27, 39, 47, 57	C9, D15, K15, P15	86, 102, 129, 155	84	
ESC_PDI_UC_IRQ	O	EtherCAT PDI IRQ Interrupt Line	56	K14	100	82	
ESC_PHY0_LINKSTATUS	I	EtherCAT PHY-0 Link Status	53, 55, 86, 232, 249	C11, H2, K13, L15, N13	20, 74, 96, 99	15, 63, 79	11
ESC_PHY1_LINKSTATUS	I	EtherCAT PHY-1 Link Status	14, 68, 233	B3, B15, H1	19, 133, 176	14, 109, 144	10
ESC_PHY_CLK	O	EtherCAT PHY Clock	48, 54	L16, N16	90, 97	80	
ESC_PHY_RESETn	O	EtherCAT PHY Active Low Reset	23, 76, 245	B8, B13, T13	76, 143, 159	115, 127	87
ESC_RX0_CLK	I	EtherCAT MII Receive-0 Clock	24, 77	A13, C8	144, 158	116, 126	
ESC_RX0_DATA0	I	EtherCAT MII Receive-0 Data-0	27, 32, 80	B12, C9, G16	117, 155	96	
ESC_RX0_DATA1	I	EtherCAT MII Receive-0 Data-1	28, 38, 81	A12, D9, E14	125, 154	104	72
ESC_RX0_DATA2	I	EtherCAT MII Receive-0 Data-2	41, 82	D10, N15	89	73	50
ESC_RX0_DATA3	I	EtherCAT MII Receive-0 Data-3	83, 84	A11, D11	148	119	81
ESC_RX0_DV	I	EtherCAT MII Receive-0 Data Valid	25, 78	D8, D12	145, 157	117, 125	86
ESC_RX0_ERR	I	EtherCAT MII Receive-0 Error	26, 79	B9, C12	146, 156	124	85
ESC_RX1_CLK	I	EtherCAT MII Receive-1 Clock	16, 69	A15, D5	2, 134	2	2
ESC_RX1_DATA0	I	EtherCAT MII Receive-1 Data-0	31, 63	B10, H14	110, 149	91	59, 82
ESC_RX1_DATA1	I	EtherCAT MII Receive-1 Data-1	37, 64	H15, R16	85, 111	92	60
ESC_RX1_DATA2	I	EtherCAT MII Receive-1 Data-2	65	H16	112	93	61
ESC_RX1_DATA3	I	EtherCAT MII Receive-1 Data-3	66	G13	113	94	62
ESC_RX1_DV	I	EtherCAT MII Receive-1 Data Valid	17, 70	B2, C14	4, 135	4, 110	4, 76
ESC_RX1_ERR	I	EtherCAT MII Receive-1 Error	2, 71	B7, B14	136, 162	111, 130	77, 90
ESC_SYNC0	O	EtherCAT SyncSignal Output 0	34, 127, 238	D1, F13, N12	9, 69, 118	7, 58, 97	40, 64
ESC_SYNC1	O	EtherCAT SyncSignal Output 1	30, 35, 239	A10, E1, P12	10, 70, 150	59, 120	41, 83
ESC_TX0_CLK	I	EtherCAT MII Transmit-0 Clock	9, 85	A5, B11	171	139	97
ESC_TX0_DATA0	O	EtherCAT MII Transmit-0 Data-0	0, 87	A8, C10	160	128	88
ESC_TX0_DATA1	O	EtherCAT MII Transmit-0 Data-1	11, 88	A4, C3	173	141	99
ESC_TX0_DATA2	O	EtherCAT MII Transmit-0 Data-2	12, 89	A3, D4	174	142	100
ESC_TX0_DATA3	O	EtherCAT MII Transmit-0 Data-3	13, 58, 90	A2, D3, K16	103, 175	85, 143	53
ESC_TX0_ENA	I/O	EtherCAT MII Transmit-0 Enable	59, 84, 219	D11, J16, M16	91, 104, 148	74, 86, 119	51, 54, 81
ESC_TX1_CLK	I	EtherCAT MII Transmit-1 Clock	44, 51, 93	E3, G14, M13	94, 114	77	
ESC_TX1_DATA0	O	EtherCAT MII Transmit-1 Data-0	1, 75	A7, C13	142, 161	129	89
ESC_TX1_DATA1	O	EtherCAT MII Transmit-1 Data-1	21, 50, 74	C2, D13, M14	7, 93, 141	76	
ESC_TX1_DATA2	O	EtherCAT MII Transmit-1 Data-2	20, 49, 73	C1, E13, M15	6, 92, 140	75	
ESC_TX1_DATA3	O	EtherCAT MII Transmit-1 Data-3	19, 72	A14, B1	5, 139	5, 114	80
ESC_TX1_ENA	I/O	EtherCAT MII Transmit-1 Enable	45, 52, 94	E4, G15, L14	95, 116	78	
FSIRXA_CLK	I	FSIRX-A Input Clock	5, 9, 13, 54, 105	A2, A5, A6, J14, L16	97, 165, 171, 175	80, 133, 139, 143	93, 97
FSIRXA_D0	I	FSIRX-A Primary Data Input	3, 8, 12, 52, 103	A3, C7, D6, D16, L14	95, 126, 163, 170, 174	78, 105, 131, 138, 142	91, 96, 100
FSIRXA_D1	I	FSIRX-A Optional Additional Data Input	4, 11, 53	A4, D7, L15	96, 164, 173	79, 132, 141	92, 99
FSIRXB_CLK	I	FSIRX-B Input Clock	11, 60	A4, J15	106, 173	88, 141	56, 99
FSIRXB_D0	I	FSIRX-B Primary Data Input	9, 58, 70	A5, C14, K16	103, 135, 171	85, 110, 139	53, 76, 97
FSIRXB_D1	I	FSIRX-B Optional Additional Data Input	59, 68	B15, J16	104, 133	86, 109	54
FSIRXC_CLK	I	FSIRX-C Input Clock	14, 16	B3, D5	2, 176	2, 144	2
FSIRXC_D0	I	FSIRX-C Primary Data Input	12, 76	A3, B13	143, 174	115, 142	100
FSIRXC_D1	I	FSIRX-C Optional Additional Data Input	13, 127	A2, F13	118, 175	97, 143	64
FSIRXD_CLK	I	FSIRX-D Input Clock	17, 39, 41, 44, 92	B2, E2, G14, N15, P15	4, 86, 89, 114	4, 73	4, 50

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
FSIRXD_D0	I	FSIRX-D Primary Data Input	42, 45	C16, G15	116, 130	107	74
FSIRXD_D1	I	FSIRX-D Optional Additional Data Input	16, 43, 100	B4, C15, D5	2, 131	2, 108	2, 75
FSITXA_CLK	O	FSITX-A Output Clock	2, 27, 51	B7, C9, M13	94, 155, 162	77, 130	90
FSITXA_D0	O	FSITX-A Primary Data Output	0, 9, 26, 49, 74, 100	A5, A8, B4, B9, D13, M15	92, 141, 156, 160, 171	75, 124, 128, 139	85, 88, 97
FSITXA_D1	O	FSITX-A Optional Additional Data Output	1, 8, 25, 50, 101	A7, B5, D6, D8, M14	93, 157, 161, 170	76, 125, 129, 138	86, 89, 96
FSITXB_CLK	O	FSITX-B Output Clock	8, 56, 65, 67	B16, D6, H16, K14	100, 112, 132, 170	82, 93, 138	61, 96
FSITXB_D0	O	FSITX-B Primary Data Output	6, 55, 69, 71, 77	A13, A15, B6, B14, K13	99, 134, 136, 144, 166	111, 116, 134	77, 94
FSITXB_D1	O	FSITX-B Optional Additional Data Output	7, 57, 66	C6, G13, K15	102, 113, 167	84, 94, 135	62
FSITXC_CLK	O	FSITX-C Output Clock	71, 73	B14, E13	136, 140	111	77
FSITXC_D0	O	FSITX-C Primary Data Output	72, 79	A14, C12	139, 146	114	80
FSITXC_D1	O	FSITX-C Optional Additional Data Output	78, 84	D11, D12	145, 148	117, 119	81
FSITXD_CLK	O	FSITX-D Output Clock	61, 64	H15, J13	108, 111	89, 92	57, 60
FSITXD_D0	O	FSITX-D Primary Data Output	31, 62	B10, H13	109, 149	90	58, 82
FSITXD_D1	O	FSITX-D Optional Additional Data Output	38, 63	E14, H14	110, 125	91, 104	59, 72
GPIO0	I/O	General-Purpose Input Output 0	0	A8	160	128	88
GPIO1	I/O	General-Purpose Input Output 1	1	A7	161	129	89
GPIO2	I/O	General-Purpose Input Output 2	2	B7	162	130	90
GPIO3	I/O	General-Purpose Input Output 3	3	C7	163	131	91
GPIO4	I/O	General-Purpose Input Output 4	4	D7	164	132	92
GPIO5	I/O	General-Purpose Input Output 5	5	A6	165	133	93
GPIO6	I/O	General-Purpose Input Output 6	6	B6	166	134	94
GPIO7	I/O	General-Purpose Input Output 7	7	C6	167	135	
GPIO8	I/O	General-Purpose Input Output 8	8	D6	170	138	96
GPIO9	I/O	General-Purpose Input Output 9	9	A5	171	139	97
GPIO10	I/O	General-Purpose Input Output 10	10	C5	172	140	98
GPIO11	I/O	General-Purpose Input Output 11	11	A4	173	141	99
GPIO12	I/O	General-Purpose Input Output 12	12	A3	174	142	100
GPIO13	I/O	General-Purpose Input Output 13	13	A2	175	143	
GPIO14	I/O	General-Purpose Input Output 14	14	B3	176	144	
GPIO15	I/O	General-Purpose Input Output 15	15	C4	1	1	1
GPIO16	I/O	General-Purpose Input Output 16	16	D5	2	2	2
GPIO17	I/O	General-Purpose Input Output 17	17	B2	4	4	4
GPIO18	I/O	General-Purpose Input Output 18	18	F2	13	10	8
GPIO19	I/O	General-Purpose Input Output 19	19	B1	5	5	
GPIO20	I/O	General-Purpose Input Output 20	20	C1	6		
GPIO21	I/O	General-Purpose Input Output 21	21	C2	7		
GPIO22	I/O	General-Purpose Input Output 22	22	F1	14	11	9
GPIO23	I/O	General-Purpose Input Output 23	23	B8	159	127	87
GPIO24	I/O	General-Purpose Input Output 24	24	C8	158	126	
GPIO25	I/O	General-Purpose Input Output 25	25	D8	157	125	86
GPIO26	I/O	General-Purpose Input Output 26	26	B9	156	124	85
GPIO27	I/O	General-Purpose Input Output 27	27	C9	155		
GPIO28	I/O	General-Purpose Input Output 28	28	D9	154		
GPIO29	I/O	General-Purpose Input Output 29	29	A9	151	121	84
GPIO30	I/O	General-Purpose Input Output 30	30	A10	150	120	83
GPIO31	I/O	General-Purpose Input Output 31	31	B10	149		82
GPIO32	I/O	General-Purpose Input Output 32	32	G16	117	96	
GPIO33	I/O	General-Purpose Input Output 33	33	P14			
GPIO34	I/O	General-Purpose Input Output 34	34	D1	9	7	
GPIO35	I/O	General-Purpose Input Output 35	35	E1	10		
GPIO36	I/O	General-Purpose Input Output 36	36	N14			
GPIO37	I/O	General-Purpose Input Output 37	37	R16	85		

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
GPIO38	I/O	General-Purpose Input Output 38	38	E14	125	104	72
GPIO39	I/O	General-Purpose Input Output 39	39	P15	86		
GPIO40	I/O	General-Purpose Input Output 40	40	P16	87		
GPIO41	I/O	General-Purpose Input Output 41	41	N15	89	73	50
GPIO42	I/O	General-Purpose Input Output 42	42	C16	130	107	74
GPIO43	I/O	General-Purpose Input Output 43	43	C15	131	108	75
GPIO44	I/O	General-Purpose Input Output 44	44	G14	114		
GPIO45	I/O	General-Purpose Input Output 45	45	G15	116		
GPIO46	I/O	General-Purpose Input Output 46	46	D14	128		
GPIO47	I/O	General-Purpose Input Output 47	47	D15	129		
GPIO48	I/O	General-Purpose Input Output 48	48	N16	90		
GPIO49	I/O	General-Purpose Input Output 49	49	M15	92	75	
GPIO50	I/O	General-Purpose Input Output 50	50	M14	93	76	
GPIO51	I/O	General-Purpose Input Output 51	51	M13	94	77	
GPIO52	I/O	General-Purpose Input Output 52	52	L14	95	78	
GPIO53	I/O	General-Purpose Input Output 53	53	L15	96	79	
GPIO54	I/O	General-Purpose Input Output 54	54	L16	97	80	
GPIO55	I/O	General-Purpose Input Output 55	55	K13	99		
GPIO56	I/O	General-Purpose Input Output 56	56	K14	100	82	
GPIO57	I/O	General-Purpose Input Output 57	57	K15	102	84	
GPIO58	I/O	General-Purpose Input Output 58	58	K16	103	85	53
GPIO59	I/O	General-Purpose Input Output 59	59	J16	104	86	54
GPIO60	I/O	General-Purpose Input Output 60	60	J15	106	88	56
GPIO61	I/O	General-Purpose Input Output 61	61	J13	108	89	57
GPIO62	I/O	General-Purpose Input Output 62	62	H13	109	90	58
GPIO63	I/O	General-Purpose Input Output 63	63	H14	110	91	59
GPIO64	I/O	General-Purpose Input Output 64	64	H15	111	92	60
GPIO65	I/O	General-Purpose Input Output 65	65	H16	112	93	61
GPIO66	I/O	General-Purpose Input Output 66	66	G13	113	94	62
GPIO67	I/O	General-Purpose Input Output 67	67	B16	132		
GPIO68	I/O	General-Purpose Input Output 68	68	B15	133	109	
GPIO69	I/O	General-Purpose Input Output 69	69	A15	134		
GPIO70	I/O	General-Purpose Input Output 70	70	C14	135	110	76
GPIO71	I/O	General-Purpose Input Output 71	71	B14	136	111	77
GPIO72	I/O	General-Purpose Input Output 72	72	A14	139	114	80
GPIO73	I/O	General-Purpose Input Output 73	73	E13	140		
GPIO74	I/O	General-Purpose Input Output 74	74	D13	141		
GPIO75	I/O	General-Purpose Input Output 75	75	C13	142		
GPIO76	I/O	General-Purpose Input Output 76	76	B13	143	115	
GPIO77	I/O	General-Purpose Input Output 77	77	A13	144	116	
GPIO78	I/O	General-Purpose Input Output 78	78	D12	145	117	
GPIO79	I/O	General-Purpose Input Output 79	79	C12	146		
GPIO80	I/O	General-Purpose Input Output 80	80	B12			
GPIO81	I/O	General-Purpose Input Output 81	81	A12			
GPIO82	I/O	General-Purpose Input Output 82	82	D10			
GPIO83	I/O	General-Purpose Input Output 83	83	A11			
GPIO84	I/O	General-Purpose Input Output 84	84	D11	148	119	81
GPIO85	I/O	General-Purpose Input Output 85	85	B11			
GPIO86	I/O	General-Purpose Input Output 86	86	C11			
GPIO87	I/O	General-Purpose Input Output 87	87	C10			
GPIO88	I/O	General-Purpose Input Output 88	88	C3			
GPIO89	I/O	General-Purpose Input Output 89	89	D4			
GPIO90	I/O	General-Purpose Input Output 90	90	D3			
GPIO91	I/O	General-Purpose Input Output 91	91	D2			

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
GPIO92	I/O	General-Purpose Input Output 92	92	E2			
GPIO93	I/O	General-Purpose Input Output 93	93	E3			
GPIO94	I/O	General-Purpose Input Output 94	94	E4			
GPIO95	I/O	General-Purpose Input Output 95	95	E5			
GPIO96	I/O	General-Purpose Input Output 96	96	F3			
GPIO97	I/O	General-Purpose Input Output 97	97	F4			
GPIO98	I/O	General-Purpose Input Output 98	98	F5			
GPIO99	I/O	General-Purpose Input Output 99	99	G5			
GPIO100	I/O	General-Purpose Input Output 100	100	B4			
GPIO101	I/O	General-Purpose Input Output 101	101	B5			
GPIO103	I/O	General-Purpose Input Output 103	103	D16	126	105	
GPIO105	I/O	General-Purpose Input Output 105	105	J14			
GPIO127	I/O	General-Purpose Input Output 127	127	F13	118	97	64
GPIO219	I/O	General-Purpose Input Output 219	219	M16	91	74	51
GPIO220	I/O	General-Purpose Input Output 220	220	E16	123	102	70
GPIO221	I/O	General-Purpose Input Output 221	221	F16	121	100	68
GPIO222	I/O	General-Purpose Input Output 222	222	T14	77	64	42
GPIO223	I/O	General-Purpose Input Output 223	223	R14	78	65	43
GPIO224	I/O	General-Purpose Input Output 224	224	L5	26	18	13
GPIO225	I/O	General-Purpose Input Output 225	225	K5	25	17	12
GPIO226	I/O	General-Purpose Input Output 226	226	H4	22	16	
GPIO227	I/O	General-Purpose Input Output 227	227	H3	21		
GPIO228	I/O	General-Purpose Input Output 228	228	G3	18		
GPIO229	I/O	General-Purpose Input Output 229	229	G4	17		
GPIO230	I/O	General-Purpose Input Output 230	230	J5	24		
GPIO231	I/O	General-Purpose Input Output 231	231	H5	23		
GPIO232	I/O	General-Purpose Input Output 232	232	H2	20	15	11
GPIO233	I/O	General-Purpose Input Output 233	233	H1	19	14	10
GPIO234	I/O	General-Purpose Input Output 234	234	G2	16	13	
GPIO235	I/O	General-Purpose Input Output 235	235	G1	15	12	
GPIO236	I/O	General-Purpose Input Output 236	236	M8	63		
GPIO237	I/O	General-Purpose Input Output 237	237	M9	64		
GPIO238	I/O	General-Purpose Input Output 238	238	N12	69	58	40
GPIO239	I/O	General-Purpose Input Output 239	239	P12	70	59	41
GPIO240	I/O	General-Purpose Input Output 240	240	N10	65		
GPIO241	I/O	General-Purpose Input Output 241	241	N11	66	55	
GPIO242	I/O	General-Purpose Input Output 242	242	T12	71	60	
GPIO243	I/O	General-Purpose Input Output 243	243	R12	72	61	
GPIO244	I/O	General-Purpose Input Output 244	244	R13	75		
GPIO245	I/O	General-Purpose Input Output 245	245	T13	76		
GPIO246	I/O	General-Purpose Input Output 246	246	P11	67	56	38
GPIO247	I/O	General-Purpose Input Output 247	247	R11	68	57	39
GPIO248	I/O	General-Purpose Input Output 248	248	P13	73	62	
GPIO249	I/O	General-Purpose Input Output 249	249	N13	74	63	
I2CA_SCL	I/OD	I2C-A Open-Drain Bidirectional Clock	1, 10, 18, 33, 43, 57, 92, 105, 239	A7, C5, C15, E2, F2, J14, K15, P12, P14	13, 70, 102, 131, 161, 172	10, 59, 84, 108, 129, 140	8, 41, 75, 89, 98
I2CA_SDA	I/OD	I2C-A Open-Drain Bidirectional Data	0, 15, 29, 31, 32, 42, 56, 91, 237, 242	A8, A9, B10, C4, C16, D2, G16, K14, M9, T12	1, 64, 71, 100, 117, 130, 149, 151, 160	1, 60, 82, 96, 107, 121, 128	1, 74, 82, 84, 88
I2CB_SCL	I/OD	I2C-B Open-Drain Bidirectional Clock	3, 23, 35, 41, 69, 222, 230	A15, B8, C7, E1, J5, N15, T14	10, 24, 77, 89, 134, 159, 163	64, 73, 127, 131	42, 50, 87, 91
I2CB_SDA	I/OD	I2C-B Open-Drain Bidirectional Data	2, 22, 34, 40, 66, 223, 225	B7, D1, F1, G13, K5, P16, R14	9, 14, 25, 78, 87, 113, 162	7, 11, 17, 65, 94, 130	9, 12, 43, 62, 90
LINA_RX	I	LIN-A Receive	7, 15, 236	C4, C6, M8	1, 63, 167	1, 135	1
LINA_TX	O	LIN-A Transmit	6, 14, 237, 247	B3, B6, M9, R11	64, 68, 166, 176	57, 134, 144	39, 94

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
LINB_RX	I	LIN-B Receive	25, 68, 233	B15, D8, H1	19, 133, 157	14, 109, 125	10, 86
LINB_TX	O	LIN-B Transmit	24, 67, 228, 239	B16, C8, G3, P12	18, 70, 132, 158	59, 126	41
MCANA_RX	I	MCAN-A Receive	65, 229, 235	G1, G4, H16	15, 17, 112	12, 93	61
MCANA_TX	O	MCAN-A Transmit	64, 234	G2, H15	16, 111	13, 92	60
MCANB_RX	I	MCAN-B Receive	7, 20, 40, 44, 72	A14, C1, C6, G14, P16	6, 87, 114, 139, 167	114, 135	80
MCANB_TX	O	MCAN-B Transmit	6, 21, 41, 45, 73	B6, C2, E13, G15, N15	7, 89, 116, 140, 166	73, 134	50, 94
MCANC_RX	I	MCAN-C Receive	5, 10, 23, 30, 36, 58, 61, 62, 70, 75, 221, 246, 247	A6, A10, B8, C5, C13, C14, F16, H13, J13, K16, N14, P11, R11	67, 68, 103, 108, 109, 121, 135, 142, 150, 159, 165, 172	56, 57, 85, 89, 90, 100, 110, 120, 127, 133, 140	38, 39, 53, 57, 58, 68, 76, 83, 87, 93, 98
MCANC_TX	O	MCAN-C Transmit	4, 8, 19, 22, 31, 37, 59, 62, 63, 71, 74, 220	B1, B10, B14, D6, D7, D13, E16, F1, H13, H14, J16, R16	5, 14, 85, 104, 109, 110, 123, 136, 141, 149, 164, 170	5, 11, 86, 90, 91, 102, 111, 132, 138	9, 54, 58, 59, 70, 77, 82, 92, 96
MCAND_RX	I	MCAN-D Receive	1, 17, 57, 68, 92, 224, 231	A7, B2, B15, E2, H5, K15, L5	4, 23, 26, 102, 133, 161	4, 18, 84, 109, 129	4, 13, 89
MCAND_TX	O	MCAN-D Transmit	0, 16, 56, 67, 91, 226	A8, B16, D2, D5, H4, K14	2, 22, 100, 132, 160	2, 16, 82, 128	2, 88
MCANE_RX	I	MCAN-E Receive	25, 47, 77	A13, D8, D15	129, 144, 157	116, 125	86
MCANE_TX	O	MCAN-E Transmit	24, 26, 46, 76	B9, B13, C8, D14	128, 143, 156, 158	115, 124, 126	85
MCANF_RX	I	MCAN-F Receive	3, 51, 84	C7, D11, M13	94, 148, 163	77, 119, 131	81, 91
MCANF_TX	O	MCAN-F Transmit	2, 50, 78	B7, D12, M14	93, 145, 162	76, 117, 130	90
OUTPUTXBAR1	O	Output X-BAR Output 1	2, 24, 34, 219, 226, 228	B7, C8, D1, G3, H4, M16	9, 18, 22, 91, 158, 162	7, 16, 74, 126, 130	51, 90
OUTPUTXBAR2	O	Output X-BAR Output 2	3, 25, 37, 220, 231, 233	C7, D8, E16, H1, H5, R16	19, 23, 85, 123, 157, 163	14, 102, 125, 131	10, 70, 86, 91
OUTPUTXBAR3	O	Output X-BAR Output 3	4, 5, 14, 26, 48, 60, 221, 230, 232	A6, B3, B9, D7, F16, H2, J5, J15, N16	20, 24, 90, 106, 121, 156, 164, 165, 176	15, 88, 100, 124, 132, 133, 144	11, 56, 68, 85, 92, 93
OUTPUTXBAR4	O	Output X-BAR Output 4	6, 15, 27, 49, 61, 222, 225, 227	B6, C4, C9, H3, J13, K5, M15, T14	1, 21, 25, 77, 92, 108, 155, 166	1, 17, 64, 75, 89, 134	1, 12, 42, 57, 94
OUTPUTXBAR5	O	Output X-BAR Output 5	7, 28, 223, 224, 247	C6, D9, L5, R11, R14	26, 68, 78, 154, 167	18, 57, 65, 135	13, 39, 43
OUTPUTXBAR6	O	Output X-BAR Output 6	9, 29, 73, 236, 238	A5, A9, E13, M8, N12	63, 69, 140, 151, 171	58, 121, 139	40, 84, 97
OUTPUTXBAR7	O	Output X-BAR Output 7	11, 16, 30, 237, 246	A4, A10, D5, M9, P11	2, 64, 67, 150, 173	2, 56, 120, 141	2, 38, 83, 99
OUTPUTXBAR8	O	Output X-BAR Output 8	14, 17, 31, 72, 239	A14, B2, B3, B10, P12	4, 70, 139, 149, 176	4, 59, 114, 144	4, 41, 80, 82
OUTPUTXBAR9	O	Output X-BAR Output 9	0, 32, 40, 91, 242	A8, D2, G16, P16, T12	71, 87, 117, 160	60, 96, 128	88
OUTPUTXBAR10	O	Output X-BAR Output 10	1, 33, 41, 92	A7, E2, N15, P14	89, 161	73, 129	50, 89
OUTPUTXBAR11	O	Output X-BAR Output 11	5, 34, 93	A6, D1, E3	9, 165	7, 133	93
OUTPUTXBAR12	O	Output X-BAR Output 12	8, 35, 94	D6, E1, E4	10, 170	138	96
OUTPUTXBAR13	O	Output X-BAR Output 13	10, 36, 42, 95	C5, C16, E5, N14	130, 172	107, 140	74, 98
OUTPUTXBAR14	O	Output X-BAR Output 14	12, 37, 43, 44, 96	A3, C15, F3, G14, R16	85, 114, 131, 174	108, 142	75, 100
OUTPUTXBAR15	O	Output X-BAR Output 15	13, 38, 45, 97	A2, E14, F4, G15	116, 125, 175	104, 143	72
OUTPUTXBAR16	O	Output X-BAR Output 16	15, 39, 75, 98	C4, C13, F5, P15	1, 86, 142	1	1
PMBUSA_ALERT	I/OD	PMBus-A Open-Drain Bidirectional Alert Signal	11, 18, 19	A4, B1, F2	5, 13, 173	5, 10, 141	8, 99
PMBUSA_CTL	I/O	PMBus-A Control Signal - Target Input/Controller Output	12, 15, 26	A3, B9, C4	1, 156, 174	1, 124, 142	1, 85, 100
PMBUSA_SCL	I/OD	PMBus-A Open-Drain Bidirectional Clock	10, 14, 23	B3, B8, C5	159, 172, 176	127, 140, 144	87, 98
PMBUSA_SDA	I/OD	PMBus-A Open-Drain Bidirectional Data	13, 22, 25, 29	A2, A9, D8, F1	14, 151, 157, 175	11, 121, 125, 143	9, 84, 86
SD1_C1	I	SDFM-1 Channel 1 Clock Input	17, 49, 53, 64, 96, 235	B2, F3, G1, H15, L4, L15, M15, N8	4, 15, 34, 92, 96, 111	4, 12, 26, 75, 79, 92	4, 17, 60
SD1_C2	I	SDFM-1 Channel 2 Clock Input	19, 51, 54, 66, 98, 248	B1, F5, G13, L16, M13, P13, R2, R8	5, 45, 73, 94, 97, 113	5, 37, 62, 77, 80, 94	26, 62

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
SD1_C3	I	SDFM-1 Channel 3 Clock Input	21, 53, 55, 68, 90, 127, 226, 231	B15, C2, D3, F13, H4, H5, K13, L15, N7, R3	7, 22, 23, 47, 96, 99, 118, 133	16, 39, 79, 97, 109	28, 64
SD1_C4	I	SDFM-1 Channel 4 Clock Input	55, 56, 70, 229	C14, G4, K13, K14, M7, R5	17, 57, 99, 100, 135	49, 82, 110	34, 76
SD1_D1	I	SDFM-1 Channel 1 Data Input	16, 36, 48, 63, 95, 100, 246	B4, D5, E5, H14, L3, N14, N16, P8, P11	2, 33, 67, 90, 110	2, 25, 56, 91	2, 16, 38, 59
SD1_D2	I	SDFM-1 Channel 2 Data Input	37, 50, 65, 97, 249	F4, H16, M14, N13, R16, T2, T8	46, 74, 85, 93, 112	38, 63, 76, 93	27, 61
SD1_D3	I	SDFM-1 Channel 3 Data Input	20, 38, 52, 67, 89, 226, 238	B16, C1, D4, E14, H4, L14, N12, P7, T3	6, 22, 48, 69, 95, 125, 132	16, 40, 58, 78, 104	29, 40, 72
SD1_D4	I	SDFM-1 Channel 4 Data Input	39, 54, 69, 74, 77, 80, 234, 242	A13, A15, B12, D13, G2, L16, M6, P15, R6, T12	16, 58, 71, 86, 97, 134, 141, 144	13, 50, 60, 80, 116	35
SD2_C1	I	SDFM-2 Channel 1 Clock Input	25, 40, 57, 80, 219, 233	B12, D8, H1, K15, M16, P3, P16, R7	19, 49, 87, 91, 102, 157	14, 41, 74, 84, 125	10, 30, 51, 86
SD2_C2	I	SDFM-2 Channel 2 Clock Input	27, 48, 58, 59, 74, 227	C9, D13, H3, J16, K16, M1, N16, R10	21, 36, 90, 103, 104, 141, 155	28, 85, 86	53, 54
SD2_C3	I	SDFM-2 Channel 3 Clock Input	59, 61, 76, 238	B13, J13, J16, L2, N12, P9	32, 69, 104, 108, 143	24, 58, 86, 89, 115	40, 54, 57
SD2_C4	I	SDFM-2 Channel 4 Clock Input	31, 60, 63, 78, 239	B10, D12, H14, J15, K4, P10, P12	30, 70, 106, 110, 145, 149	22, 59, 88, 91, 117	41, 56, 59, 82
SD2_D1	I	SDFM-2 Channel 1 Data Input	24, 41, 49, 56, 79, 228	C8, C12, G3, K14, M15, N15, P4, T7	18, 50, 89, 92, 100, 146, 158	42, 73, 75, 82, 126	31, 50
SD2_D2	I	SDFM-2 Channel 2 Data Input	26, 50, 58, 73, 242	B9, E13, K16, M2, M14, R9, T12	35, 71, 93, 103, 140, 156	27, 60, 76, 85, 124	53, 85
SD2_D3	I	SDFM-2 Channel 3 Data Input	28, 51, 75, 247	C13, D9, L1, M13, N9, R11	31, 68, 94, 142, 154	23, 57, 77	39
SD2_D4	I	SDFM-2 Channel 4 Data Input	30, 52, 62, 77, 243	A10, A13, H13, K3, L14, R12, T11	29, 72, 95, 109, 144, 150	21, 61, 78, 90, 116, 120	58, 83
SD3_C1	I	SDFM-3 Channel 1 Clock Input	72, 76, 105, 245	A14, B13, J14, N4, T13	51, 76, 139, 143	43, 114, 115	80
SD3_C2	I	SDFM-3 Channel 2 Clock Input	78, 82, 84	D10, D11, D12, P5, R1	44, 55, 145, 148	36, 47, 117, 119	25, 81
SD3_C3	I	SDFM-3 Channel 3 Clock Input	80, 86, 221	B12, C11, F16, M3, T5	40, 59, 121	32, 51, 100	21, 68
SD3_C4	I	SDFM-3 Channel 4 Clock Input	44, 46, 88, 223	C3, D14, G14, P2, R14, T10	42, 78, 114, 128	34, 65	23, 43
SD3_D1	I	SDFM-3 Channel 1 Data Input	71, 77, 232	A13, B14, H2, M5	20, 52, 136, 144	15, 44, 111, 116	11, 77
SD3_D2	I	SDFM-3 Channel 2 Data Input	72, 79, 83	A11, A14, C12, N5, P1	43, 56, 139, 146	35, 48, 114	24, 80
SD3_D3	I	SDFM-3 Channel 3 Data Input	57, 81, 85, 220	A12, B11, E16, K15, M4, T6	39, 60, 102, 123	31, 52, 84, 102	20, 70
SD3_D4	I	SDFM-3 Channel 4 Data Input	45, 87, 222	C10, G15, N3, T9, T14	41, 77, 116	33, 64	22, 42
SD4_C1	I	SDFM-4 Channel 1 Clock Input	14, 90, 225	B3, D3, K2, K5	25, 176	17, 144	12
SD4_C2	I	SDFM-4 Channel 2 Clock Input	12, 92, 236	A3, E2, J2, M8	63, 174	142	100
SD4_C3	I	SDFM-4 Channel 3 Clock Input	40, 42, 47, 94, 240	C16, D15, E4, J4, N10, P16	65, 87, 129, 130	107	74
SD4_C4	I	SDFM-4 Channel 4 Clock Input	42, 100, 103, 244	B4, C16, D16, N6, R13	75, 126, 130	105, 107	74
SD4_D1	I	SDFM-4 Channel 1 Data Input	11, 89, 230	A4, D4, J5, K1	24, 173	141	99
SD4_D2	I	SDFM-4 Channel 2 Data Input	13, 91, 224	A2, D2, J1, L5	26, 175	18, 143	13
SD4_D3	I	SDFM-4 Channel 3 Data Input	41, 93, 237	E3, J3, M9, N15	64, 89	73	50
SD4_D4	I	SDFM-4 Channel 4 Data Input	43, 73, 76, 78, 99, 241	B13, C15, D12, E13, G5, N11, P6	66, 131, 140, 143, 145	55, 108, 115, 117	75
SENT1	I/O	SENT Input Pin 1	15, 58, 235, 242	C4, G1, K16, T12	1, 15, 71, 103	1, 12, 60, 85	1, 53
SENT2	I/O	SENT Input Pin 2	10, 59, 234, 243	C5, G2, J16, R12	16, 72, 104, 172	13, 61, 86, 140	54, 98
SENT3	I/O	SENT Input Pin 3	29, 60, 229, 248	A9, G4, J15, P13	17, 73, 106, 151	62, 88, 121	56, 84

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
SENT4	I/O	SENT Input Pin 4	18, 62, 228, 249	F2, G3, H13, N13	13, 18, 74, 109	10, 63, 90	8, 58
SENT5	I/O	SENT Input Pin 5	22, 63, 233, 244	F1, H1, H14, R13	14, 19, 75, 110	11, 14, 91	9, 10, 59
SENT6	I/O	SENT Input Pin 6	23, 64, 232, 245	B8, H2, H15, T13	20, 76, 111, 159	15, 92, 127	11, 60, 87
SPIA_CLK	I/O	SPI-A Clock	34, 56, 60, 227	D1, H3, J15, K14	9, 21, 100, 106	7, 82, 88	56
SPIA_PICO	I/O	SPI-A Peripheral In, Controller Out (PICO)	16, 32, 54, 58, 100, 231	B4, D5, G16, H5, K16, L16	2, 23, 97, 103, 117	2, 80, 85, 96	2, 53
SPIA_POCI	I/O	SPI-A Peripheral Out, Controller In (POCI)	17, 33, 55, 59, 232	B2, H2, J16, K13, P14	4, 20, 99, 104	4, 15, 86	4, 11, 54
SPIA_PTE	I/O	SPI-A Peripheral Transmit Enable (PTE)	19, 35, 57, 61, 226	B1, E1, H4, J13, K15	5, 10, 22, 102, 108	5, 16, 84, 89	57
SPIB_CLK	I/O	SPI-B Clock	26, 65, 235	B9, G1, H16	15, 112, 156	12, 93, 124	61, 85
SPIB_PICO	I/O	SPI-B Peripheral In, Controller Out (PICO)	24, 63, 225, 229	C8, G4, H14, K5	17, 25, 110, 158	17, 91, 126	12, 59
SPIB_POCI	I/O	SPI-B Peripheral Out, Controller In (POCI)	25, 64, 224, 228	D8, G3, H15, L5	18, 26, 111, 157	18, 92, 125	13, 60, 86
SPIB_PTE	I/O	SPI-B Peripheral Transmit Enable (PTE)	27, 66, 234	C9, G2, G13	16, 113, 155	13, 94	62
SPIC_CLK	I/O	SPI-C Clock	52, 71, 222, 249	B14, L14, N13, T14	74, 77, 95, 136	63, 64, 78, 111	42, 77
SPIC_PICO	I/O	SPI-C Peripheral In, Controller Out (PICO)	20, 50, 69, 84, 100, 248	A15, B4, C1, D11, M14, P13	6, 73, 93, 134, 148	62, 76, 119	81
SPIC_POCI	I/O	SPI-C Peripheral Out, Controller In (POCI)	21, 51, 70, 101, 245	B5, C2, C14, M13, T13	7, 76, 94, 135	77, 110	76
SPIC_PTE	I/O	SPI-C Peripheral Transmit Enable (PTE)	53, 72, 103, 223, 244	A14, D16, L15, R13, R14	75, 78, 96, 126, 139	65, 79, 105, 114	43, 80
SPID_CLK	I/O	SPI-D Clock	32, 75, 90, 93, 223, 241	C13, D3, E3, G16, N11, R14	66, 78, 117, 142	55, 65, 96	43
SPID_PICO	I/O	SPI-D Peripheral In, Controller Out (PICO)	30, 91, 222, 240	A10, D2, N10, T14	65, 77, 150	64, 120	42, 83
SPID_POCI	I/O	SPI-D Peripheral Out, Controller In (POCI)	31, 44, 92, 127, 220, 247	B10, E2, E16, F13, G14, R11	68, 114, 118, 123, 149	57, 97, 102	39, 64, 70, 82
SPID_PTE	I/O	SPI-D Peripheral Transmit Enable (PTE)	33, 45, 89, 94, 221, 246	D4, E4, F16, G15, P11, P14	67, 116, 121	56, 100	38, 68
SPIE_CLK	I/O	SPI-E Clock	12, 42	A3, C16	130, 174	107, 142	74, 100
SPIE_PICO	I/O	SPI-E Peripheral In, Controller Out (PICO)	8, 38	D6, E14	125, 170	104, 138	72, 96
SPIE_POCI	I/O	SPI-E Peripheral Out, Controller In (POCI)	9, 41	A5, N15	89, 171	73, 139	50, 97
SPIE_PTE	I/O	SPI-E Peripheral Transmit Enable (PTE)	11, 43	A4, C15	131, 173	108, 141	75, 99
SYNCOUT	O	External ePWM Synchronization Pulse	6, 230	B6, J5	24, 166	134	94
TDI	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.	222	T14	77	64	42
TDO	O	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.	223	R14	78	65	43
UARTA_RX	I/O	UART-A Serial Data Receive	3, 28, 39, 43, 73, 85	B11, C7, C15, D9, E13, P15	86, 131, 140, 154, 163	108, 131	75, 91
UARTA_TX	I/O	UART-A Serial Data Transmit	2, 27, 38, 42, 72, 84	A14, B7, C9, C16, D11, E14	125, 130, 139, 148, 155, 162	104, 107, 114, 119, 130	72, 74, 80, 81, 90
UARTB_RX	I/O	UART-B Serial Data Receive	23, 45, 71, 223	B8, B14, G15, R14	78, 116, 136, 159	65, 111, 127	43, 77, 87
UARTB_TX	I/O	UART-B Serial Data Transmit	22, 44, 70, 222	C14, F1, G14, T14	14, 77, 114, 135	11, 64, 110	9, 42, 76
UARTC_RX	I/O	UART-C Serial Data Receive	13, 18, 37, 47	A2, D15, F2, R16	13, 85, 129, 175	10, 143	8
UARTC_TX	I/O	UART-C Serial Data Transmit	10, 17, 36, 46	B2, C5, D14, N14	4, 128, 172	4, 140	4, 98
UARTD_RX	I/O	UART-D Serial Data Receive	9, 49, 53, 77, 87	A5, A13, C10, L15, M15	92, 96, 144, 171	75, 79, 116, 139	97
UARTD_TX	I/O	UART-D Serial Data Transmit	8, 48, 52, 76, 86	B13, C11, D6, L14, N16	90, 95, 143, 170	78, 115, 138	96
UARTE_RX	I/O	UART-E Serial Data Receive	1, 19, 29	A7, A9, B1	5, 151, 161	5, 121, 129	84, 89
UARTE_TX	I/O	UART-E Serial Data Transmit	0, 26	A8, B9	156, 160	124, 128	85, 88
UARTF_RX	I/O	UART-F Serial Data Receive	5, 35, 65, 226	A6, E1, H4, H16	10, 22, 112, 165	16, 93, 133	61, 93
UARTF_TX	I/O	UART-F Serial Data Transmit	4, 34, 64, 225	D1, D7, H15, K5	9, 25, 111, 164	7, 17, 92, 132	12, 60, 92

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEX	176 PTS	144 RFS	100 PZS
X1	I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.	220	E16	123	102	70
X2	I/O	Crystal oscillator output.	221	F16	121	100	68
XCLKOUT	O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.	73, 219	E13, M16	91, 140	74	51

5.3.3 Power and Ground

Table 5-4. Power and Ground

SIGNAL NAME	DESCRIPTION	256 ZEX	176 PTS	144 RFS	100 PZS
VDD	1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.	E8, E9, E12, F6, F12, G6, L11, L12	8, 11, 80, 84, 105, 119, 137, 153, 169	6, 8, 67, 71, 87, 98, 112, 123, 137	5, 6, 45, 49, 55, 66, 78, 95
VDDA	3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin. Connect this pin to 3.3-V supply.	K6, L6	27, 62	19, 54	14, 37
VDDIO	3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin. Connect this pin to 3.3-V supply.	E6, E7, E10, E11, F15, G12, H6, H12, J6, J12, K12, L8, L9, L10, L13, M10, M11	3, 12, 79, 81, 88, 98, 101, 107, 115, 120, 127, 138, 147, 152, 168	3, 9, 66, 68, 72, 81, 83, 95, 99, 106, 113, 118, 122, 136	3, 7, 44, 46, 52, 63, 67, 73, 79
VSS	Digital Ground	A1, A16, F7, F8, F9, F10, F11, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K8, K9, K10, K11, T16	PAD	PAD	PAD
VSSA	Analog Ground	K7, L7, T1	28, 61	20, 53	15, 36
VSSOSC	Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. Connect this pin to board ground.	E15	122	101	69

ADVANCE INFORMATION

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEX	176 PTS	144 RFS	100 PZS
FLT3	I/O	Flash test pin 3. Reserved for TI. Must be left unconnected.	M12			
TCK	I	JTAG test clock with internal pullup.	R15	83	70	48
TMS	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.	T15	82	69	47
VREGENZ	I	Internal voltage regulator enable with internal pullup. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply.				65
XRSn	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup.	F14	124	103	71

ADVANCE INFORMATION

5.4 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 5-6 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 5-6 with pullups and pulldowns are always on and cannot be disabled.

Table 5-6. Pins With Internal Pullup and Pulldown

PIN	RESET (XRSn = 0)	DEVICE BOOT	APPLICATION
GPIOx	Pullup disabled	Pullup disabled(1)	Application defined
GPIO222/TDI	Pullup disabled		Application defined
GPIO223/TDO	Pullup disabled		Application defined
TCK	Pullup active		
TMS	Pullup active		
XRSn	Pullup active		
Other pins (including AIOs)	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.5 Pin Multiplexing

Table 5-7 lists the GPIO muxed pins.

ADVANCE INFORMATION

5.5.1 GPIO Muxed Pins

Table 5-7. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A	EMIF1_A13	EMIF1_D0	MCAND_TX	I2CA_SDA	UARTE_TX	OUTPUTXBAR9	ESC_TX0_DATA0	ESC_GPI0	FSITXA_D0			
GPIO1	EPWM1_B	EMIF1_A14	EMIF1_D3	MCAND_RX	I2CA_SCL	UARTE_RX	OUTPUTXBAR10	ESC_TX1_DATA0	ESC_GPI1	FSITXA_D1			
GPIO2	EPWM2_A	EMIF1_A15	EMIF1_D4	UARTA_TX	I2CB_SDA	MCANF_TX	OUTPUTXBAR1	ESC_RX1_ERR	ESC_GPI2	FSITXA_CLK			
GPIO3	EPWM2_B	EMIF1_A16	EMIF1_D5	UARTA_RX	I2CB_SCL	MCANF_RX	OUTPUTXBAR2		ESC_GPI3	FSIRXA_D0			
GPIO4	EPWM3_A	EMIF1_A17	EMIF1_D9	MCANC_TX		UARTF_TX	OUTPUTXBAR3		ESC_GPI4	FSIRXA_D1		ERRORSTS	
GPIO5	EPWM3_B	EMIF1_A18	EMIF1_D10	MCANC_RX		UARTF_RX	OUTPUTXBAR11	OUTPUTXBAR3	ESC_GPI5	FSIRXA_CLK			
GPIO6	EPWM4_A	EMIF1_DQM0	EMIF1_CLK	MCANB_TX	LINA_TX		OUTPUTXBAR4	SYNCOUT	ESC_GPI6	FSITXB_D0			
GPIO7	EPWM4_B	EMIF1_DQM1	EMIF1_CAS	MCANB_RX	LINA_RX		OUTPUTXBAR5		ESC_GPI7	FSITXB_D1			
GPIO8	EPWM5_A	EMIF1_RAS	EPWM4_B	MCANC_TX	SPIE_PICO	UARTD_TX	OUTPUTXBAR12	ADCSOCAO	ESC_GPO0	FSITXB_CLK	FSITXA_D1	FSIRXA_D0	
GPIO9	EPWM5_B	EMIF1_D11			SPIE_POCI	UARTD_RX	OUTPUTXBAR6	ESC_TX0_CLK	ESC_GPO1	FSIRXB_D0	FSITXA_D0	FSIRXA_CLK	
GPIO10	EPWM8_A	PMBUSA_SCL	ADCSOCBO	MCANC_RX	UARTC_TX	I2CA_SCL	SENT2			ESC_GPI19	ADCA_EXTMUXSEL2	OUTPUTXBAR13	
GPIO11	EPWM6_B	EMIF1_D15	EPWM7_B		SPIE_PTE	SD4_D1	PMBUSA_ALERT	ESC_TX0_DATA1	ESC_GPO3	FSIRXB_CLK	FSIRXA_D1	OUTPUTXBAR7	
GPIO12	EPWM7_A	EMIF1_A1	ADCSOCAO		SPIE_CLK	SD4_C2	PMBUSA_CTL	ESC_TX0_DATA2	ESC_GPO4	FSIRXC_D0	FSIRXA_D0	OUTPUTXBAR14	
GPIO13	EPWM7_B	EMIF1_CS0n	EMIF1_D9		UARTC_RX	SD4_D2	PMBUSA_SDA	ESC_TX0_DATA3	ESC_GPO5	FSIRXC_D1	FSIRXA_CLK	OUTPUTXBAR15	
GPIO14	EPWM6_A	EMIF1_D17	EPWM18_A	EMIF1_D13	LINA_TX	OUTPUTXBAR3	PMBUSA_SCL	ESC_PHY1_LINKSTATUS	ESC_GPO6	FSIRXC_CLK	SD4_C1	OUTPUTXBAR8	
GPIO15	EPWM8_B		PMBUSA_CTL	I2CA_SDA	LINA_RX	OUTPUTXBAR4	SENT1	ESC_GPO7		ESC_GPI20	ADCA_EXTMUXSEL3	OUTPUTXBAR16	
GPIO16	EPWM9_A	EMIF1_D29	EMIF1_BA0	SPIA_PICO		MCAND_TX		ESC_RX1_CLK	SD1_D1	FSIRXD_D1	FSIRXC_CLK	OUTPUTXBAR7	
GPIO17	EPWM9_B	EMIF1_DQM3	EMIF1_BA1	SPIA_POCI		MCAND_RX		ESC_RX1_DV	SD1_C1	FSIRXD_CLK	UARTC_TX	OUTPUTXBAR8	
GPIO18	EPWM15_A		PMBUSA_ALERT	I2CA_SCL	UARTC_RX		SENT4			ESC_GPI21	ADCB_EXTMUXSEL0		
GPIO19	EPWM10_B	EMIF1_CS3n	ADCSOCBO	SPIA_PTE	UARTE_RX	MCANC_TX	PMBUSA_ALERT	ESC_TX1_DATA3	SD1_C2				
GPIO20	EPWM11_A	EMIF1_BA0	EMIF1_DQM2		SPIC_PICO	MCANB_RX		ESC_TX1_DATA2	SD1_D3				
GPIO21	EPWM11_B	EMIF1_BA1			SPIC_POCI	MCANB_TX		ESC_TX1_DATA1	SD1_C3				
GPIO22	EPWM12_A		PMBUSA_SDA	I2CB_SDA	UARTB_TX	MCANC_TX	SENT5	ESC_GPO2		ESC_GPI22	ADCB_EXTMUXSEL1		
GPIO23	EPWM12_B		PMBUSA_SCL	I2CB_SCL	UARTB_RX	MCANC_RX	SENT6	ESC_PHY_RESETn		ESC_GPI23	ADCC_EXTMUXSEL0		
GPIO24	EPWM13_A	EMIF1_DQM0		SPIB_PICO	LINB_TX	MCANE_TX		ESC_RX0_CLK	SD2_D1	ESC_GPI24	EPWM2_A	OUTPUTXBAR1	
GPIO25	EPWM13_B	EMIF1_DQM1		SPIB_POCI	LINB_RX	MCANE_RX	PMBUSA_SDA	ESC_RX0_DV	SD2_C1	FSITXA_D1	EPWM2_B	OUTPUTXBAR2	

ADVANCE INFORMATION

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO26	EPWM14_A	EMIF1_DQM2		SPIB_CLK	UARTE_TX	MCANE_TX	PMBUSA_CTL	ESC_RX0_ERR	SD2_D2	FSITXA_D0	ESC_MDIO_CLK	OUTPUTXBAR3	
GPIO27	EPWM14_B	EMIF1_DQM3		SPIB_PTE	UARTA_TX		EPWM4_A	ESC_RX0_DATA0	SD2_C2	FSITXA_CLK	ESC_MDIO_DATA	OUTPUTXBAR4	
GPIO28	EPWM15_A	EMIF1_CS4n	EMIF1_CS2n		UARTA_RX		EPWM4_B	ESC_RX0_DATA1	SD2_D3			OUTPUTXBAR5	
GPIO29	EPWM15_B	PMBUSA_SDA			UARTE_RX	I2CA_SDA	SENT3	ESC_LATCH0		ESC_I2C_SDA	ADCC_EXTMUXSEL1	OUTPUTXBAR6	
GPIO30	EPWM16_A	EMIF1_CLK	EMIF1_CS4n	MCANC_RX	SPID_PICO	EMIF1_A12		ESC_LATCH1	SD2_D4	ESC_I2C_SCL	ESC_SYNC1	OUTPUTXBAR7	
GPIO31	EPWM16_B	EMIF1_WEn	EMIF1_RNW	MCANC_TX	SPID_POCI	I2CA_SDA		ESC_RX1_DATA0	SD2_C4	FSITXD_D0		OUTPUTXBAR8	
GPIO32		EMIF1_CS0n	EMIF1_OEn	SPIA_PICO	SPID_CLK	I2CA_SDA	OUTPUTXBAR9	ESC_RX0_DATA0					
GPIO33		EMIF1_RNW	EMIF1_BA0	SPIA_POCI	SPID_PTE	I2CA_SCL	OUTPUTXBAR10	ESC_LED_ERR					
GPIO34	EPWM18_A	EMIF1_CS2n	EMIF1_BA1	SPIA_CLK	UARTF_TX	I2CB_SDA	OUTPUTXBAR11	ESC_LATCH0		EPWM3_B	ESC_SYNC0	OUTPUTXBAR1	
GPIO35	EPWM18_B	EMIF1_CS3n	EMIF1_A0	SPIA_PTE	UARTF_RX	I2CB_SCL	OUTPUTXBAR12	ESC_LATCH1			ESC_SYNC1		
GPIO36		EMIF1_WAIT	EMIF1_A1	UARTC_TX	MCANC_RX		OUTPUTXBAR13		SD1_D1		EMIF1_WEn		
GPIO37	EPWM18_A	EMIF1_OEn	EMIF1_A2	UARTC_RX	MCANC_TX		OUTPUTXBAR14	ESC_RX1_DATA1	SD1_D2		EMIF1_D24	OUTPUTXBAR2	
GPIO38	EPWM18_B	EMIF1_A0	EMIF1_A3	UARTA_TX	SPIE_PICO		OUTPUTXBAR15	ESC_RX0_DATA1	SD1_D3	FSITXD_D1	EMIF1_CS2n		
GPIO39		EMIF1_A1	EMIF1_A4	UARTA_RX			OUTPUTXBAR16	ESC_MDIO_DATA	SD1_D4	FSIRXD_CLK		ESC_LED_RUN	
GPIO40	EPWM13_A	EMIF1_A2		MCANB_RX	I2CB_SDA		OUTPUTXBAR9	ESC_GPO2	SD4_C3		EPWM1_A	SD2_C1	
GPIO41	EPWM13_B	EMIF1_A3	EPWM18_A	MCANB_TX	SPIE_POCI	I2CB_SCL	OUTPUTXBAR10	ESC_RX0_DATA2	SD4_D3	FSIRXD_CLK	EPWM1_B	SD2_D1	
GPIO42	EPWM14_A	EMIF1_A2	EMIF1_A13	UARTA_TX	SPIE_CLK	I2CA_SDA	OUTPUTXBAR13	SD4_C3	SD4_C4	FSIRXD_D0	ADCE_EXTMUXSEL2		
GPIO43	EPWM14_B	EMIF1_A4	EMIF1_D13	UARTA_RX	SPIE_PTE	I2CA_SCL	OUTPUTXBAR14		SD4_D4	FSIRXD_D1	ADCE_EXTMUXSEL3		
GPIO44		EMIF1_A4		SPID_POCI	MCANB_RX	UARTB_TX	OUTPUTXBAR14	ESC_TX1_CLK	SD3_C4	FSIRXD_CLK			
GPIO45		EMIF1_A5		SPID_PTE	MCANB_TX	UARTB_RX	OUTPUTXBAR15	ESC_TX1_ENA	SD3_D4	FSIRXD_D0			
GPIO46	EPWM4_A	EMIF1_A6	EPWM14_A	UARTC_TX		MCANE_TX		ESC_MDIO_CLK	SD3_C4				
GPIO47	EPWM4_B	EMIF1_A7	EPWM14_B	UARTC_RX		MCANE_RX		ESC_MDIO_DATA	SD4_C3				
GPIO48		EMIF1_A8		UARTD_TX			OUTPUTXBAR3	ESC_PHY_CLK	SD1_D1	EPWM3_A		SD2_C2	
GPIO49		EMIF1_A9	EMIF1_A5	UARTD_RX			OUTPUTXBAR4	ESC_TX1_DATA2	SD1_C1	FSITXA_D0		SD2_D1	
GPIO50	EPWM15_A	EMIF1_A10	EMIF1_A6		SPIC_PICO	MCANF_TX		ESC_TX1_DATA1	SD1_D2	FSITXA_D1	ESC_GPI25	SD2_D2	
GPIO51	EPWM15_B	EMIF1_A11	EMIF1_A7		SPIC_POCI	MCANF_RX		ESC_TX1_CLK	SD1_C2	FSITXA_CLK	ESC_GPI26	SD2_D3	

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO52	EPWM16_A	EMIF1_A12	EMIF1_A8	UARTD_TX	SPIC_CLK			ESC_TX1_ENA	SD1_D3	FSIRXA_D0		SD2_D4	
GPIO53	EPWM16_B	EMIF1_D31	EMIF1_A9	UARTD_RX	SPIC_PTE			ESC_PHY0_LINKSTATUS	SD1_C3	FSIRXA_D1	ESC_GPI28	SD1_C1	
GPIO54		EMIF1_D30	EMIF1_A10	SPIA_PICO				ESC_PHY_CLK	SD1_D4	FSIRXA_CLK	ESC_GPI29	SD1_C2	
GPIO55	EPWM16_B	EMIF1_D29	EMIF1_D0	SPIA_POCI	EMIF1_WAIT			ESC_PHY0_LINKSTATUS	SD1_C4	FSITXB_D0		SD1_C3	
GPIO56	EPWM17_A	EMIF1_D28	EMIF1_D1	SPIA_CLK	MCAND_TX	I2CA_SDA		ESC_PDI_UC_IRQ	SD2_D1	FSITXB_CLK	ESC_GPI30	SD1_C4	
GPIO57	EPWM17_B	EMIF1_D27	EMIF1_D2	SPIA_PTE	MCAND_RX	I2CA_SCL		ESC_MDIO_DATA	SD2_C1	FSITXB_D1	ESC_GPI31	SD3_D3	
GPIO58	EPWM13_A	EMIF1_D26	EPWM8_A	SPIA_PICO		MCANC_RX	SENT1	ESC_LED_LINK0_ACTIVE	SD2_D2	FSIRXB_D0	ESC_TX0_DATA3	SD2_C2	
GPIO59	EPWM5_A	EMIF1_D25	EPWM8_B	SPIA_POCI		MCANC_TX	SENT2	ESC_LED_LINK1_ACTIVE	SD2_C2	FSIRXB_D1	ESC_TX0_ENA	SD2_C3	
GPIO60	EPWM3_B	EMIF1_D24	EMIF1_D0	SPIA_CLK	OUTPUTXBAR3		SENT3	ESC_LED_ERR	ESC_LATCH0	FSIRXB_CLK		SD2_C4	
GPIO61	EPWM17_B	EMIF1_D23	EMIF1_D6	SPIA_PTE		MCANC_RX	OUTPUTXBAR4	ESC_LED_RUN	SD2_C3	FSITXD_CLK	ESC_LATCH1		
GPIO62	EPWM17_A	EMIF1_D22	EMIF1_D7		MCANC_RX	MCANC_TX	SENT4	ESC_LED_STATE_RUN	SD2_D4	FSITXD_D0	ESC_MDIO_CLK		
GPIO63	EPWM9_A	EMIF1_D21	EMIF1_RNW	SPIB_PICO	MCANC_TX		SENT5	ESC_RX1_DATA0	SD1_D1	FSITXD_D1	ADCD_EXTMUXSEL0	SD2_C4	
GPIO64	EPWM9_B	EMIF1_D20	EMIF1_WAIT	SPIB_POCI	MCANA_TX	UARTF_TX	SENT6	ESC_RX1_DATA1	SD1_C1	FSITXD_CLK	ADCD_EXTMUXSEL1		
GPIO65	EPWM10_A	EMIF1_D19	EMIF1_WEn	SPIB_CLK	MCANA_RX	UARTF_RX		ESC_RX1_DATA2	SD1_D2	FSITXB_CLK	ADCD_EXTMUXSEL2	ESC_GPI13	
GPIO66	EPWM10_B	EMIF1_D18	EMIF1_OEn	SPIB_PTE	I2CB_SDA			ESC_RX1_DATA3	SD1_C2	FSITXB_D1	ADCD_EXTMUXSEL3	ESC_GPI14	
GPIO67	EPWM17_A	EMIF1_D17		LINB_TX	MCAND_TX				SD1_D3	FSITXB_CLK			
GPIO68	EPWM17_B	EMIF1_D16	EMIF1_D4	LINB_RX	MCAND_RX	EMIF1_D13		ESC_PHY1_LINKSTATUS	SD1_C3	FSIRXB_D1		ESC_GPI15	
GPIO69	EPWM11_A	EMIF1_D15		SPIC_PICO	I2CB_SCL			ESC_RX1_CLK	SD1_D4	FSITXB_D0			
GPIO70	EPWM11_B	EMIF1_D14		SPIC_POCI	MCANC_RX	UARTB_TX		ESC_RX1_DV	SD1_C4	FSIRXB_D0		ESC_GPI16	
GPIO71	EPWM12_A	EPWM11_A	EMIF1_D5	SPIC_CLK	MCANC_TX	UARTB_RX	EMIF1_D13	ESC_RX1_ERR	SD3_D1	FSITXC_CLK	FSITXB_D0		
GPIO72	EPWM12_B	EMIF1_D12		SPIC_PTE	MCANB_RX	UARTA_TX	OUTPUTXBAR8	ESC_TX1_DATA3	SD3_D2	FSITXC_D0	SD3_C1		
GPIO73	EPWM5_B	EMIF1_D11	XCLKOUT		MCANB_TX	UARTA_RX	OUTPUTXBAR6	ESC_TX1_DATA2	SD4_D4	FSITXC_CLK	SD2_D2		
GPIO74	EPWM8_A	EMIF1_D10			MCANC_TX			ESC_TX1_DATA1	SD1_D4	FSITXA_D0	SD2_C2		
GPIO75	EPWM8_B	EMIF1_D9		SPID_CLK	MCANC_RX		OUTPUTXBAR16	ESC_TX1_DATA0			SD2_D3		
GPIO76	EPWM9_A	EMIF1_D8		UARTD_TX		MCANE_TX	SD4_D4	ESC_PHY_RESETn	SD3_C1	FSIRXC_D0	SD2_C3	ESC_GPI17	
GPIO77	EPWM9_B	EMIF1_D7		UARTD_RX		MCANE_RX	SD1_D4	ESC_RX0_CLK	SD3_D1	FSITXB_D0	SD2_D4		

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO78	EPWM10_A	EMIF1_D6	EPWM11_A			MCANF_TX	SD4_D4	ESC_RX0_DV	SD3_C2	FSITXC_D1	SD2_C4	ESC_GPI18	
GPIO79	EPWM10_B	EMIF1_D5		ERRORSTS				ESC_RX0_ERR	SD3_D2	FSITXC_D0	SD2_D1		
GPIO80	EPWM11_A	EMIF1_D4		ERRORSTS			SD1_D4	ESC_RX0_DATA0	SD3_C3		SD2_C1		
GPIO81	EPWM11_B	EMIF1_D3						ESC_RX0_DATA1	SD3_D3				
GPIO82	EPWM12_A	EMIF1_D2						ESC_RX0_DATA2	SD3_C2				
GPIO83	EPWM12_B	EMIF1_D1						ESC_RX0_DATA3	SD3_D2				
GPIO84	EPWM12_B	EMIF1_D1	EMIF1_CS4n	SPIC_PICO	UARTA_TX	MCANF_RX		ESC_TX0_ENA	SD3_C2	FSITXC_D1	ESC_RX0_DATA3	ESC_GPO24	
GPIO85	EPWM13_A	EMIF1_D0			UARTA_RX		EMIF1_DQM2	ESC_TX0_CLK	SD3_D3				
GPIO86	EPWM13_B	EMIF1_A13	EMIF1_CAS		UARTD_TX			ESC_PHY0_LINKSTATUS	SD3_C3				
GPIO87	EPWM14_A	EMIF1_A14	EMIF1_RAS		UARTD_RX		EMIF1_DQM3	ESC_TX0_DATA0	SD3_D4				
GPIO88	EPWM14_B	EMIF1_A15	EMIF1_DQM0				EMIF1_DQM1	ESC_TX0_DATA1	SD3_C4				
GPIO89	EPWM15_A	EMIF1_A16	EMIF1_DQM1	SPID_PTE			EMIF1_CAS	ESC_TX0_DATA2	SD1_D3		SD4_D1		
GPIO90	EPWM15_B	EMIF1_A17	EMIF1_DQM2	SPID_CLK			EMIF1_RAS	ESC_TX0_DATA3	SD1_C3		SD4_C1		
GPIO91	EPWM16_A	EMIF1_A18	EMIF1_DQM3	SPID_PICO	I2CA_SDA	MCAND_TX	EMIF1_DQM2		SD4_D2		OUTPUTXBAR9		
GPIO92	EPWM16_B	EMIF1_A19	EMIF1_BA1	SPID_POCI	I2CA_SCL	MCAND_RX	EMIF1_DQM0	FSIRXD_CLK	SD4_C2		OUTPUTXBAR10		
GPIO93	EPWM17_A		EMIF1_BA0	SPID_CLK				ESC_TX1_CLK	SD4_D3		OUTPUTXBAR11		
GPIO94	EPWM17_B			SPID_PTE			EMIF1_BA1	ESC_TX1_ENA	SD4_C3		OUTPUTXBAR12		
GPIO95	EPWM18_A							ESC_GPO10	SD1_D1		OUTPUTXBAR13		
GPIO96	EPWM18_B							ESC_GPO11	SD1_C1		OUTPUTXBAR14		
GPIO97								ESC_GPI17	SD1_D2		OUTPUTXBAR15		
GPIO98								ESC_GPI18	SD1_C2		OUTPUTXBAR16		
GPIO99	EPWM8_A	EMIF1_DQM3	EMIF1_D17					ESC_GPI21	SD4_D4				
GPIO100	EPWM9_A	EMIF1_BA1	EMIF1_D24	SPIC_PICO	SPIA_PICO		SD1_D1	ESC_GPI0	SD4_C4	FSITXA_D0	FSIRXD_D1		
GPIO101	EPWM18_A	EMIF1_A5		SPIC_POCI				ESC_GPI1		FSITXA_D1			
GPIO103	EPWM8_B	EMIF1_BA0	EMIF1_D3	SPIC_PTE				ESC_GPI3	SD4_C4	FSIRXA_D0		ESC_GPO25	
GPIO105	EPWM18_B			I2CA_SCL				ESC_GPI5	SD3_C1	FSIRXA_CLK			

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO127	EPWM18_A	EMIF1_D18	EMIF1_A11	SPID_POCI				ESC_GPI27	SD1_C3	FSIRXC_D1	ESC_SYNC0	ESC_GPO26	
GPIO219	ERRORSTS	EMIF1_A19	EPWM18_B				OUTPUTXBAR1	XCLKOUT	SD2_C1	ESC_GPI8	ESC_TX0_ENA	ESC_GPO27	
GPIO220	EPWM6_A			SPID_POCI	MCANC_TX		OUTPUTXBAR2		SD3_D3	ESC_GPI9		ESC_GPO28	X1
GPIO221	EPWM6_B		EMIF1_CAS	SPID_PTE	MCANC_RX		OUTPUTXBAR3		SD3_C3	ESC_GPI10		ESC_GPO29	X2
GPIO222	TDI	EPWM7_A		SPID_PICO	UARTB_TX	I2CB_SCL	OUTPUTXBAR4	SPIC_CLK	SD3_D4	ESC_GPI11		ESC_GPO30	
GPIO223	TDO	EPWM7_B		SPID_CLK	UARTB_RX	I2CB_SDA	OUTPUTXBAR5	SPIC_PTE	SD3_C4	ESC_GPI12		ESC_GPO31	
GPIO224	EPWM12_A	EPWM12_B		SPIB_POCI	MCAND_RX		OUTPUTXBAR5		SD4_D2		ADCA_EXTMUXSEL0	ESC_GPO8	
GPIO225	EPWM11_B			SPIB_PICO	I2CB_SDA	UARTF_TX	OUTPUTXBAR4		SD4_C1		ADCA_EXTMUXSEL1	ESC_GPO9	
GPIO226	EPWM10_A			SPIA_PTE	MCAND_TX	UARTF_RX	OUTPUTXBAR1	SD1_C3	SD1_D3		ADCA_EXTMUXSEL2	ESC_GPO10	
GPIO227	EPWM14_B			SPIA_CLK			OUTPUTXBAR4		SD2_C2		ADCA_EXTMUXSEL3		
GPIO228	EPWM18_A	EPWM13_A		SPIB_POCI	LINB_TX		OUTPUTXBAR1	SENT4	SD2_D1				
GPIO229	EPWM17_B	EPWM12_B		SPIB_PICO	MCANA_RX			SENT3	SD1_C4				
GPIO230	EPWM11_A		SYNCOUT		I2CB_SCL		OUTPUTXBAR3		SD4_D1		ADCB_EXTMUXSEL0		
GPIO231	EPWM10_B			SPIA_PICO	MCAND_RX		OUTPUTXBAR2		SD1_C3		ADCB_EXTMUXSEL1		
GPIO232	EPWM14_A	EPWM8_B		SPIA_POCI			OUTPUTXBAR3	SENT6	SD3_D1	ESC_PHY0_LINKSTATUS	ADCB_EXTMUXSEL2	ESC_GPO11	
GPIO233	EPWM18_B	EPWM13_B			LINB_RX		OUTPUTXBAR2	SENT5	SD2_C1	ESC_PHY1_LINKSTATUS	ADCB_EXTMUXSEL3	ESC_GPO12	
GPIO234	EPWM17_A	EPWM12_A		SPIB_PTE	MCANA_TX			SENT2	SD1_D4			ESC_GPO13	
GPIO235	EPWM9_B			SPIB_CLK	MCANA_RX			SENT1	SD1_C1			ESC_GPO14	
GPIO236	EPWM12_B	EPWM8_A			LINA_RX		OUTPUTXBAR6		SD4_C2	ESC_I2C_SDA	ADCC_EXTMUXSEL0		
GPIO237	EPWM14_A	EPWM8_B	EPWM17_B		LINA_TX	I2CA_SDA	OUTPUTXBAR7		SD4_D3	ESC_I2C_SCL	ADCC_EXTMUXSEL1		
GPIO238	EPWM15_B						OUTPUTXBAR6	SD1_D3	SD2_C3	ESC_SYNC0	ADCC_EXTMUXSEL2	ESC_GPO15	
GPIO239	EPWM16_B				LINB_TX	I2CA_SCL	OUTPUTXBAR8		SD2_C4	ESC_SYNC1	ADCC_EXTMUXSEL3	ESC_GPO16	
GPIO240	EPWM14_B			SPID_PICO					SD4_C3	ESC_LED_RUN	ADCD_EXTMUXSEL0		
GPIO241	EPWM8_A			SPID_CLK					SD4_D4	ESC_LED_ERR	ADCD_EXTMUXSEL1	ESC_GPO17	
GPIO242					SD1_D4	I2CA_SDA	OUTPUTXBAR9	SENT1	SD2_D2	ESC_LED_STATE_RUN	ADCD_EXTMUXSEL2	ESC_GPO18	
GPIO243	EPWM8_B							SENT2	SD2_D4	ESC_LED_LINK0_ACTIVE	ADCD_EXTMUXSEL3	ESC_GPO19	

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO244				SPIC_PTE				SENT5	SD4_C4	ESC_LED_LINK1_ACTIVE			
GPIO245				SPIC_POCI				SENT6	SD3_C1	ESC_PHY_RESETn			
GPIO246	EPWM16_A			SPID_PTE	MCANC_RX		OUTPUTXBAR7		SD1_D1		ADCE_EXTMUXSEL0	ESC_GPO20	
GPIO247	EPWM15_A	ERRORSTS		SPID_POCI	MCANC_RX	LINA_TX	OUTPUTXBAR5		SD2_D3		ADCE_EXTMUXSEL1	ESC_GPO21	
GPIO248		EMIF1_SDCKE		SPIC_PICO				SENT3	SD1_C2	ESC_LED_RUN	ADCE_EXTMUXSEL2	ESC_GPO22	
GPIO249				SPIC_CLK				SENT4	SD1_D2	ESC_PHY0_LINKSTATUS	ADCE_EXTMUXSEL3	ESC_GPO23	
AIO160									SD3_C2				
AIO161									SD3_D2				
AIO162									SD2_C2				
AIO163									SD2_D2				
AIO164									SD2_C3				
AIO165									SD2_D3				
AIO166									SD4_C1				
AIO167									SD4_D1				
AIO168									SD3_C3				
AIO169									SD3_D3				
AIO170									SD3_C4				
AIO171									SD3_D4				
AIO172									SD1_C1				
AIO173									SD1_D1				
AIO174									SD2_C4				
AIO175									SD2_D4				
AIO176									SD4_C2				
AIO177									SD4_D2				
AIO178									SD4_C3				
AIO179									SD4_D3				
AIO180									SD1_C2				
AIO181									SD1_D2				
AIO182									SD3_C1				
AIO183									SD3_D1				
AIO184									SD3_C2				
AIO185									SD3_D2				
AIO186									SD1_C1				
AIO187									SD1_D1				
AIO188									SD1_C2				
AIO189									SD1_D2				
AIO190									SD1_C3				

ADVANCE INFORMATION

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
AIO191									SD1_D3				
AIO192									SD1_C3				
AIO193									SD1_D3				
AIO194									SD1_C4				
AIO195									SD1_D4				
AIO196									SD4_C4				
AIO197									SD4_D4				
AIO198									SD1_C4				
AIO199									SD1_D4				
AIO200									SD2_C1				
AIO201									SD2_D1				
AIO202									SD2_C1				
AIO203									SD2_D1				
AIO204									SD3_C3				
AIO205									SD3_D3				
AIO206									SD3_C4				
AIO207									SD3_D4				
AIO208									SD2_C2				
AIO209									SD2_D2				
AIO210									SD2_C3				
AIO211									SD2_D3				
AIO212									SD2_C4				
AIO213									SD2_D4				

ADVANCE INFORMATION

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 5-8 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 5-8, any are acceptable. Pins not listed in Table 5-8 must be connected according to the Pin Attributes table.

Table 5-8. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
Analog	
VREFHIx	Tie to VDDA
VREFLOx	Tie to VSSA
ADCINx (except DAC pins)	• No Connect • Tie to VSSA
ADCINx (DAC pins)	• No Connect • Pulldown to VSSA through 5-kΩ resistor
Digital	
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
X1	Tie to VSS
X2	No Connect
TCK	• No Connect • Pullup resistor
TDI	• No Connect • Pullup resistor
TDO	No Connect
TMS	No Connect
ERRORSTS	No Connect
Power and Ground	
VDD	All VDD pins must be connected per the *Pin Attributes* table.
VDDA	If a dedicated analog supply is not used, tie to VDDIO.
VDDIO	All VDDIO pins must be connected per the *Pin Attributes* table.
VSS	All VSS pins must be connected to board ground.
VSSA	If a dedicated analog ground is not used, tie to VSS.
VSSOSC	Connect this pin to the board ground.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD with respect to VSS	–0.3	1.5	V
Supply voltage	VDDIO with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage (7)	V_{IN} (3.3 V)	–0.3	4.6	V
	V_{IN} (5.0 V) (5)	–0.3	6.0	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current - per pin (4) (6)	I_{IK} - V_{IN} < VSS/VSSA - V_{IN} > VDDIO/VDDA)	–20	20	mA
Input clamp current - per pin: GPIO10/15/18/22/23/29	I_{IK} - V_{IN} < VSS	–20		
Input clamp current - total for all inputs (4) (6)	$I_{IKTOTAL}$ - V_{IN} < VSS/VSSA - V_{IN} > VDDIO/VDDA)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Operating junction temperature	T_J	–40	150	°C
Storage temperature(3)	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(4) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.
(5) GPIO10,GPIO15,GPIO18,GPIO22,GPIO23 and GPIO29
(6) Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current to flow to the respective supply rail. If this occurs, the current must be kept within the MIN/MAX listed to prevent permanent damage to the device.
(7) Input clamp current must also be observed.

6.2 F29H85x ESD Ratings – Commercial

				VALUE	UNIT
850TU9, 850DU7, 850DM7 in 256-ball ZEX package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner balls on 256-ball ZEX: A1, A16, T16, T1	±750	
850TU9, 850DU7, 850DM7 in 176-pin PTS package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 176-pin PTS: 1, 44, 45, 88, 89, 132, 133, 176	±750	
850TU9, 850DU7, 850DM7 in 144-pin RFS package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 144-pin RFS: 1, 36, 37, 72, 73, 108, 109, 144	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 F29H85x ESD Ratings – Automotive

				VALUE	UNIT
859TU8, 859TM8, 859DU6, 859DM6 in 256-ball ZEX package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner balls on 256-ball ZEX: A1, A16, T16, T1	±750	
859TU8, 859TM8, 859DU6, 859DM6 in 176-pin PTS package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PTS: 1, 44, 45, 88, 89, 132, 133, 176	±750	
859TU8, 859TM8, 859DU6, 859DM6 in 144-pin RFS package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 144-pin RFS: 1, 36, 37, 72, 73, 108, 109, 144	±750	
859TU8, 859TM8, 859DU6, 859DM6 in 100-pin PZS package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 100-pin PZS: 1, 25, 26, 50, 51, 75, 76, 100	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ADVANCE INFORMATION

6.4 F29P58x ESD Ratings – Commercial

				VALUE	UNIT
580DM5 in 256-ball ZEX package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner balls on 256-ball ZEX: A1, A16, T16, T1	±750	
580DM5 in 176-pin PTS package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 176-pin PTS: 1, 44, 45, 88, 89, 132, 133, 176	±750	
580DM5 in 144-pin RFS package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 144-pin RFS: 1, 36, 37, 72, 73, 108, 109, 144	±750	
580DM5 in 100-pin PZS package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 100-pin PZS: 1, 25, 26, 50, 51, 75, 76, 100	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ADVANCE INFORMATION

6.5 F29P58x ESD Ratings – Automotive

				VALUE	UNIT
589DU5, 589DM5 in 256-ball ZEX package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner balls on 256-ball ZEX: A1, A16, T16, T1	±750	
589DU5, 589DM5 in 176-pin PTS package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PTS: 1, 44, 45, 88, 89, 132, 133, 176	±750	
589DU5, 589DM5 in 144-pin RFS package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 144-pin RFS: 1, 36, 37, 72, 73, 108, 109, 144	±750	
589DU5, 589DM5 in 100-pin PZS package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 100-pin PZS: 1, 25, 26, 50, 51, 75, 76, 100	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ADVANCE INFORMATION

6.6 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, VDDIO and VDDA	Internal BOR enabled(3)	$V_{BOR-VDDIO}$(MAX) + $V_{BOR-VDDIO-GB}$ (2)	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device supply voltage, VDD		1.19	1.25	1.31	V
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS.(4)				
V_{IN}	Digital input voltage (6)	VSS – 0.3		VDDIO + 0.3	V
	Digital input voltage (GPIO10, 15, 18, 22, 23 and 29) (5)	VSS – 0.3		5.5	V
	Analog input voltage (6)	VSSA – 0.3		VDDA + 0.3	V
Junction temperature, T_J	S version(1)	–40		150	°C
Free-Air temperature, T_A	Q version(1) (AEC Q100 qualification)	–40		125	°C

(1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.
(2) See the *Power Management Module (PMM)* section.
(3) Internal BOR is enabled by default.
(4) See the *Power Management Module Operating Conditions* table.
(5) These pins support applied voltage prior to the device being powered.
(6) Applying a VIN greater than VDDIO/VDDA or less than VSS/VSSA voltage will internally rise and could impact other electrical characteristics.

ADVANCE INFORMATION

6.7 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations.

6.7.1 System Current Consumption VREG Enabled

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING MODE						
I_{DDIO}	VDDIO current consumption during operational usage	F29P58xDxx (1)		TBD	674	mA
I_{DDA}	VDDA current consumption during operational usage			TBD	11	mA
IDLE MODE						
I_{DDIO}	VDDIO current consumption while device is in Idle mode	F29P58xDxx • CPU is in IDLE mode • Flash is powered down • XCLKOUT is turned off		TBD	462	mA
I_{DDA}	VDDA current consumption while device is in Idle mode			TBD	11	mA
STANDBY MODE						
I_{DDIO}	VDDIO current consumption while device is in Standby mode	F29P58xDxx • CPU is in STANDBY mode • Flash is powered down • XCLKOUT is turned off		TBD	446	mA
I_{DDA}	VDDA current consumption while device is in Standby mode			TBD	11	mA
FLASH ERASE/PROGRAM						
I_{DDIO}	VDDIO current consumption during Erase/Program cycle(2)	- CPU is running from RAM. - SYSCLK at 120 MHz. - I/Os are inputs with pullups enabled. - Peripheral clocks are turned off.		TBD	TBD	mA
I_{DDA}	VDDA current consumption during Erase/Program cycle			TBD	TBD	mA
RESET MODE						
I_{DDIO}	VDDIO current consumption while reset is active(3)			TBD		mA
I_{DDA}	VDDA current consumption while reset is active(3)			TBD		mA

(1) This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency.
(2) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
(3) This is the current consumption while reset is active, that is XRSn is low.

ADVANCE INFORMATION

6.7.2 System Current Consumption VREG Disable - External Supply

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING MODE						
I_{DD}	CPU1 and CPU2 active in lockstep mode. CPU3 active. VDD current consumption during operational usage.	F29H85xTxx: SYSCLK = 200MHz (1)		TBD	1167	mA
I_{DD}	CPU1 and CPU2 active in non lockstep mode. CPU3 active. VDD current consumption during operational usage.	F29H85xTxx: SYSCLK = 200MHz (1)		TBD	TBD	mA
I_{DD}	CPU1 and CPU3 active. VDD current consumption during operational usage.	F29H85xDxx: SYSCLK = 200MHz (1)		TBD	TBD	mA
I_{DD}	CPU1 and CPU2 active in lockstep mode. VDD current consumption during operational usage.	F29P58xDx5: SYSCLK = 200MHz (1)		TBD	1053	mA
I_{DDIO}	VDDIO current consumption while device is in operating mode	SYSCLK = 200MHz		TBD	66	mA
I_{DDA}	VDDA current consumption while device is in operating mode	SYSCLK = 200MHz		TBD	11	mA
IDLE MODE						
I_{DD}	VDD current consumption while device is in Idle mode	F29H85xTxx • CPU is in IDLE mode • Flash is powered down • XCLKOUT is turned off		TBD	611	mA
I_{DD}	VDD current consumption while device is in Idle mode	F29P58xDxx • CPU is in IDLE mode • Flash is powered down • XCLKOUT is turned off		TBD	463	mA
I_{DDIO}	VDDIO current consumption while device is in Idle mode	• CPU is in IDLE mode • Flash is powered down • XCLKOUT is turned off		TBD	66	mA
I_{DDA}	VDDA current consumption while device is in Idle mode			TBD	11	mA

ADVANCE INFORMATION

6.7.2 System Current Consumption VREG Disable - External Supply (continued)

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDBY MODE						
I_{DD}	VDD current consumption while device is in Standby mode	F29H85xTxx • CPU is in STANDBY mode • Flash is powered down • XCLKOUT is turned off		TBD	577	mA
I_{DD}	VDD current consumption while device is in Standby mode	F29P58xDxx • CPU is in STANDBY mode • Flash is powered down • XCLKOUT is turned off		TBD	447	mA
I_{DDIO}	VDDIO current consumption while device is in Standby mode	• CPU is in STANDBY mode • Flash is powered down • XCLKOUT is turned off		TBD	66	mA
I_{DDA}	VDDA current consumption while device is in Standby mode			TBD	11	mA
FLASH ERASE/PROGRAM						
I_{DD}	VDD Current consumption during Erase/Program cycle(2)	• CPU is running from Flash, performing Erase and Program on the unused sector. • SYSCLK is running at 200 MHz. • I/Os are inputs with pullups enabled. • Peripheral clocks are turned OFF.		500		mA
I_{DDIO}	VDDIO Current consumption during Erase/Program cycle(2)	• CPU is running from Flash, performing Erase and Program on the unused sector. • SYSCLK is running at 200 MHz. • I/Os are inputs with pullups enabled. • Peripheral clocks are turned OFF.		30		mA

(1) Current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency.
(2) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

ADVANCE INFORMATION

6.7.3 Operating Mode Test Description

Section 6.7.1 and Section 6.7.4.1 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- CPU1 and CPU2 are operating at 200 MHz.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.7.4 Reducing Current Consumption

The F29H85x and F29P58x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. The Typical Current Reduction per Disabled Peripheral table lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

6.7.4.1 Typical Current Reduction per Disabled Peripheral

PERIPHERAL	I_{DDIO} CURRENT REDUCTION (mA)
ADC(1)	TBD
CLA	TBD
CLA BGCRC	TBD
CLB	TBD
CMPSS(1)	TBD
CPU BGCRC	TBD
CPU TIMER	TBD
GPDAC	TBD
DCAN	TBD
DCC	TBD
DMA	TBD
eCAP1 and eCAP2	TBD
eCAP3(2)	TBD
ePWM1 to ePWM4(3)	TBD
ePWM5 to ePWM8	TBD
ERAD	TBD
eQEP	TBD
FSI RX	TBD
FSI TX	TBD
HWBIST	TBD
I2C	TBD
LIN	TBD
MCAN (CAN-FD)	TBD
PMBUS	TBD
SCI	TBD
SDFM	TBD
SPI	TBD

(1) This current represents the current drawn by the digital portion of the each module.
(2) eCAP3 can also be configured as HRCAP.
(3) ePWM1 to ePWM4 can also be configured as HRPWM.

ADVANCE INFORMATION

6.8 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	VDDIO * 0.8			V
			I_{OH} = –100 µA	VDDIO – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100 µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
	Low-level output sink current for all output pins - GPIO10/15/18/22/23/29	IO_DRVSEL:DRVSELGPIOx = 0				4	mA
		IO_DRVSEL:DRVSELGPIOx = 1				12	mA
R_{OH}	High-level output impedance for all output pins		VOH=VDDS-0.4V	50	66	96	Ω
R_{OL}	Low-level output impedance for all output pins		VOL=0.4V	48	60	84	Ω
V_{IH}	High-level input voltage			2.0			V
	High-level input voltage - GPIO10/15/18/22/23/29	IO_MODSEL:MODSELGPIOx = 0		0.7*VDDIO			V
		IO_MODSEL:MODSELGPIOx = 1		1.35			V
V_{IL}	Low-level input voltage					0.8	V
	Low-level input voltage - GPIO10/15/18/22/23/29	IO_MODSEL:MODSELGPIOx = 0				0.3*VDDIO	V
		IO_MODSEL:MODSELGPIOx = 1				0.8	V
$V_{HYSTERESIS}$	Input hysteresis (AIO)			125			mV
	Input hysteresis (GPIO)			125			
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDDIO = 3.3 V V_{IN} = VDDIO		120		µA
I_{PULLUP}	Input current	Digital inputs with pullup enabled[1]	VDDIO = 3.3 V V_{IN} = 0 V		160		µA
$R_{PULLDOWN}$	Weak pulldown resistance			22	31	62	kΩ
R_{PULLUP}	Weak pullup resistance			19	29	54	kΩ
		GPIO10/15/18/22/23/29		20	31	65	kΩ
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDDIO			0.1	µA
		Digital inputs (GPIO10/15/18/22/23/29)				20	
		Analog pins	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins[2]					

6.8 Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREG and BOR							
VREG, POR, BOR(3)							

(1) See the *Pins With Internal Pullup and Pulldown* table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see the *Per-Channel Parasitic Capacitance* table that is in the *ADC Input Models* section.
(3) See the *Power Management Module (PMM)* section.

ADVANCE INFORMATION

6.9 Thermal Resistance Characteristics for ZEX Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	4.4
	Junction-to-case thermal resistance, bottom	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	5.7
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	18.6
Psi_{JT}	Junction-to-package top	0.4
Psi_{JB}	Junction-to-board	5.5

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.10 Thermal Resistance Characteristics for PTS Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	4.7
	Junction-to-case thermal resistance, bottom	0.2
$R\Theta_{JB}$	Junction-to-board thermal resistance	6.6
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	17.9
Psi_{JT}	Junction-to-package top	0.1
Psi_{JB}	Junction-to-board	6.3

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.11 Thermal Resistance Characteristics for RFS Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	4.8
	Junction-to-case thermal resistance, bottom	0.2
$R\Theta_{JB}$	Junction-to-board thermal resistance	5.8
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	17.9
Psi_{JT}	Junction-to-package top	0.1
Psi_{JB}	Junction-to-board	5.8

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.12 Thermal Resistance Characteristics for PZS Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	5.0
	Junction-to-case thermal resistance, bottom	0.2
$R\Theta_{JB}$	Junction-to-board thermal resistance	5.0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	18.0
Psi_{JT}	Junction-to-package top	0.1
Psi_{JB}	Junction-to-board	4.8

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.13 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application note *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

ADVANCE INFORMATION

ADVANCE INFORMATION

6.14 System

6.14.1 Power Management Module (PMM)

6.14.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.14.1.2 Overview

The block diagram of the PMM is shown in Figure 6-1. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

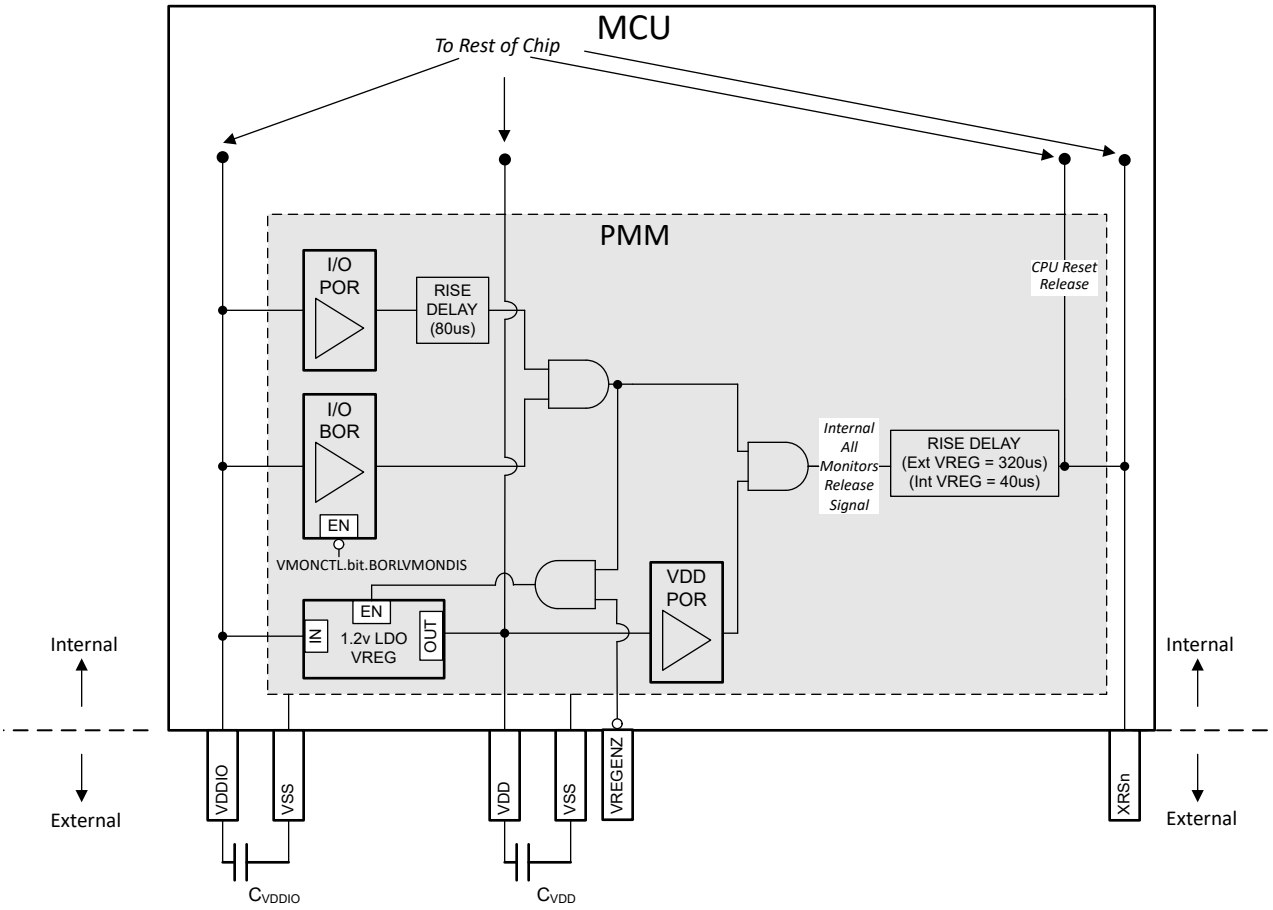


Figure 6-1. PMM Block Diagram

6.14.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.14.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.14.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-2 shows the operating region of the I/O BOR.

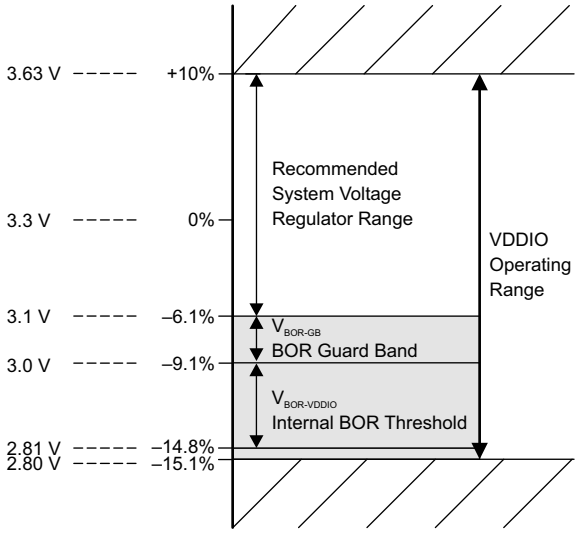


Figure 6-2. I/O BOR Operating Region

6.14.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.14.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

ADVANCE INFORMATION

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.
- VDD supplied from an external supply: The VDD POR is not supported for application use. If VDD monitoring is required by the application, an external supervisor can be used to monitor the VDD rail.

Note

The use of an external supervisor with the internal VREG is not supported.If VDD monitoring is required by the application, a package with a VREGENZ pin must be used to power VDD externally.

6.14.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. This is to ensure that the voltages are stable when XRSn releases. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in Power Management Module Electrical Data and Timing for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.14.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.14.1.2.5 VREGENZ

The VREGENZ (VREG disable) pin controls the state of the internal VREG. To enable the internal VREG, connect the VREGENZ pin to a logic low voltage. For applications supplying VDD externally (external VREG), disable the internal VREG by tying the VREGENZ pin high.

Note

Not all device packages have VREGENZ pinned out. For packages without VREGENZ pinned out, internal VREG mode is not supported.

6.14.1.3 External Components

6.14.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.14.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in Power Management Module Electrical Data and Timing. The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of C_{VDDIO} * VDDIO pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

ADVANCE INFORMATION

6.14.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in Power Management Module Electrical Data and Timing.

In external VREG mode, the actual amount of decoupling capacitance to use is a requirement of the power supply driving VDD.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL equally across the VDD pins. In this configuration, the VDD pins may be separated at the PCB level.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL. In this configuration, all VDD pins must be connected to each other on the PCB.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.14.1.4 Power Sequencing

6.14.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In external VREG mode, the VDD pins should be tied together and supplied from a single source.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.14.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

CAUTION

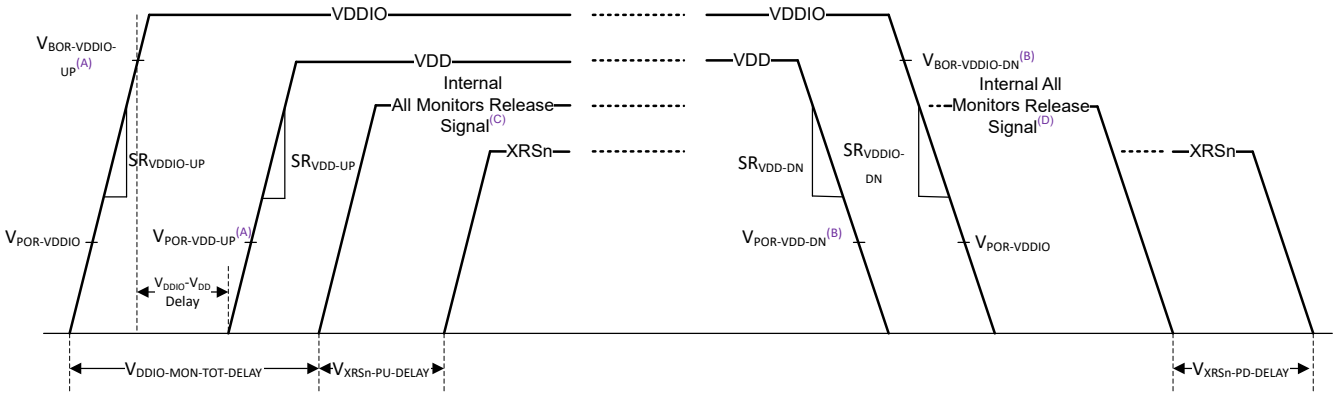
If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

ADVANCE INFORMATION

6.14.1.4.3 Supply Pins Power Sequence

6.14.1.4.3.1 External VREG/VDD Mode Sequence

Figure 6-3 depicts the power sequencing requirements for external VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the *Power Management Module Characteristics* table.
B. This trip point is the trip point after XRSn releases. See the *Power Management Module Characteristics* table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the *PMM Block Diagram*.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the *PMM Block Diagram*.

Figure 6-3. External VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
  2. VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
  3. The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
  4. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PD-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  5. The I/O BOR monitor has different release points during power up and power down.
  6. During power up, both VDDIO and VDD rails have to be up before XRSn releases.
- **For Power Down:**
  1. There is no requirement between VDDIO and VDD on which should power down first; however, there is a minimum slew rate specification.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. Any of the POR or BOR monitors that trips during power down will cause XRSn to go low after $V_{XRSN-PD-DELAY}$.

Note

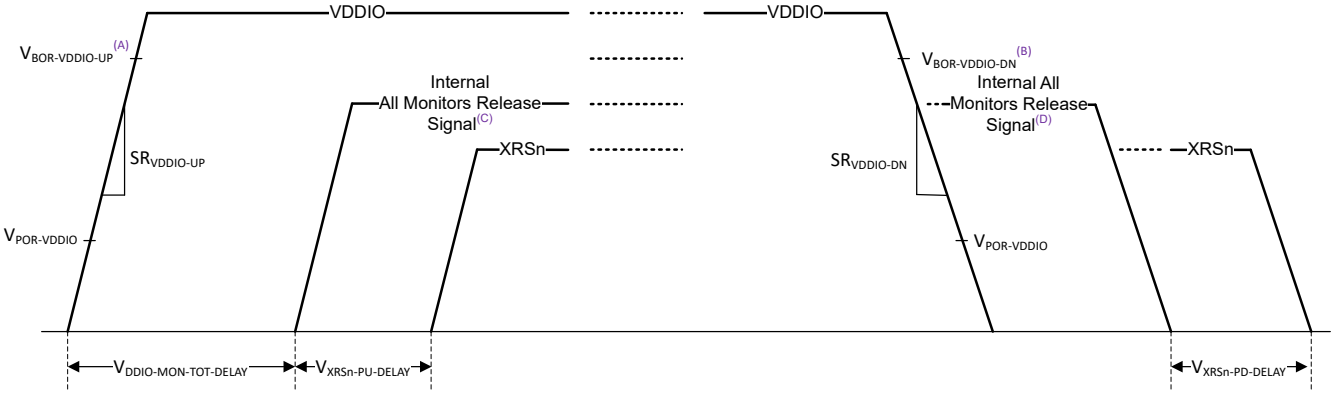
The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.14.1.4.3.2 Internal VREG/VDD Mode Sequence

Figure 6-4 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the *Power Management Module Characteristics* table.
B. This trip point is the trip point after XRSn releases. See the *Power Management Module Characteristics* table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the *PMM Block Diagram*.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the *PMM Block Diagram*.

Figure 6-4. Internal VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
  2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
  3. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PU-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  4. The I/O BOR monitor has different release points during power up and power down.
- **For Power Down:**
  1. The only requirement on VDDIO during power down is the slew rate.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSN-PD-DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.14.1.4.3.3 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION

Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in Supply Pins Power Sequence is recommended.

ADVANCE INFORMATION

Table 6-1. External VREG Sequence Summary

CASE	RAILS POWER-UP ORDER			ACCEPTABLE
	VDDIO	VDDA	VDD	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	No
D	2	3	1	No
E	3	2	1	No
F	3	1	2	No
G	1	1	2	Yes
H	2	2	1	No

Table 6-2. Internal VREG Sequence Summary

CASE	RAILS POWER-UP ORDER		ACCEPTABLE
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	No
C	1	1	Yes

Note

The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.14.1.4.3.4 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note

The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

VDD has a minimum slew rate requirement in external VREG mode. If the minimum slew rate is not met, the VDD POR may release before the VDD operational minimum voltage is met and the device may not start in a properly reset state.

ADVANCE INFORMATION

6.14.1.5 Power Management Module Electrical Data and Timing

6.14.1.5.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
C_{VDDIO} (1) (2)	VDDIO Capacitance Per Pin		0.1			uF
C_{VDDA} (1) (2)	VDDA Capacitance Per Pin		2.2			uF
SR_{VDD33} (3)	Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA). Internal/External VREG		3		100	mV/us
$V_{BOR-VDDIO-GB}$ (5)	VDDIO Brown Out Reset Voltage Guardband			0.1		V
External VREG						
$C_{VDD\ TOTAL}$ (1) (4)	Total VDD Capacitance		10			uF
SR_{VDD12} (3)	Supply Ramp Rate of 1.2V Rail (VDD)		2		100	mV/us
V_{DD33} - V_{DD12} Delay (6)	Ramp Delay Between VDD33 and VDD12		0			us
Internal VREG						
$C_{VDD\ TOTAL}$ (4)	Total VDD Capacitance		10			uF
$I_{VREG-LOAD}$	Voltage Regulator Load Current				500	mA

(1) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
(3) Supply ramp rate faster than the max can trigger the on-chip ESD protection.
(4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
(5) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(6) Delay between when the 3.3-V rail ramps up and when the 1.2-V rail ramps up. See the *External VREG Sequence Summary* table and the *Internal VREG Sequence Summary* table for the allowable supply ramp sequences.

6.14.1.5.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG}	Internal Voltage Regulator Output			1.23		V
$V_{VREG-INRUSH}$ (5)	Internal Voltage Regulator Inrush Current			1150		mA
$V_{POR-VDDIO}$	VDDIO Power on Reset Voltage	Before and After XRSn Release		2.3		V
$V_{BOR-VDDIO-UP}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Up	Before XRSn Release			3.0	V
$V_{BOR-VDDIO-DOWN}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Down	After XRSn Release	2.81		3.0	V
$V_{POR-VDD-UP}$ (2)	VDD Power on Reset Voltage on Ramp Up	Before XRSn Release		1.0		V
$V_{POR-VDD-DOWN}$ (2)	VDD Power on Reset Voltage on Ramp Down	After XRSn Release		1.0		V
$V_{XRSn-PU-DELAY}$ (3)	XRSn Release Delay after Supplies are Ramped Up During Power-Up	Internal VREG		40		us

ADVANCE INFORMATION

6.14.1.5.2 Power Management Module Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{XRSn-PD-DELAY}$ (4)	XRSn Trip Delay after Supplies are Ramped Down During Power-Down	External VREG		320		us
$V_{XRSn-PD-DELAY}$ (4)	XRSn Trip Delay after Supplies are Ramped Down During Power-Down			2		ns
$V_{DDIO-MON-TOT-DELAY}$	Total Delays in Path of VDDIO Monitors (POR, BOR)			80		us
$V_{XRSn-MON--RELEASE-DELAY}$	XRSn Release Delay after a VDD POR Event	Internal VREG, Supplies Within Operating Range		360		us
	XRSn Release Delay after a VDDIO BOR			360		us
	XRSn Release Delay after a VDDIO POR Event			440		us
	XRSn Release Delay after a VDD POR Event	External VREG, Supplies Within Operating Range		360		us
	XRSn Release Delay after a VDDIO BOR			360		us
	XRSn Release Delay after a VDDIO POR Event			440		us

(1) See the *I/O BOR Operating Region* figure.
(2) $V_{POR-VDD}$ is not supported and it is set to trip at a level below the recommended operating conditions. If monitoring of VDD is needed, an external supervisor is required.
(3) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect.
(4) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply.
(5) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

6.14.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-5 shows the recommended reset circuit.

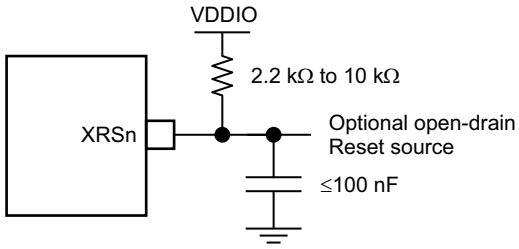


Figure 6-5. Reset Circuit

ADVANCE INFORMATION

6.14.2.1 Reset Sources

The *Reset Signals* table summarizes the various reset signals and their effect on the device.

Table 6-3. Reset Signals

RESET SOURCE	LPOST	HSM RESET	CPU1 SUBSYSTEM RESET	CPU2 SUBSYSTEM RESET	CPU3 SUBSYSTEM RESET	JTAG/ DEBUG LOGIC RESET	IOs	XRSn OUTPUT
PORESETn_RAW	Yes	Yes	Yes	Yes	Yes	Yes	Hi-Z	Yes
PORESETn	-	Yes	Yes	Yes	Yes	Yes	Hi-Z	Yes
XRSn Pin	-	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1.SIMRESET.XRSn	-	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1.WDRSn	-	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
ESM CPU1.NMIWDRSn(1)	-	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1.SYSRSn (Debugger Reset)	-	-	Yes	Yes	Yes	-	Hi-Z	-
CPU2.WDRSn	-	-	-	Yes	-	-	-	-
ESM CPU2.NMIWDRSn(1)	-	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU2.SYSRSn (Debugger Reset)	-	-	-	Yes	-	-	-	-
CPU3.WDRSn	-	-	-	-	Yes	-	-	-
ESM CPU3.NMIWDRSn(1)	-	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU3.SYSRSn (Debugger Reset)	-	-	-	-	Yes	-	-	-
ECAT_RESET_OUT	-	Yes	Yes	Yes	Yes	-	Hi-Z	Yes

(1) Applicable only if ESM CPU instances are programmed in ESMXRSNCTL register to trigger XRSn. For more details, refer to the Error Signaling Module (ESM_C29) chapter in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

See the *Resets* section of the System Control chapter in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

6.14.2.2 Reset Electrical Data and Timing

6.14.2.2.1 Reset XRSn Timing Requirements

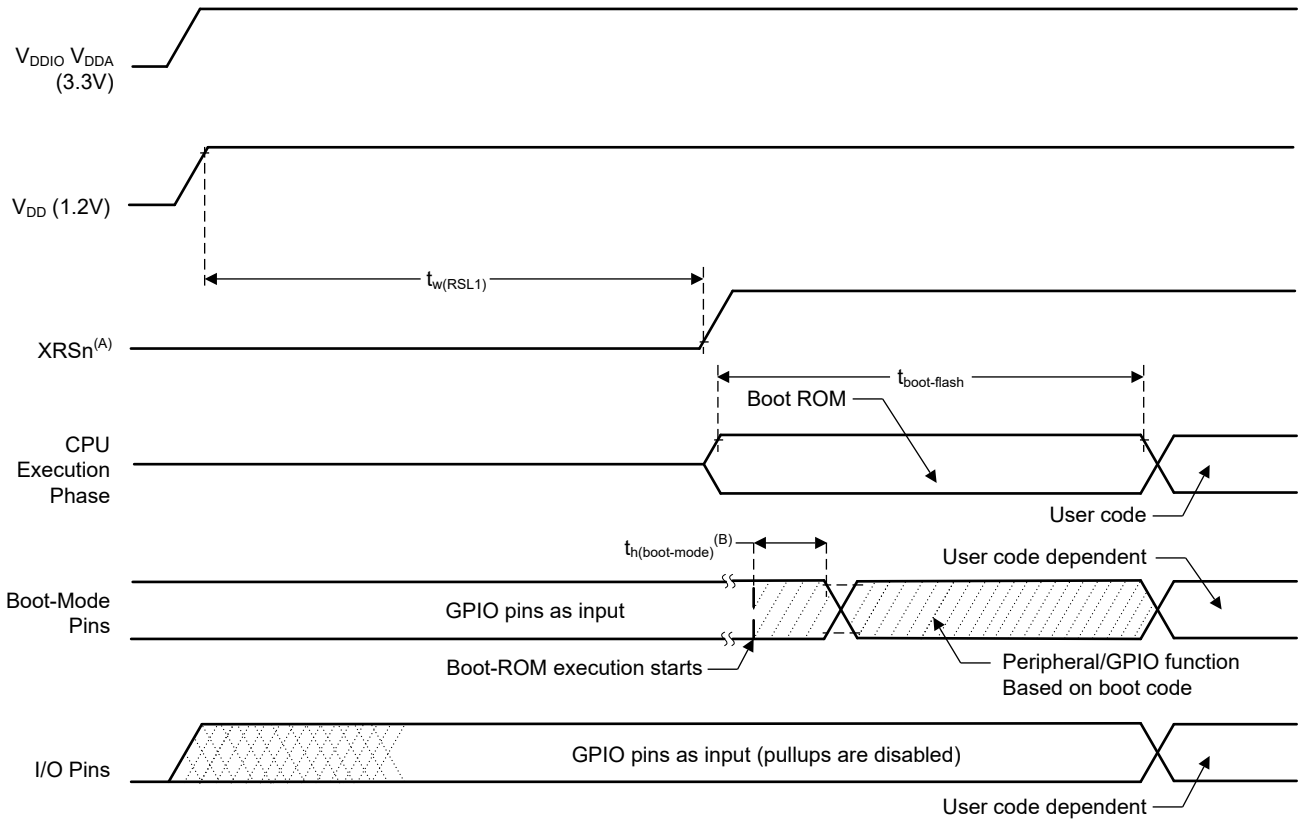
		MIN	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low on warm reset	3.2		µs

6.14.2.2.2 Reset XRSn Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, XRSn driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{boot-flash}$	Boot-ROM execution time to first instruction fetch in flash			80	ms

6.14.2.2.3 Reset Timing Diagrams

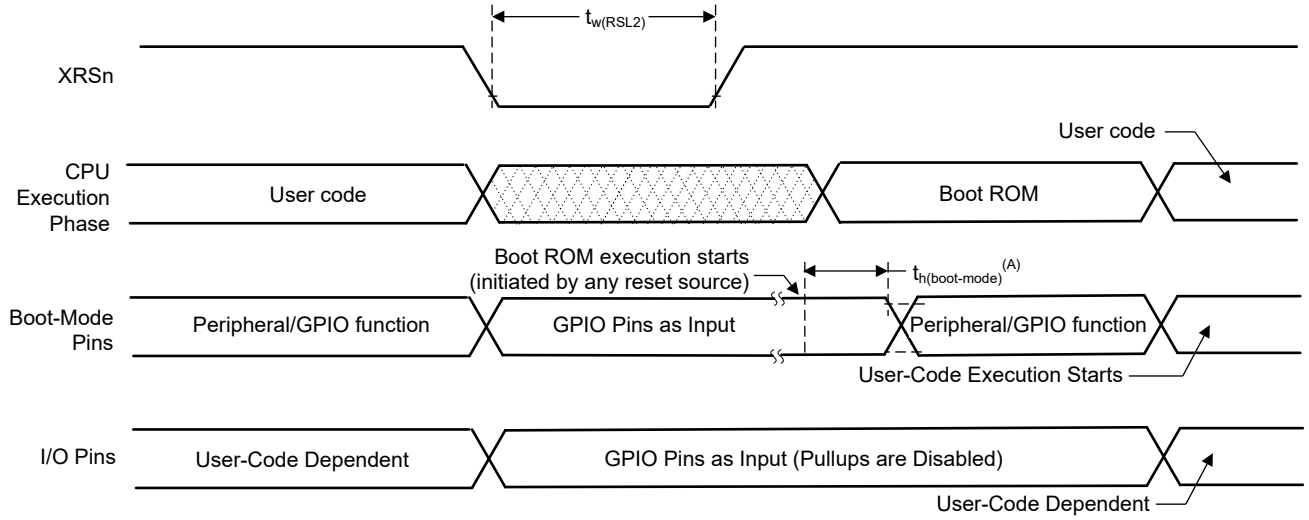


A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the *Pin Attributes* table. On-chip monitors will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see the *Reset Sources* section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-6. Power-on Reset

ADVANCE INFORMATION



A. After reset from any source (see the *Reset Sources* section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-7. Warm Reset

ADVANCE INFORMATION

6.14.3 Clock Specifications

6.14.3.1 Clock Sources

Table 6-4. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1	Can be used to provide clock for: • Watchdog block • Main PLL • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.
AUXCLKIN	Can be used to provide clock for: • MCAN bit clock	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for system PLL (OSCCLK).

ADVANCE INFORMATION

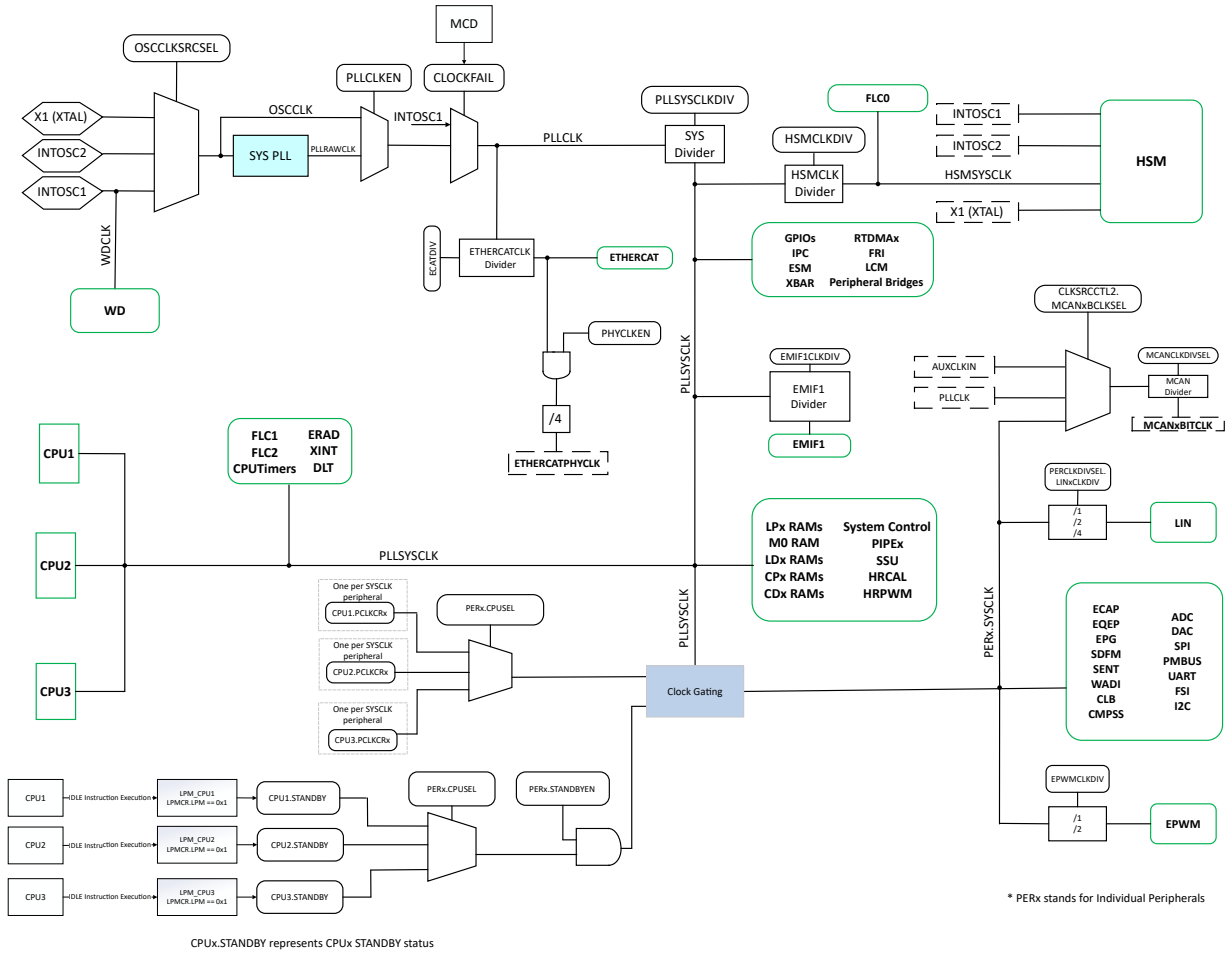


Figure 6-8. Clocking System

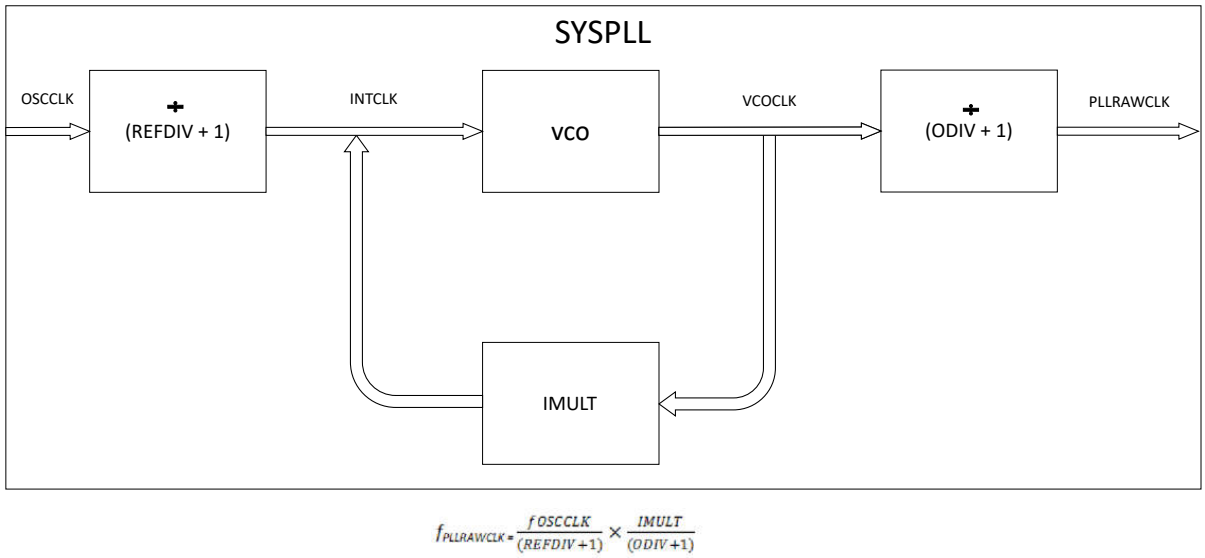


Figure 6-9. SYSPLL

6.14.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.14.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.14.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	10	25	MHz

6.14.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

6.14.3.2.1.3 X1 Input Level Characteristics When Using an External Clock Source Not a Crystal

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3	0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO	VDDIO + 0.3	V

6.14.3.2.1.4 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

6.14.3.2.1.5 AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(AUXI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(AUXI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(AUXL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(AUXH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

6.14.3.2.1.6 APLL Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Clock Out Accuracy			0.2	%
PLL Lock time				
SYS/AUX PLL Lock Time(1)			5µs + (1024 * (REFDIV + 1) * $t_{c(OSCCLK)}$)	us

(1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.14.3.2.1.7 XCLKOUT Switching Characteristics PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2[2]	H + 2[2]	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2[2]	H + 2[2]	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

ADVANCE INFORMATION

6.14.3.3 Input Clocks

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 6-10 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 (also referred to as XTAL) and AUXCLKIN.

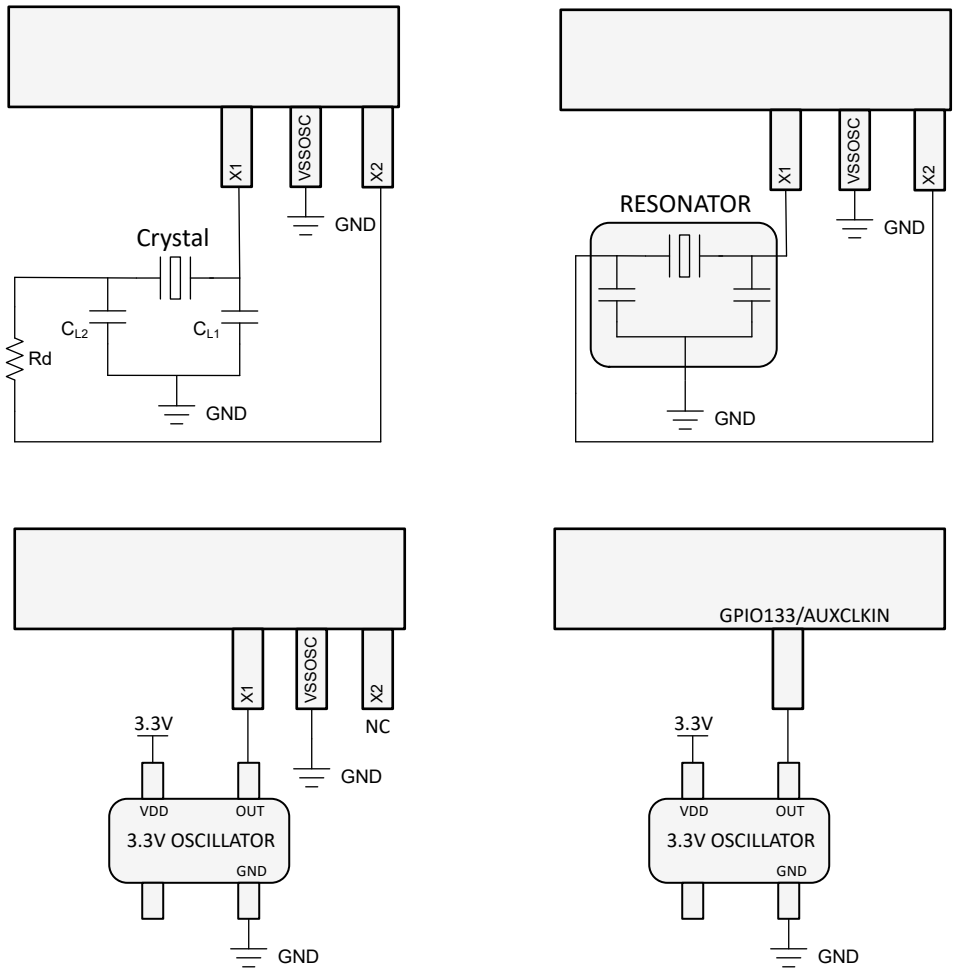


Figure 6-10. Connecting Input Clocks to a F29H85x and F29P58x Device

6.14.3.4 XTAL Oscillator

6.14.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.14.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.14.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 6-11 illustrates the components of the electrical oscillator and the tank circuit.

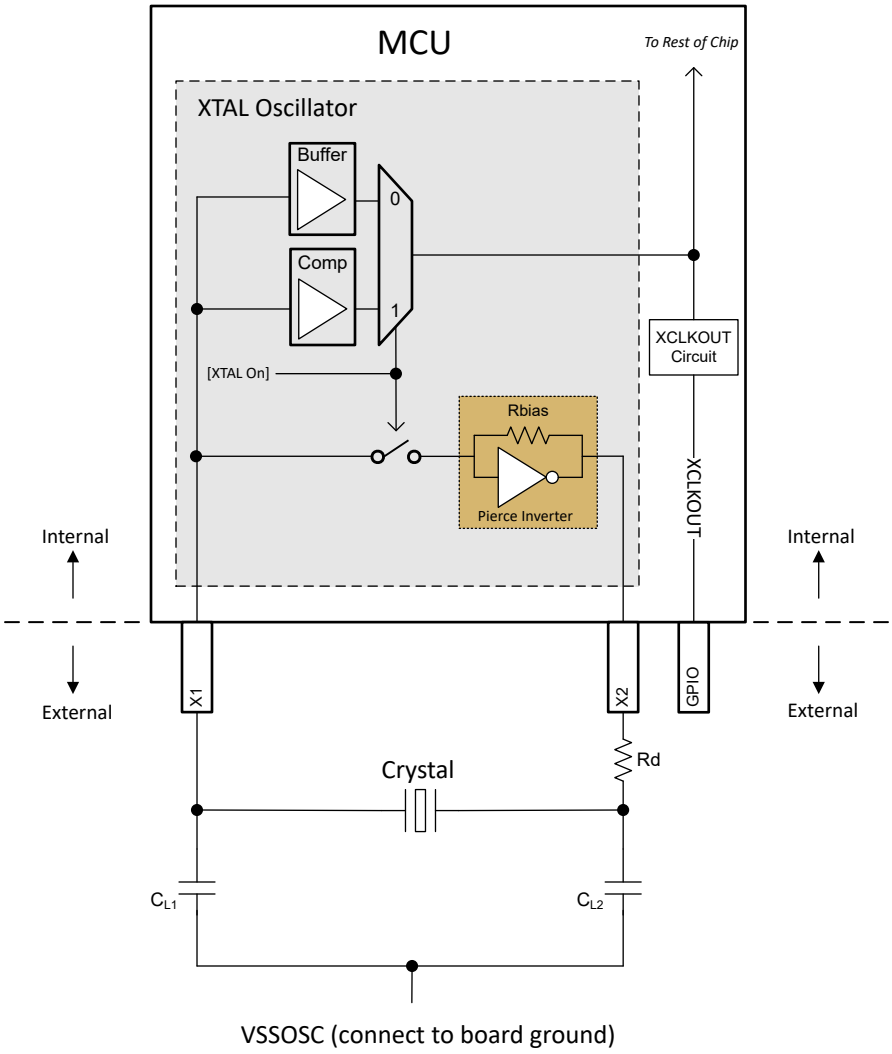


Figure 6-11. Electrical Oscillator Block Diagram

6.14.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.14.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when [XTAL On] = 1, which is achieved by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

6.14.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

ADVANCE INFORMATION

This mode is enabled when [XTAL On] = 0, which can be achieved by setting XTALCR.OSCOFF = 1 and XTALCR.SE = 1.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.14.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the *GPIO Muxed Pins* table for a list of GPIOs that XCLKOUT comes out on.

6.14.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-12 and explained below.

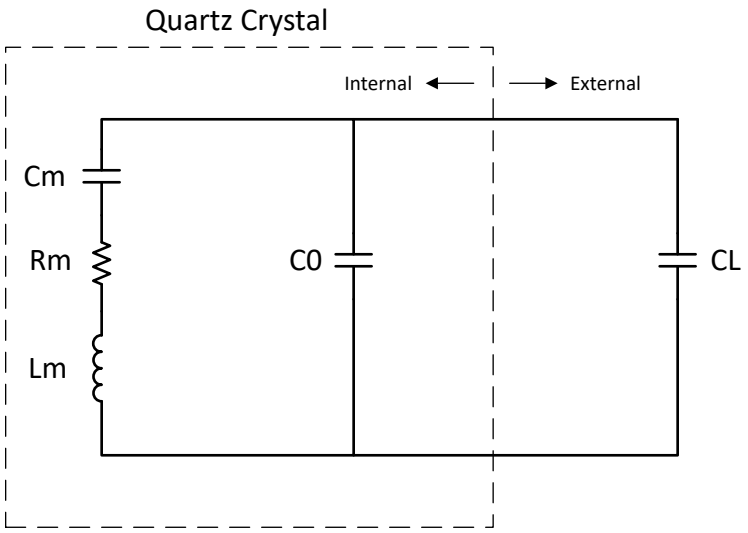


Figure 6-12. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-11, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.14.3.4.2.3 GPIO Modes of Operation

Refer to the *External Oscillator (XTAL)* section of the .

6.14.3.4.3 Functional Operation

6.14.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \quad (1)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.14.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 6-13 and Figure 6-14 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 6-5 for minimum and maximum values for design considerations.

6.14.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the *Rneg – Negative Resistance* section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to the *Crystal Oscillator Specifications* section for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.14.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified

ADVANCE INFORMATION

by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.14.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
   - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
   - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

6.14.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.14.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the *How to Choose a Crystal* section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

6.14.3.4.7 Crystal Oscillator Specifications

6.14.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time[1]	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.14.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 6-5. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

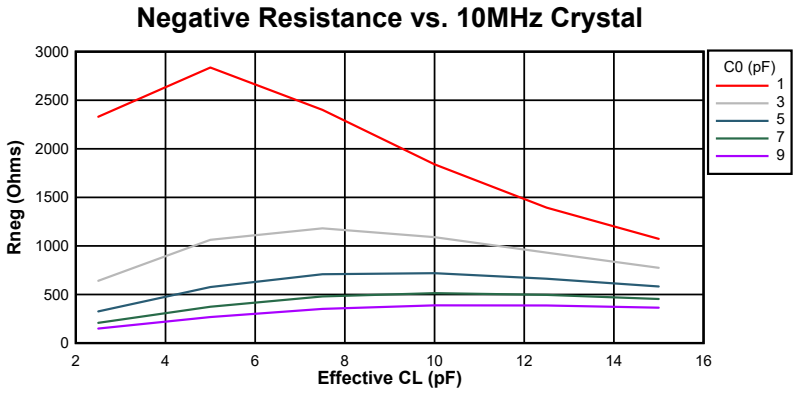


Figure 6-13. Negative Resistance Variation at 10 MHz

ADVANCE INFORMATION

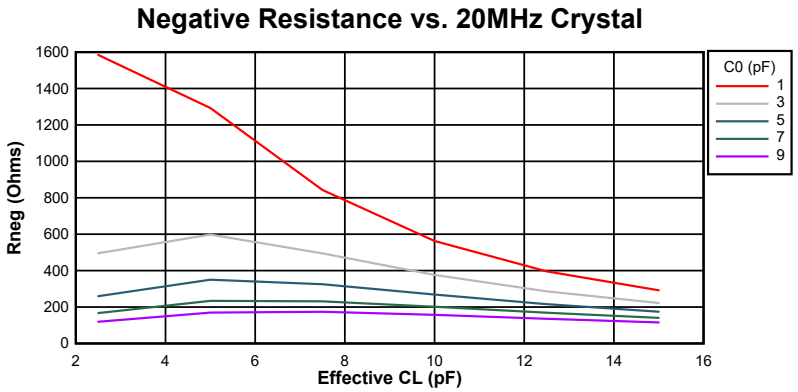


Figure 6-14. Negative Resistance Variation at 20 MHz

6.14.3.4.7.3 Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

6.14.3.4.7.4 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time[1]	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

ADVANCE INFORMATION

6.14.3.5 Internal Oscillators

To reduce production board costs and application development time, all devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

6.14.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		PACKAGE SUFFIX	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{INTOSC}	Frequency, INTOSC1 and INTOSC2(1)	All	-40°C to 125°C	9.7 (–3%)	10	10.3 (3.0%)	MHz
$f_{INTOSC-STABILITY}$	Frequency stability at room temperature	All	30°C, Nominal VDD		±0.1		%
$t_{INT0SC-ST}$	Start-up and settling time	All				20	µs

(1) INTOSC frequency may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.

ADVANCE INFORMATION

6.14.4 Flash Parameters

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 256-bit-wide prefetch reads, a pipeline buffer and code block cache. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM.

This device also has an One-Time-Programmable (OTP) sector used for the dual code security module (DCSM), which cannot be erased after it is programmed.

Table 6-6 lists the minimum required wait states for C29 flash and Table 6-7 for HSM flash at different frequencies. The *Flash Parameters* table lists the flash parameters.

Table 6-6. Minimum Required C29 Flash Wait States with Different Clock Frequencies

CPUCLK (MHz)	Wait States (FRDCNTL[RWAIT](1))
150 < CPUCLK ≤ 200	3
100 < CPUCLK ≤ 150	2
0 < CPUCLK ≤ 100	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

Table 6-7. Minimum Required HSM Flash Wait States with Different Clock Frequencies

HSMCLK (MHz)	Wait States (FRDCNTL[RWAIT])(1)
80 < HSMCLK ≤ 100	2
0 < HSMCLK ≤ 80	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

ADVANCE INFORMATION

6.14.4.1 Flash Parameters

PARAMETER		MIN	TYP	MAX	UNIT
Program Time(1)	128 data bits + 16 ECC bits		TBD	TBD	µs
	2KB (Sector)		TBD	TBD	ms
EraseTime(2) (3) at < 25 cycles	2KB (Sector)		TBD	TBD	ms
	64KB		TBD	TBD	ms
	128KB		TBD	TBD	ms
	256KB		TBD	TBD	ms
	512KB		TBD	TBD	ms
EraseTime(2) (3) at 1000 cycles	2KB (Sector)		TBD	TBD	ms
	64KB		TBD	TBD	ms
	128KB		TBD	TBD	ms
	256KB		TBD	TBD	ms
	512KB		TBD	TBD	ms
EraseTime(2) (3) at 2000 cycles	2KB (Sector)		TBD	TBD	ms
	64KB		TBD	TBD	ms
	128KB		TBD	TBD	ms
	256KB		TBD	TBD	ms
	512KB		TBD	TBD	ms
EraseTime(2) (3) at 20K cycles	2KB (Sector)		TBD	TBD	ms
	64KB		TBD	TBD	ms
	128KB		TBD	TBD	ms
	256KB		TBD	TBD	ms
	512KB		TBD	TBD	ms
N_{wec} Write/Erase Cycles per sector				20000	cycles
N_{wec} Write/Erase Cycles for entire Flash (combined all sectors)				100000	cycles
$t_{retention}$ Data retention duration at T_J = 85°C		20			years
F_{clk}				50	MHz

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

ADVANCE INFORMATION

6.14.5 Memory Subsystem (MEMSS)

6.14.5.1 Introduction

The MEMSS, or Memory Subsystem, covers the memory architecture used on the C29x platform. Each CPU has a 128-bit program bus, two 64-bit read buses, and a 64-bit write bus. RAM test and memory initialization can only be done from CPU1. Disable the dataline buffer using the enable bit in the MEM_DLB_CONFIG register before initializing memory or running the test mode to invalidate the last buffered data.

Table 6-8. Naming Conventions

Name	Read Word Access	Zero Wait State Optimization
LPAx RAM	128-bit word	Program Access for CPU1 and CPU2
LDAx RAM	64-bit word	Data Access for CPU1 and CPU2
CPAx RAM	128-bit word	Program Access for CPU1 and CPU3
CDAx RAM	64-bit word	Data Access for CPU1 and CPU3

6.14.5.2 Features

The MEMSS implements the following features for memory:

- RAM:
  - RTDMA throughput optimization with local lookahead address generation
  - Common dataline buffer for each CPU (2x64-bit words)
  - Common program bridge for each CPU
  - ECC support with 32-bit granularity
  - Read-modify-write for write access smaller than ECC granularity
  - Posted write to minimize stalls on read-modify-write operation
  - Test mode to read/write ECC bits and error injection
- ROM:
  - ECC support with 64-bit granularity to reduce ECC bits overhead
  - One wait state program and data access
  - Prefetch with 256-bit wide memory
  - Dedicated local line buffer of 256 bits
  - ROM patching for boot code
  - Test mode to read ECC bits
- To reduce ECC bit overhead, there are no separate address ECC bits; ECC is generated by combining data and address

6.14.5.3 RAM Specifications

Table 6-9. RAM Parameters

RAM SECTION	MEMORY WORD	INTERLEAVED	CPU1	CPU2	CPU3	HSM	RTDMA1	RTDMA2
LPAx RAM	128	Yes	0WS program 1WS data	0WS program 1WS data	3WS data	N/A	1WS	1WS
LDAx RAM	64	Yes	1WS program 0WS data	1WS program 0WS data	3WS data	2WS	1WS	1WS
M0 RAM	64	Yes	1WS program 0WS data	1WS program 0WS data	3WS data	N/A	1WS	1WS
CPAx RAM	128	Yes	0WS program 1WS data	3WS data	0WS program 1WS data	N/A	1WS	1WS
CDAx RAM	64	Yes	1WS program 0WS data	3WS data	1WS program 0WS data	N/A	1WS	1WS
CPU1 ROM	256	Yes	1WS program 1WS data	N/A	N/A	N/A	N/A	N/A
CPU2 ROM	256	Yes	N/A	1WS program 1WS data	N/A	N/A	N/A	N/A
CPU3 ROM	256	Yes	N/A	N/A	1WS program 1WS data	N/A	N/A	N/A

Table 6-10. RAM Initialization Timings

RAM TYPE	SIZE	MEMORY WIDTH (BITS)	INITIALIZATION TIME (CYCLES)
LDAx RAM	16KB	64 bits	2048
CDAx RAM	16KB	64 bits	2048
LPAx RAM	32KB	128 bits	2048
CPAx RAM	32KB	128 bits	2048

Note

The reason the timings are the same in Table 6-10 is because for 128-bit wide memory 16 bytes are initialized every cycle, whereas for 64-bit wide memory 8 bytes are initialized every cycle.

ADVANCE INFORMATION

6.14.6 Debug/JTAG

External debugger connects to the device via the serial Debug Sub System which supports the two modes below:

1. 4-wire mode: JTAG Protocol
2. 2-wire mode: Serial Wire Debug (SWD) Protocol

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO222 (TDI) and GPIO223 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). Figure 6-15 shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 6-16 shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

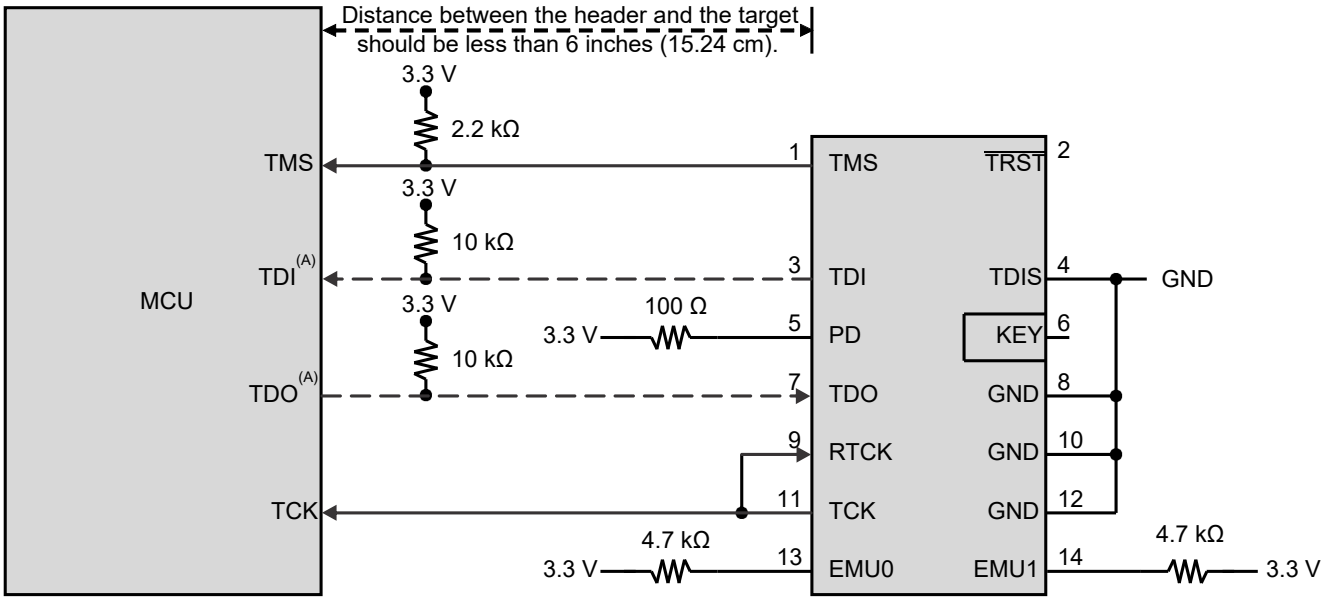
For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints in CCS for C2000 devices.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

Note

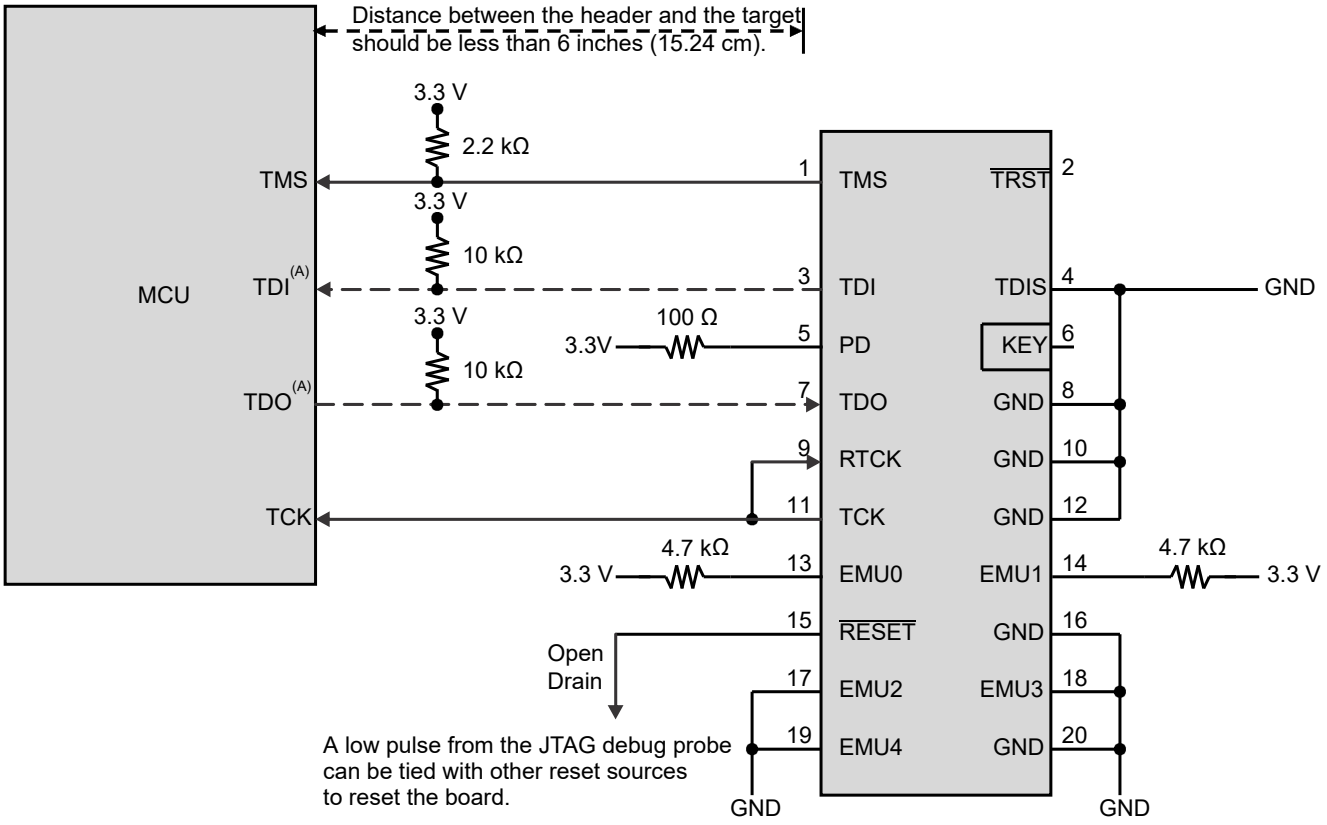
JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the 2-wire option, this pin can be used as GPIO.



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-15. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-16. Connecting to the 20-Pin JTAG Header

ADVANCE INFORMATION

6.14.6.1 JTAG Electrical Data and Timing

6.14.6.1.1 DEBUGSS Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	28.5		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	11		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	11		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	-1.5		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	-1.4		ns
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		ns
5	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	-1.4		ns
5	$t_{su(TMS-TCKL)}$	Input setup time, TMS valid to TCK low	-1.4		ns
6	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		ns
6	$t_{h(TCKL-TMS)}$	Input hold time, TMS valid from TCK low	7		ns

6.14.6.1.2 DEBUGSS Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid		15.7	ns
2	$t_{d(TCKL-TMS)}$	Delay time, TCK low to TMS valid		15	ns
7	$t_{d(TCKL-TMS)}$	Delay time, TCK high to TMS disable		15	ns

6.14.6.1.3 JTAG Timing Diagram

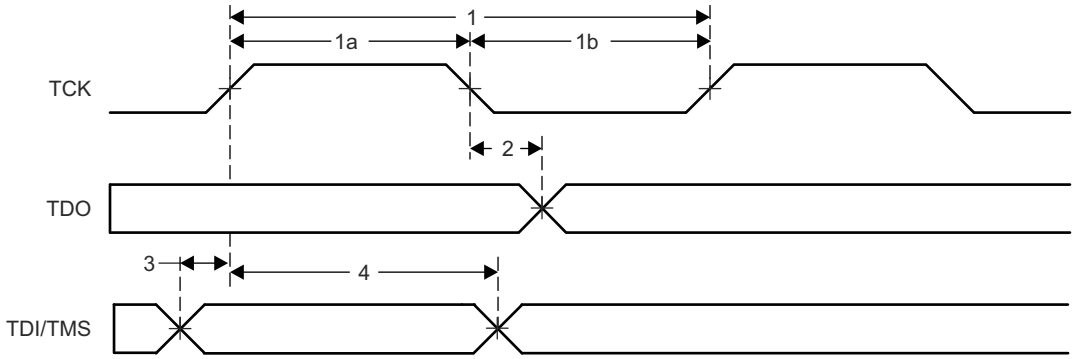


Figure 6-17. JTAG Timing

6.14.6.1.4 SWD Timing Diagram

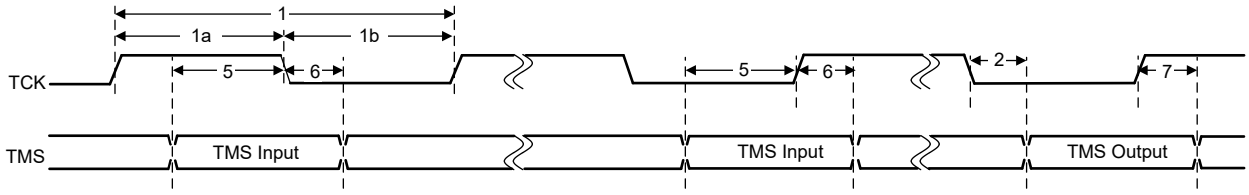


Figure 6-18. SWD Timing

6.14.7 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

Many GPIOs have mux options for Output X-BAR which allows an assortment of internal signals to be routed to a GPIO. All of the GPIOs are connected to each Input X-BAR which can route the GPIO's high or low state to different IP blocks, such as the ADCs, eCAPs, ePWMs, and external interrupts.For more details, see the X-BAR chapter in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

6.14.7.1 GPIO – Output Timing

6.14.7.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8(1)	ns
t_{fGPO}	Toggling frequency, GPIO pins			50	MHz

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

6.14.7.1.2 General-Purpose Output Timing Diagram

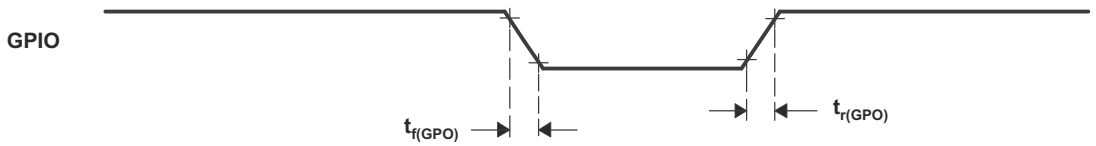


Figure 6-19. General-Purpose Output Timing

ADVANCE INFORMATION

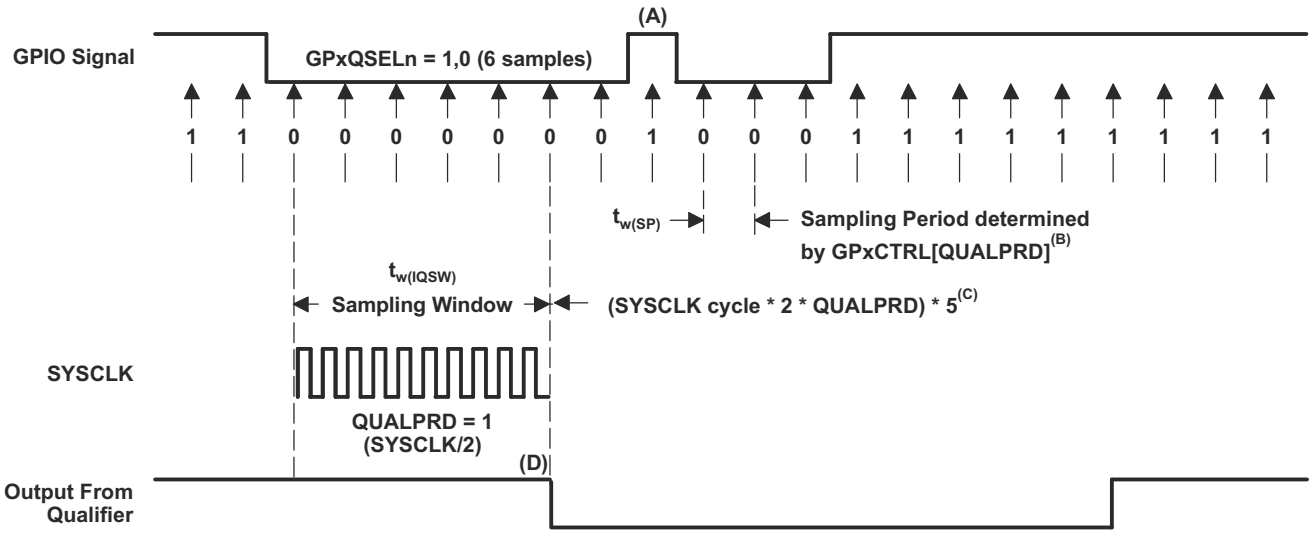
6.14.7.2 GPIO – Input Timing

6.14.7.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.14.7.2.2 Sampling Mode



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-20. Sampling Mode

ADVANCE INFORMATION

6.14.7.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

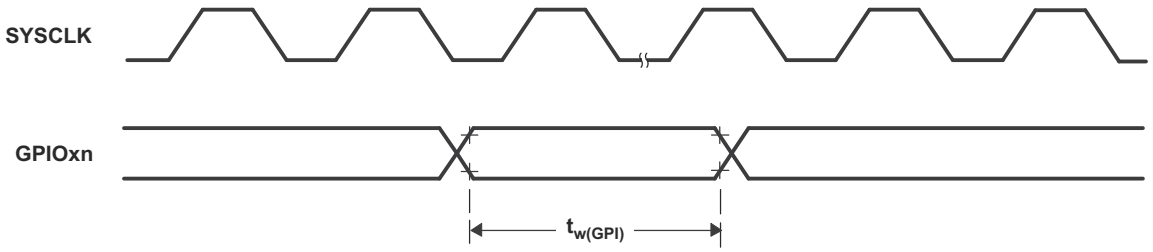


Figure 6-21. General-Purpose Input Timing

6.14.8 Real-Time Direct Memory Access (RTDMA)

6.14.8.1 Introduction

The strength of a controller is not measured purely in processor speed, but in total system capabilities. As a part of the equation, any time the CPU bandwidth for a given function can be reduced, the greater the system capabilities. Many times applications spend a significant amount of their bandwidth moving data, whether moving data from off-chip memory to on-chip memory, from a peripheral such as an analog-to-digital converter (ADC) to RAM, or from one peripheral to another. Furthermore, many times this data comes in a format that is not conducive to the optimal processing powers of the CPU. The RTDMA module described in this chapter has the ability to free up CPU bandwidth and rearrange the data into a pattern for more streamlined processing in real time.

The RTDMA module is an event-based machine, meaning the RTDMA module requires a peripheral, channel, or software trigger to start a RTDMA transfer. The RTDMA module can be made into a periodic time-driven machine by configuring a timer as the RTDMA trigger source as well as utilizing the channels within the module itself to start memory transfers periodically. The RTDMA module has ten independent RTDMA channels that can be configured separately, and each channel contains their own independent Interrupt Controller interrupt to let the CPU know when a RTDMA transfer has either started or completed. All ten channels can be configured at one of four priority levels with one selected channel at a higher priority than the others. At the heart of the RTDMA is a state machine and tightly coupled address control logic. This address control logic allows for rearrangement of the block of data during the transfer as well as the process of ping-ponging data between buffers. Each of these features is discussed in detail in this chapter.

6.14.8.1.1 Features

RTDMA features include:

- 10 RTDMA channels with software configurable priority levels and independent Interrupt Controller interrupts
- Up to 256 hardware trigger sources to initiate RTDMA transfers
- Internal trigger generation for data transfers and trigger sources for channels
- Independent Read and Write buses
- Word Size: 8-bit, 16-bit, 32-bit, and 64-bit transfers
- Throughput: 1 cycle/word after the initial read-write access with 0 cycle read/write stall
- FIFO implemented within hardware to optimize data transfers
- Linear and circular addressing modes
- Support for multiple data transformation functions as data is transferred from source to destination
  - Ability to reverse words, half words, etc.
- Burst Mode Support (for transfers with EMIF)
- Access protection through the Memory Protection Unit (MPU)

6.14.8.1.2 Block Diagram

Figure 6-22 shows the block diagram of the RTDMA.

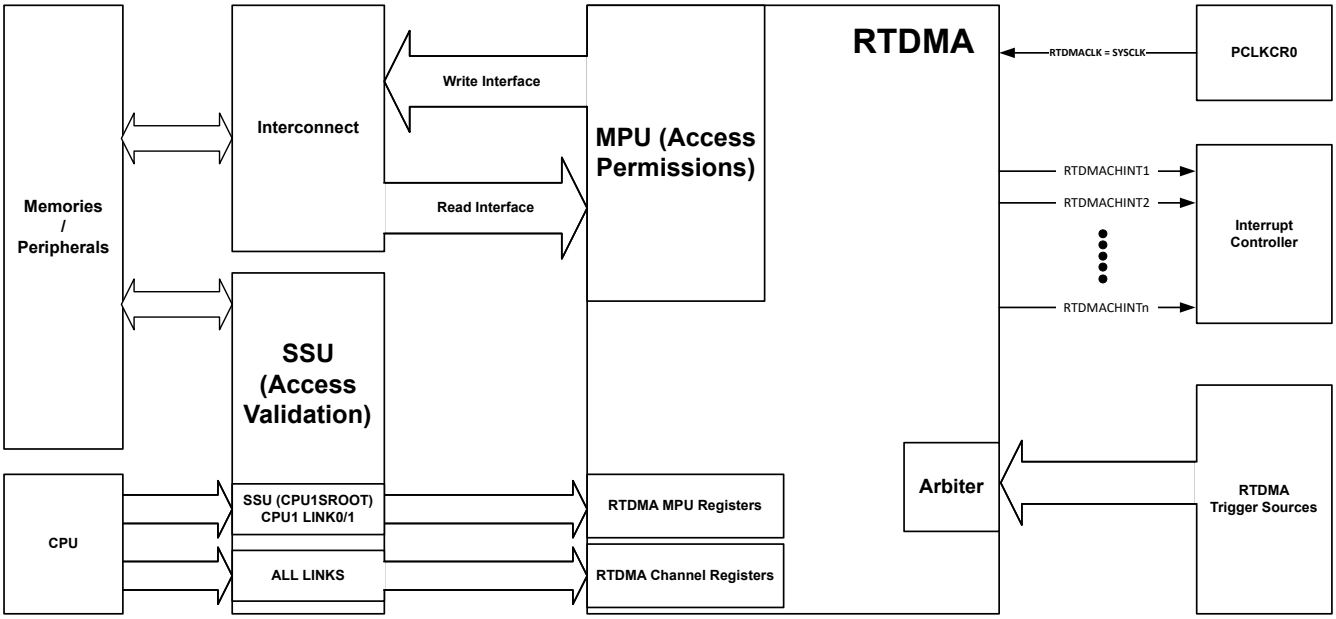


Figure 6-22. RTDMA Block Diagram

ADVANCE INFORMATION

6.14.9 Low-Power Modes

This device has IDLE and STANDBY as clock-gating low-power modes. Wake-up from STANDVY low-power mode can also be triggered by CMPSS trip outputs.

6.14.9.1 Clock-Gating Low-Power Modes

Table 6-11. Clock-Gating Low-Power Modes

MODULES/CLOCK DOMAIN	CPU1		CPU2		CPU3	
	IDLE	STANDBY	IDLE	STANDBY	IDLE	STANDBY
CPU1.CLOCK	Active	Gated	N/A	N/A	N/A	N/A
CPU2.CLOCK	N/A	N/A	Active	Gated	N/A	N/A
CPU3.CLOCK	N/A	N/A	N/A	N/A	Active	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Controlled by PERxSYSCONFIG	Active	Controlled by PERxSYSCONFIG	Active	Controlled by PERxSYSCONFIG
WD1CLK	Active	Active	Active	Active	Active	Active
WD2CLK	Active	Active	Active	Active	Active	Active
WD3CLK	Active	Active	Active	Active	Active	Active
HSM.SYSCLK	Active	Active	Active	Active	Active	Active
M0 RAM Clock	Active	Active	Active	Active	Active	Active
Ecat_PHYCLK, Ecat_CLK25, Ecat_CLK100, MCANxBITCLK	Active	Active	Active	Active	Active	Active

ADVANCE INFORMATION

6.14.9.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.14.9.2.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

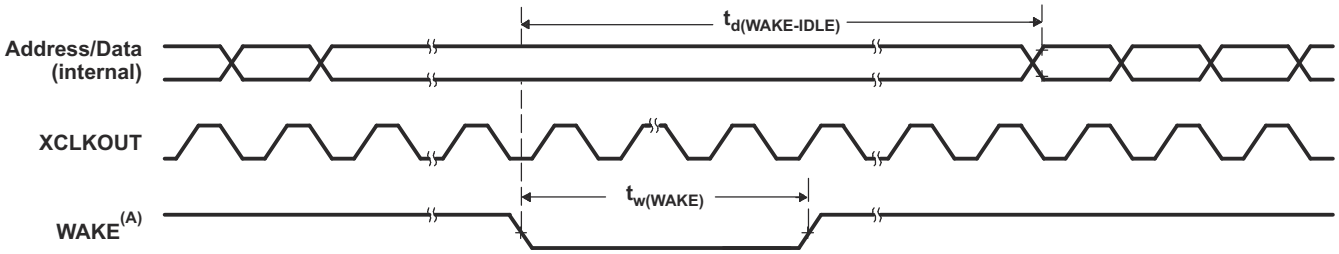
6.14.9.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume(1)	From Flash (active state)	Without input qualifier		$40t_{c(SYSCLK)}$	cycles
			With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles
		From Flash (sleep state)	Without input qualifier		$6700t_{c(SYSCLK)}$ (2)	cycles
			With input qualifier		$6700t_{c(SYSCLK)}$ (2) + $t_{w(WAKE)}$	cycles
		From RAM	Without input qualifier		$25t_{c(SYSCLK)}$	cycles
			With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.14.9.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-23. IDLE Entry and Exit Timing Diagram

ADVANCE INFORMATION

6.14.9.2.4 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | (2 + QUALSTDBY)$t_{c(OSCCLK)}$ (1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

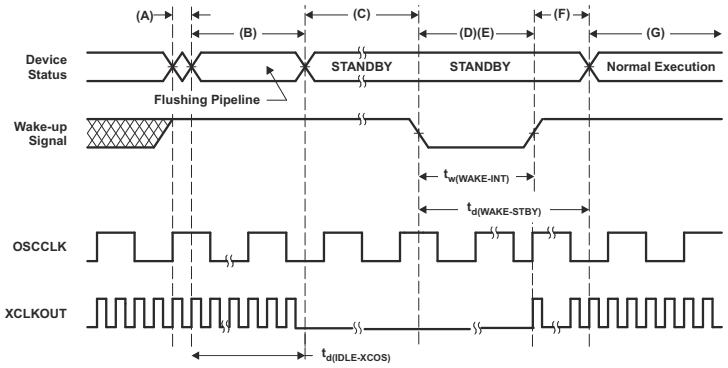
6.14.9.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)	Wakeup from flash (Flash module in active state)		$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from flash (Flash module in sleep state)		$6700t_{c(SYSCLK)}$ (2) $+ t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from RAM		$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.14.9.2.6 STANDBY Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-24. STANDBY Entry and Exit Timing Diagram

6.14.10 External Memory Interface (EMIF)

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

6.14.10.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects ($\overline{\text{EMIF\_CS[4:2]}}$). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable time-out
- Select strobe option

6.14.10.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select ($\overline{\text{EMIF\_CS[0]}}$).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in C2000Ware for C2000 MCUs and the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* .

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with 8-, 9-, 10-, and 11-column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. The EMIF module does not support mobile SDRAM devices.

On this device, the EMIF does not support burst access for SDRAM configurations. This means every access to an external SDRAM device will have CAS latency.

6.14.10.3 EMIF Electrical Data and Timing

6.14.10.3.1 EMIF Synchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EMIFDV-EM\_CLKH)}$	Input setup time, read data valid on EMxD[y:0] before EMxCLK rising	2		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMxD[y:0] after EMxCLK rising	1.5		ns

6.14.10.3.2 EMIF Synchronous Memory Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK	10		ns
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK (With 210MHz Timing Closure)	9.52		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMxCLK high or low	3		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ valid		8	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ invalid	1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMxCLK rising to EMxDQM[y:0] valid		8	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMxCLK rising to EMxDQM[y:0] invalid	1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid		8	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid	1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMxCLK rising to EMxD[y:0] valid		8	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMxCLK rising to EMxD[y:0] invalid	1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMxCLK rising to EMxRAS valid		8	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMxCLK rising to EMxRAS invalid	1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMxCLK rising to EMxCAS valid		8	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMxCLK rising to EMxCAS invalid	1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxWE}}$ valid		8	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxWE}}$ invalid	1		ns
17	$t_{d(CLKH-DHZ)}$	Delay time, EMxCLK rising to EMxD[y:0] tri-stated		8	ns
18	$t_{oh(CLKH-DLZ)}$	Output hold time, EMxCLK rising to EMxD[y:0] driving	1		ns

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6.14.10.3.3 EMIF Synchronous Memory Timing Diagrams

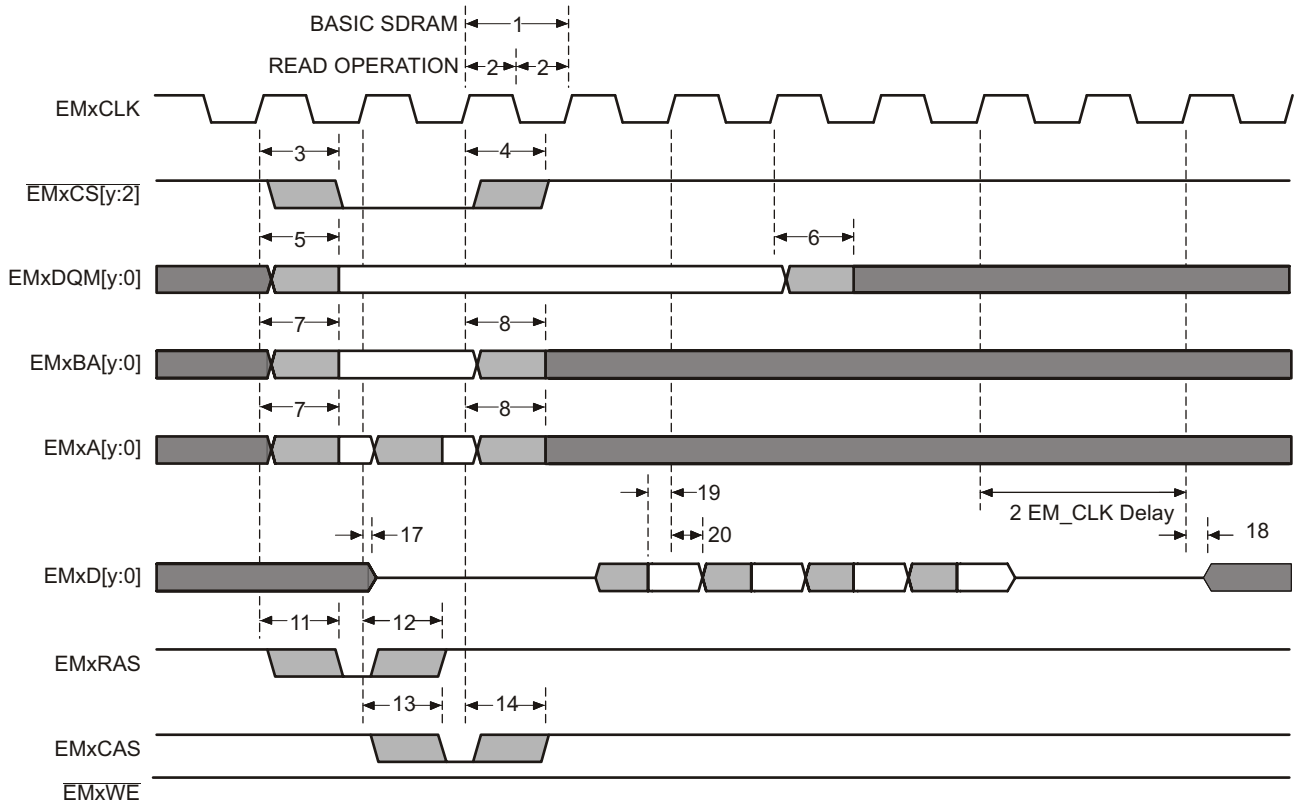

Figure 6-25. Basic SDRAM Read Operation

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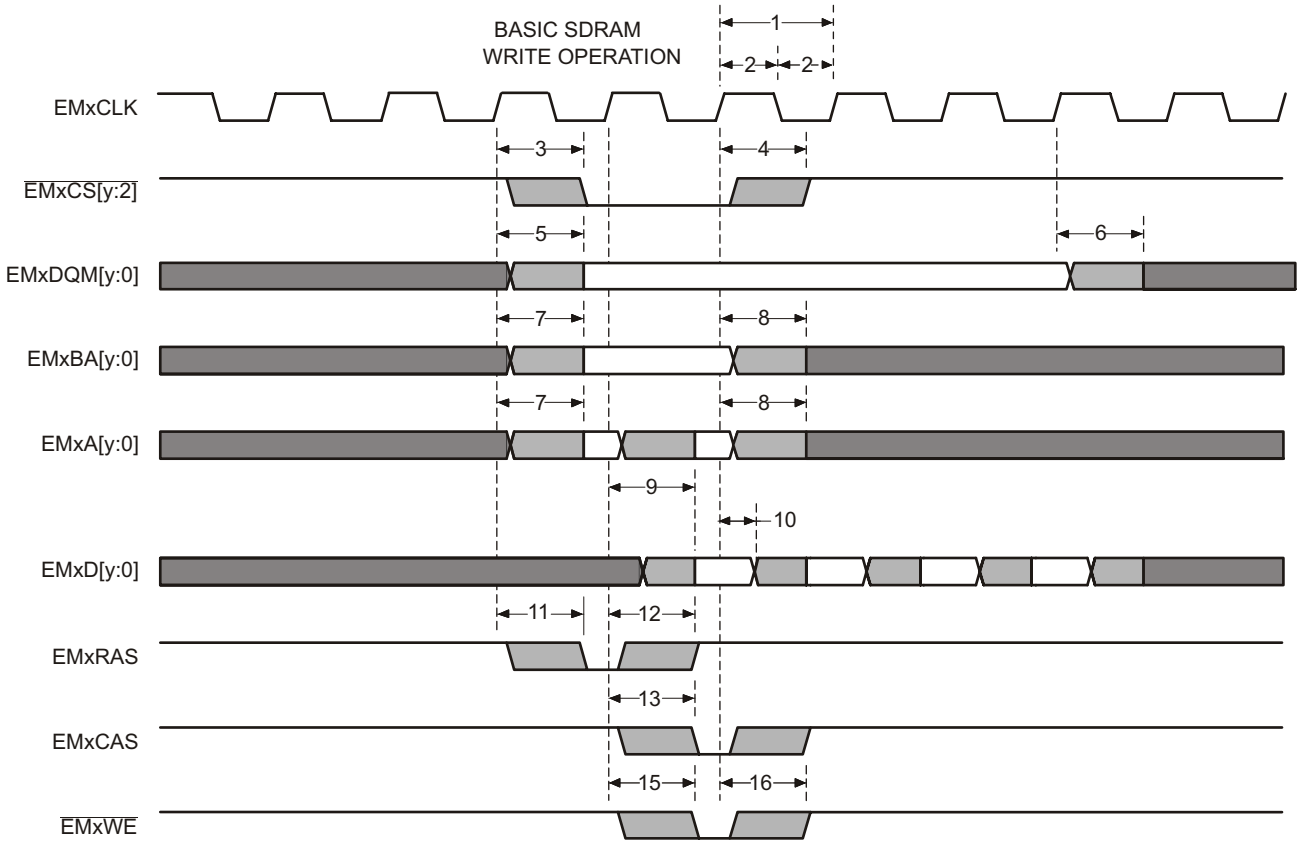

Figure 6-26. Basic SDRAM Write Operation

6.14.10.3.4 EMIF Asynchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
Reads and Writes					
	E	EMIF clock period	$t_{c(SYSCLK)}$		ns
2	$t_{w(EM\_WAIT)}$	Pulse duration, EMxWAIT assertion and deassertion	2E(1)		ns
Reads					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMxD[y:0] valid before $\overline{EMxOE}$ high	15		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMxD[y:0] valid after $\overline{EMxOE}$ high	0		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20(1)		ns
Writes					
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20(1)		ns

(1) E = EMxCLK period in ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. The *EMxWAIT Read Timing Requirements* figure and the *EMxWAIT Write Timing Requirements* figure describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

6.14.10.3.5 EMIF Asynchronous Memory Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER(1) (2) (3)		MIN	MAX	UNIT
1	$t_{d(TURNAROUND)}$	Turn around time TA=0	(TA)*E–3	(TA)*E+2	ns
Reads					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E–3	(RS+RST+RH)*E+2	ns
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 1)	(RS+RST+RH+ (EWC*16))*E–3	(RS+RST+RH+ (EWC*16))*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxOE}$ low (SS = 0) RS=0	(RS)*E–3	(RS)*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxOE}$ low (SS = 1)	–3	2	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS}$[y:2] high (SS = 0)	(RH)*E–3	(RH)*E	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS}$[y:2] high (SS = 1)	–3	0	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxBA[y:0] invalid	(RH)*E–3	(RH)*E	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxA[y:0] invalid	(RH)*E–3	(RH)*E	ns
10	$t_{w(EMOEL)}$	$\overline{EMxOE}$ active low width (EW = 0)	(RST)*E–1	(RST)*E+1	ns
10	$t_{w(EMOEL)}$	$\overline{EMxOE}$ active low width (EW = 1)	(RST+(EWC*16))*E–1	(RST+(EWC*16))*E+1	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxOE}$ high	4*E+10	5*E+15	ns
29	$t_{su(EMDQMV-EMOEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
30	$t_{h(EMOEH-EMDQMIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxDQM[y:0] invalid	(RH)*E–3	(RH)*E	ns

ADVANCE INFORMATION

6.14.10.3.5 EMIF Asynchronous Memory Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1] [2] [3]		MIN	MAX	UNIT
Writes					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E–3	(WS+WST+WH)*E+2	ns
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 1)	(WS+WST+WH+ (EWC*16))*E–3	(WS+WST+WH+ (EWC*16))*E+2	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxWE}$ low (SS = 0)	(WS)*E–3	(WS)*E+2	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxWE}$ low (SS = 1)	–3	2	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS}$[y:2] high (SS = 0)	(WH)*E–3	(WH)*E	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS}$[y:2] high (SS = 1)	–3	0	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+2	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxDQM[y:0] invalid	(WH)*E–3	(WH)*E	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+2	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxBA[y:0] invalid	(WH)*E–3	(WH)*E	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+2	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxA[y:0] invalid	(WH)*E–3	(WH)*E	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 0)	(WST)*E–1	(WST)*E+1	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 1)	(WST+(EWC*16))*E–1	(WST+(EWC*16))*E+1	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxWE}$ high	4*E+10	5*E+15	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMxD[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+2	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxD[y:0] invalid	(WH)*E–3	(WH)*E	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–4], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for more information.

(2) E = EMxCLK period in ns.

(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256–1]. The maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for more information.

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6.14.10.3.6 EMIF Asynchronous Memory Timing Diagrams

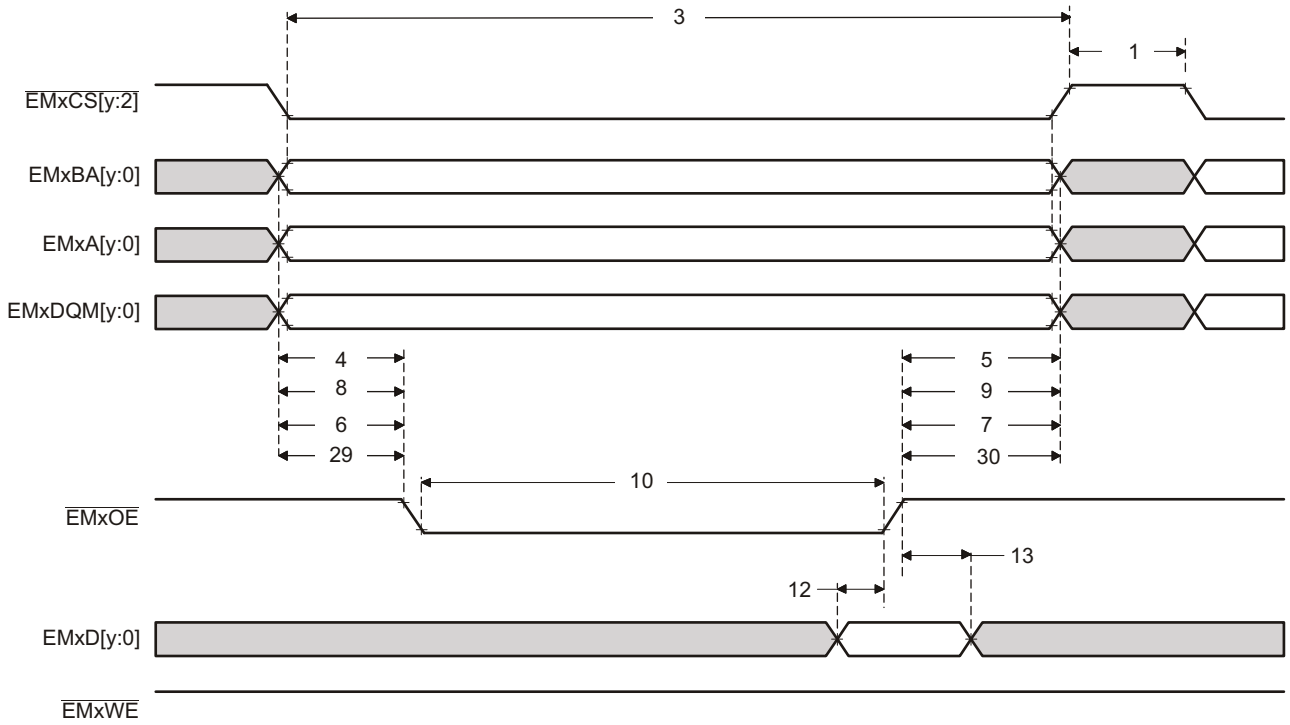

Figure 6-27. Asynchronous Memory Read Timing

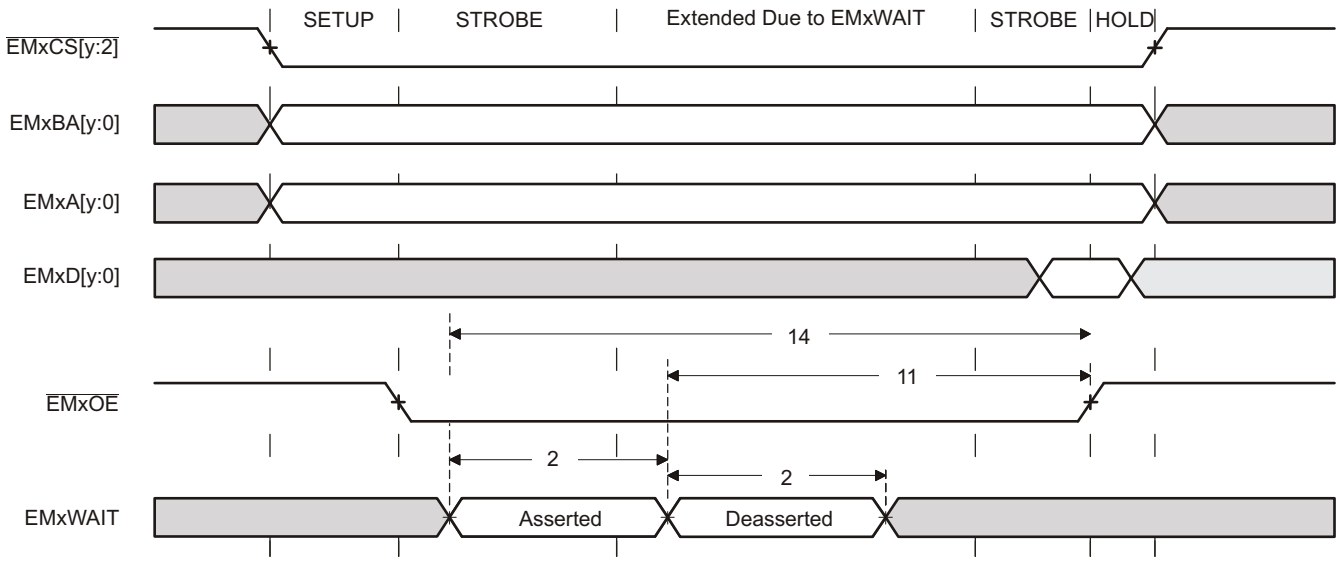

Figure 6-28. EMxWAIT Read Timing Requirements

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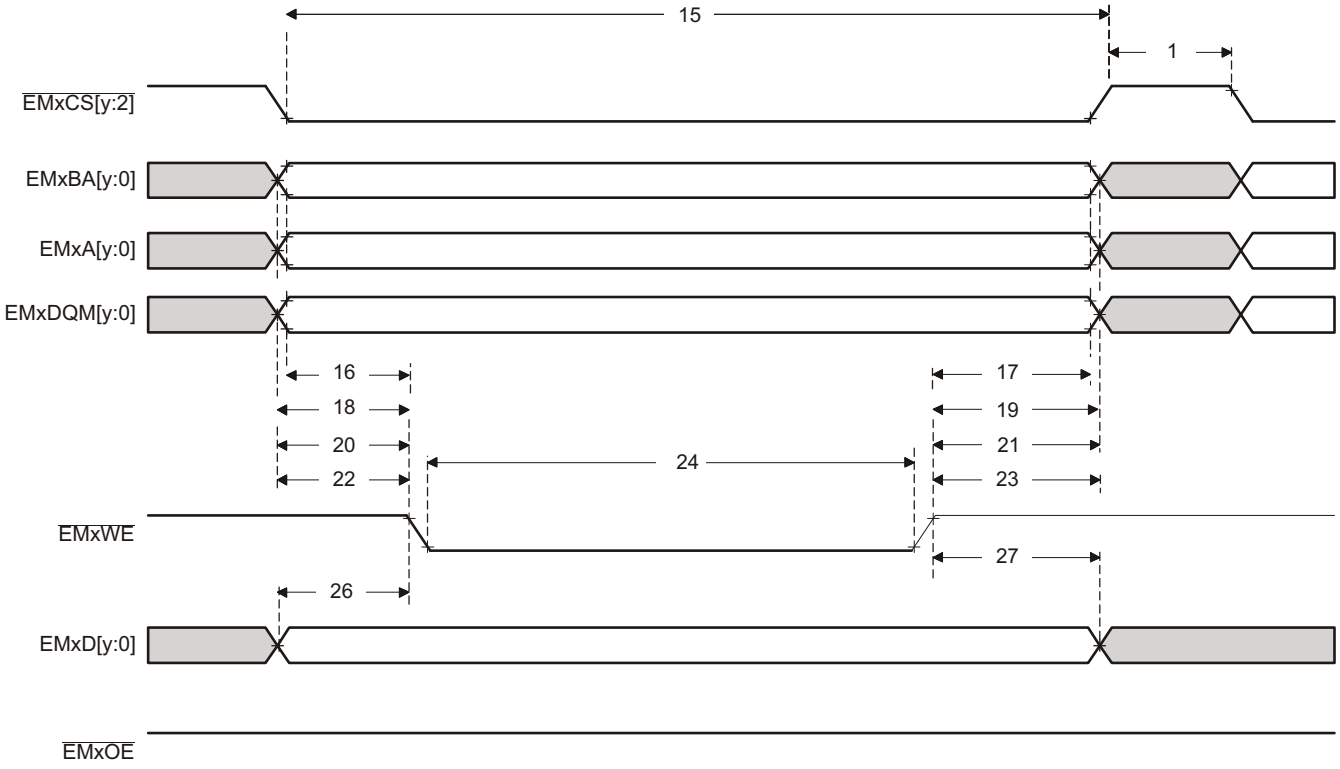

Figure 6-29. Asynchronous Memory Write Timing

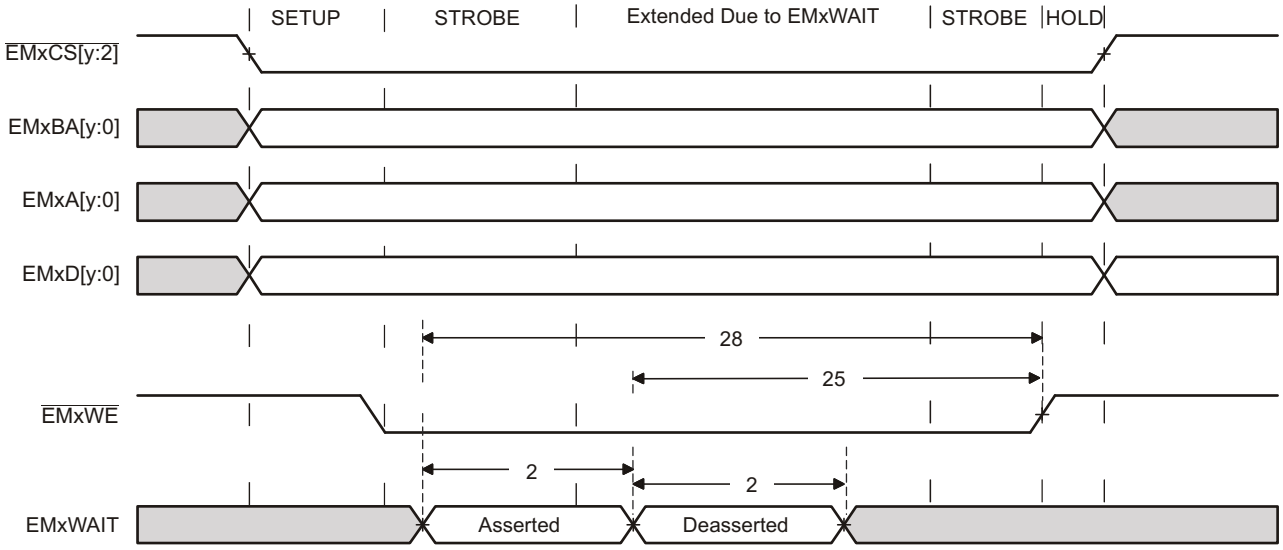

Figure 6-30. EMxWAIT Write Timing Requirements

6.15 C29x Analog Peripherals

6.15.1 Analog Subsystem

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Buffered Digital-to-Analog Converter (DAC), and Comparator Subsystem (CMPSS).

6.15.1.1 Features

The analog subsystem has the following features:

- Flexible voltage references:
  - The ADCs are referenced to VREFHIx and VREFLOx pins.
    - VREFHIAB and VREFHICDE pin voltages can be driven in externally or can be generated by an internal bandgap voltage reference.
    - The internal voltage reference range can be selected to be 0 V to 2.5 V for ADC A and ADC B when operated in 16-bit mode, however the internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V for ADC A and ADC B when operated in 12-bit mode.
    - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V for ADC C, ADC D and ADC E.
  - The buffered DACs are referenced to VREFHIx and VSSA
    - Alternately, these DACs can be referenced to the VDAC pin and VSSA
  - The comparator DACs are referenced to VDDA and VSSA
    - Alternately, these DACs can be referenced to the VDAC pin and VSSA
- Flexible pin usage
  - Buffered DAC outputs, comparator subsystem inputs, and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs
  - Internal connection to V_{REFLO} for offset self-calibration

6.15.1.2 Block Diagram

The following analog subsystem block diagrams show the connections between the different integrated analog modules to the device pins. These pins fall into two categories: analog module inputs/outputs and reference pins.

There are two reference pair pins, VREFHIAB /VREFLOAB and VREFHICDE/VREFLOCDE. VREFHIAB and VREFLOAB supply the reference for ADC A and ADC B modules which support both 16-bit and 12-bit mode. VREFHICDE and VREFLOCDE supply ADC C, ADC D and ADC E modules which only support 12-bit mode. VREFHIAB can also be used to supply DAC A, and VREFHICDE can also be used to supply DAC B

The VDAC reference pin can be used to set an alternate range for DAC A and DAC B, and for the DACs inside the CMPSS modules (the CMPSS DACs are referenced to VDDA and VSSA by default). Using this pin as a reference prevents the channel from being used as an ADC input (but the ADC can be used to sample the VDAC voltage, if desired). The choice of reference is configurable per module for each CMPSS or buffered DAC; the selection is made using the module's configuration registers.

Some analog pins support digital functionality through muxed AIOs and AGPIOs. AIOs only support digital input functionality, while AGPIOs support full digital input and output functionality.

The following notes apply to all packages:

- Not all analog pins are available on all devices. See the device data sheet to determine which pins are available.
- See the device data sheet to determine the allowable voltage range for VREFHI and VREFLO.
- An external capacitor is required on the VREFHI pins. See the device data sheet for the specific value required.
- For buffered DAC modules, VSSA is the low reference whether VREFHIx or VDAC is selected as the high reference.
- For CMPSS modules, VSSA is the low reference whether VDAC or VDDA is selected as the high reference.

The following figures show how each analog group is structured. The *Analog Pin Connections* table lists the analog pins and internal connections.

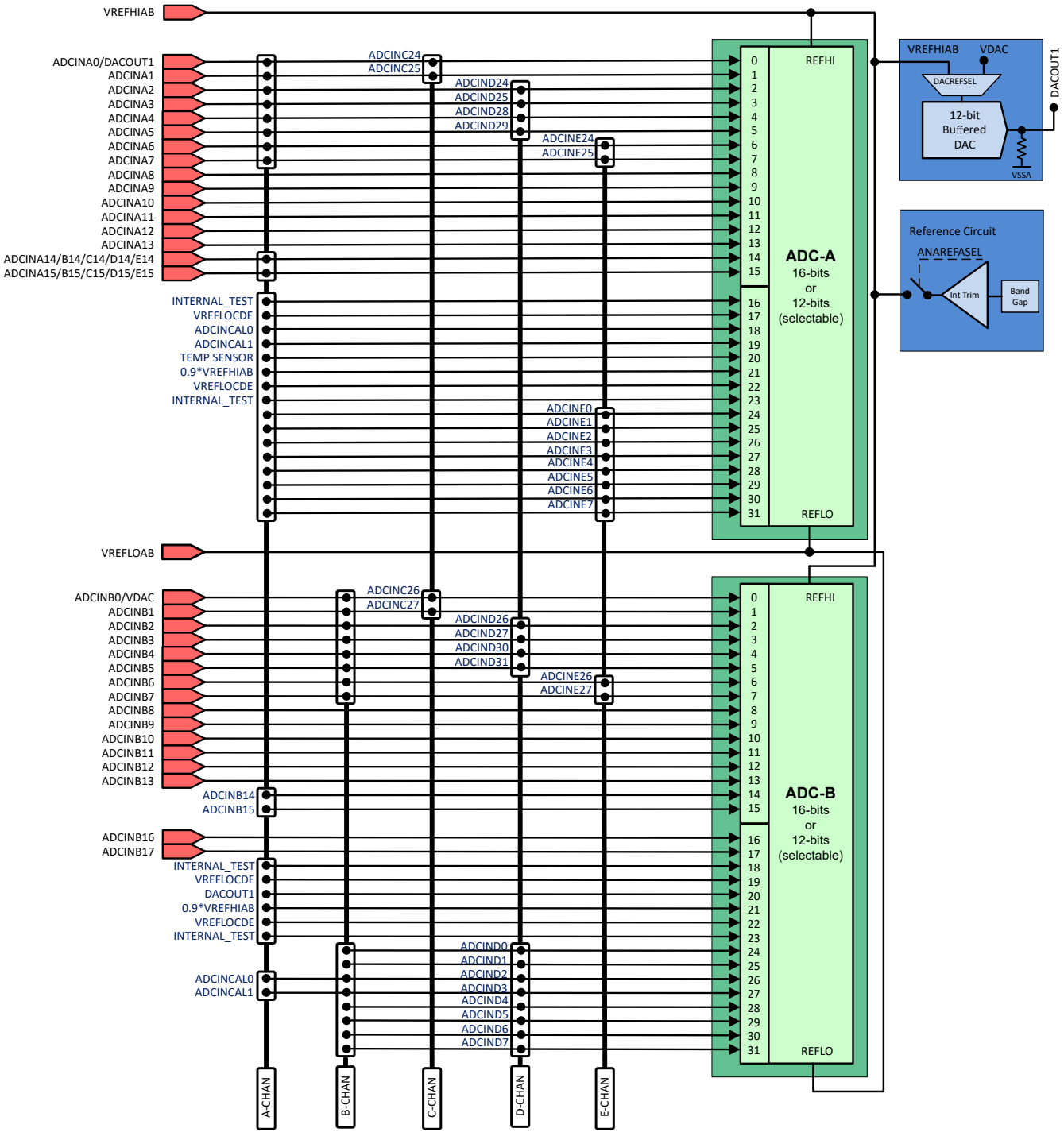

Figure 6-31. Analog Subsystem Block Diagram (ADC A and ADC B)

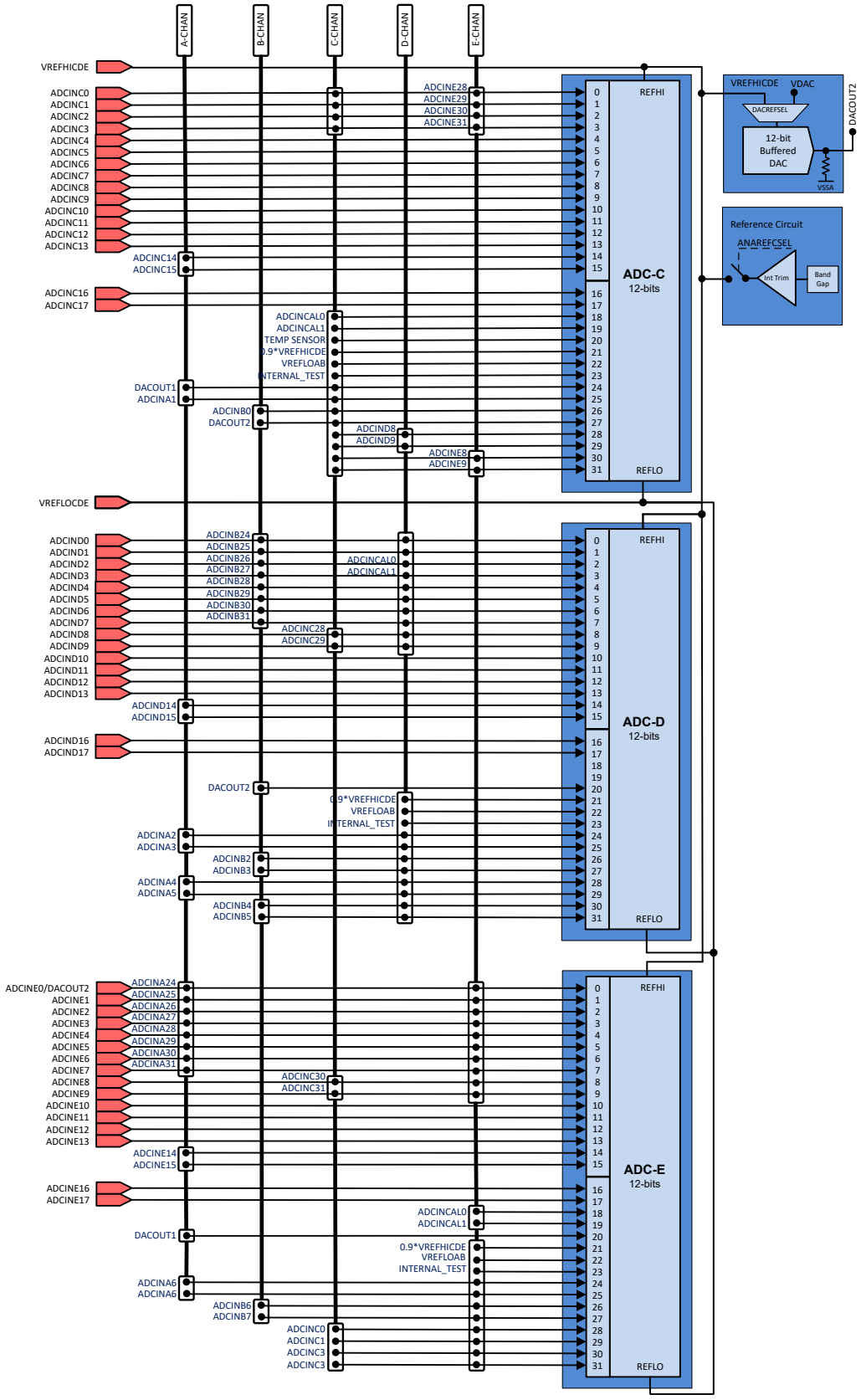

Figure 6-32. Analog Subsystem Block Diagram (ADC C, ADC D and ADC E)

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Input connections to the CMPSS modules are selectable through a programmable input mux. Figure 6-33 shows the CMPSS input connections. Table 6-12 shows the mapping of ADC input signals to CMPSS mux inputs.

- To configure the CMPH_POSIN input mux for CMPSSx, write to the CMPxHPMXSEL field in the CMPHPMXSEL or CMPHPMXSEL1 analog subsystem register.
- To configure the CMPH_NEGIN input mux for CMPSSx, write to the CMPxHNMXSEL field in the CMPHNMXSEL analog subsystem register.
- To configure the CMPL_POSIN input mux for CMPSSx, write to the CMPxLPMXSEL field in the CMPLPMXSEL or CMPLPMXSEL1 analog subsystem register.
- To configure the CMPL_NEGIN input mux for CMPSSx, write to the CMPxLNMXSEL field in the CMPLNMXSEL analog subsystem register.

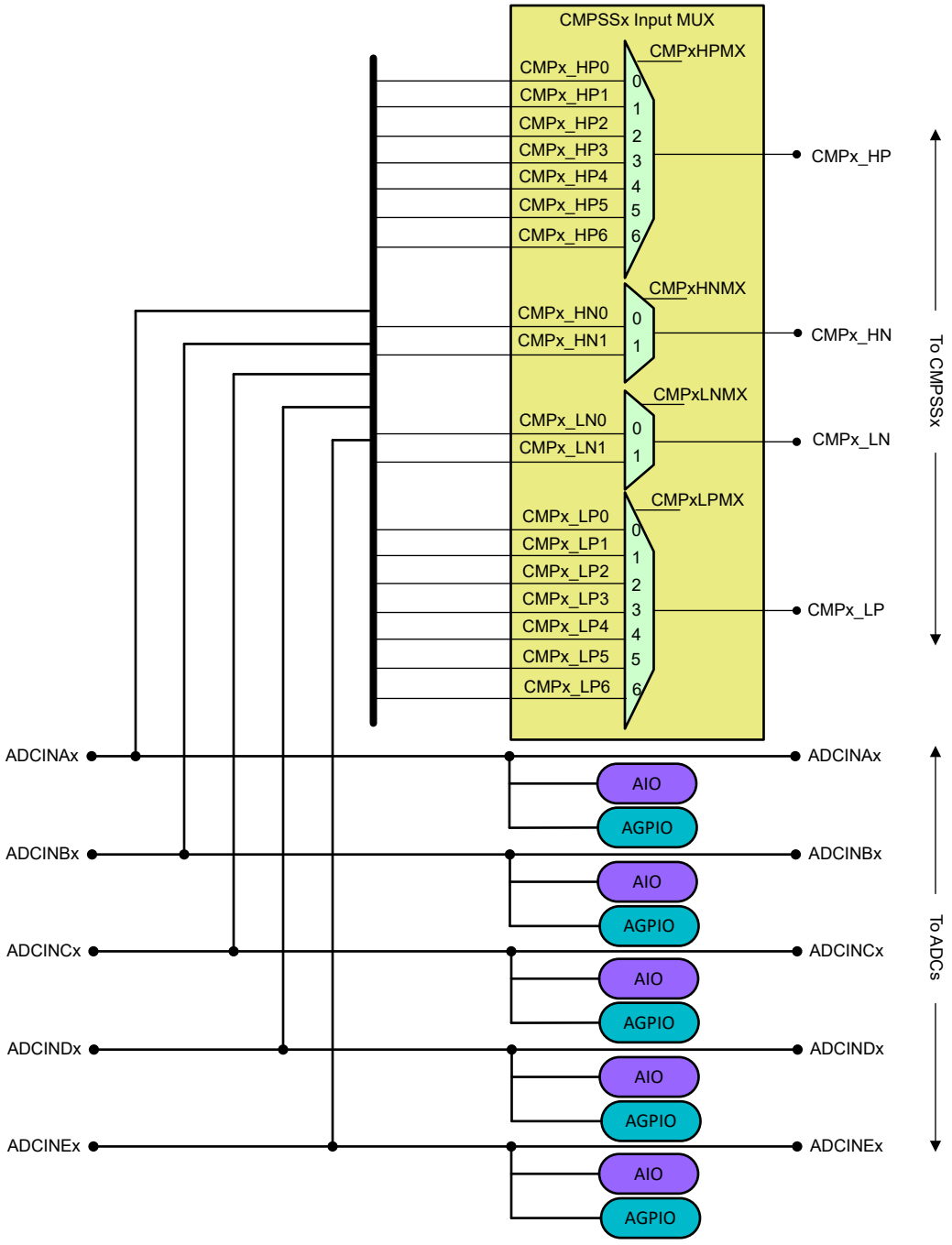


Figure 6-33. Analog Group Connections

Table 6-12. CMPSS Input Mux Options

CMPSSx Input MUX	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7	CMP8	CMP9	CMP10	CMP11	CMP12
HP0	A4	A6	B2	A0	D12	D8	D1	D3	C1	C0	C1	C8
HP1	A2	E8	B0	D5	E6	E17	B4	E4	C2	E10	E11	E1
HP2	A3	E9	B1	D0	E7	E16	B5	E5	A7	E12	E13	0.9*VREF HIAB
HP3	B3	D13	TempSense	D2	TempSense	0.9*VREF HIAB	0.9*VREF HICDE	A8	C9	D3	E1	0.9*VREF HICDE
HP4	D6	D7	E2	E3	A8	A9	A10	A11	B6	B7	B8	B9
HP5	A12	A13	A14	A15	C7	C8	C9	C10	B16	B17	C11	C12
HP6	B0	B2	D1	B8	C0	E0	A1	B9	A0	D0	A14	A15
HN0	A5	A7	B3	A1	D13	D9	D2	D4	A2	E8	B6	A6
HN1	A3	A4	B5	D5	E6	E17	B4	E4	E9	D12	C2	B1
LP0	A4	A6	B2	A0	D12	D8	D1	D3	C1	C0	C1	C8
LP1	A2	E8	B0	D5	E6	E17	B4	E4	C2	E10	E11	E1
LP2	A3	E9	B1	D0	E7	E16	B5	E5	A7	E12	E13	0.9*VREF HIAB
LP3	B3	D13	D9	D2	D4	0.9*VREF HIAB	0.9*VREF HICDE	A8	C9	D3	E1	0.9*VREF HICDE
LP4	D6	D7	E2	E3	B10	B11	B12	B13	C3	C4	C5	C6
LP5	A12	A13	A14	A15	C13	C16	C17	D10	D11	D16	D17	E0
LP6	B0	B2	D1	B8	C0	E0	A1	B9	A0	D0	A14	A15
LN0	A5	A7	B3	A1	D13	D9	D2	D4	A2	E8	B6	A6
LN1	A3	A4	B5	D5	E6	E17	B4	E4	E9	D12	C2	B1

6.15.1.3 Analog Pin Connections

Table 6-13. Analog Pin Connections

Pin Name	Pins/Package				ADC					DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	256 ZEX	176 PTS	144 RFS	100 PZS	A	B	C	D	E		High Positive	High Negative	Low Positive	Low Negative	
VREFHIAB	N2	38	30	19											
VREFHICDE	R4	54	45	33											
VFEFLOAB	N1	37	29	18			C22	D22	E22						
VREFLOCDE	T4	53	44	32	A17,A22	B19,B22									
Analog Group 1											**CMP1 and other comparators**				
ADCINA3	M2	35	27		A3			D25			CMP1 (HPMXSEL=2)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=2)	CMP1 (LNMXSEL=1)	AIO163
ADCINA5	L1	31	23		A5			D29				CMP1 (HNMXSEL=0)		CMP1 (LNMXSEL=0)	AIO165
ADCINA12	K2				A12						CMP1 (HPMXSEL=5)		CMP1 (LPMXSEL=5)		AIO166
ADCIND6	T12	71	60			B30		D6			CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		GPIO242
ADCINA4	L2	32	24		A4			D28			CMP1 (HPMXSEL=0)	CMP2 (HNMXSEL=1)	CMP1 (LPMXSEL=0)	CMP2 (LNMXSEL=1)	AIO164
ADCINB0	P2	42	34	23		B0	C26			VDAC	CMP1 (HPMXSEL=6) CMP3 (HPMXSEL=1)		CMP1 (LPMXSEL=6) CMP3 (LPMXSEL=1)		AIO170
ADCINB3	L3	33	25	16		B3		D27			CMP1 (HPMXSEL=3)	CMP3 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP3 (LNMXSEL=0)	AIO173
ADCINA2	M1	36	28		A2			D24			CMP1 (HPMXSEL=1)	CMP9 (HNMXSEL=0)	CMP1 (LPMXSEL=1)	CMP9 (LNMXSEL=0)	AIO162
Analog Group 2											**CMP2 and other comparators**				
ADCINA13	K1				A13						CMP2 (HPMXSEL=5)		CMP2 (LPMXSEL=5)		AIO167
ADCIND7	R12	72	61			B31		D7			CMP2 (HPMXSEL=4)		CMP2 (LPMXSEL=4)		GPIO243
ADCINB2	L4	34	26	17		B2		D26			CMP2 (HPMXSEL=6) CMP3 (HPMXSEL=0)		CMP2 (LPMXSEL=6) CMP3 (LPMXSEL=0)		AIO172 AIO172
ADCIND13	M6							D13			CMP2 (HPMXSEL=3)	CMP5 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP5 (LNMXSEL=0)	AIO199
ADCINA7	J3	25	17	12	A7				E25		CMP9 (HPMXSEL=2)	CMP2 (HNMXSEL=0)	CMP9 (LPMXSEL=2)	CMP2 (LNMXSEL=0)	GPIO225
ADCINE9	R10						C31		E9		CMP2 (HPMXSEL=2)	CMP9 (HNMXSEL=1)	CMP2 (LPMXSEL=2)	CMP9 (LNMXSEL=1)	AIO207
ADCINE8	T10						C30		E8		CMP2 (HPMXSEL=1)	CMP10 (HNMXSEL=0)	CMP2 (LPMXSEL=1)	CMP10 (LNMXSEL=0)	AIO206
ADCINA6	J4	26	18	13	A6				E24		CMP2 (HPMXSEL=0)	CMP12 (HNMXSEL=0)	CMP2 (LPMXSEL=0)	CMP12 (LNMXSEL=0)	GPIO224
Analog Group 3											**CMP3 and other comparators**				
ADCINE2	R6	59	51		A26				E2		CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO204
TempSensor					A20		C20				CMP3 (HPMXSEL=3) CMP5 (HPMXSEL=3)				
ADCIND9	T13	76					C29	D9				CMP6 (HNMXSEL=0)	CMP3 (LPMXSEL=3)	CMP6 (LNMXSEL=0)	GPIO245
ADCIND1	T3	48	40	29		B25		D1			CMP3 (HPMXSEL=6) CMP7 (HPMXSEL=0)		CMP3 (LPMXSEL=6) CMP7 (LPMXSEL=0)		AIO193
ADCINB5	K3	29	21			B5		D31			CMP7 (HPMXSEL=2)	CMP3 (HNMXSEL=1)	CMP7 (LPMXSEL=2)	CMP3 (LNMXSEL=1)	AIO175
ADCINA14	M3	40	32	21	A14	B14	C14	D14	E14		CMP3 (HPMXSEL=5) CMP11 (HPMXSEL=6)		CMP3 (LPMXSEL=5) CMP11 (LPMXSEL=6)		AIO168
ADCINB1	N3	41	33	22		B1	C27				CMP3 (HPMXSEL=2)	CMP12 (HNMXSEL=1)	CMP3 (LPMXSEL=2)	CMP12 (LNMXSEL=1)	AIO171

ADVANCE INFORMATION

Table 6-13. Analog Pin Connections (continued)

Pin Name	Pins/Package				ADC					DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	256 ZEX	176 PTS	144 RFS	100 PZS	A	B	C	D	E		High Positive	High Negative	Low Positive	Low Negative	
Analog Group 4											**CMP4 and other comparators**				
ADCIND5	N11	66	55			B29		D5			CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	GPIO241
ADCINE3	T6	60	52		A27				E3		CMP4 (HPMXSEL=4)		CMP4 (LPMXSEL=4)		AIO205
ADCINA1	P1	43	35	24	A1		C25				CMP7 (HPMXSEL=6)	CMP4 (HNMXSEL=0)	CMP7 (LPMXSEL=6)	CMP4 (LNMXSEL=0)	AIO161
ADCIND2	R5	57	49	34		B26		D2			CMP4 (HPMXSEL=3)	CMP7 (HNMXSEL=0)	CMP4 (LPMXSEL=3)	CMP7 (LNMXSEL=0)	AIO194
ADCINA0	R1	44	36	25	A0	C24				DACOUT1	CMP4 (HPMXSEL=0)		CMP4 (LPMXSEL=0)		AIO160
											CMP9 (HPMXSEL=6)		CMP9 (LPMXSEL=6)		
ADCIND0	R3	47	39	28		B24		D0			CMP4 (HPMXSEL=2)		CMP4 (LPMXSEL=2)		AIO192
											CMP10 (HPMXSEL=6)		CMP10 (LPMXSEL=6)		
ADCINB8	G2	20	15	11		B8					CMP4 (HPMXSEL=6)		CMP4 (LPMXSEL=6)		GPIO232
											CMP11 (HPMXSEL=4)				
ADCINA15	M4	39	31	20	A15	B15	C15	D15	E15		CMP4 (HPMXSEL=5)		CMP4 (LPMXSEL=5)		AIO169
											CMP12 (HPMXSEL=6)		CMP12 (LPMXSEL=6)		
Analog Group 5											**CMP5 and other comparators**				
ADCINB10	F1	16	13			B10							CMP5 (LPMXSEL=4)		GPIO234
ADCINC7	M9	64					C7				CMP5 (HPMXSEL=5)				GPIO237
ADCINC13	T8						C13						CMP5 (LPMXSEL=5)		AIO189
ADCINE6	P13	73	62		A30				E6		CMP5 (HPMXSEL=1)	CMP5 (HNMXSEL=1)	CMP5 (LPMXSEL=1)	CMP5 (LNMXSEL=1)	GPIO248
ADCINE7	N13	74	63		A31				E7		CMP5 (HPMXSEL=2)		CMP5 (LPMXSEL=2)		GPIO249
ADCINA8	G4	22	16		A8						CMP5 (HPMXSEL=4)				GPIO226
											CMP8 (HPMXSEL=3)		CMP8 (LPMXSEL=3)		
ADCIND4	N10	65				B28		D4				CMP8 (HNMXSEL=0)	CMP5 (LPMXSEL=3)	CMP8 (LNMXSEL=0)	GPIO240
ADCINC0	R2	45	37	26			C0		E28		CMP5 (HPMXSEL=6)		CMP5 (LPMXSEL=6)		AIO180
											CMP10 (HPMXSEL=0)		CMP10 (LPMXSEL=0)		
ADCIND12	R5							D12			CMP5 (HPMXSEL=0)	CMP10 (HNMXSEL=1)	CMP5 (LPMXSEL=0)	CMP10 (LNMXSEL=1)	AIO198
Analog Group 6											**CMP6 and other comparators**				
ADCINA9	G3	21			A9						CMP6 (HPMXSEL=4)				GPIO227
ADCINB11	F2	15	12			B11							CMP6 (LPMXSEL=4)		GPIO235
ADCINC16	N7						C16						CMP6 (LPMXSEL=5)		AIO190
ADCIND8	R13	75					C28	D8			CMP6 (HPMXSEL=0)		CMP6 (LPMXSEL=0)		GPIO244
ADCINE16	P10								E16		CMP6 (HPMXSEL=2)		CMP6 (LPMXSEL=2)		AIO212
ADCINE17	T11								E17		CMP6 (HPMXSEL=1)	CMP6 (HNMXSEL=1)	CMP6 (LPMXSEL=1)	CMP6 (LNMXSEL=1)	AIO213
ADCINC8	N12	69	58	40			C8				CMP6 (HPMXSEL=5)				GPIO238
											CMP12 (HPMXSEL=0)		CMP12 (LPMXSEL=0)		
ADCINE0	P3	49	41	30	A24				E0	DACOUT2	CMP6 (HPMXSEL=6)		CMP6 (LPMXSEL=6)		AIO202
													CMP12 (LPMXSEL=5)		
0.9*VREFHIAB					A21	B21					CMP6 (HPMXSEL=3)		CMP6 (LPMXSEL=3)		
											CMP12 (HPMXSEL=2)		CMP12 (LPMXSEL=2)		

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-13. Analog Pin Connections (continued)

Pin Name	Pins/Package				ADC					DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	256 ZEX	176 PTS	144 RFS	100 PZS	A	B	C	D	E		High Positive	High Negative	Low Positive	Low Negative	
Analog Group 7											**CMP7 and other comparators**				
ADCINA10	F3	18			A10						CMP7 (HPMXSEL=4)				GPIO228
ADCINB4	K4	30	22			B4		D30			CMP7 (HPMXSEL=1)	CMP7 (HNMXSEL=1)	CMP7 (LPMXSEL=1)	CMP7 (LNMXSEL=1)	AIO174
ADCINB12	J2					B12							CMP7 (LPMXSEL=4)		AIO176
ADCINC17	P7						C17						CMP7 (LPMXSEL=5)		AIO191
ADCINC9	P12	70	59	41			C9				CMP7 (HPMXSEL=5)				GPIO239
											CMP9 (HPMXSEL=3)		CMP9 (LPMXSEL=3)		
0.9*VREFHICDE							C21	D21	E21		CMP7 (HPMXSEL=3)		CMP7 (LPMXSEL=3)		
											CMP12 (HPMXSEL=3)		CMP12 (LPMXSEL=3)		
Analog Group 8											**CMP8 and other comparators**				
ADCINB13	J1					B13							CMP8 (LPMXSEL=4)		AIO177
ADCINA11	F4	17			A11						CMP8 (HPMXSEL=4)				GPIO229
ADCINC10	N8						C10				CMP8 (HPMXSEL=5)				AIO186
ADCIND10	N6							D10					CMP8 (LPMXSEL=5)		AIO196
ADCINE4	P11	67	56	38	A28				E4		CMP8 (HPMXSEL=1)	CMP8 (HNMXSEL=1)	CMP8 (LPMXSEL=1)	CMP8 (LNMXSEL=1)	GPIO246
ADCINE5	R11	68	57	39	A29				E5		CMP8 (HPMXSEL=2)		CMP8 (LPMXSEL=2)		GPIO247
ADCIND3	T5	58	50	35		B27		D3			CMP8 (HPMXSEL=0)		CMP8 (LPMXSEL=0)		AIO195
											CMP10 (HPMXSEL=3)		CMP10 (LPMXSEL=3)		
ADCINB9	G1	19	14	10		B9					CMP8 (HPMXSEL=6)		CMP8 (LPMXSEL=6)		GPIO233
											CMP12 (HPMXSEL=4)				
Analog Group 9											**CMP9 and other comparators**				
ADCINB16	H2					B16					CMP9 (HPMXSEL=5)				AIO178
ADCINC3	M5	52	44				C3		E30				CMP9 (LPMXSEL=4)		AIO183
ADCIND11	P6							D11					CMP9 (LPMXSEL=5)		AIO197
ADCINB6	H4	24				B6			E26		CMP9 (HPMXSEL=4)	CMP11 (HNMXSEL=0)		CMP11 (LNMXSEL=0)	GPIO230
ADCINC1	T2	46	38	27			C1		E29		CMP9 (HPMXSEL=0)		CMP9 (LPMXSEL=0)		AIO181
											CMP11 (HPMXSEL=0)		CMP11 (LPMXSEL=0)		
ADCINC2	N4	51	43				C2		E30		CMP9 (HPMXSEL=1)		CMP9 (LPMXSEL=1)		AIO182
												CMP11 (HNMXSEL=1)		CMP11 (LNMXSEL=1)	
Analog Group 10											**CMP10 and other comparators**				
ADCINB7	H3	23				B7			E27		CMP10 (HPMXSEL=4)				GPIO231
ADCINB17	H1					B17					CMP10 (HPMXSEL=5)				AIO179
ADCINC4	P5	55	47				C4						CMP10 (LPMXSEL=4)		AIO184
ADCIND16	R7							D16					CMP10 (LPMXSEL=5)		AIO200
ADCINE10	T9								E10		CMP10 (HPMXSEL=1)		CMP10 (LPMXSEL=1)		AIO208
ADCINE12	P9								E12		CMP10 (HPMXSEL=2)		CMP10 (LPMXSEL=2)		AIO210
Analog Group 11											**CMP11 and other comparators**				
ADCINC5	N5	56	48				C5						CMP11 (LPMXSEL=4)		AIO185

Table 6-13. Analog Pin Connections (continued)

Pin Name	Pins/Package				ADC					DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	256 ZEX	176 PTS	144 RFS	100 PZS	A	B	C	D	E		High Positive	High Negative	Low Positive	Low Negative	
ADCINC11	P8						C11				CMP11 (HPMXSEL=5)				AIO187
ADCIND17	T7							D17					CMP11 (LPMXSEL=5)		AIO201
ADCINE11	R9								E11		CMP11 (HPMXSEL=1)		CMP11 (LPMXSEL=1)		AIO209
ADCINE13	N9								E13		CMP11 (HPMXSEL=2)		CMP11 (LPMXSEL=2)		AIO211
ADCINE1	P4	50	42	31	A25				E1		CMP11 (HPMXSEL=3)		CMP11 (LPMXSEL=3)		AIO203
											CMP12 (HPMXSEL=1)		CMP12 (LPMXSEL=1)		
Analog Group 12											**CMP12 and other comparators**				
ADCINC6	M8	63					C6						CMP12 (LPMXSEL=4)		GPIO236
ADCINC12	B8						C12				CMP12 (HPMXSEL=5)				AIO188

ADVANCE INFORMATION

6.15.2 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits selectable resolution of 12 bits or 16 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based.

Each ADC has the following features:

- Selectable resolution of 12 bits or 16 bits Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended or differential signal mode
- Input multiplexer with up to channels
- 32 configurable SOCs
- 32 individually addressable result registers
- External analog input mux selection per SOC, up to 4 bits
- Sample cap reset feature for memory crosstalk mitigation
- Multiple trigger sources
  - Software immediate start
  - All ePWMs: ADCSOC A or B
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
  - ECAP events in capture mode (CEVT1, CEVT2, CEVT3, and CEVT4) and APWM mode (period match, compare match, or both).
  - Global software trigger for multiple ADCs
- Four flexible interrupts
- Burst-mode triggering option
- Hardware oversampling mode up to 128x, with configurable trigger spread delay
- Hardware undersampling mode
- Trigger phase delay function
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Configurable digital filter for high/low/zero-crossing compare
  - Trigger-to-sample delay capture
  - Absolute value calculation
  - 24-bit accumulation register for oversampling, with configurable binary shift
  - Minimum/maximum calculation for outlier rejection

Note

Not every channel can be pinned out from all ADCs. See the *Pin Configuration and Functions* section to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-34.

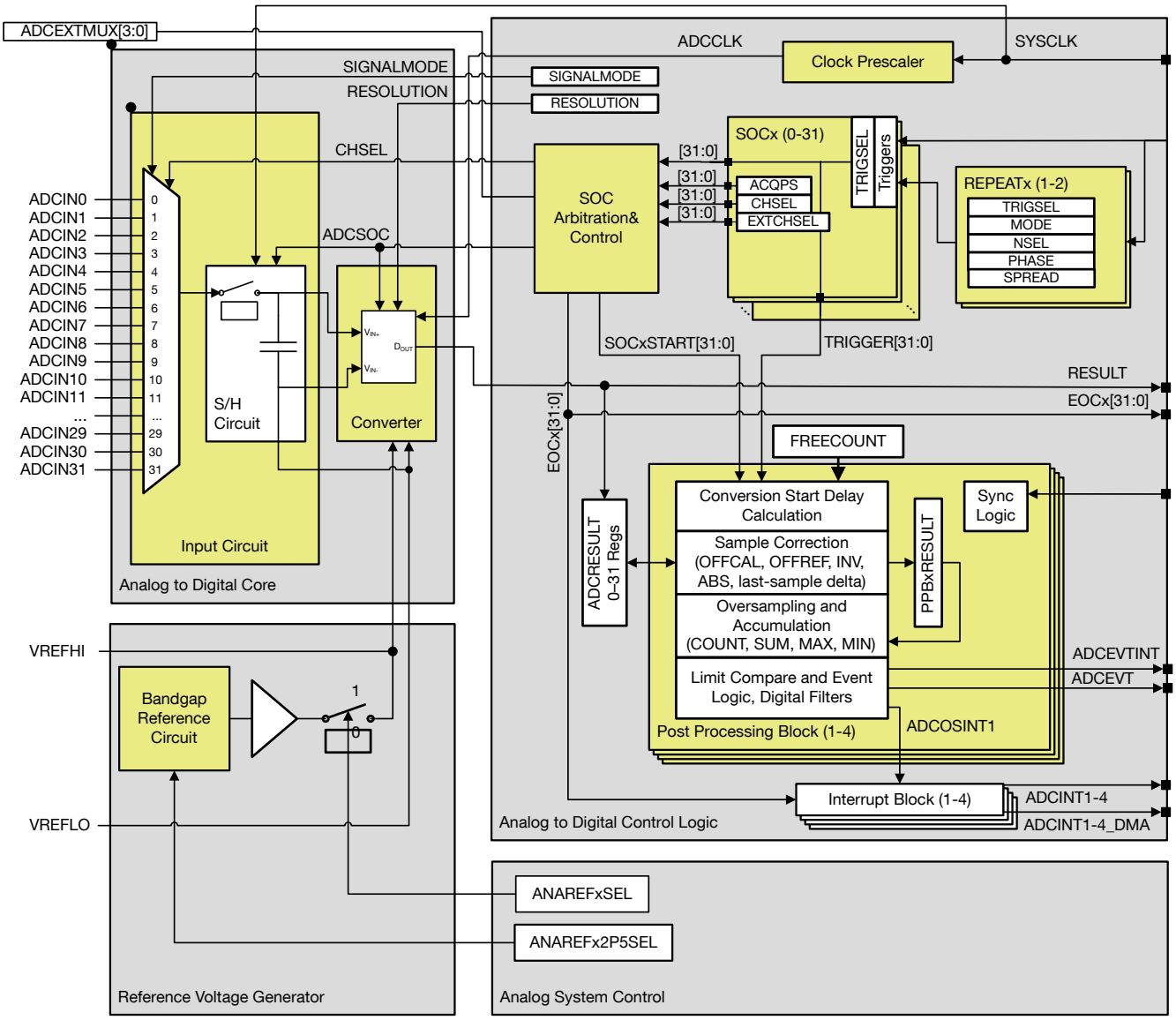


Figure 6-34. ADC Module Block Diagram

ADVANCE INFORMATION

6.15.2.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-14 summarizes the basic ADC options and their level of configurability.

Table 6-14. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	Per module(1)
Resolution	Not configurable (12-bit resolution only) Per module(1)
Signal mode	Not configurable (single-ended signal mode only) Per module
Reference voltage source	Per module (external or internal)(2) (3)
Trigger source	Per SOC(1)
Converted channel	Per SOC
Acquisition window duration	Per SOC(1)
EOC location	Per module
Burst mode	Per module(1)

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the *Ensuring Synchronous Operation* section of the Analog-to-Digital Converter (ADC) chapter in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* .
(2) Lower pin count packages may share one VREFHI pin among multiple ADCs. In this case, the ADCs that share a reference pin must have their reference modes configured identically.
(3) 3.3 V internal reference mode is not supported when using 16-bit resolution.

6.15.2.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

The ADC supports two signal modes: single-ended and differential. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. In differential signaling mode, the input voltage to the converter is sampled through a pair of input pins, one of which is the positive input (ADCINxP) and the other is the negative input (ADCINxN). The actual input voltage is the difference between the two (ADCINxP − ADCINxN). Figure 6-35 shows the differential signaling mode. Figure 6-36 shows the single-ended signaling mode.

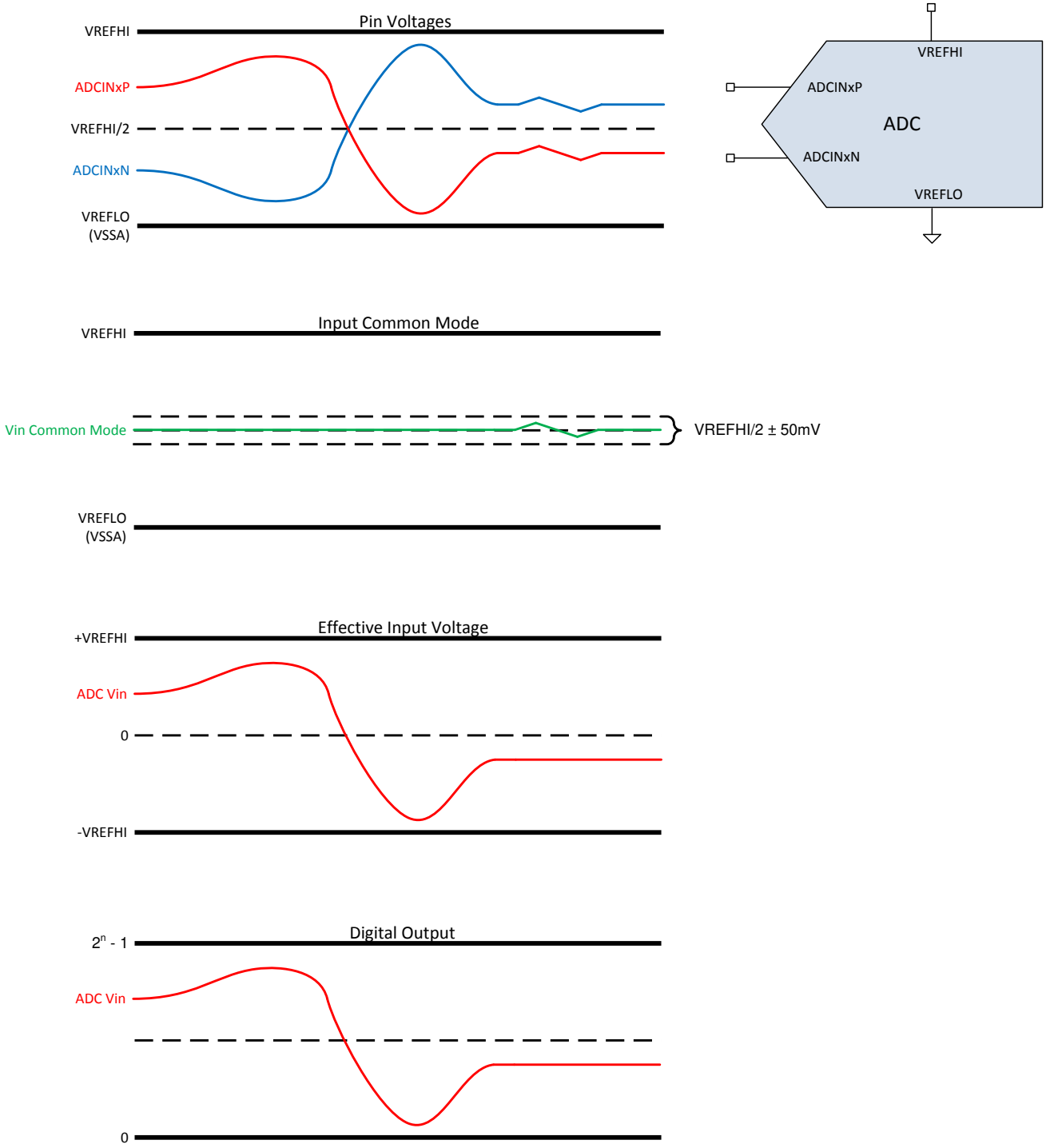


Figure 6-35. Differential Signaling Mode

ADVANCE INFORMATION

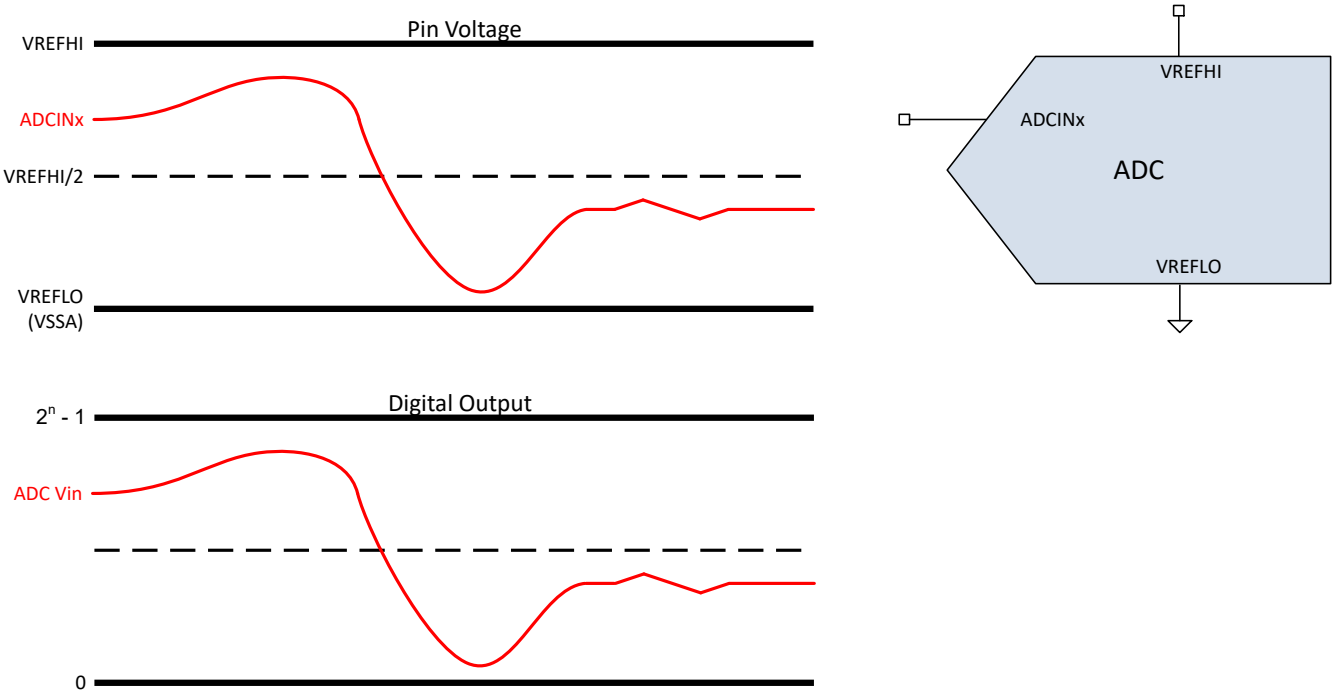


Figure 6-36. Single-ended Signaling Mode

ADVANCE INFORMATION

6.15.2.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.15.2.2.1 ADC Operating Conditions 12-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		60	MHz
Sample rate (3)	200-MHz SYSCLK			3.7	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	75			ns
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.15.2.2.2 ADC Operating Conditions 12-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		60	MHz
Sample rate (3)	200-MHz SYSCLK			3.7	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	75			ns
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.15.2.2.3 ADC Operating Conditions 16-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		60	MHz
Sample rate	200-MHz SYSCLK			1.1	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	320			ns
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.15.2.2.4 ADC Operating Conditions 16-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		60	MHz
Sample rate	200-MHz SYSCLK			1.1	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	320			ns
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.15.2.2.5 ADC Timing Requirements

		MIN	MAX	UNIT
$t_{su(ADCCHSEL-SOC)}$	ADCCHSEL valid before ADCSOC high	0.5		ns
$t_{su(ADCSOC)}$	ADCSOC low before ADCCLK high	1		ns
$t_{w(ADCCLK)}$	Width of ADCCLK	0.8		ns
$t_{w(ADCSOC)}$	Width of ADCSOC	0.6		ns

ADVANCE INFORMATION

6.15.2.2.6 ADC Characteristics 12-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	10.1		11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			130		µA
Internal Reference Capacitor Value(2)		2.2			µF
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error	Internal reference	–45		45	LSB
	External reference	–5	±3	5	
Offset Error		–4	±2	4	LSB
Channel-to-Channel Gain Error(4)			±2		LSB
Channel-to-Channel Offset Error(4)			±2		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		±4		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		±2		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±1.0	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		69.1		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		69.1		
THD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		–88		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		89		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		69.0		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		69.0		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.2		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.2		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs, 256-ball ZEJ package		10.9		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs, 169-ball NMR package		10.9		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs, 176-pin PTP package		9.7		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs, 100-pin PZP package		9.7		

6.15.2.2.6 ADC Characteristics 12-bit Single-Ended (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

6.15.2.2.7 ADC Characteristics 12-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	10.1		11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			130		µA
Internal Reference Capacitor Value(2)		2.2			µF
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error	Internal reference	–45		45	LSB
	External reference	–5	±3	5	
Offset Error		–5	±2	5	LSB
Channel-to-Channel Gain Error(4)			2		LSB
Channel-to-Channel Offset Error(4)			2		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		4		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		2		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±1.0	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		68.8		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		60.1		
THD(3)	VREFHI = 2.5 V, fin = 100 kHz		–80.6		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz		79.2		dB

ADVANCE INFORMATION

6.15.2.2.7 ADC Characteristics 12-bit Differential (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		68.5		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		60.0		
ENOB[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.0		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.0		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

6.15.2.2.8 ADC Characteristics 16-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	29.6		31	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current[1]			190		µA
Internal Reference Capacitor Value[2]		4.7	22		µF
External Reference Capacitor Value[2]		4.7	22		µF
DC Characteristics					
Gain Error	Internal reference 2.5V	-720		720	LSB
	External reference	–64	±20	64	LSB
Offset Error	(Across temperature) Internal reference 2.5V	-6	±4	6	LSB
Offset Error		–6	±4	6	LSB
Channel-to-Channel Gain Error[4]			±6		LSB
Channel-to-Channel Offset Error[4]			±6		LSB
ADC-to-ADC Gain Error[5]	Identical VREFHI and VREFLO for all ADCs		±6		LSB
ADC-to-ADC Offset Error[5]	Identical VREFHI and VREFLO for all ADCs		±6		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–6	±1.5	6	LSB

6.15.2.2.8 ADC Characteristics 16-bit Single-Ended (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–2		2	LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		83.5		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		78.2		
THD(3)	VREFHI = 2.5 V, fin = 100 kHz		–94		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz		93		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		83.4		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		76.0		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		13.5		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		13.5		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		77		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 800 kHz		74		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		77		
	VDDA = 3.3-V DC + 200 mV Sine at 800 kHz		74		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable. In external reference mode, capacitance is dependent on reference IC buffer output requirements.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

6.15.2.2.9 ADC Characteristics 16-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	29.6		31	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			190		µA
Internal Reference Capacitor Value(2)		4.7	22		µF
External Reference Capacitor Value(2)		4.7	22		µF
DC Characteristics					
Gain Error	Internal reference 2.5 V	–720		720	LSB
	External reference	–64	±9	64	LSB
Offset Error	(Across temperature) Internal reference 2.5 V	–6	±4	6	LSB

ADVANCE INFORMATION

6.15.2.2.9 ADC Characteristics 16-bit Differential (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Error		–6	±4	6	LSB
Channel-to-Channel Gain Error(4)			±6		LSB
Channel-to-Channel Offset Error(4)			±3		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		±6		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		±3		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–3.5	±1.0	3.5	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–2		2	LSBs
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs		not supported		dB
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		89.8		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		66.3		
THD(3)	VREFHI = 2.5 V, fin = 100 kHz		–98		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz		99		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		89.2		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		66.1		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		14.52		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		14.52		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		77		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		74		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		77		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		74		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable. In external reference mode, capacitance is dependent on reference IC buffer output requirement.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

ADVANCE INFORMATION

6.15.2.2.10 ADC INL and DNL

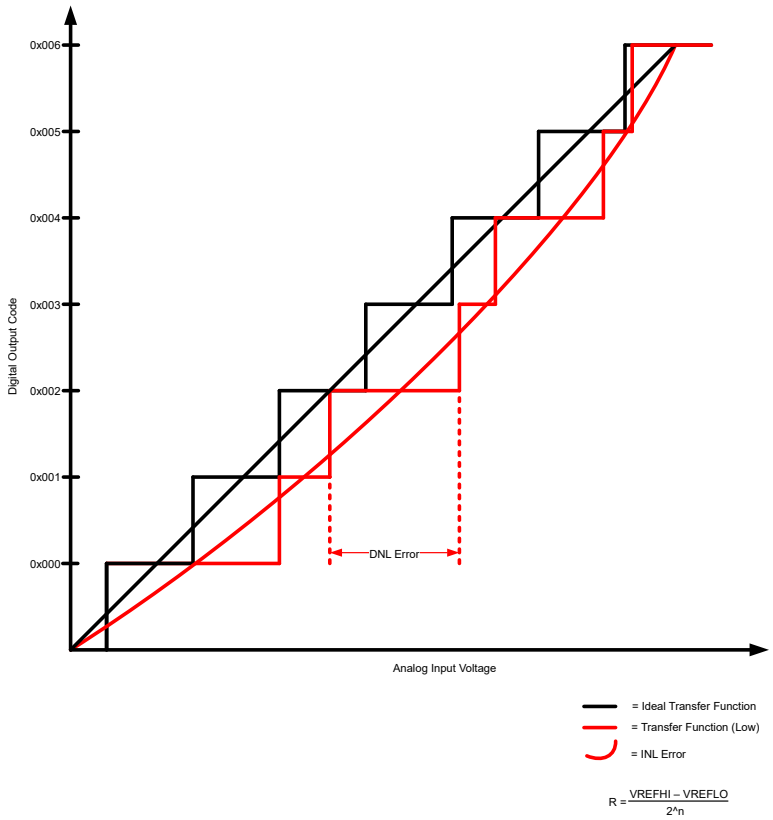


Figure 6-37. ADC INL and DNL

6.15.2.2.11 ADC Input Model Models

The ADC input characteristics are given by Table 6-15 and Figure 6-38 for Type 5 12-bit ADC.

The ADC input characteristics are given by Table 6-16, Table 6-17, Figure 6-38, and Figure 6-39 for Type 4 12-bit/16-bit ADC.

Table 6-15. Input Model Parameters for 12-bit ADC (ADC CDE)

	DESCRIPTION	REFERENCE MODE	VALUE
C_p	Parasitic input capacitance	All	See Table 6-20 (channels Cx,Dx,Ex).
R_{on}	Sampling switch resistance	External Reference, 2.5-V Internal Reference	500 Ω
		3.3-V Internal Reference	860 Ω
C_h	Sampling capacitor	External Reference, 2.5-V Internal Reference	12.5 pF
		3.3-V Internal Reference	7.5 pF
R_s	Nominal source impedance	All	50 Ω

Table 6-16. Single-Ended Input Model Parameters (12-bit Resolution) for 12-bit/16-bit ADC (ADC AB)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-20 (channels Ax,Bx)
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	14.5 pF
R_s	Nominal source impedance	50 Ω

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-17. Single-Ended Input Model Parameters (16-bit Resolution) for 12-bit/16-bit ADC (ADC AB)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-20 (channels Ax,Bx).
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	32.5 pF
R_s	Nominal source impedance	50 Ω

Table 6-18. Differential Input Model Parameters (12-bit Resolution) for 12-bit/16-bit ADC (ADC AB)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-20 (channels Ax,Bx).
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	7.5 pF
R_s	Nominal source impedance	50 Ω

Table 6-19. Differential Input Model Parameters (16-bit Resolution) for 12-bit/16-bit ADC (ADC AB)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-20 (channels Ax,Bx).
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

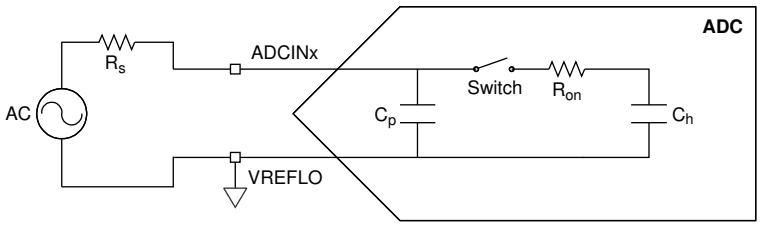


Figure 6-38. Single-Ended Input Model

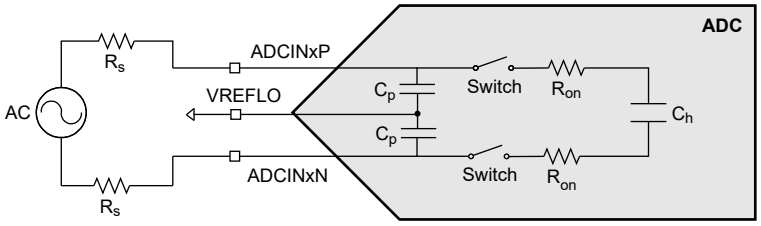


Figure 6-39. Differential Input Model

These input models should be used with actual signal source impedance to determine the acquisition window duration. For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Note.

Table 6-20. Per-Channel Parasitic Capacitance

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/DACOUT1	5.4	6.9
A1	4.1	5.6
A2	4.1	5.6
A3	5.6	7.1
A4	4.2	5.7

Table 6-20. Per-Channel Parasitic Capacitance (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A5	4.9	6.4
A6	0.2	1.7
A7	0.3	1.6
A8	0.3	1.8
A9	0.3	1.7
A10	0.3	1.8
A11	0.3	1.8
A12	5.2	6.7
A13	4.9	6.4
A14,B14,C14,D14,E14	5.7	7.2
A15,B15,C15,D15,E15	5.5	7.0
B0/VDAC	27.1	28.6
B1	4.0	5.5
B2	4.6	6.1
B3	5.1	6.6
B4	3.5	5.0
B5	4.9	6.4
B6	0.3	1.8
B7	0.4	1.9
B8	0.2	1.7
B9	0.3	1.8
B10	0.3	1.8
B11	0.3	1.8
B12	4.9	6.4
B13	4.7	6.2
B16	5.1	6.6
B17	4.1	5.6
C0	5.0	6.5
C1	4.4	5.9
C2	4.9	6.4
C3	4.9	6.4
C4	2.9	4.4
C5	2.7	4.2
C6	0.3	1.8
C7	0.3	1.8
C8	0.3	1.8
C9	0.3	1.8
C10	3.3	4.8

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 6-20. Per-Channel Parasitic Capacitance (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
C11	3.1	4.6
C12	2.9	4.4
C13	3.0	4.4
C16	3.1	4.6
C17	3.4	4.9
D0	3.3	4.8
D1	3.3	4.8
D2	5.0	6.5
D3	5.7	7.2
D4	0.2	1.7
D5	0.2	1.7
D6	0.2	1.7
D7	0.5	2.0
D8	0.5	2.0
D9	0.4	1.9
D10	3.8	5.3
D11	3.0	4.5
D12	3.3	4.8
D13	3.3	4.8
D16	2.9	4.4
D17	3.1	4.6
E0/DACOUT2	6.4	7.9
E1	3.3	4.8
E2	3.1	4.6
E3	3.3	4.8
E4	0.3	1.8
E5	0.3	1.8
E6	0.5	2.0
E7	0.4	1.9
E8	4.4	5.9
E9	3.9	5.4
E10	3.4	4.9
E11	3.4	4.9
E12	3.4	4.9
E13	3.6	5.1
E16	3.5	5.0
E17	3.6	5.1

6.15.2.2.12 ADC Timing Diagrams

The following diagrams show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the interrupt controller).

Table 6-21 lists the descriptions of the ADC timing parameters. Table 6-22 and Table 6-23 list the ADC timings.

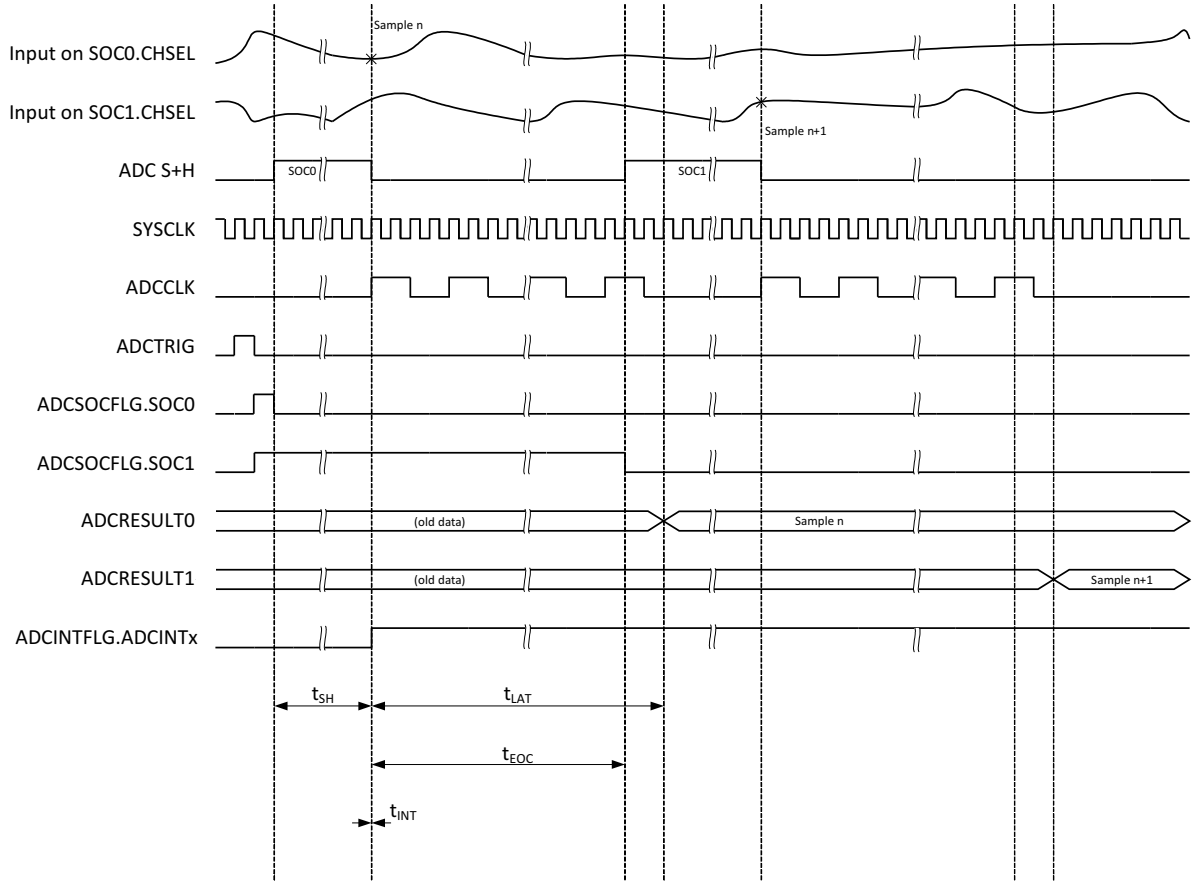


Figure 6-40. ADC Timings for 12-bit Mode in Early Interrupt Mode

ADVANCE INFORMATION

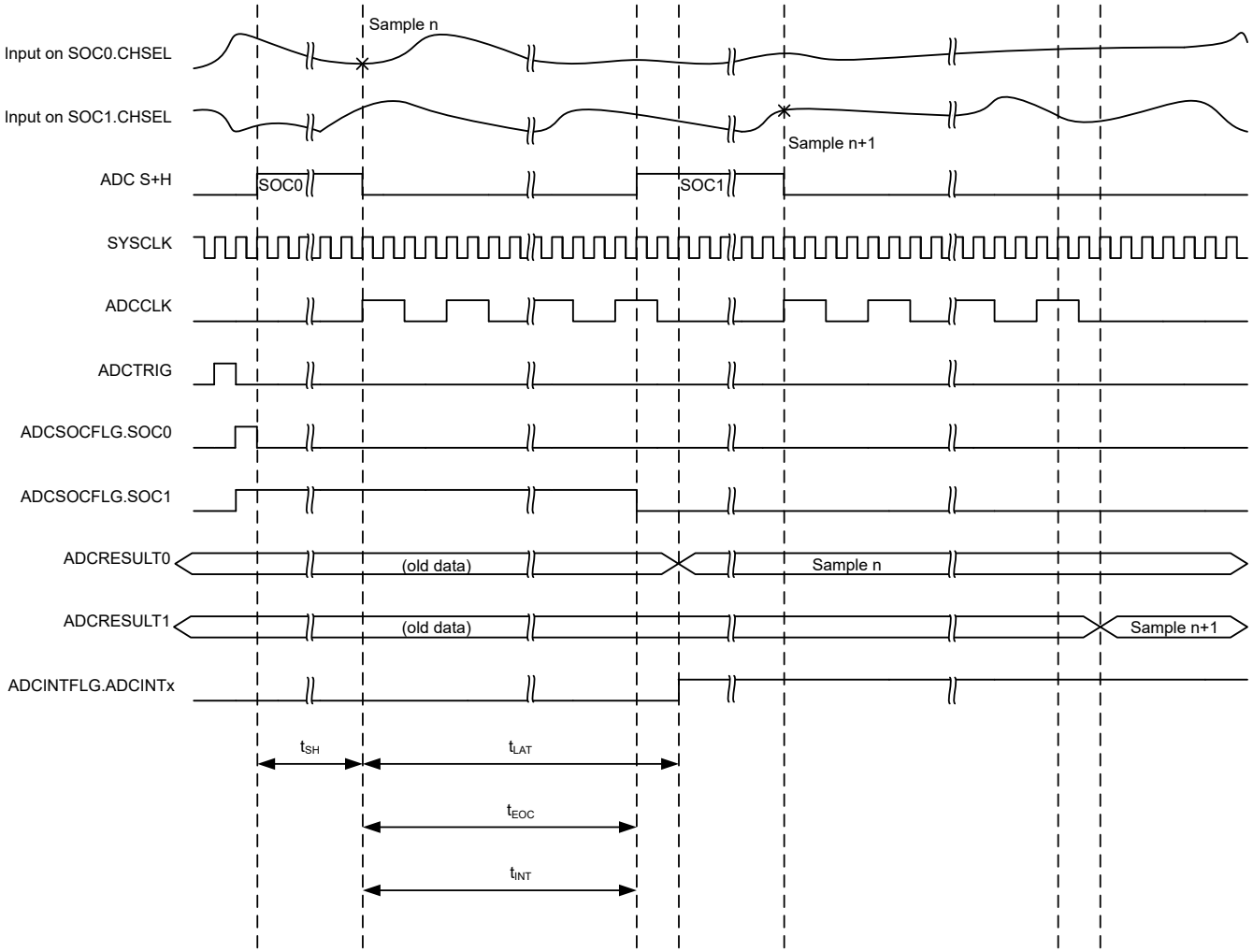


Figure 6-41. ADC Timings for 12-bit Mode in Late Interrupt Mode

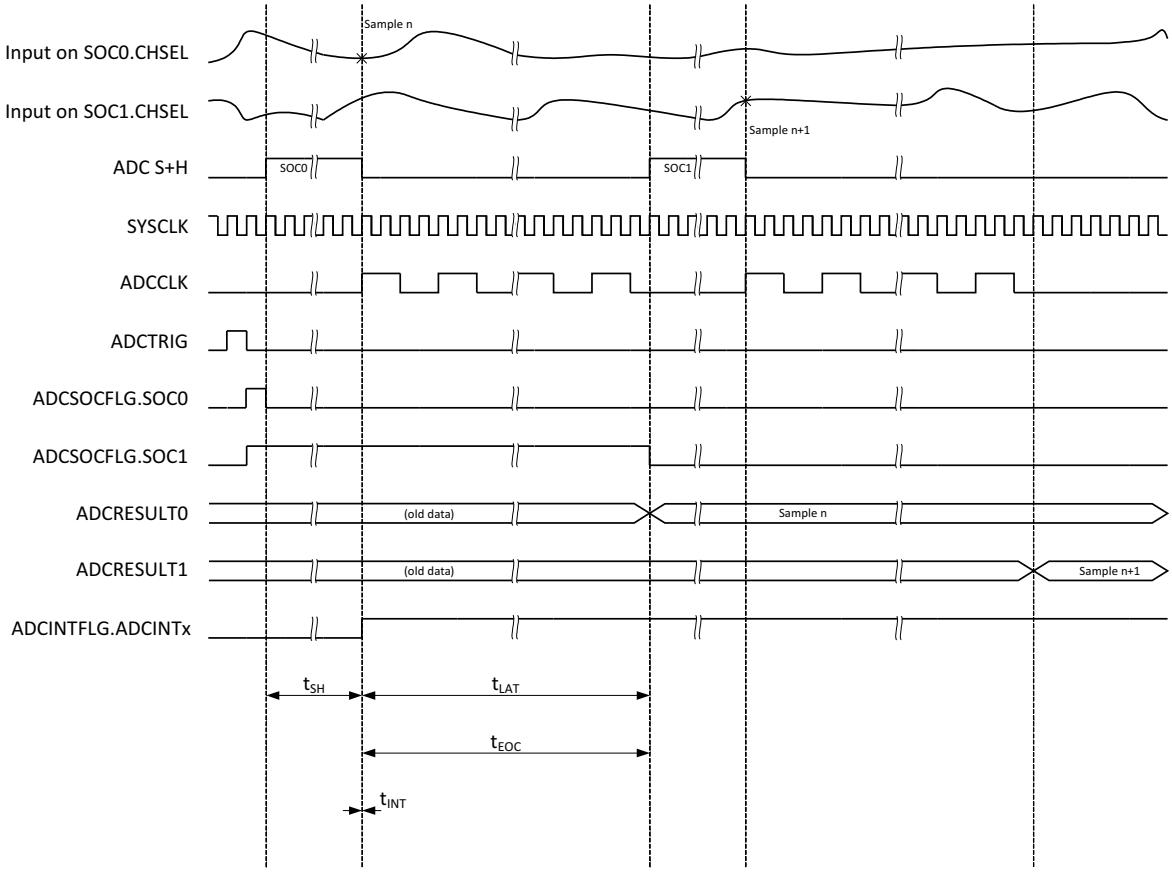


Figure 6-42. ADC Timings for 16-bit Mode in Early Interrupt Mode

ADVANCE INFORMATION

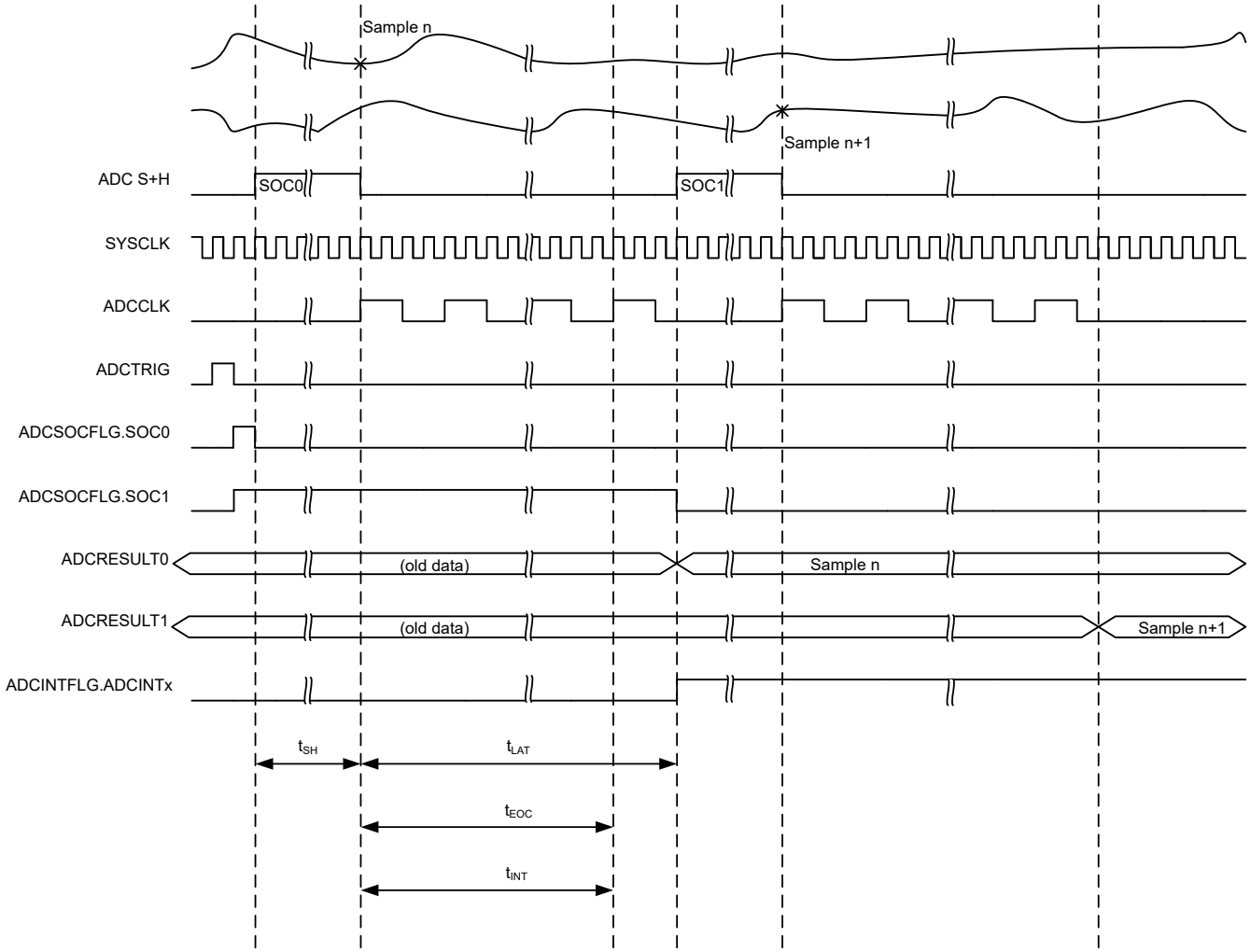


Figure 6-43. ADC Timings for 16-bit Mode in Late Interrupt Mode (SYSCLK Cycles)

Table 6-21. ADC Timing Parameter Descriptions

PARAMETER	DESCRIPTION
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs. **Note:** The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned.
t_{EOC}	The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched. In 16-bit mode, this coincides with the latching of the conversion results, while in 12-bit mode, the subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal. If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read).
t_{DMA}	The time from the end of the S+H window until a DMA read of the ADC conversion result is triggered, when ADCCTL1.TDMAEN = 1. If TDMAEN is set to 0, then the DMA trigger occurs at T_{INT}. In certain conditions, the ADCINT flag can be set before the ADCRESULT value is latched. To make sure that the DMA read occurs after the ADCRESULT value has been latched, write 1 to ADCCTL1.TDMAEN to enable DMA timings.

ADVANCE INFORMATION

Table 6-22. ADC Timings in 12-bit Mode

ADCCLK Prescale		SYSCLK Cycles				
ADCCTL2. PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)	t_{DMA}
0	1	11	13	0	11	13
2	2	21	23	0	21	23
3	2.5	26	28	0	26	28
4	3	31	34	0	31	34
5	3.5	36	39	0	36	39
6	4	41	44	0	41	44
7	4.5	46	49	0	46	49
8	5	51	55	0	51	55
9	5.5	56	60	0	56	60
10	6	61	65	0	61	65
11	6.5	66	70	0	66	70
12	7	71	76	0	71	76
13	7.5	76	81	0	76	81
14	8	81	86	0	81	86
15	8.5	86	91	0	86	91

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

Table 6-23. ADC Timings in 16-bit Mode

ADCCLK Prescale		SYSCLK Cycles				
ADCCTL2. PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)	t_{DMA}
0	1	31	32	0	31	32
2	2	60	61	0	60	61
3	2.5	75	75	0	75	75
4	3	90	91	0	90	91
5	3.5	104	106	0	104	106
6	4	119	120	0	119	120
7	4.5	134	134	0	134	134
8	5	149	150	0	149	150
9	5.5	163	165	0	163	165
10	6	178	179	0	178	179
11	6.5	193	193	0	193	193
12	7	208	209	0	208	209
13	7.5	222	224	0	222	224
14	8	237	238	0	237	238
15	8.5	252	252	0	252	252

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

6.15.3 Temperature Sensor

6.15.3.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the *Temperature Sensor Characteristics* table.

6.15.3.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	External reference		±15		°C
$t_{startup}$	Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)			500		µs
t_{acq}	ADC acquisition time		450			ns

ADVANCE INFORMATION

6.15.4 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs, and two digital filters. The subsystem also includes two ramp generators. The ramp generators ramp up and down. Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the Analog Subsystem chapter of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. Two ramp generator circuits are optionally available to control the reference 12-bit DAC values for the high and low comparators in the subsystem. The DAC along with a wrapper can be used to generate a ramp which is used for slope compensation in Peak Current Mode Control (PCMC) and other applications. The subsystem also works with the EPWM to support Diode Emulation Mode.

Each CMPSS includes:

- Two analog comparators
- Two independently programmable reference 12-bit DACs
- Dual decrementing/incrementing ramp generators
- Two digital filters with max filter clock prescale of 2^{24}
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- External connection to CMPSS filters
- Diode emulation support
- Supports connection with ePWM for diode emulation
- Ramp generator prescaler
- Wake-up from standby and halt LPM (Low Power Modes) triggered by CMPSS trip outputs

6.15.4.1 CMPSS Connectivity Diagram

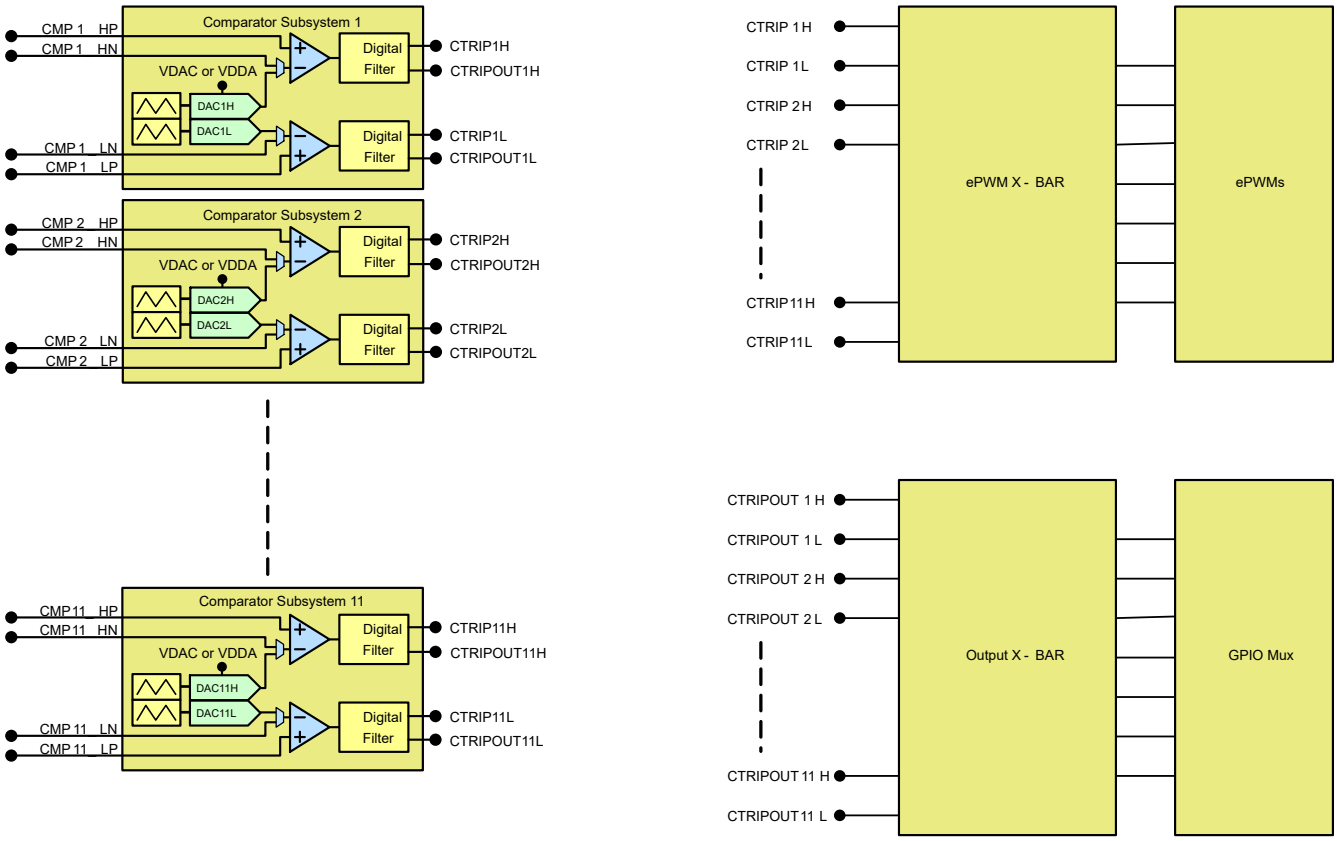


Figure 6-44. CMPSS Connectivity

6.15.4.2 Block Diagram

The block diagram for the CMPSS is shown in Figure 6-45.

- CTRIPx(x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. See the Enhanced Pulse Width Modulator (ePWM) chapter of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for more details on the ePWM X-BAR mux configuration.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the General-Purpose Input/Output (GPIO) chapter of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for more details on the Output X-BAR mux configuration.

ADVANCE INFORMATION

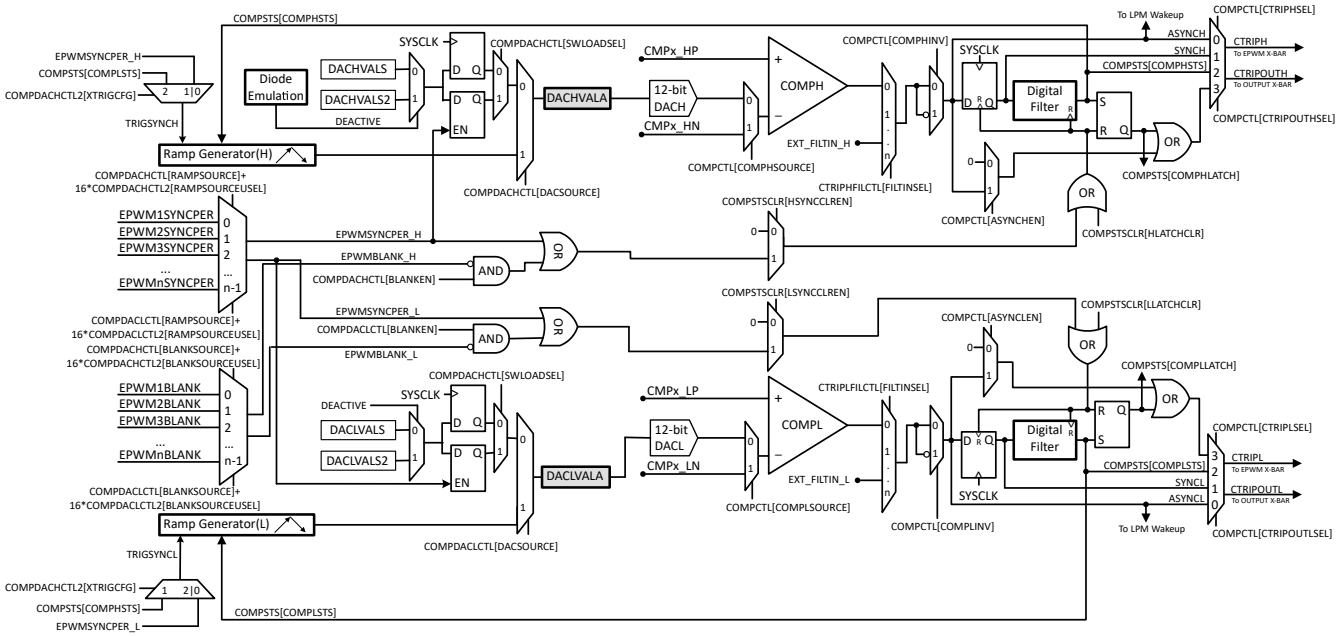


Figure 6-45. CMPSS Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. Some CMPSS instances also allow the low DAC output to be routed to a pin to act as an external DAC. In this case, all other CMPSS module functionality is not useable, including the high DAC, both comparators, ramp generation, and the digital filters. The reference 12-bit DAC is illustrated in Figure 6-46.

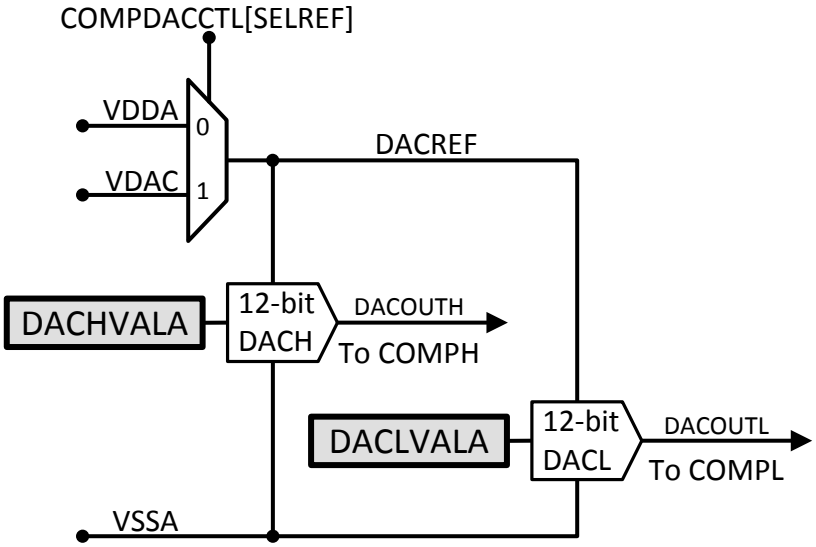


Figure 6-46. Reference DAC Block Diagram

6.15.4.3 CMPSS Electrical Data and Timing

6.15.4.3.1 Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time				500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Low common mode, inverting input set to 50mV	–20		20	mV
Hysteresis(1)		1x		12		LSB
		2x		24		
		3x		36		
		4x		48		
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)		Step response		21	60	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		ns
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

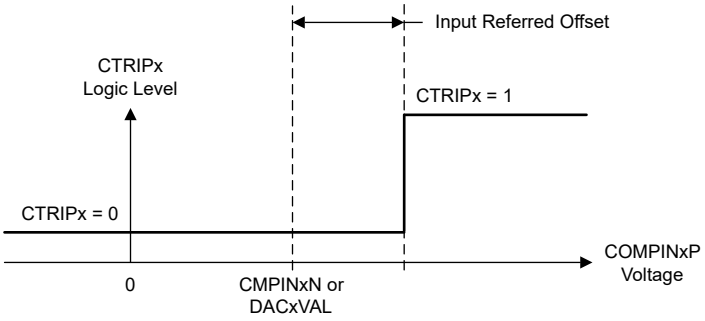


Figure 6-47. CMPSS Comparator Input Referred Offset

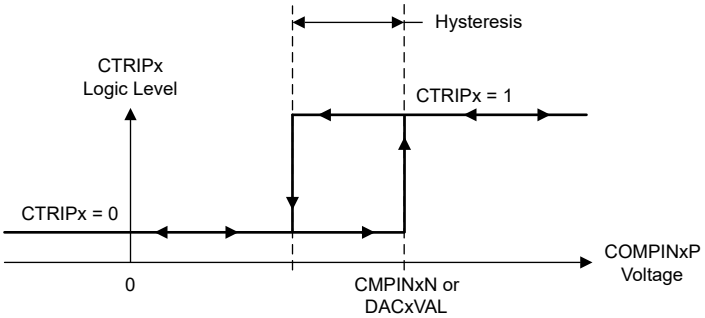


Figure 6-48. CMPSS Comparator Hysteresis

ADVANCE INFORMATION

6.15.4.3.2 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		VDDA	V
	External reference	0		VDAC(4)	
Static offset error(1)		–25		25	mV
Static gain error(1)		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance(2)	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time(2)				200	ns
VDAC reference voltage	When VDAC is reference	2.4	2.5 or 3.0	VDDA	V
VDAC load(3)	When VDAC is reference	6	8	10	kΩ

(1) Includes comparator input referred errors.
(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(3) Per active CMPSS module.
(4) The maximum output voltage is VDDA when VDAC > VDDA.

6.15.4.3.3 CMPSS Illustrative Graphs

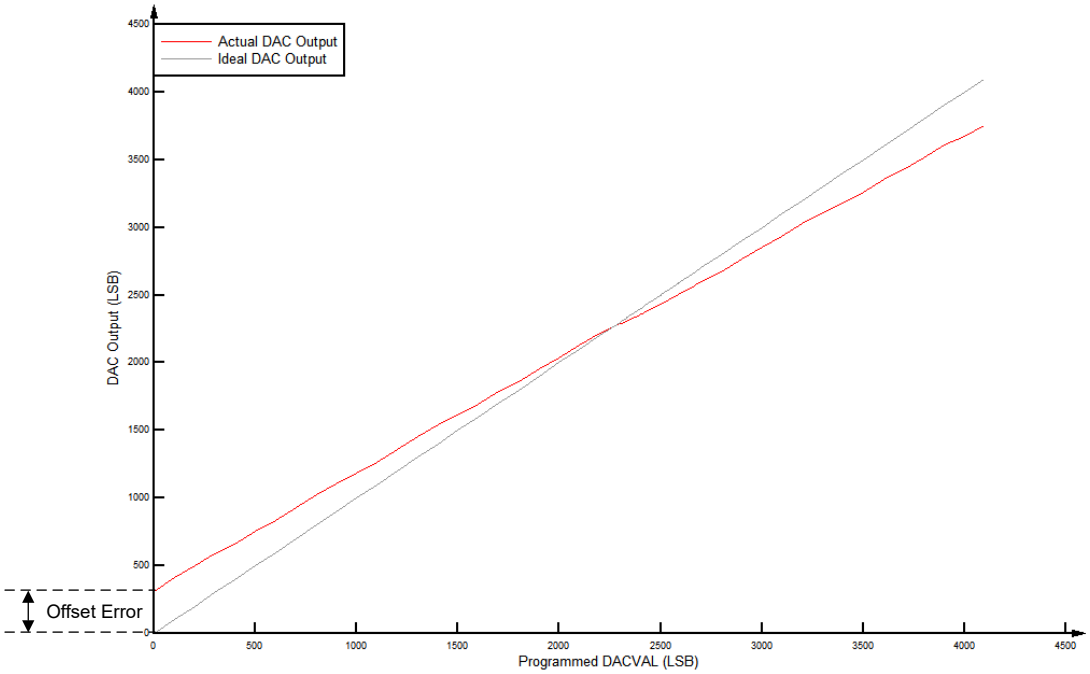


Figure 6-49. CMPSS DAC Static Offset

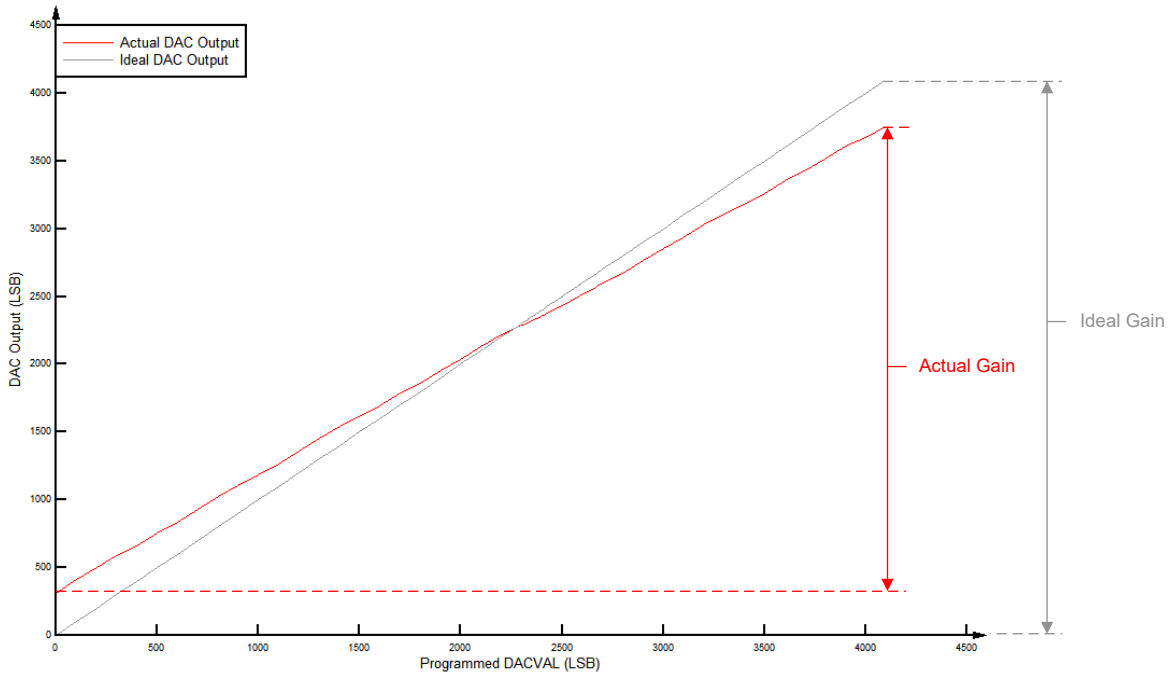


Figure 6-50. CMPSS DAC Static Gain

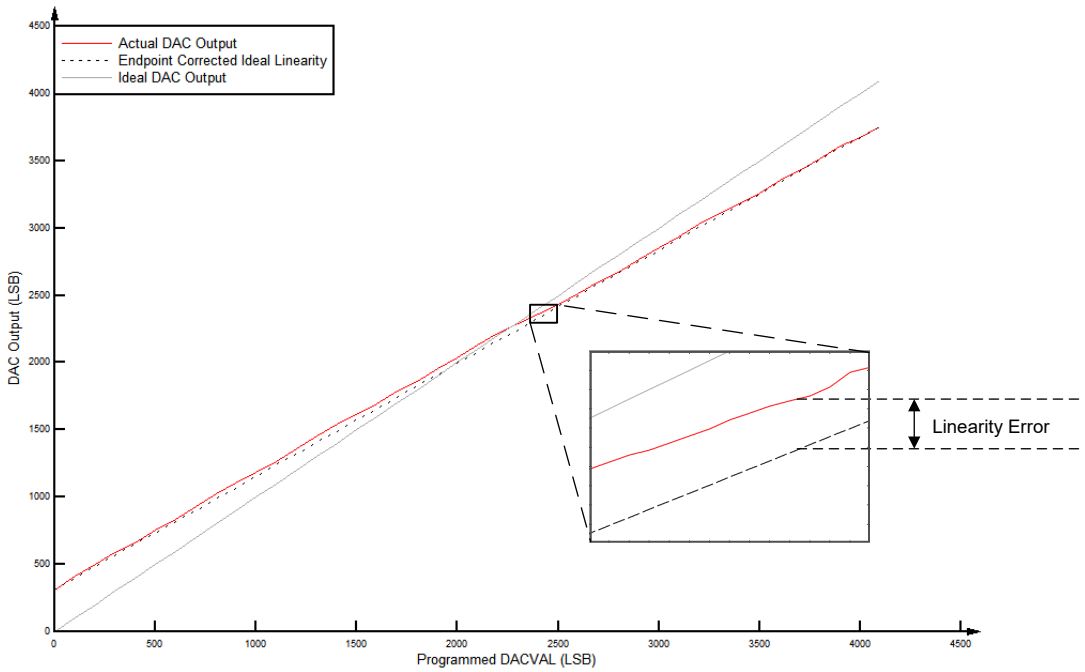


Figure 6-51. CMPSS DAC Static Linearity

ADVANCE INFORMATION

6.15.5 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that can drive an external load. For driving even higher loads than typical, a trade-off can be made between load size and output voltage swing. For the load conditions of the buffered DAC, see the *Buffered DAC Electrical Data and Timing* section. The buffered DAC is a general-purpose DAC that can be used to generate a DC voltage or AC waveforms such as sine waves, square waves, triangle waves and so forth. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCO events.

Each buffered DAC has the following features:

- 12-bit resolution
- Selectable reference voltage source
- x1 and x2 gain modes when using internal VREFHI
- Ability to synchronize with EPWMSYNCPER

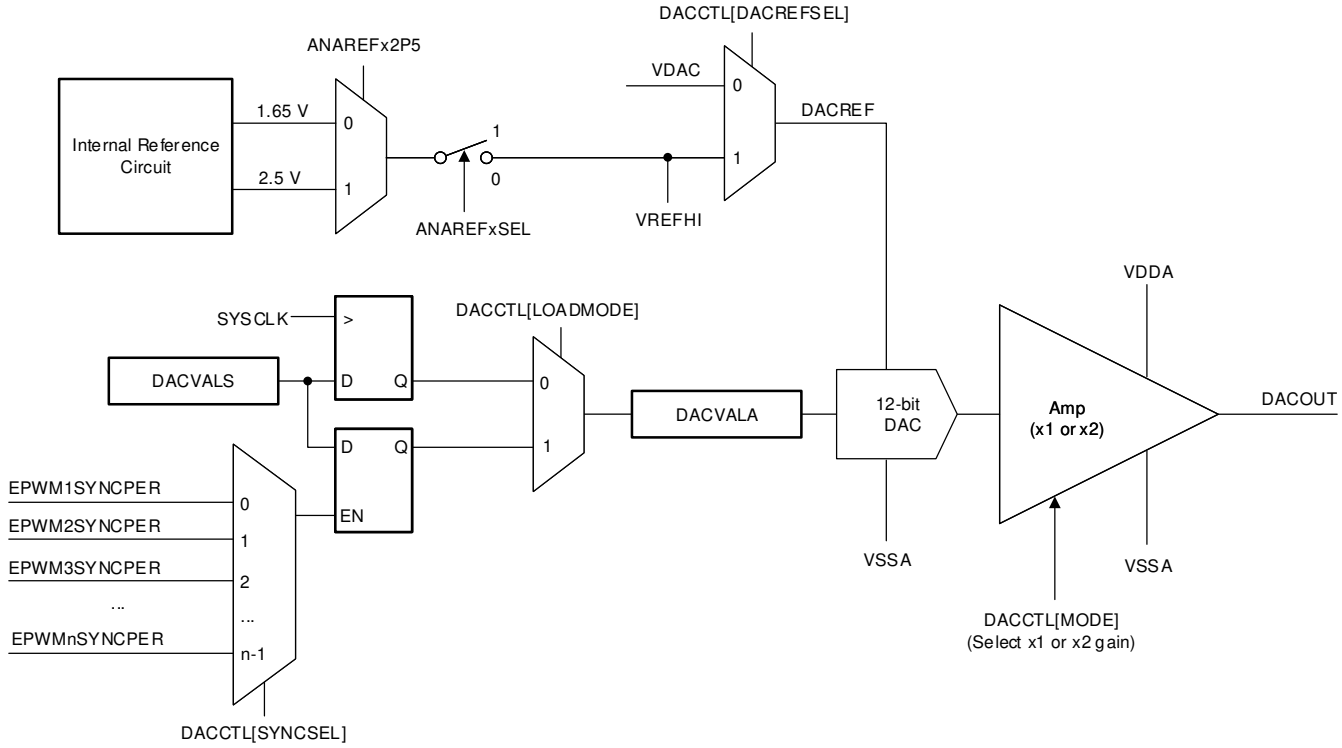


Figure 6-52. DAC Module Block Diagram

6.15.5.1 Buffered DAC Electrical Data and Timing

6.15.5.1.1 Buffered DAC Operating Conditions

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Resistive Load(2)		5			kΩ
C_L	Capacitive Load				100	pF
V_{OUT}	Valid Output Voltage Range(3)	R_L = 5 kΩ	0.3		VDDA – 0.3	V
		R_L = 1 kΩ	0.6		VDDA – 0.6	V
Reference Voltage(4)		VDAC or VREFHI	2.4	2.5 or 3.0	VDDA	V

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
(3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(4) For best PSRR performance, VDAC or VREFHI should be less than VDDA.

6.15.5.1.2 Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Resolution				12		bits
Load Regulation			–1		1	mV/V
Glitch Energy				1.5		V-ns
Voltage Output Settling Time Full-Scale		Settling to 2 LSBs after 0.3V-to-3V transition			2	µs
Voltage Output Settling Time 1/4th Full-Scale		Settling to 2 LSBs after 0.3V-to-0.75V transition			1.6	µs
Voltage Output Slew Rate		Slew rate from 0.3V-to-3V transition	2.8		4.5	V/µs
Load Transient Settling Time		5-kΩ Load			328	ns
		1-kΩ Load			557	ns
Reference Input Resistance(2)		VDAC or VREFHI	160	200	240	kΩ
TPU	Power Up Time	External Reference mode			500	µs
		Internal Reference mode			5000	µs
DC Characteristics						
Offset	Offset Error	Midpoint	–10		10	mV
Gain	Gain Error(3)		–2.5		2.5	% of FSR
DNL	Differential Non Linearity(4)	Endpoint corrected	–1	±0.4	1	LSB
INL	Integral Non Linearity	Endpoint corrected	–5	±2	5	LSB
AC Characteristics						
Output Noise		Integrated noise from 100 Hz to 100 kHz		600		µVrms
		Noise density at 10 kHz		800		nVrms/√Hz
SNR	Signal to Noise Ratio	1 kHz, 200 KSPS		64		dB
THD	Total Harmonic Distortion	1 kHz, 200 KSPS		–64.2		dB
SFDR	Spurious Free Dynamic Range	1 kHz, 200 KSPS		66		dB
SINAD	Signal to Noise and Distortion Ratio	1 kHz, 200 KSPS		61.7		dB

ADVANCE INFORMATION

6.15.5.1.2 Buffered DAC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power Supply Rejection Ratio(5)	DC		70		dB
		100 kHz		30		dB

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) Per active Buffered DAC module.
(3) Gain error is calculated for linear output range.
(4) The DAC output is monotonic.
(5) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.

ADVANCE INFORMATION

6.16 C29x Control Peripherals

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

6.16.1 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this section include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

6.16.1.1 eCAP Block Diagram

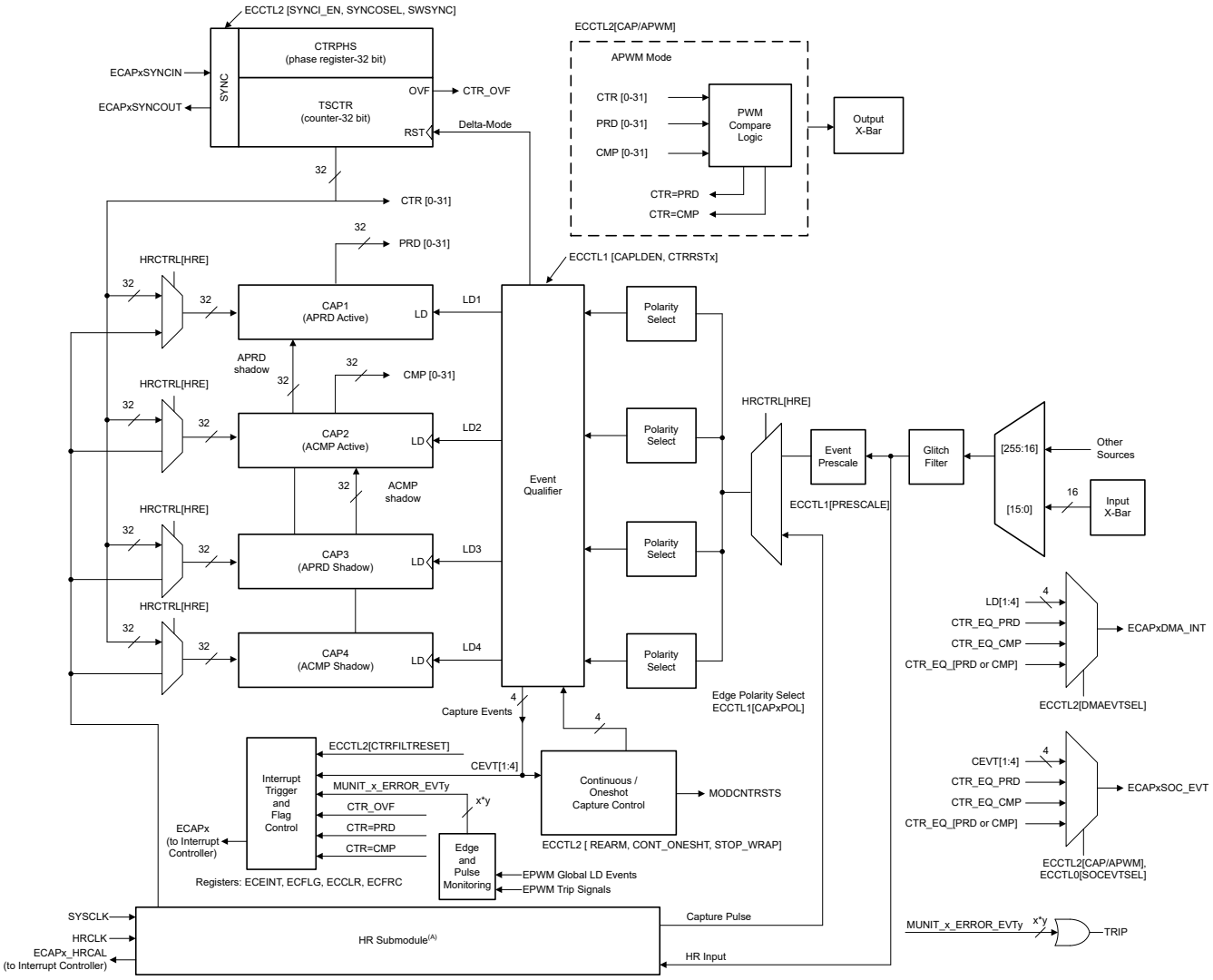


Figure 6-53. eCAP Block Diagram

6.16.1.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-54.

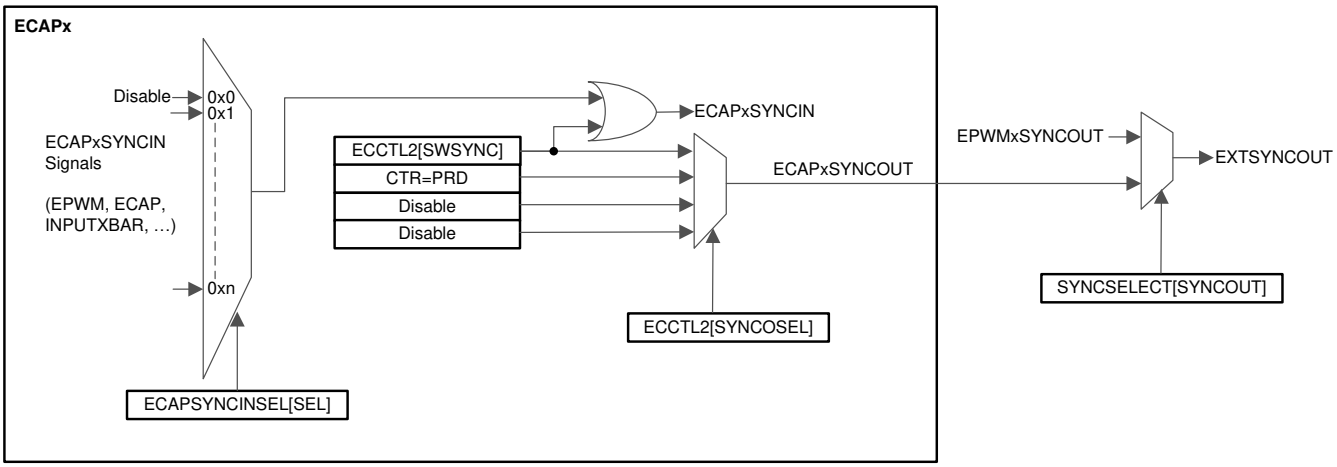


Figure 6-54. eCAP Synchronization Scheme

6.16.1.3 eCAP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.16.1.3.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w\_(IQSW)}$			

6.16.1.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

ADVANCE INFORMATION

6.16.2 High-Resolution Capture (HRCAP)

The eCAP3 module can be configured as high-resolution capture (HRCAP) submodules. The HRCAP submodule measures the difference, in time, between pulses asynchronously to the system clock. This submodule is new to the eCAP Type 1 module, and features many enhancements over the Type 0 HRCAP module.

Applications for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty-cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning
- Flow measurements

The HRCAP submodule includes the following features:

- Pulse-width capture in either non-high-resolution or high-resolution modes
- Absolute mode pulse-width capture
- Continuous or "one-shot" capture
- Capture on either falling or rising edge
- Continuous mode capture of pulse widths in 4-deep buffer
- Hardware calibration logic for precision high-resolution capture
- All of the resources in this list are available on any pin using the Input X-BAR.

The HRCAP submodule includes one high-resolution capture channel in addition to a calibration block. The calibration block allows the HRCAP submodule to be continually recalibrated, at a set interval, with no “down time”. Because the HRCAP submodule now uses the same hardware as its respective eCAP, if the HRCAP is used, the corresponding eCAP will be unavailable.

Each high-resolution-capable channel has the following independent key resources.

- All hardware of the respective eCAP
- High-resolution calibration logic
- Dedicated calibration interrupt

6.16.2.1 eCAP and HRCAP Block Diagram

For the HRCAP Block Diagram, see the eCAP and HRCAP Block Diagram in the *Enhanced Capture (eCAP)* section.

6.16.2.2 HRCAP Electrical Data and Timing

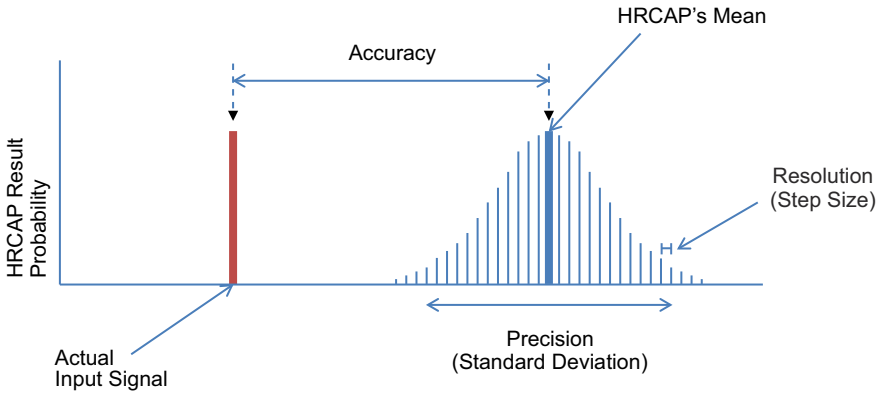
6.16.2.2.1 HRCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input pulse width		110			ns
Accuracy(1) (2) (3) (4)	Measurement length ≤ 5 µs		±390	540	ps
	Measurement length > 5 µs		±450	1450	ps
Standard deviation			See HRCAP Standard Deviation Characteristics figure		
Resolution			300		ps

(1) Value obtained using an oscillator of 100 PPM, oscillator accuracy directly affects the HRCAP accuracy.
(2) Measurement is completed using rising-rising or falling-falling edges
(3) Opposite polarity edges will have an additional inaccuracy due to the difference between V_{IH} and V_{IL}. This effect is dependent on the signal's slew rate.
(4) Accuracy only applies to time-converted measurements.

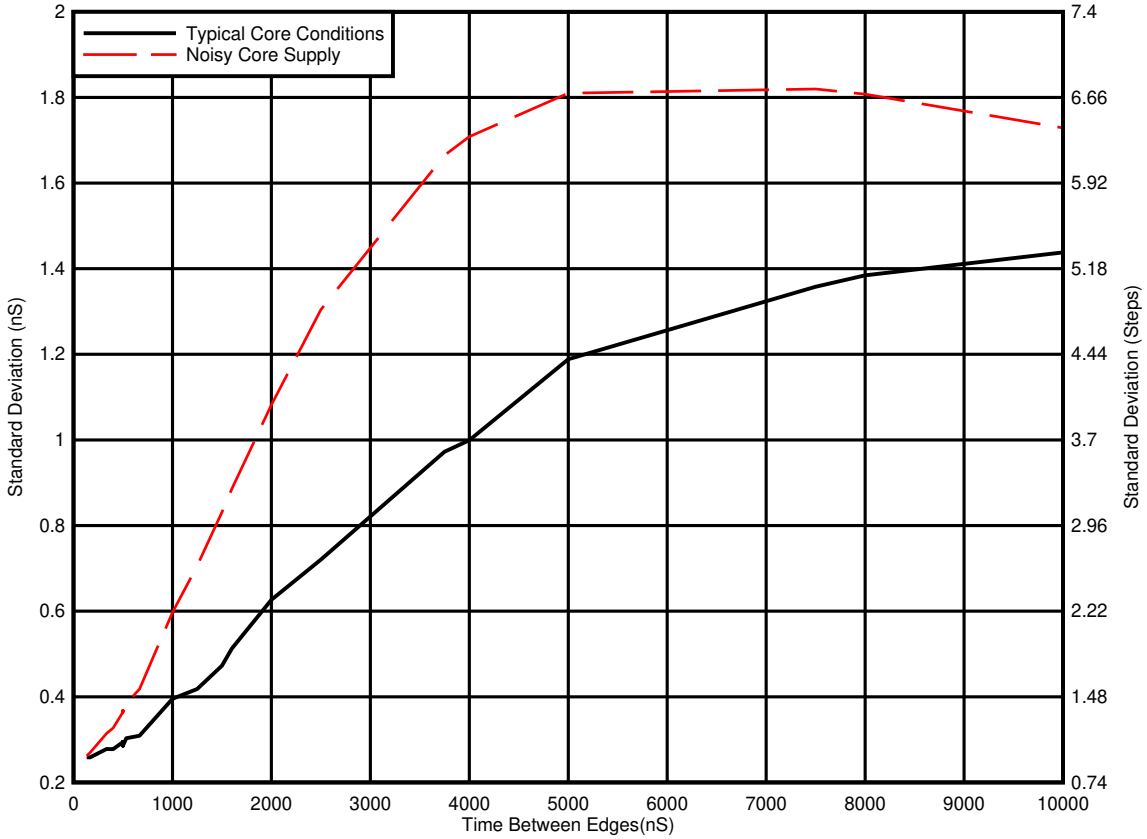
6.16.2.2.2 HRCAP Figure and Graph



A. The HRCAP has some variation in performance, this results in a probability distribution which is described using the following terms:
- Accuracy: The time difference between the input signal and the mean of the HRCAP's distribution.
- Precision: The width of the HRCAP's distribution, this is given as a standard deviation.
- Resolution: The minimum measurable increment.

Figure 6-55. HRCAP Accuracy Precision and Resolution

ADVANCE INFORMATION



A. Typical core conditions: All peripheral clocks are enabled.
B. Noisy core supply: All core clocks are enabled and disabled with a regular period during the measurement.
C. Fluctuations in current and voltage on the 1.2-V rail cause the standard deviation of the HRCAP to rise. Care should be taken to ensure that the 1.2-V supply is clean, and that noisy internal events, such as enabling and disabling clock trees, have been minimized while using the HRCAP.

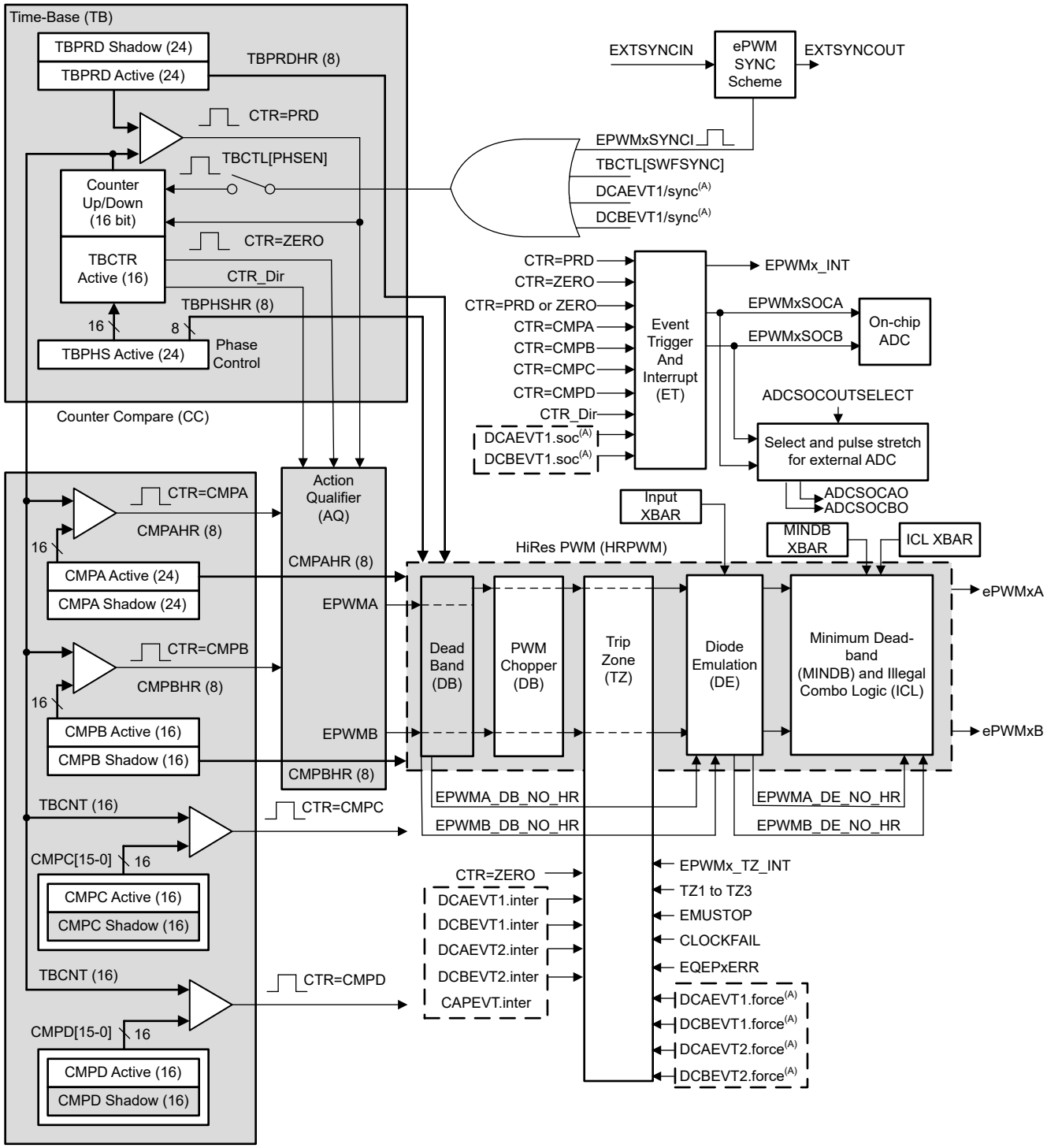
Figure 6-56. HRCAP Standard Deviation Characteristics

6.16.3 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities. ePWM type-5 enhancements include expansion of sync chain options, link and global load pulse selection flexibility, XCMP complex waveform generation, event capture capability, addition of diode emulation submodule and minimum dead-band and illegal combo logic submodule, and event trigger submodule enhancements to allow for unevenly spaced over-sampling of ePWM period.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-57 shows the ePWM module. Figure 6-58 shows the ePWM trip input connectivity.



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-57. ePWM Submodules and Critical Internal Signal Interconnects

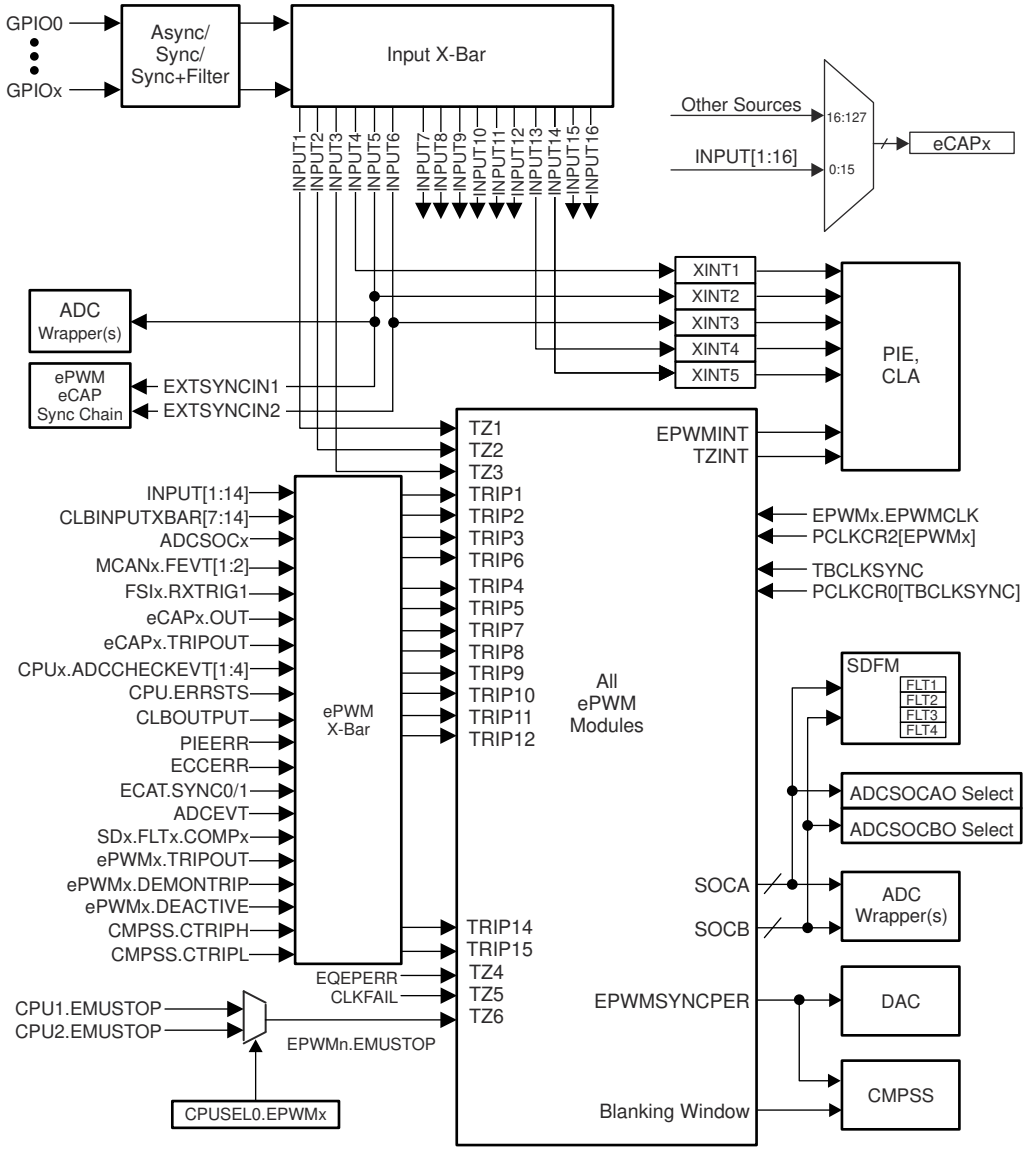


Figure 6-58. ePWM Trip Input Connectivity

ADVANCE INFORMATION

6.16.3.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Figure 6-59 shows the synchronization scheme.

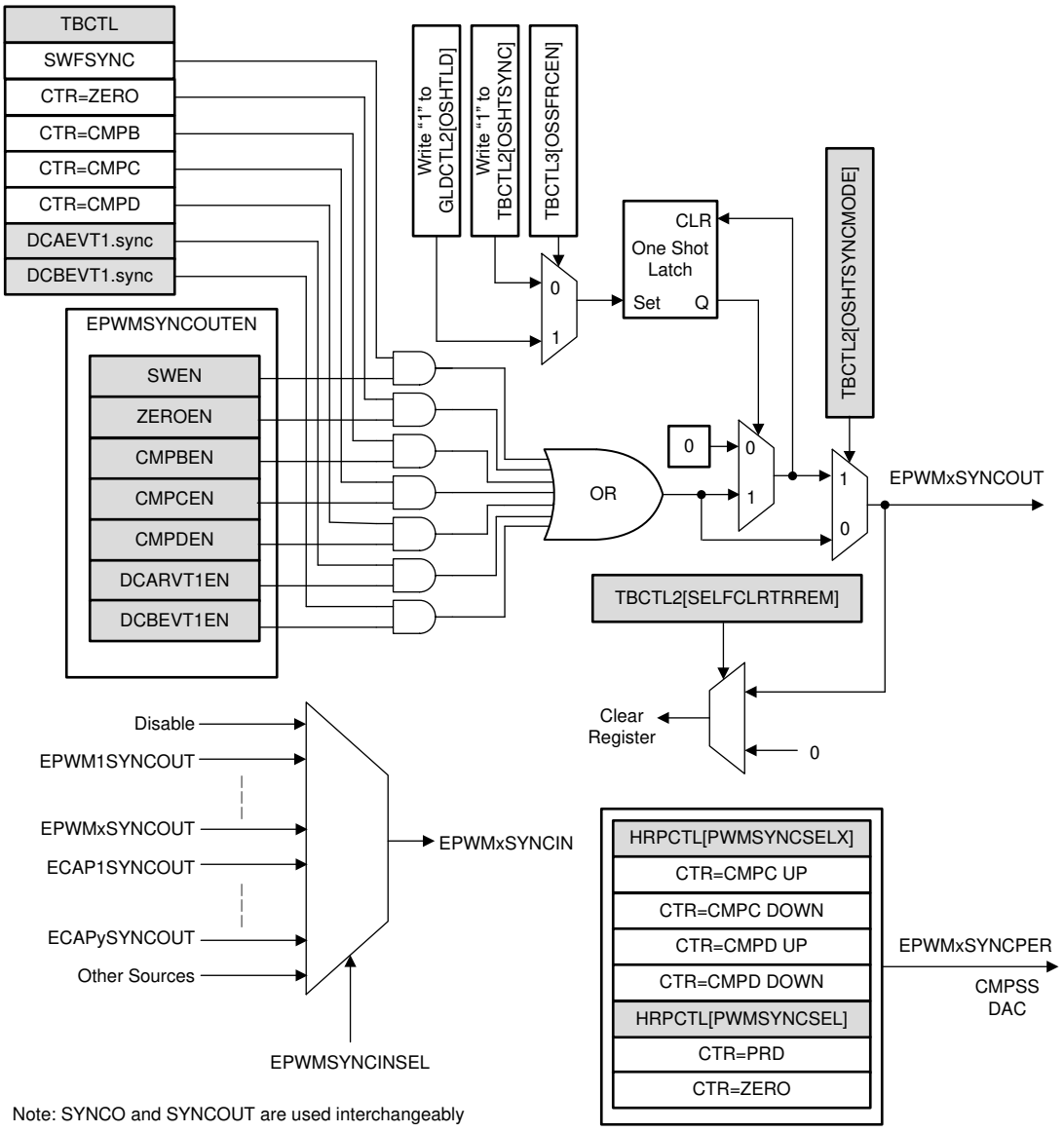


Figure 6-59. Synchronization Chain Architecture

6.16.3.2 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.16.3.2.1 ePWM Timing Requirements

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.16.3.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

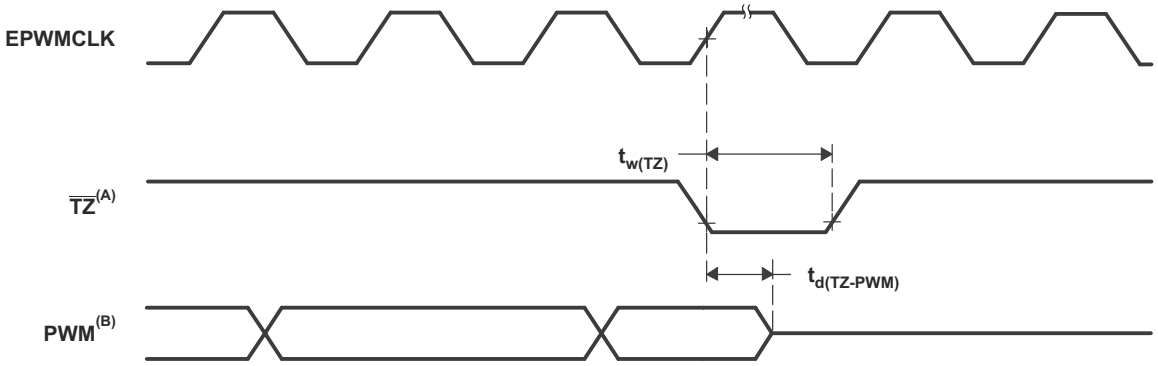
PARAMETER[1]		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		30	ns
tskew	Skew of all ePWM outputs (Shortest Path)[2]		5.1	ns
tskew	Skew of all ePWM outputs (Longest Path)[2]		8.9	ns
tskew	Skew of all ePWM outputs through HRPWM (Shortest Path)[2]		5.1	ns
tskew	Skew of all ePWM outputs through HRPWM (Longest Path)[2]		8.9	ns

(1) 20-pF load on pin.
(2) The EPWMs have a similar configuration.

6.16.3.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.16.3.2.3.1 PWM Hi-Z Characteristics Timing Diagram



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12
B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-60. PWM Hi-Z Characteristics

ADVANCE INFORMATION

6.16.4 External ADC Start-of-Conversion Electrical Data and Timing

6.16.4.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(SYSCLK)}$		cycles

6.16.4.2 $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing Diagram

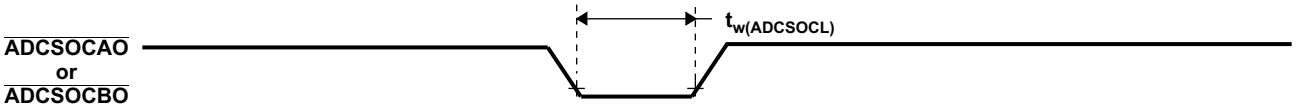


Figure 6-61. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

ADVANCE INFORMATION

6.16.5 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.16.5.1 HRPWM Electrical Data and Timing

6.16.5.1.1 High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)	43	100	152	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

ADVANCE INFORMATION

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6.16.6 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-62):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

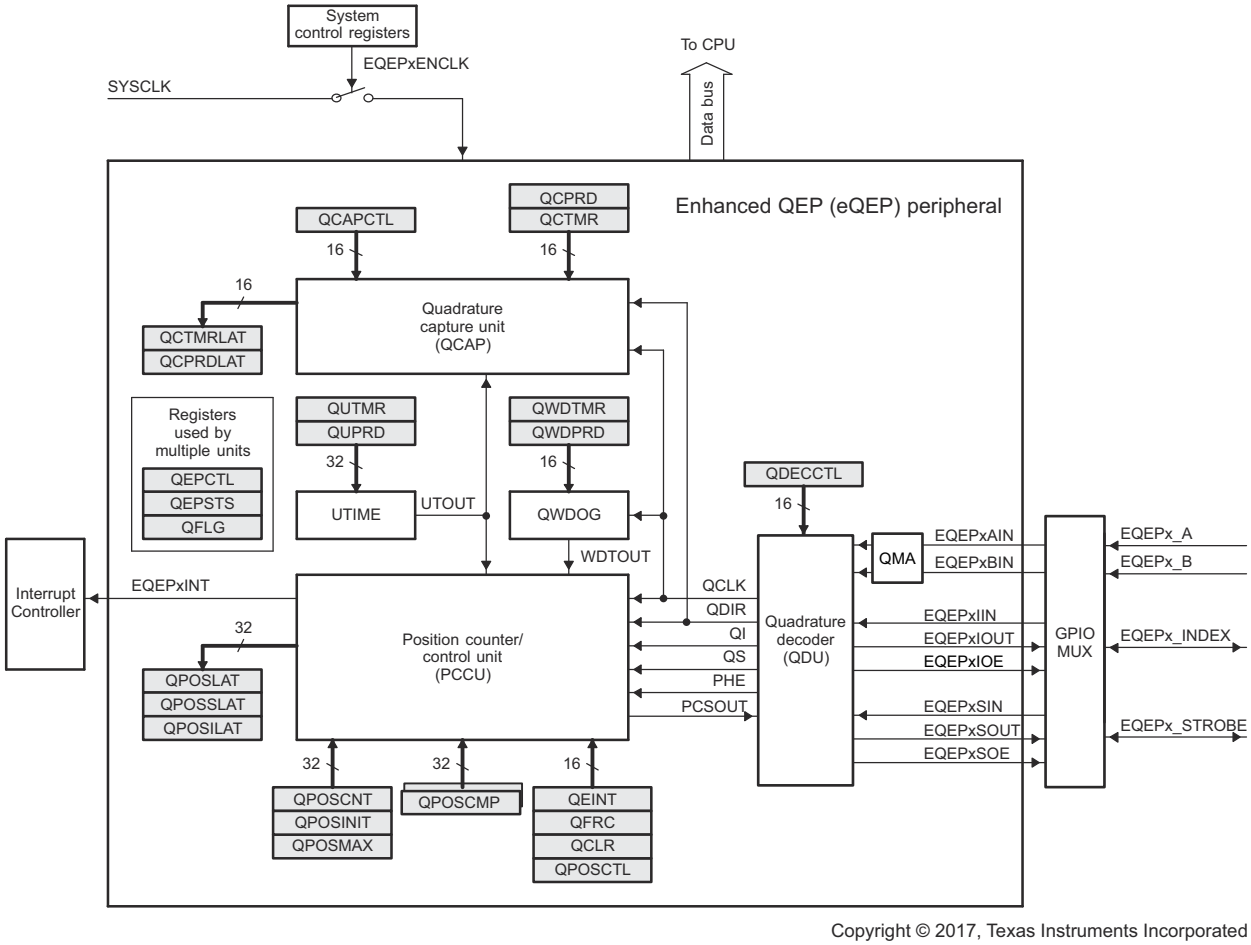


Figure 6-62. eQEP Block Diagram

6.16.6.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.16.6.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(QEPP)}$	QEP input period	Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.16.6.1.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

ADVANCE INFORMATION

6.16.7 Sigma-Delta Filter Module (SDFM)

SDFM features include:

- Eight external pins per SDFM module
  - Four sigma-delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Different configurable modulator clock modes supported:
  - Mode 0: Modulator clock rate equals the modulator data rate.
- Four independent, configurable secondary filter (comparator) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - Ability to detect over-value condition, under-value condition, and Threshold-crossing conditions
    1. Two independent Higher Threshold comparators (used to detect over-value condition)
    2. Two independent Lower Threshold comparators (used to detect under-value condition)
    3. One independent Threshold-Crossing comparator (used to measure duty cycle/frequency with eCAP)
  - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- Four independent configurable primary filter (data filter) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - OSR value for data filter unit (DOSR) programmable from 1 to 256
  - Ability to enable or disable (or both) individual filter module
  - Ability to synchronize all four independent filters of an SDFM module by using the Main Filter Enable (MFE) bit or by using PWM signals
- Data filter output can be represented in either 16 bits or 32 bits.
- Data filter unit has a programmable mode FIFO to reduce interrupt overhead. The FIFO has the following features:
  - The primary filter (data filter) has a 16-deep x 32-bit FIFO.
  - The FIFO can interrupt the CPU after programmable number of data-ready events.
  - FIFO Wait-for-Sync feature: Ability to ignore data-ready events until the PWM synchronization signal (SDSYNC) is received. Once the SDSYNC event is received, the FIFO is populated on every data-ready event.
  - Data filter output can be represented in either 16 bits or 32 bits.
- PWMx.SOCA/SOCB can be configured to serve as SDSYNC source on a per-data-filter-channel basis.
- PWMs can be used to generate a modulator clock for sigma-delta modulators.
- Configurable Input Qualification available for both SD-Cx and SD-Dx
- Ability to use one filter channel clock (SD-C1) to provide clock to other filter clock channels.
- Configurable digital filter available on comparator filter events to blank out comparator events caused by spurious noise

Figure 6-63 shows the SDFM module block diagram.

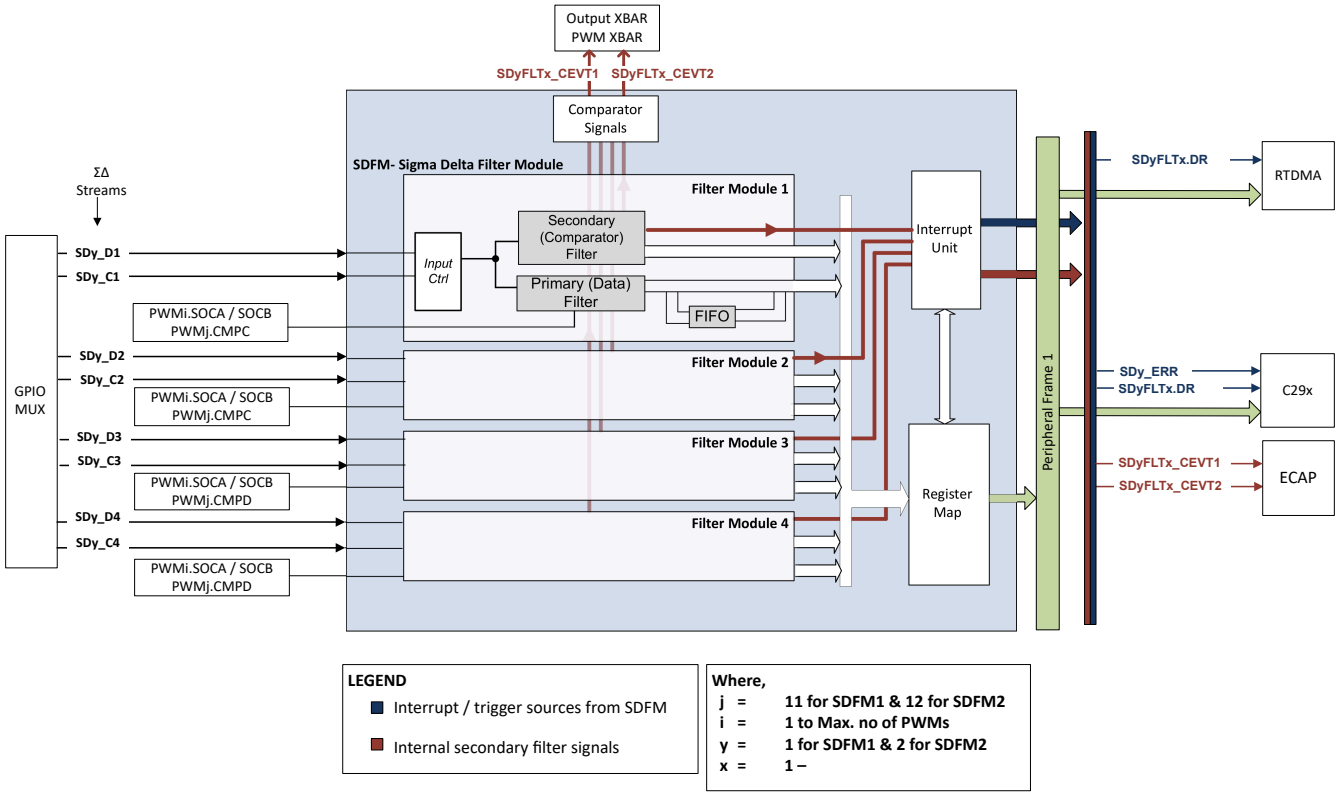


Figure 6-63. Sigma Delta Filter Module (SDFM) Block Diagram

ADVANCE INFORMATION

6.16.7.1 SDFM Electrical Data and Timing

6.16.7.1.1 SDFM Electrical Data and Timing (Synchronized GPIO)

Note

The SDFM Synchronized GPIO (SYNC) option provides protection against SDFM module corruption due to occasional random noise glitches on the SDx_Cy pin that may result in a false comparator trip and filter output.

The SDFM Synchronized GPIO (SYNC) mode does not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

6.16.7.1.2 SDFM Electrical Data and Timing (Using ASYNC)

The *SDFM Timing Requirements When Using Asynchronous GPIO ASYNC Option* table lists the SDFM timing requirements. The following configurations should be made:

- SDFM GPIO pins should be configured in ASYNC mode only (using GPYQSELn = 0b11).
- Both SDx-Cy and SDx-Dy signals need to be synchronized to PLLRAWCLK (using SDCTLPARMx registers).

Figure 6-64 shows the SDFM timing diagram.

6.16.7.1.2.1 SDFM Timing Requirements When Using Asynchronous GPIO ASYNC Option

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	4 * $t_{c(PLLRAWCLK)}$	256 * SYSCLK period	ns
$t_{w(SDDHL)M0}$	Pulse duration, SDx_Dy (high / Low)	2 * $t_{c(PLLRAWCLK)}$		ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	1 * $t_{c(PLLRAWCLK)}$ + 3		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	1 * $t_{c(PLLRAWCLK)}$ + 3		ns

6.16.7.1.2.2 SDFM Timing Requirements When Using Synchronous GPIO SYNC Option

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	5 * SYSCLK period	256 * SYSCLK period	ns
$t_{w(SDDHL)M0}$	Pulse duration, SDx_Dy (high / Low)	2 * SYSCLK period		ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	2 * SYSCLK period		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	2 * SYSCLK period		ns

6.16.7.1.3 SDFM Timing Diagram

WARNING

Special precautions should be taken on both SD-Cx and SD-Dx signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination resistors for ringing noise due to any impedance mismatch of clock driver and spacing of traces from other noisy signals are recommended.

Note

The SDFM SD-Cx and SD-Dx signals, when synchronized to PLLRAWCLK, provide protection against SDFM module corruption due to occasional random noise glitches that may result in a false comparator trip and filter output. However, the signals do not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

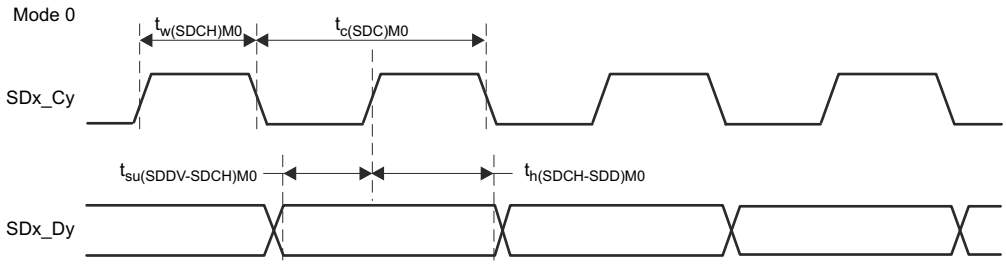


Figure 6-64. SDFM Timing Diagram – Mode 0

ADVANCE INFORMATION

6.17 C29x Communications Peripherals

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

6.17.1 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices may coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

Note

The availability of the CAN FD feature is dependent on the device's part number.

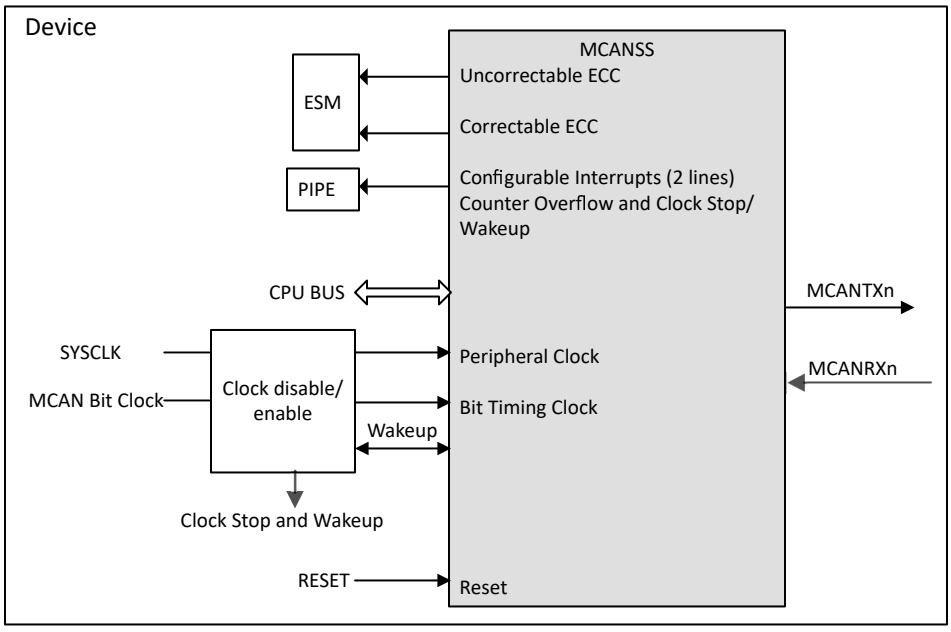


Figure 6-65. MCAN Module Overview

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Flexible Message RAM allocation (maximum configuration below is for a device with 4352 32-bit word message RAM)
  - Up to 32 dedicated transmit buffers
  - Configurable transmit FIFO, up to 32 elements
  - Configurable transmit queue, up to 32 elements
  - Configurable transmit Event FIFO, up to 32 elements
  - Up to 64 dedicated receive buffers
  - Two configurable receive FIFOs, up to 64 elements each
  - Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt (two configurable interrupt lines, correctable ECC, counter overflow and clock stop/ wakeup)
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock/host clock)
- ECC check for Message RAM
- Clock stop and wake-up support
- Timestamp counter

Non-supported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

6.17.2 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- SPI compatibility mode (limited features available)

Operating the FSI at maximum speed (60 MHz) at dual data rate (120Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The *Fast Serial Interface (FSI) Skew Compensation* Application Note provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in the *FSI Transmitter* section and the *FSI Receiver*

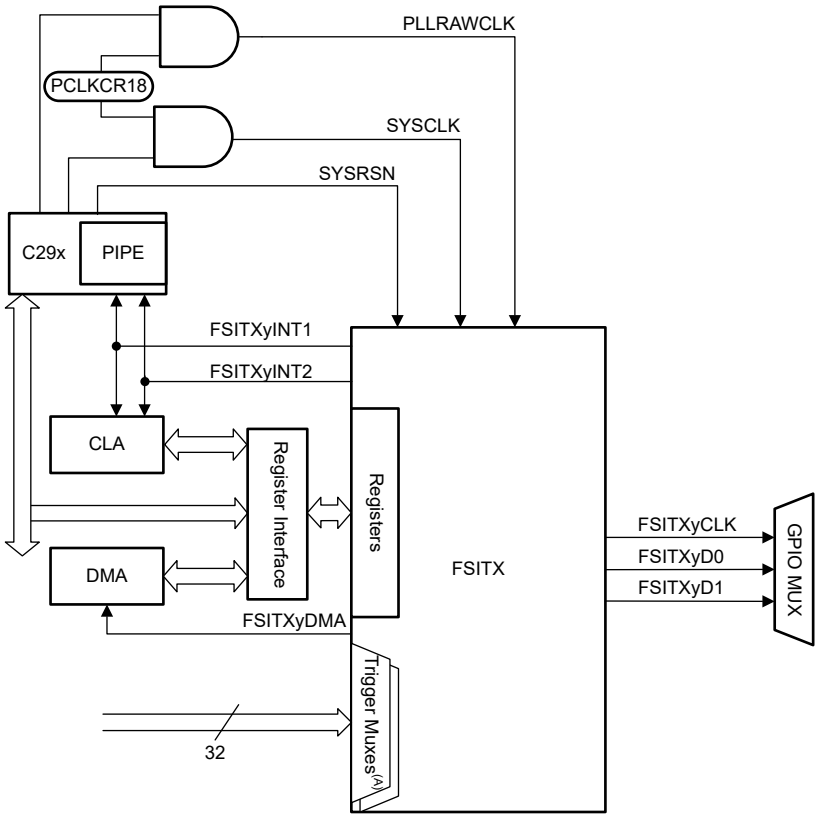
6.17.2.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support

Figure 6-66 shows the FSITX CPU interface. Figure 6-67 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.



A. The signals connected to the trigger muxes are described in the *External Frame Trigger Mux* section of the Fast Serial Interface (FSI) chapter in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

Figure 6-66. FSITX CPU Interface

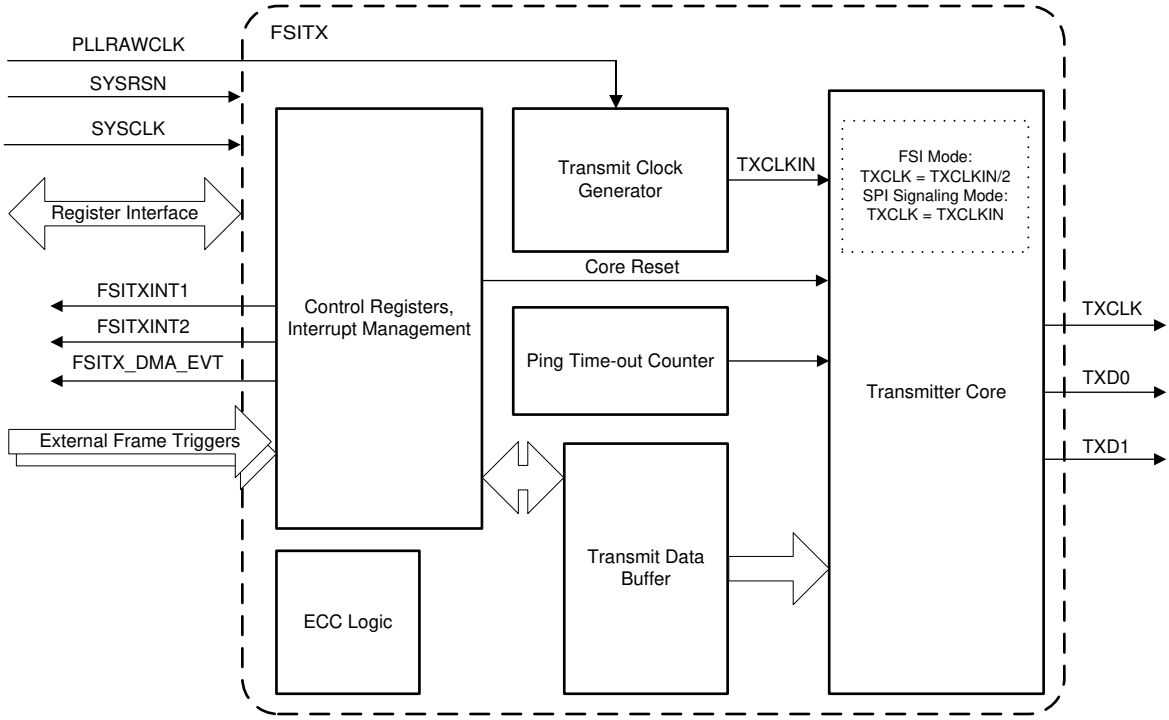


Figure 6-67. FSITX Block Diagram

6.17.2.1.1 FSITX Electrical Data and Timing

6.17.2.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER[1]		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	16.67		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) - 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLK–TXD)}$	Delay time, TXCLK rising or falling toTXD valid	$(0.25t_{c(TXCLK)}) - 2$	$(0.25t_{c(TXCLK)}) + 2$	ns
4	$t_{d(TXCLK)}$	TXCLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
5	$t_{d(TXD0)}$	TXD0 delay compensation at TX_DLYLINE_CTRL[TXD0_DLY]=31	9.95	30	ns
6	$t_{d(TXD1)}$	TXD1 delay compensation at TX_DLYLINE_CTRL[TXD1_DLY]=31	9.95	30	ns
7	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for TXCLK, TXD0, and TXD1	0.29	1	ns

(1) 10-pF load on pin.

6.17.2.1.1.2 FSITX Timings

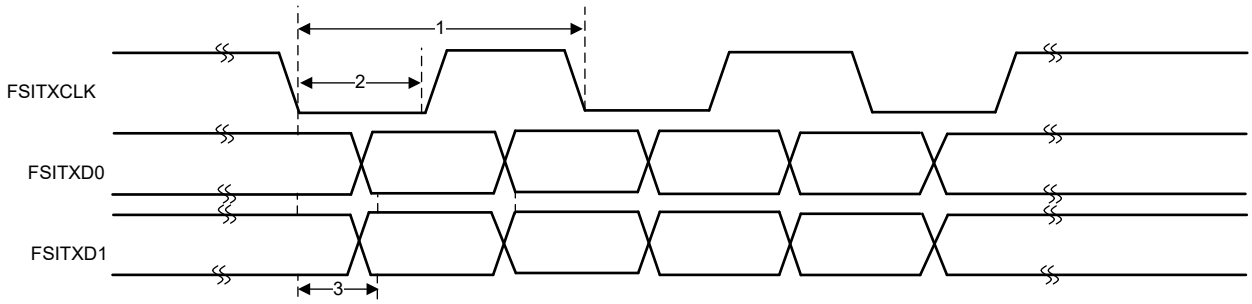


Figure 6-68. FSITX Timings

ADVANCE INFORMATION

6.17.2.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU program, control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- SPI compatibility mode

Figure 6-69 shows the FSIRX CPU interface. Figure 6-70 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

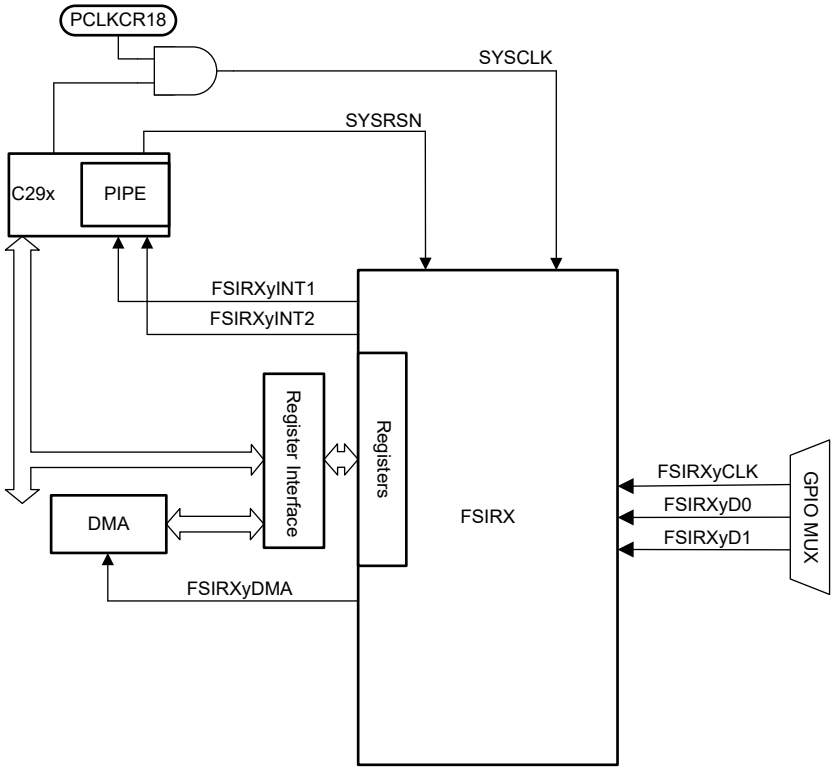


Figure 6-69. FSIRX CPU Interface

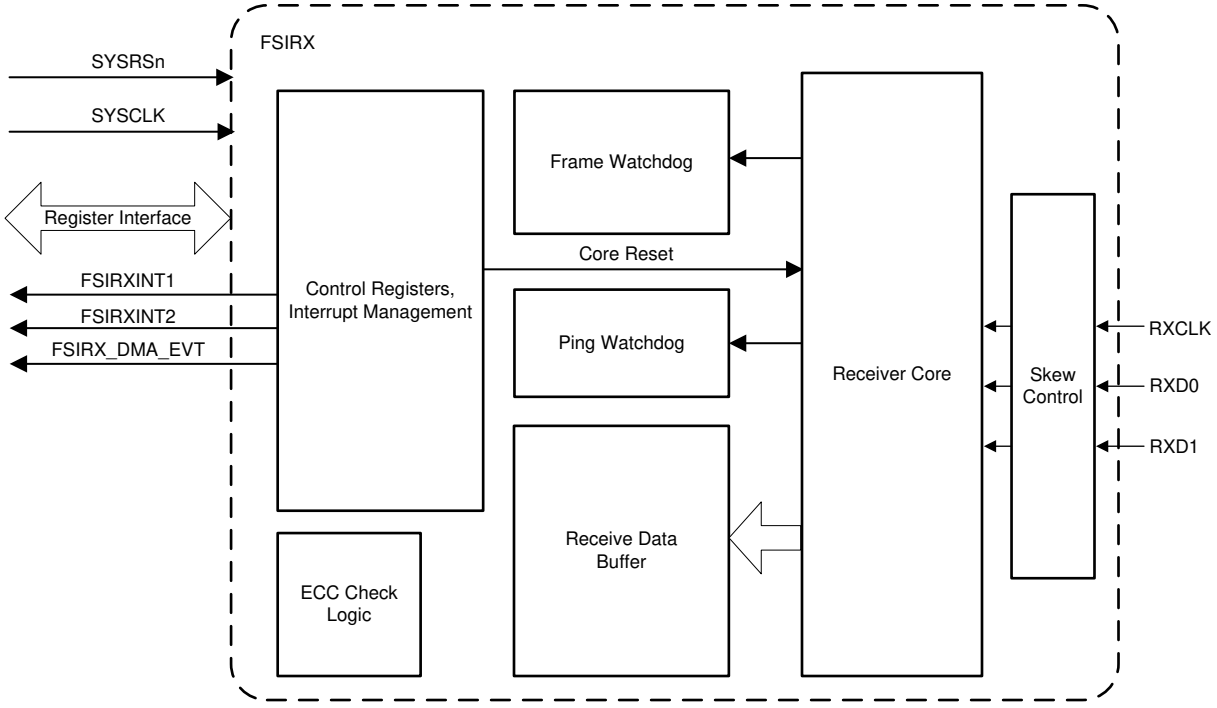


Figure 6-70. FSIRX Block Diagram

6.17.2.2.1 FSIRX Electrical Data and Timing

6.17.2.2.1.1 FSIRX Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(RXCLK)}$	Cycle time, RXCLK	19.417		ns
2	$t_{w(RXCLK)}$	Pulse width, RXCLK low or RXCLK high.	$0.35t_{c(RXCLK)}$	$0.65t_{c(RXCLK)}$	ns
3	$t_{su(RXCLK–RXD)}$	Setup time with respect to RXCLK, applies to both edges of the clock	1.7		ns
4	$t_{h(RXCLK–RXD)}$	Hold time with respect to RXCLK, applies to both edges of the clock	2		ns

6.17.2.2.1.2 FSIRX Switching Characteristics

NO.	PARAMETER(1)		MIN	MAX	UNIT
1	$t_{d(RXCLK)}$	RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	9.7	30	ns
2	$t_{d(RXD0)}$	RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31	9.7	30	ns
3	$t_{d(RXD1)}$	RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31	9.7	30	ns
4	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for RXCLK, RXD0, and RXD1	0.29	1	ns
TDM1	$t_{skew(TDM\_CLK-TDM\_Dx)}$	Delay skew introduced between RXCLK-TDM_CLK delay and RXDx-TDM_Dx delays	-3	3	ns
TDM1	$t_{d(RXCLK-TDM\_CLK)}$	Delay time, RXCLK input to TDM_CLK output	2	19.5	ns
TDM2	$t_{d(RXD0-TXD0)}$	Delay time, RXD0 input to TXD0 output	2	19.5	ns
TDM3	$t_{d(RXD1-TXD1)}$	Delay time, RXD1 input to TXD1 output	2	19.5	ns

(1) 10-pF load on pin.

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6.17.2.2.1.3 FSIRX Timings

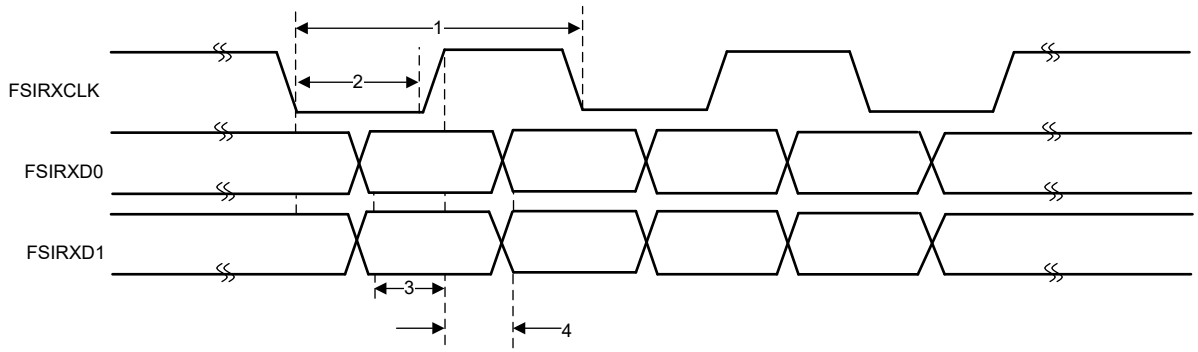

Figure 6-71. FSIRX Timings

6.17.2.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI peripheral configuration because the FSI TXCLK cannot take an external clock source.

6.17.2.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in the *FSIRX Timing Requirements* table are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

6.17.2.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER(1)		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	19.417		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) - 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLKH–TXD0)}$	Delay time, TXD0 valid after TXCLK high		3	ns
4	$t_{d(TXD1-TXCLK)}$	Delay time, TXCLK high after TXD1 low	$t_{w(TXCLK)} - 3$		ns
5	$t_{d(TXCLK-TXD1)}$	Delay time, TXD1 high after TXCLK low	$t_{w(TXCLK)}$		ns

(1) 10-pF load on pin

6.17.2.3.1.2 FSITX SPI Signaling Mode Timings

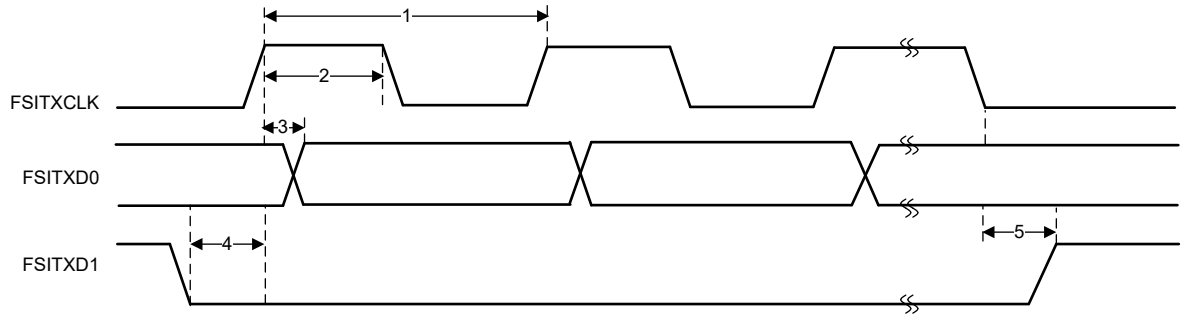

Figure 6-72. FSITX SPI Signaling Mode Timings

ADVANCE INFORMATION

6.17.3 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I^2C-bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple controller-transmitters and target-receivers
  - Support for multiple target-transmitters and controller-receivers
  - Combined controller transmit/receive and receive/transmit mode
  - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two interrupts
  - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
    - Transmit Ready
    - Receive Ready
    - Register-Access Ready
    - No-Acknowledgment
    - Arbitration-Lost
    - Stop Condition Detected
    - Addressed-as-Target
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-73 shows how the I2C peripheral module interfaces within the device.

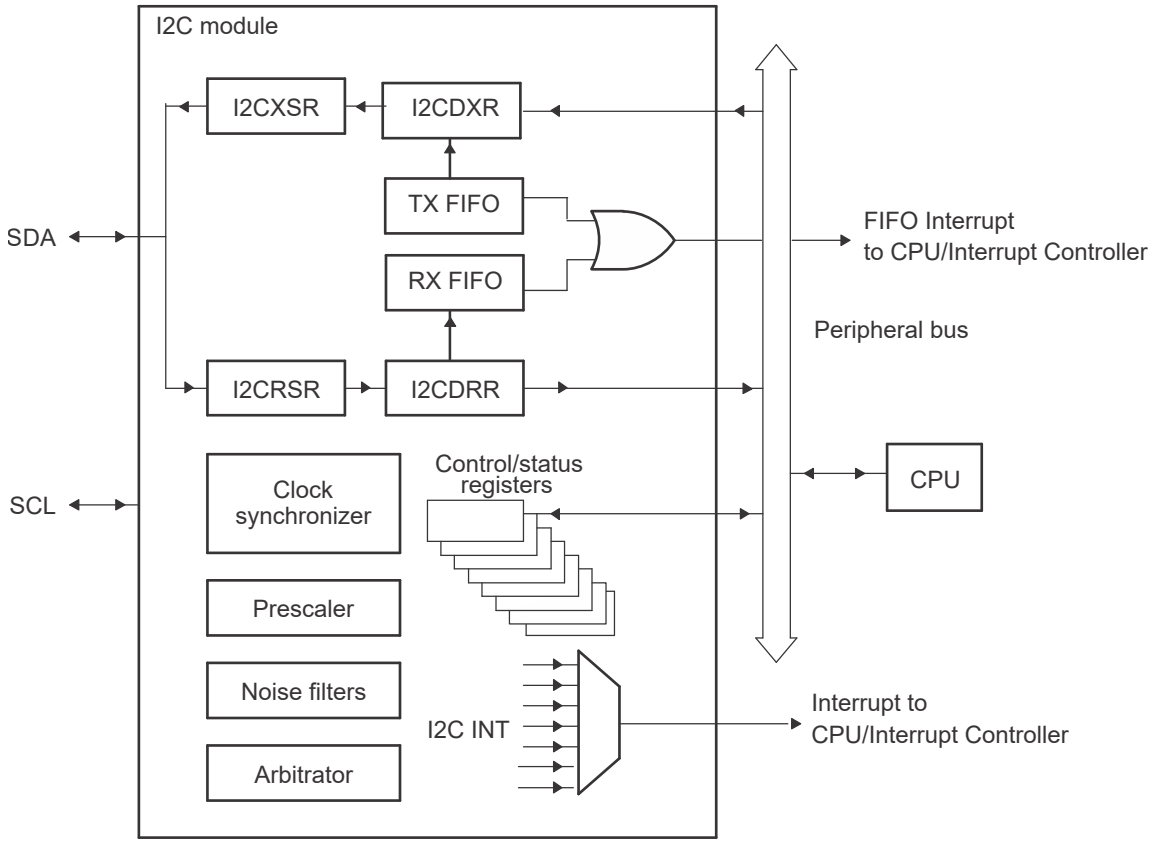

Figure 6-73. I2C Peripheral Module Interfaces

ADVANCE INFORMATION

6.17.3.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the *I2C Bus Pullup Resistor Calculation* Application Note.

6.17.3.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.0		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

ADVANCE INFORMATION

6.17.3.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA

6.17.3.1.3 I2C Timing Diagram

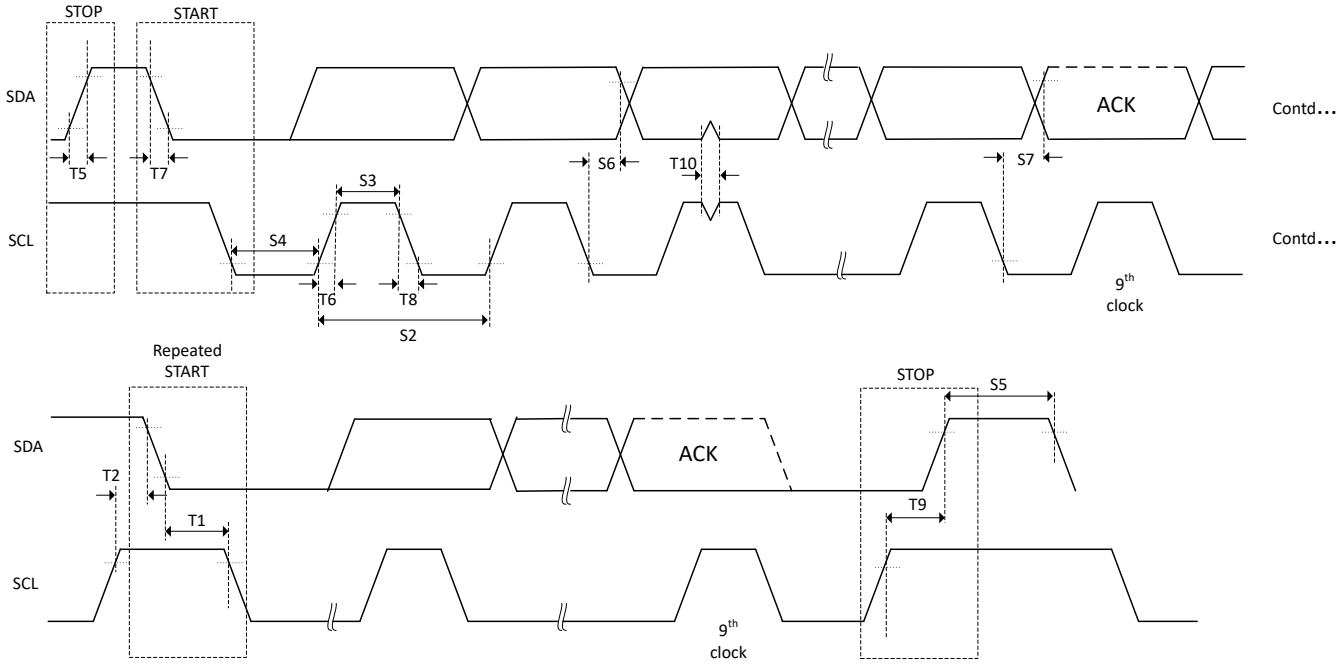

Figure 6-74. I2C Timing Diagram

ADVANCE INFORMATION

6.17.4 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Supports voltage thresholds compatible to:
  - PMBus and below
  - SMBus and below
- Support for controller and target
- Support for I2C mode
- Support for speeds:
  - Standard Mode: Up to 100 kHz
  - Fast Mode: 400 kHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
  - Receive data ready
  - Transmit buffer empty
  - Target address received
  - End of message
  - ALERT input asserted
  - Clock low time-out
  - Clock high time-out
  - Bus free

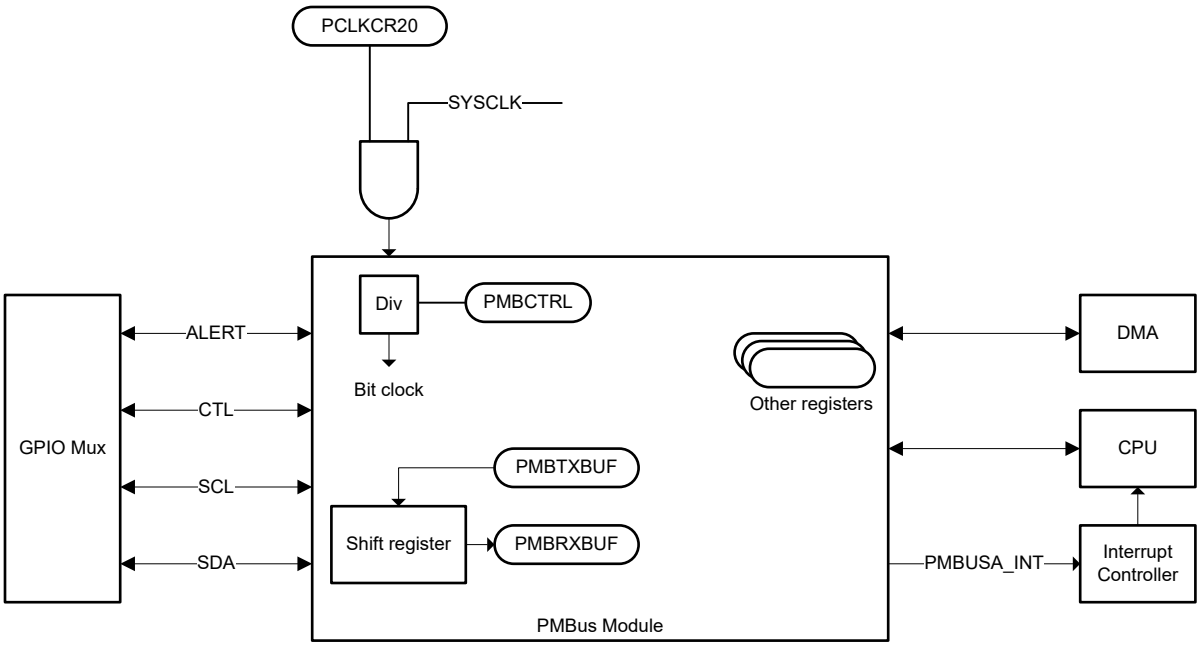

Figure 6-75. PMBus Block Diagram

6.17.4.1 PMBus Electrical Data and Timing

6.17.4.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Valid low-level input voltage				0.8	V
V_{IH}	Valid high-level input voltage		2.1		VDDIO	V
V_{OL}	Low-level output voltage	At I_{pullup} = 4 mA			0.4	V
I_{OL}	Low-level output current	V_{OL} ≤ 0.4 V	4			mA
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0		50	ns
I_i	Input leakage current on each pin	0.1 Vbus < Vi < 0.9 Vbus	–10		10	µA
C_i	Capacitance on each pin				10	pF

6.17.4.1.2 PMBus Fast Plus Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{mod}	PMBus Module Clock Frequency(2)		20		25	MHz
f_{SCL}	SCL clock frequency	3.3V Nominal Bus Voltage	10		1000(3)	kHz
		5.0V Nominal Bus Voltage	10		1000(4)	kHz
t_{BUF}	Bus free time between STOP and START conditions		0.5			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		0.26			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		0.26			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		0.26			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
	Data hold time after SCL fall PMBCTRL_ZH_EN = 1 (1)		0			ns
$t_{SU;DAT}$	Data setup time before SCL rise		50			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		0.5			µs
t_{HIGH}	High period of the SCL clock		0.26		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (target device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (controller device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL	5% to 95%	20		120	ns
t_f	Fall time of SDA and SCL	95% to 5%	20		120	ns

(1) This bit must be set to enable 0ns hold time/SMBUS3.0 Compliance
(2) If the max clock is used all below timings will be met with the default register configurations for the PMBUS
(3) Due to max IO drive strength of 12mA, 1MHz SCL clock is only valid for bus capacitances up to 520pF
(4) Due to max IO drive strength of 12mA, 1MHz SCL clock is only valid for bus capacitances up to 330pF

ADVANCE INFORMATION

6.17.4.1.3 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{mod}	PMBus Module Clock Frequency (2)		$f_{(SYSCLK)}$ / 32		10	MHz
f_{SCL}	SCL clock frequency		10		400	kHz
t_{BUF}	Bus free time between STOP and START conditions		1.3			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		0.6			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		0.6			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		0.6			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
	Data hold time after SCL fall PMBCTRL_INC_1[ZH+EN] = 1 (1)		0			ns
$t_{SU;DAT}$	Data setup time before SCL rise		100			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		1.3			µs
t_{HIGH}	High period of the SCL clock		0.6		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (target device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (controller device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL	5% to 95%	20		300	ns
t_f	Fall time of SDA and SCL	95% to 5%	20		300	ns

(1) This bit must be set to enable 0ns hold time/SMBUS3.0 Compliance
(2) If the max clock is used all below timings will be met with the default register configurations for the PMBUS

6.17.4.1.4 PMBus Standard Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{mod}	PMBus Module Clock Frequency(2)		$f_{(SYSCLK)}$ / 32		10	MHz
f_{SCL}	SCL clock frequency		10		100	kHz
t_{BUF}	Bus free time between STOP and START conditions		4.7			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		4			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		4.7			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		4			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
	Data hold time after SCL fall PMBCTRL_INC_1[ZH+EN] = 1 (1)		0			ns
$t_{SU;DAT}$	Data setup time before SCL rise		250			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		4.7			µs
t_{HIGH}	High period of the SCL clock		4		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (target device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (controller device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL				1000	ns
t_f	Fall time of SDA and SCL				300	ns

(1) This bit must be set to enable 0ns hold time/SMBUS3.0 Compliance
(2) If the max clock is used all below timings will be met with the default register configurations for the PMBUS

ADVANCE INFORMATION

6.17.5 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the controller or peripheral operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPIPOCI: SPI peripheral-output/controller-input pin
- SPIPICO: SPI peripheral-input/controller-output pin
- $\overline{\text{SPIPTE}}$: SPI peripheral transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Controller and Peripheral
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPIPTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-76 shows the SPI CPU interfaces.

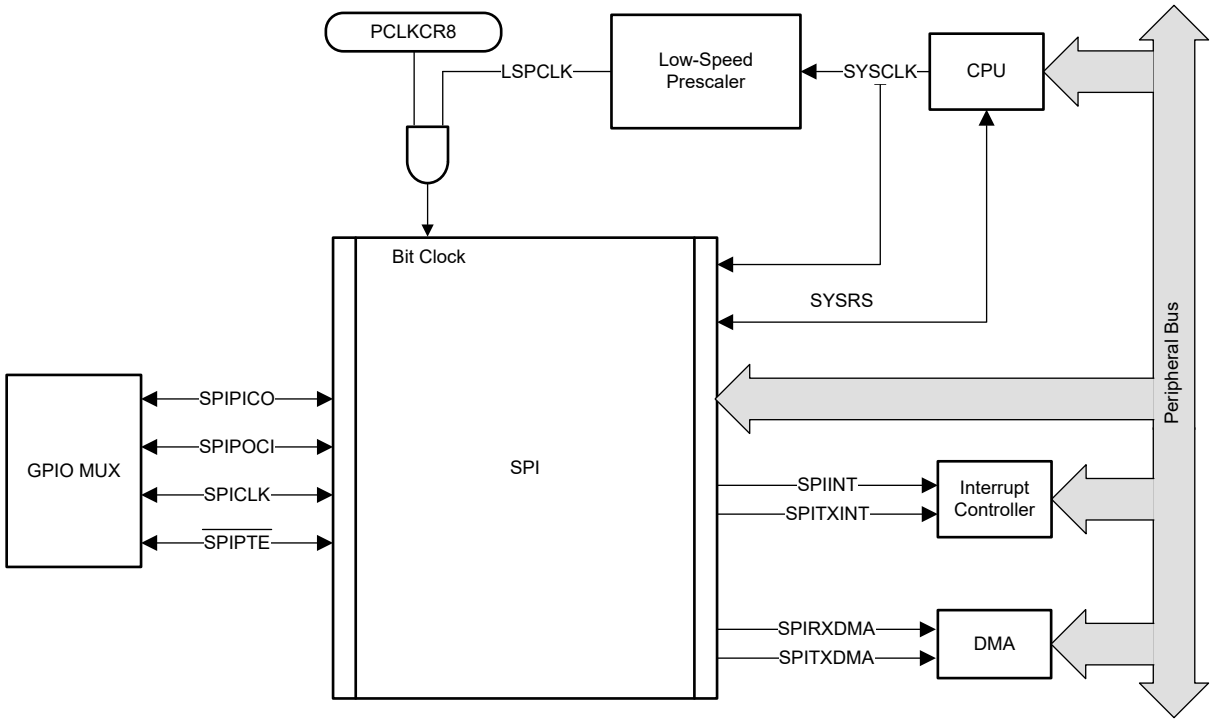

Figure 6-76. SPI CPU Interface

ADVANCE INFORMATION

6.17.5.1 SPI Controller Mode Timings

The following sections contain the SPI Controller Mode timings.

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPIPICO, and SPIPOCI.

6.17.5.1.1 SPI Controller Mode Switching Characteristics Clock Phase 0

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1] [2]		(BRR + 1) CONDITION[3]	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPIPTE}$ active to SPICLK	Even	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
			Odd	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$	
24	$t_{v(PTE)M}$	Valid time, SPICLK to $\overline{SPIPTE}$ inactive	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
High-Speed Mode						
4	$t_{d(PICO)M}$	Delay time, SPICLK to SPIPICO valid	Even, Odd		1	ns
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
Normal Mode						
4	$t_{d(PICO)M}$	Delay time, SPICLK to SPIPICO valid	Even, Odd		5	ns
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

(1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.17.5.1.2 SPI Controller Mode Switching Characteristics Clock Phase 1

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER(1) (2)		(BRR + 1) CONDITION(3)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPIPTE}$ valid to SPICLK	Even, Odd	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
24	$t_{v(PTE)M}$	Valid time, SPICLK to $\overline{SPIPTE}$ invalid	Even	– 3	+3	ns
			Odd	– 3	+3	
High-Speed Mode						
4	$t_{d(PICO)M}$	Delay time, SPIPICO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
Normal Mode						
4	$t_{d(PICO)M}$	Delay time, SPIPICO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 5$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 5$		
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

(1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.17.5.1.3 SPI Controller Mode Timing Requirements

NO.			(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
High-Speed Mode						
8	$t_{su(POCI)M}$	Setup time, SPIPOCI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(POCI)M}$	Hold time, SPIPOCI valid after SPICLK	Even, Odd	5		ns
Normal Mode						
8	$t_{su(POCI)M}$	Setup time, SPIPOCI valid before SPICLK	Even, Odd	20		ns
9	$t_{h(POCI)M}$	Hold time, SPIPOCI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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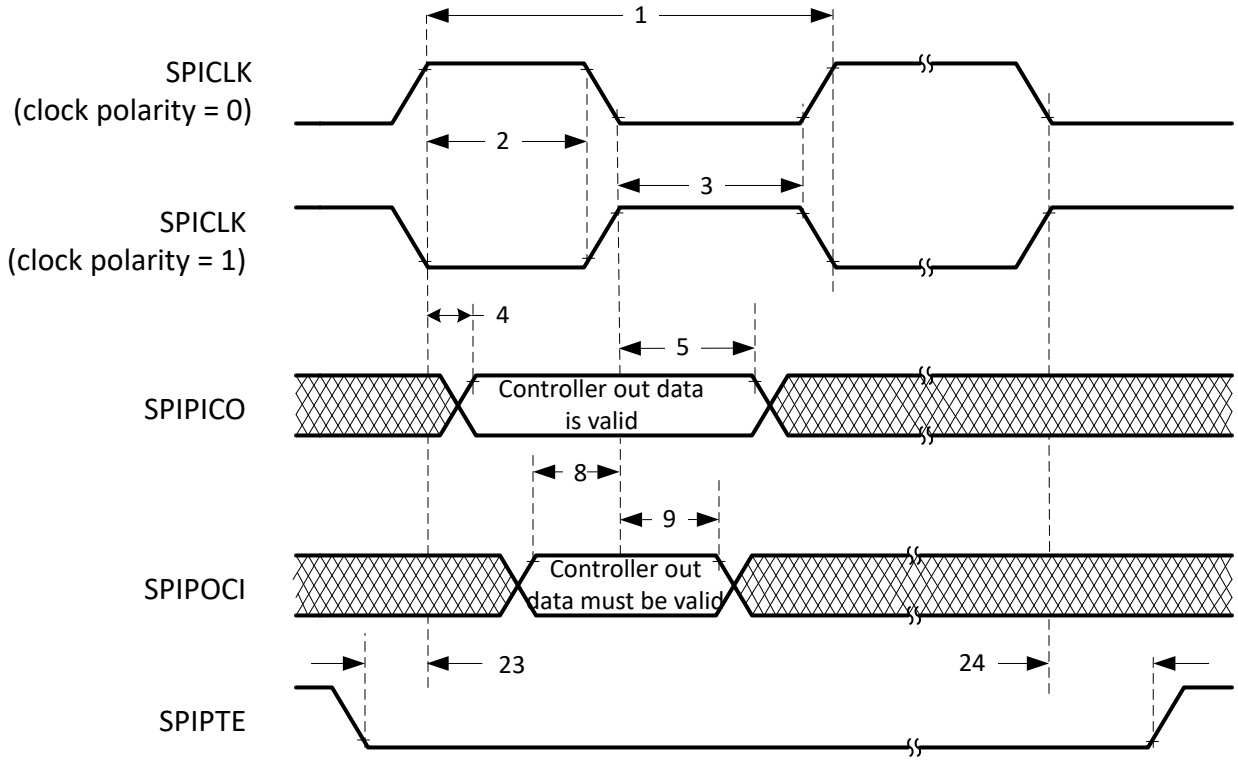
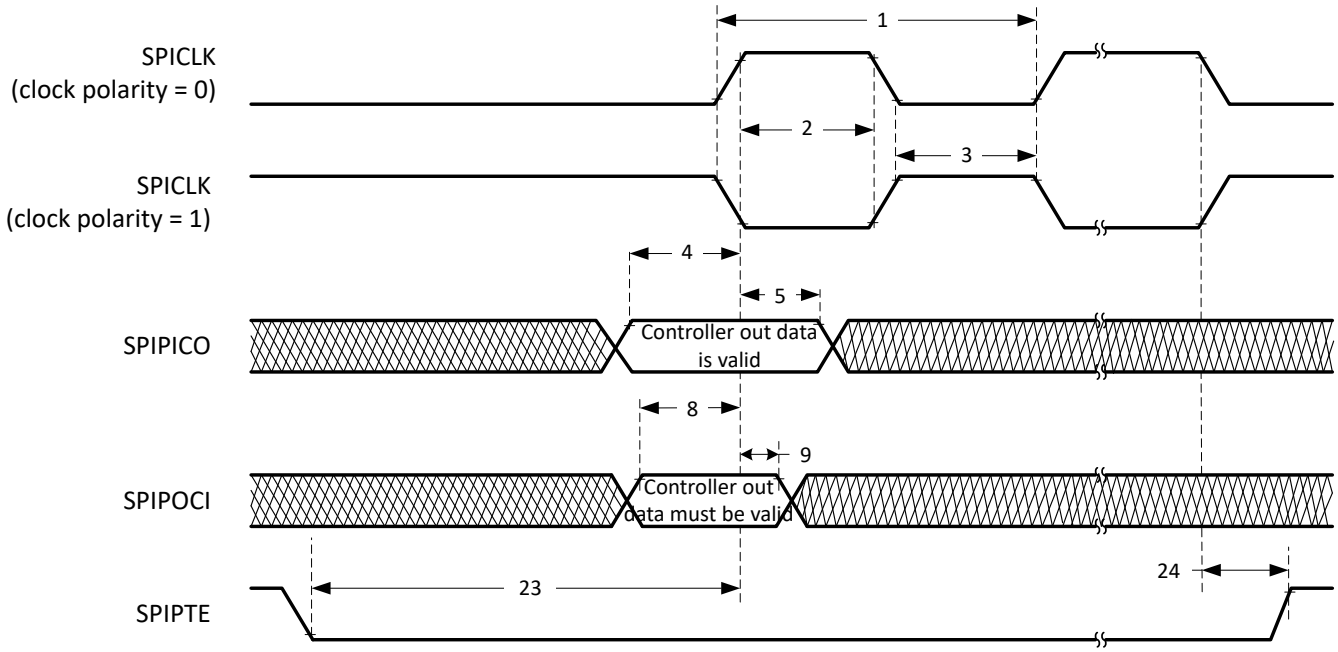
6.17.5.1.4 SPI Controller Mode Timing Diagrams



A. On the trailing end of the word, $\overline{\text{SPIPTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-77. SPI Controller Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPIPTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-78. SPI Controller Mode External Timing (Clock Phase = 1)

6.17.5.2 SPI Peripheral Mode Timings

The following sections contain the SPI Peripheral Mode timings.

6.17.5.2.1 SPI Peripheral Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1]		MIN	MAX	UNIT
High-Speed Mode					
15	$t_{d(POCI)S}$	Delay time, SPICLK to SPIPOCI valid		9	ns
16	$t_{v(POCI)S}$	Valid time, SPIPOCI valid after SPICLK	0		ns
Normal Mode					
15	$t_{d(POCI)S}$	Delay time, SPICLK to SPIPOCI valid		20	ns
16	$t_{v(POCI)S}$	Valid time, SPIPOCI valid after SPICLK	0		ns

(1) 20-pF load on pin.

6.17.5.2.2 SPI Peripheral Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(PICO)S}$	Setup time, SPIPICO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(PICO)S}$	Hold time, SPIPICO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(PTE)S}$	Setup time, $\overline{\text{SPIPTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 11$		ns
		Setup time, $\overline{\text{SPIPTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 20$		ns
26	$t_{h(PTE)S}$	Hold time, $\overline{\text{SPIPTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

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6.17.5.2.3 SPI Peripheral Mode Timing Diagrams

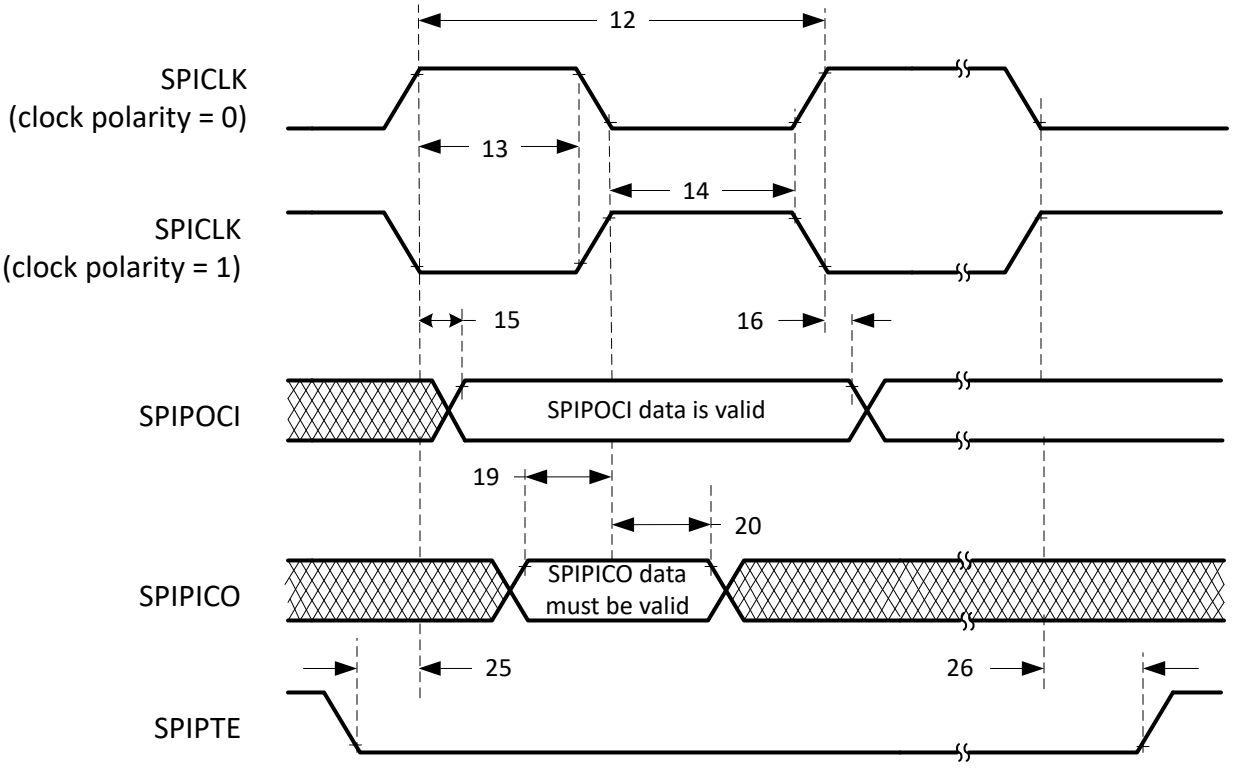

Figure 6-79. SPI Peripheral Mode External Timing (Clock Phase = 0)

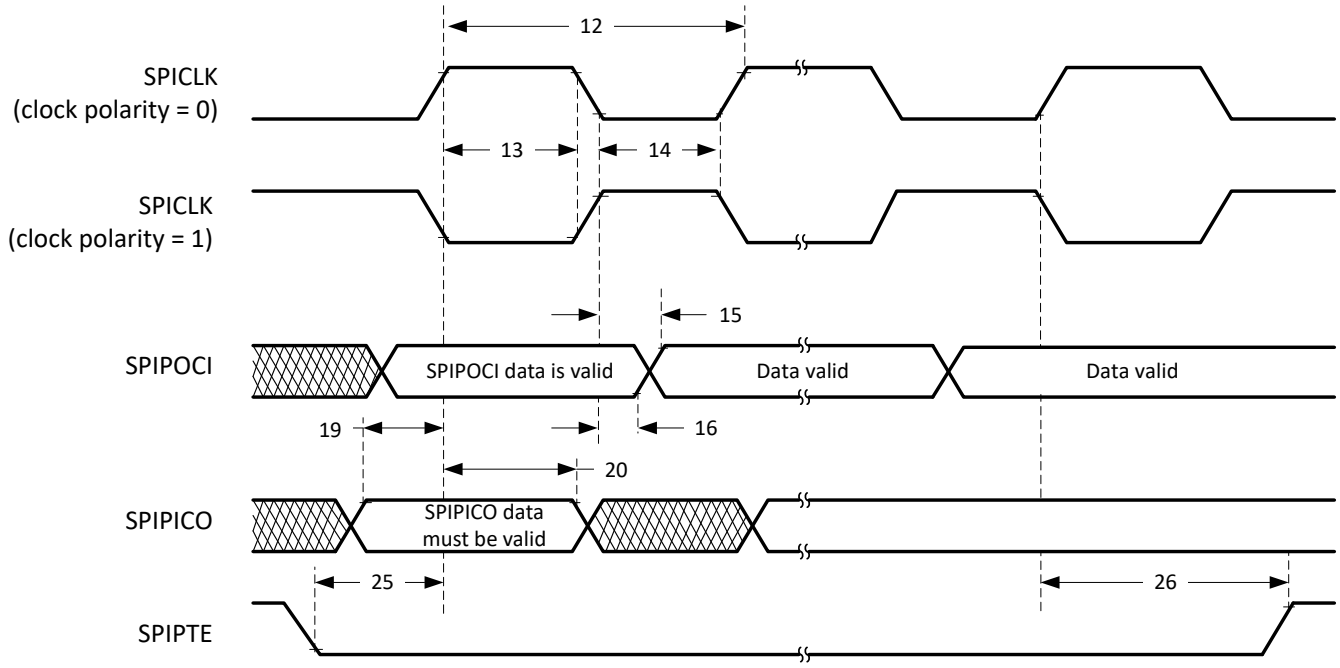

Figure 6-80. SPI Peripheral Mode External Timing (Clock Phase = 1)

6.17.6 Single Edge Nibble Transmission (SENT)

6.17.6.1 Introduction

The SENT module is based on the open standard SAE J2716 with additional enhancements such as additional sensor format support.

Note

The term 'channel' within this chapter and 'sensor' in the register descriptions are equivalent.

6.17.6.2 Features

The SENT module includes the following features:

- Based on SAE J2716 (J2716 January 2010 and J2716 April 2016)
- Supports 2007 and 2010 CRC checksum calculation
- Fast channel receiver
- Slow channel receiver
  - Short serial message (8-bit data and 4-bit message ID)
  - Enhanced serial 12-bit message (12-bit data and 8-bit message ID)
  - Enhanced serial 12-bit message (12-bit data and 8-bit message ID)
- Configurable memory depth
- Master Trigger Pulse Generator (MTPG) enables multiple sensors for the same SENT bus
- 5 SENT channels that can each be set to be triggered by one of 63 trigger sources
- Nibble sorting to minimize CPU intervention
- Timeout feature in SENT channel can be re-purposed for watchdog (only usable in continuous receive mode)
- RXD_I_R bit in the CSENT_RXD register is used for debugging 1 bit of the SENT receive at a time
- Time stamp captures for received data frames
  - Uses 32-bit free running counter
  - Can use external counter for one or all SENT modules
- Receiver and Interrupt Features
  - Programmable glitch filter on input (bypass mode available)
  - Automatic detection of CRC error and framing error on Fast and Slow Channel Data
  - Option to save data received with error
  - Configurable number of data nibbles to receive (1-8)
  - FIFO and direct map support for received data frames
  - RTDMA and interrupts can be used to send data depending on how full the FIFO is
  - Error Detection Supported:
    - Timeout
    - Calibration
    - FIFO Overflow/Underflow
    - Frequency Drift
    - Overflow Trigger Request

6.17.7 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-commander and multiple-responder with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic commander header generation
  - Programmable synchronization break field
  - Synchronization field
  - Identifier field
- Responder automatic synchronization
  - Synchronization break detection
  - Optional baud rate update
  - Synchronization validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wake-up support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error
  - Bus error
  - No-response error
  - Checksum error
  - Synchronization field error
  - Parity error
- Two interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

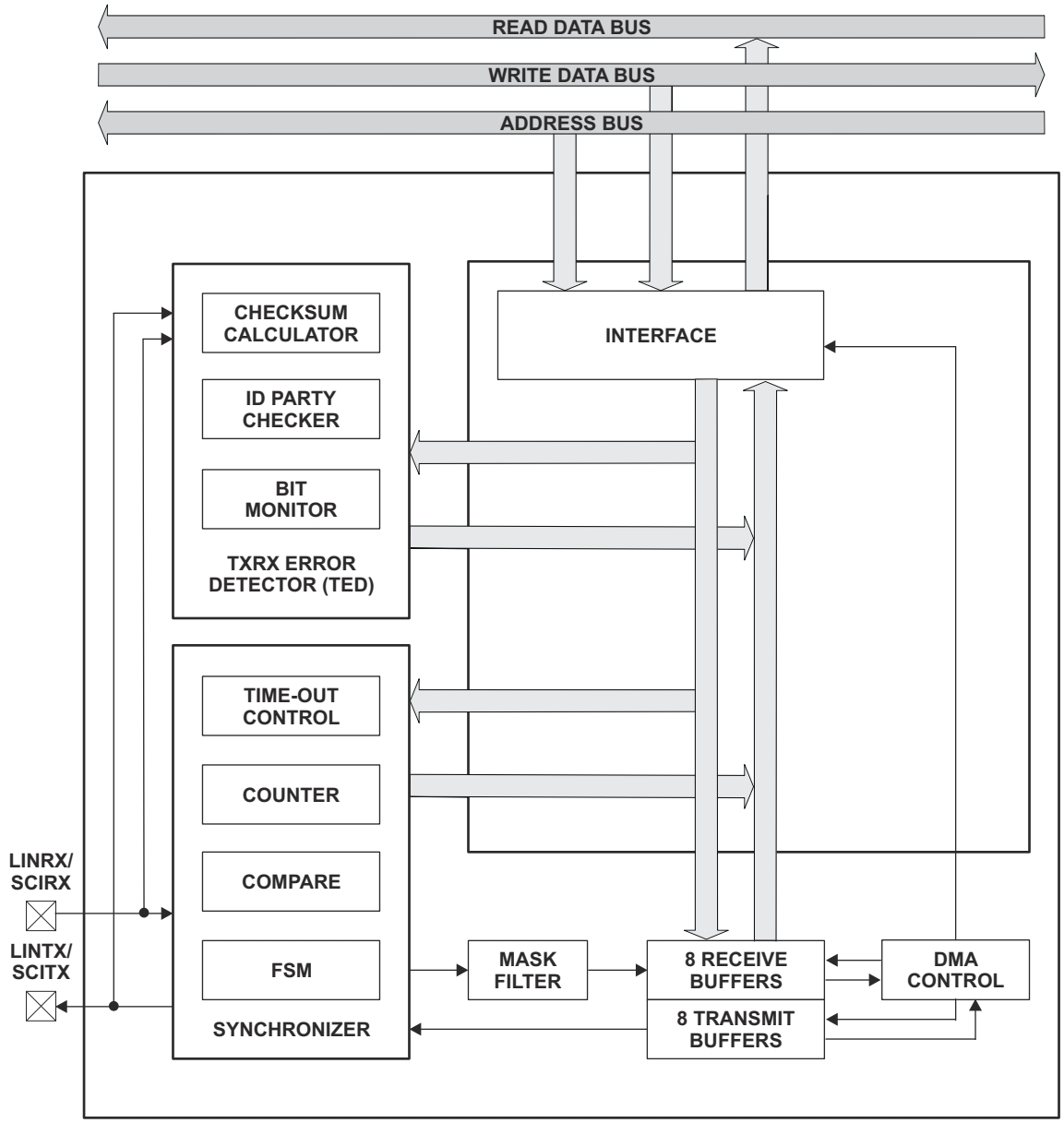

Figure 6-81. LIN Block Diagram

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6.17.8 EtherCAT SubordinateDevice Controller (ESC)

Ethernet for Control Automation Technology (EtherCAT®) is an Ethernet-based fieldbus system, invented by Beckhoff Automation and is standardized in IEC 61158. All the SubordinateDevice (or SubDevice) nodes connected to the bus interpret, process, and modify the data addressed to them quickly, without having to buffer the frame inside the node. This real-time behavior, frame processing, and forwarding requirements are implemented by the EtherCAT SubDevice controller (ESC) hardware. EtherCAT does not require software interaction for data transmission inside the SubDevices. EtherCAT only defines the MAC layer while the higher-layer protocols and stack are implemented in software on the microcontrollers connected to the ESC.

The EtherCAT:

- Involves MainDevice (or MDevice) and SubDevices setup where SubDevice nodes are physically connected daisy-chain style but logically operate on a loop
- Specializes in precise, low-jitter synchronization across SubDevice nodes
- Uses IEEE 802.3 Ethernet physical layer and standard Ethernet frames

6.17.8.1 ESC Features

The ESC on this MCU provides the following functionality:

- Up to 2 MII ports to connect to EtherCAT PHYs
- Process data interface through 16-bit asynchronous interface
- 64-bit distributed clocking
  - Sync output signals to synchronize device events and latch input signals supporting time-stamping for events
  - Distributed clock features of SYNC0/1 (o/ps) and LATCH0/1 able to synchronize GPIOs and allow inputs from any GPIOs as well as other muxing options for internal device events
- 8 Field bus Memory Management Units (FMMUs)
  - Support all native types of RD/, WR/, RDWR, and built-in features of bit- and byte-addressing
- 8 Sync Managers
- I2C EEPROM interface
- Up-to 32 general-purpose inputs (GPIs) and 32 general-purpose outputs (GPOs)
- 2 SYNC and 2 LATCH signals connected to GPIO pads
- 16KB RAM with parity

6.17.8.2 ESC Subsystem Integrated Features

In addition to the ESC features, the following are the device-specific features provided by the integration of the ESC and the MCU:

- ESC access allocation to the CPU1 subsystem during initialization
- EtherCAT reset request from MDevice can be routed to NMI or general interrupt controller on MCU
- RAM Parity error routed to NMI on MCU
- DMA access to EtherCAT RAM
- Up to 32 GPIs and up to 32 GPOs feature integrated to 16-bit ASYNC PDI interface
- Interface to CLB
- Distributed clock feature of SYNC0/1 able to synchronize PWMs, generate interrupt/DMA requests, or trigger eCAP capture to allow external component action through GPIO access.
- EtherCAT SYNC0/1 pulse can trigger a CLA task.
- Distributed clock feature of LATCH0/1 allows inputs from any GPIO or PWM crossbar triggers

6.17.8.3 EtherCAT IP Block Diagram

Figure 6-82 shows the general functionality of EtherCAT IP.

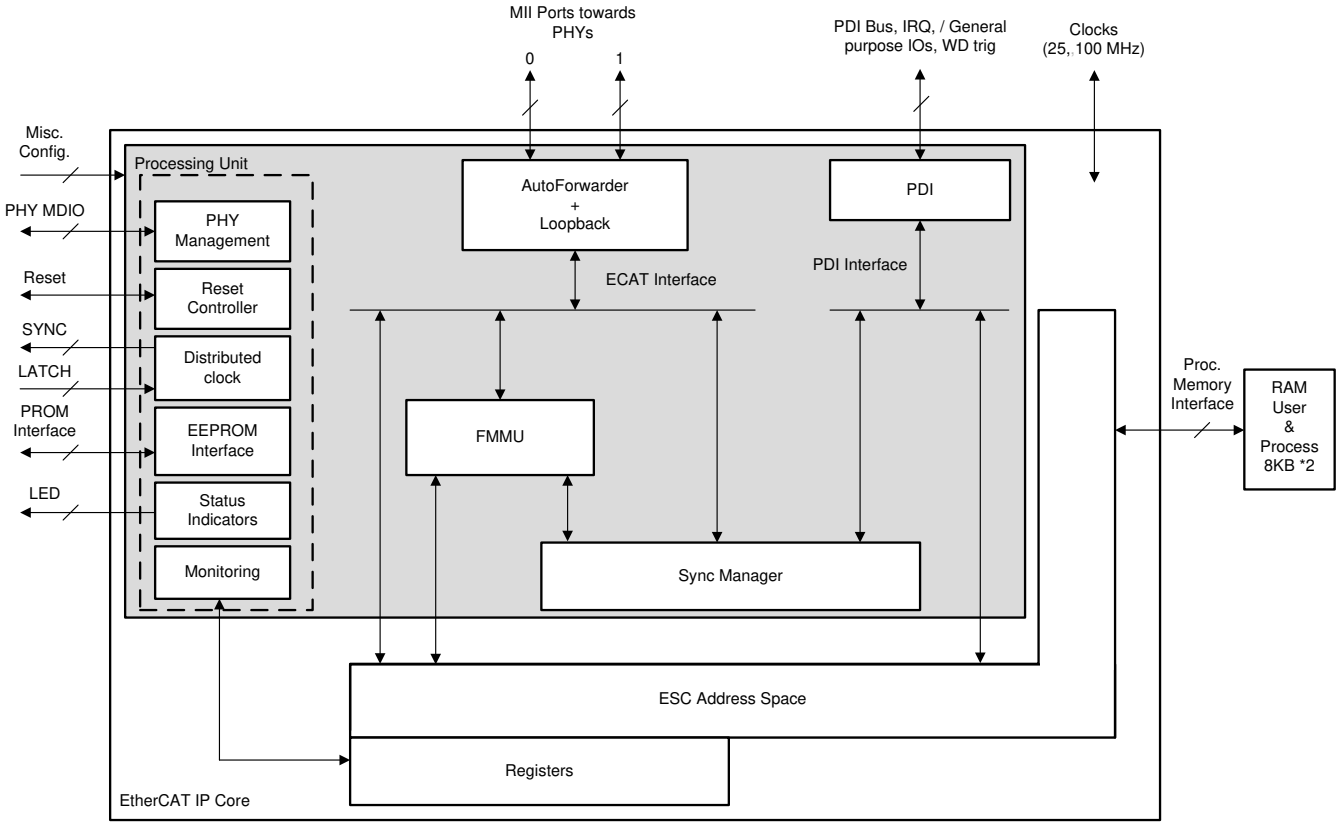

Figure 6-82. EtherCAT IP Block Diagram

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6.17.8.4 EtherCAT Electrical Data and Timing

6.17.8.4.1 EtherCAT Timing Requirements

			MIN	NOM	MAX	UNIT
EtherCAT						
	$t_{c(ECATCLK)}$	Cycle time, ECATCLK		10		ns
MII1	$t_{c(TXCLK)}$	Cycle time, ESC_TXy_CLK		40		ns
MII2/MII3	$t_{w(TXCK)}$	Pulse duration, ESC_TXy_CLK high or low	16		24	ns
MII4	$t_{c(RXCK)}$	Cycle time, ESC_RXy_CLK		40		ns
MII5/MII6	$t_{w(RXCK)}$	Pulse duration, ESC_RXy_CLK high or low	16		24	ns
MII8	$t_{su(RXDV-RXCKH)}$	Setup time, receive signals valid before ESC_RXy_CLK high	10			ns
MII9	$t_{h(RXCKH-RXDV)}$	Hold time, receive signals valid after ESC_RXy_CLK high	2			ns
MDIO						
MDIO4	$t_{su(MDV-MCKH)}$	Setup time, ESC_MDIO_DATA valid before ESC_MDIO_CLK high	20			ns
MDIO5	$t_{h(MCKH-MDV)}$	Hold time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	–1			ns

6.17.8.4.2 EtherCAT Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER		MIN	TYP	MAX	UNIT
Auto Shift Compensation						
MII7	$t_{d(TXCLK-TXDV)}$	Delay time, ESC_TXy_CLK to ESC_TXy_DATA[3:0] and ESC_TXy_ENA	20 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK\_100)}$		30 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK\_100)}$	ns
MDIO						
MDIO1	$t_{c(MCK)}$	Cycle time, ESC_MDIO_CLK		400		ns
MDIO2/MDIO3	$t_{w(MCK)}$	Pulse duration, ESC_MDIO_CLK high or low	160		240	ns
MDIO7	$t_{d(MCKH-MDV)}$	Delay time, ESC_MDIO_CLK high to ESC_MDIO_DATA valid			$0.5t_{c(MCK)}$ + 30	ns
	$t_{v(MCKH-MDV)}$	Valid time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	$0.5t_{c(MCK)}$ – 3.0			ns

6.17.8.4.3 EtherCAT Timing Diagrams

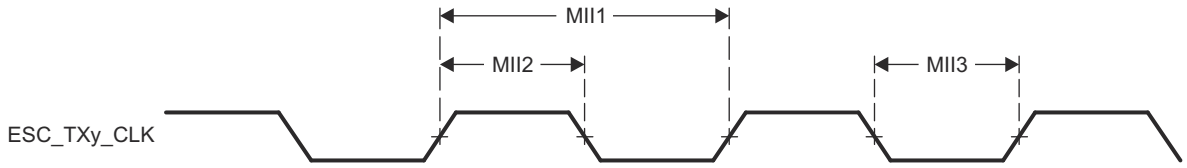

Figure 6-83. EtherCAT Transmit Clock Timing (MII Operation)

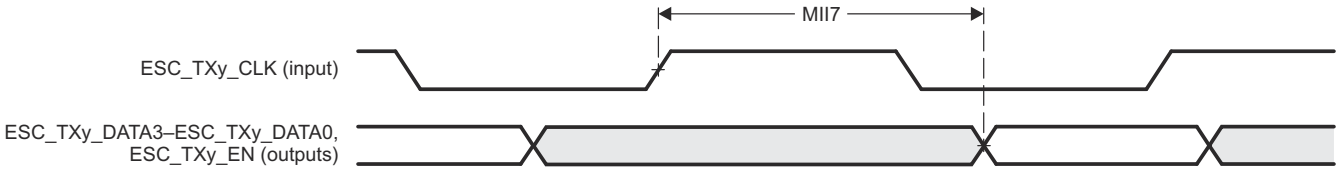

Figure 6-84. EtherCAT Transmit Interface Timing (MII Operation)

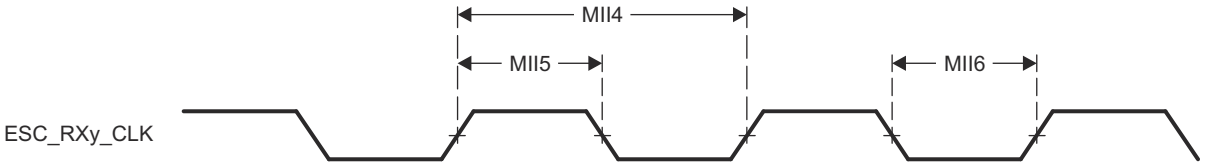

Figure 6-85. EtherCAT Receive Clock Timing (MII Operation)

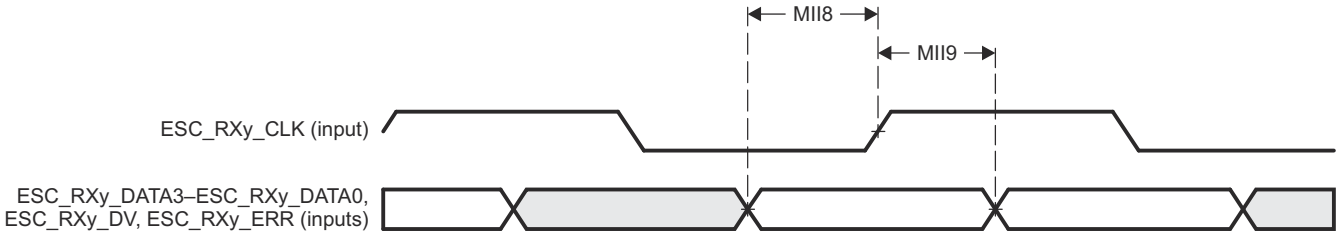

Figure 6-86. EtherCAT Receive Interface Timing (MII Operation)

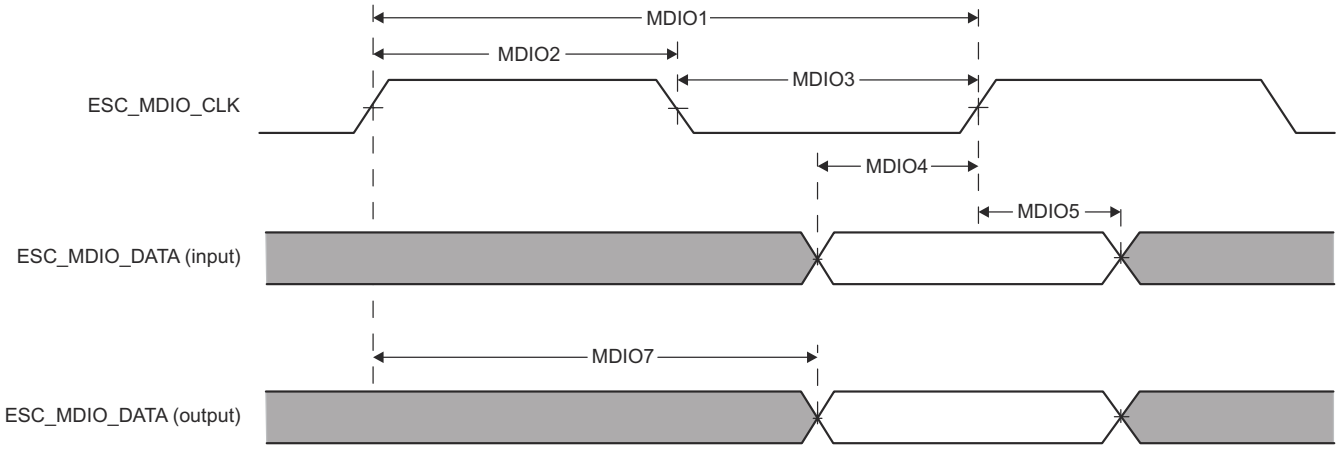

Figure 6-87. EtherCAT MDIO Timing Diagrams

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6.17.9 Universal Asynchronous Receiver-Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) module in this device contains the following features:

- Programmable baud-rate generator allowing speeds of up to 12.5Mbps for regular speed (divide by 16) and 25Mbps for high speed (divide by 8)
- Separate 16-level-deep and 8-bit-wide transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of ⅛, ¼, ½, ¾, and ⅞
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity-bit generation and detection
  - 1 or 2 stop-bit generation
- IrDA serial-IR (SIR) encoder and decoder providing:
  - Programmable use of IrDA SIR or UART input/output
  - Support of IrDA SIR encoder and decoder functions for data rates of up to 115.2Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41 to 2.23 µs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power-mode bit duration
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission (EOT) interrupts
- Efficient transfers using Real-Time Direct Memory Access (RTDMA) Controller
  - Separate channels for transmit and receive
  - Receive burst request asserted at programmed FIFO level
  - Transmit burst request asserted at programmed FIFO level

Figure 6-88 shows the UART module block diagram.

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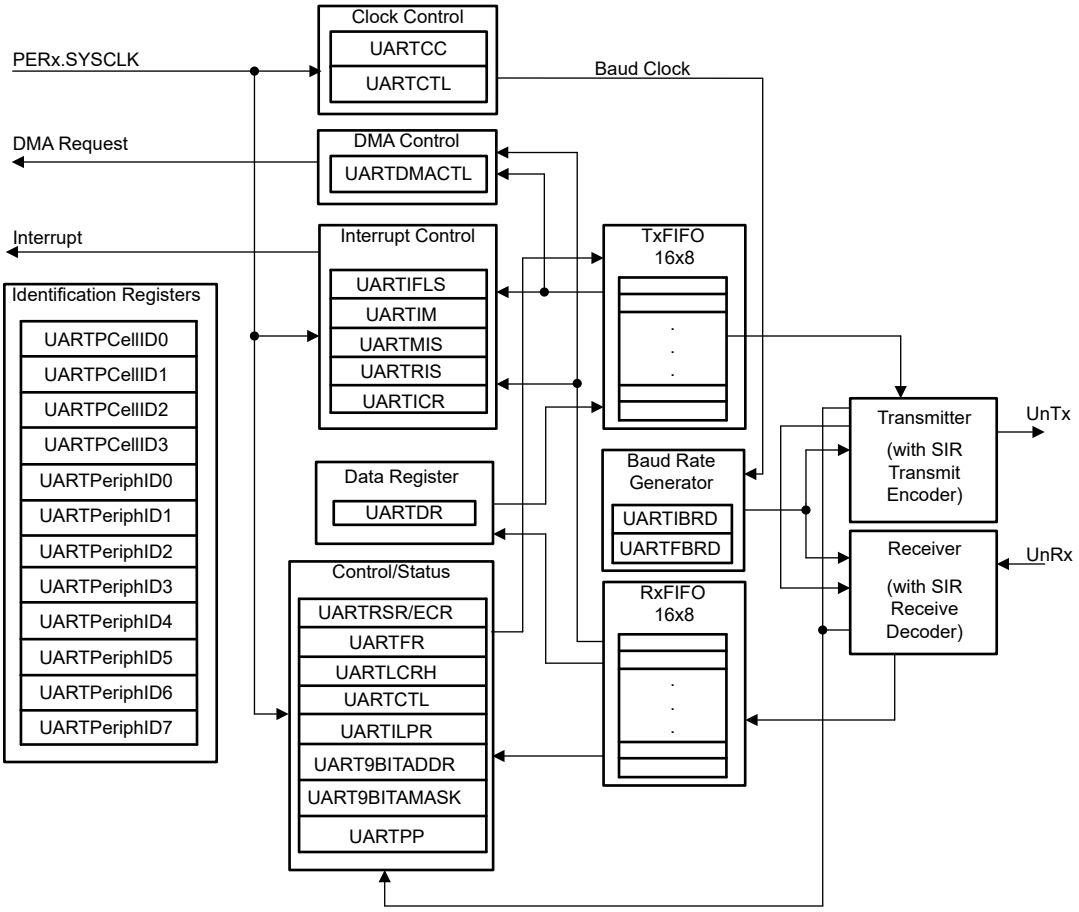

Figure 6-88. UART Module Block Diagram

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7 Detailed Description

7.1 Overview

The F29H85x and F29P58x are members of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- Electrical vehicles and transportation
- Motor control
  - Traction inverter motor control
  - HVAC motor control
  - Mobile robot motor control
- Solar inverters
  - Central inverter
  - Micro inverter
  - String inverter
- Digital power
- Industrial motor drives
- EV charging infrastructure

The real-time control subsystem has up to three 200MHz C29x DSP cores. The C29x supports 32-bit and 64-bit floating- and fixed-point signal-processing running from on-chip flash or RAM. The C29x CPU is boosted by trigonometric math instructions, speeding up common algorithms key to real-time control systems.

Many features are included to support a system-level ASIL-D functional safety solution. The C29x CPU1 and CPU2 cores can be put in lockstep for detection of permanent and transient faults. Logic Power-On Self-Test (LPOST) and Memory Power-On Self-Test (MPOST) provide start-up detection of latent faults. Safe interconnects provide fault detection between the CPU and the peripherals. The ADC safety checker compares ADC conversion results from multiple ADC modules without additional CPU cycles. The Waveform Analyzer and Diagnostic (WADI) can monitor multiple signals for proper operation and take action to ensure a safe state is maintained. The device architecture features a Safe Interconnect (SIC) for end-to-end code and data safety, with CPU-based ECC protection for all memories and peripheral endpoints.

Hardware Security Manager (HSM) provides EVITA-full security support. Features include Secure Boot, secure storage and keyring support, secure debug authentication, and cryptographic accelerator engines. The HSM enables secure key and code provisioning in untrusted factory environments, and supports Firmware-Over-The-Air updates of HSM and host application firmware, with A/B swap capability and rollback control.

SSU (Safety and Security unit) enables superior run-time safety and security features. This feature can be used create safety isolation (Freedom From Interference) among the threads running on same CPU or different CPUs. The SSU features a context-sensitive MPU mechanism that automatically switches access permissions in hardware based on currently executing thread or task. This eliminates software overhead, enabling real-time code performance without compromising system safety. The SSU provides multi-user debug authentication, and also supports Live Firmware Update (LFU) and FOTA fpr application firmware updates with A/B swap and rollback control.

High-performance analog blocks are tightly integrated with the processing and control units to provide optimal real-time signal chain performance. Two 16-bit Analog-to-Digital Converters (ADC) and three 12-bit ADCs have up to 80 analog channels as well as an integrated post-processing block and hardware oversampling. Two 12-bit buffered DACs and twenty-four comparator channels are available.

Thirty-six frequency-independent PWMs, all with high-resolution capability, enable control of multiple power stages, from 3-phase inverters to advanced multilevel power topologies. The PWMs have been enhanced with Minimum Dead-Band Logic (MINDL), Diode Emulation (DE), and Illegal Combo Logic (ICL) features.

The Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

An EtherCAT SubDevice Controller, Ethernet MAC, and other industry-standard protocols like CAN FD are available on this device. The Fast Serial Interface (FSI) enables up to 200Mbps of robust communications across an isolation boundary.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000 real-time microcontrollers page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the F29H85X-SOM-EVM evaluation board, and download the MCU-SDK-F29H85x software development kit.

7.2 Functional Block Diagram

Figure 7-1 shows the CPU system and associated peripherals.

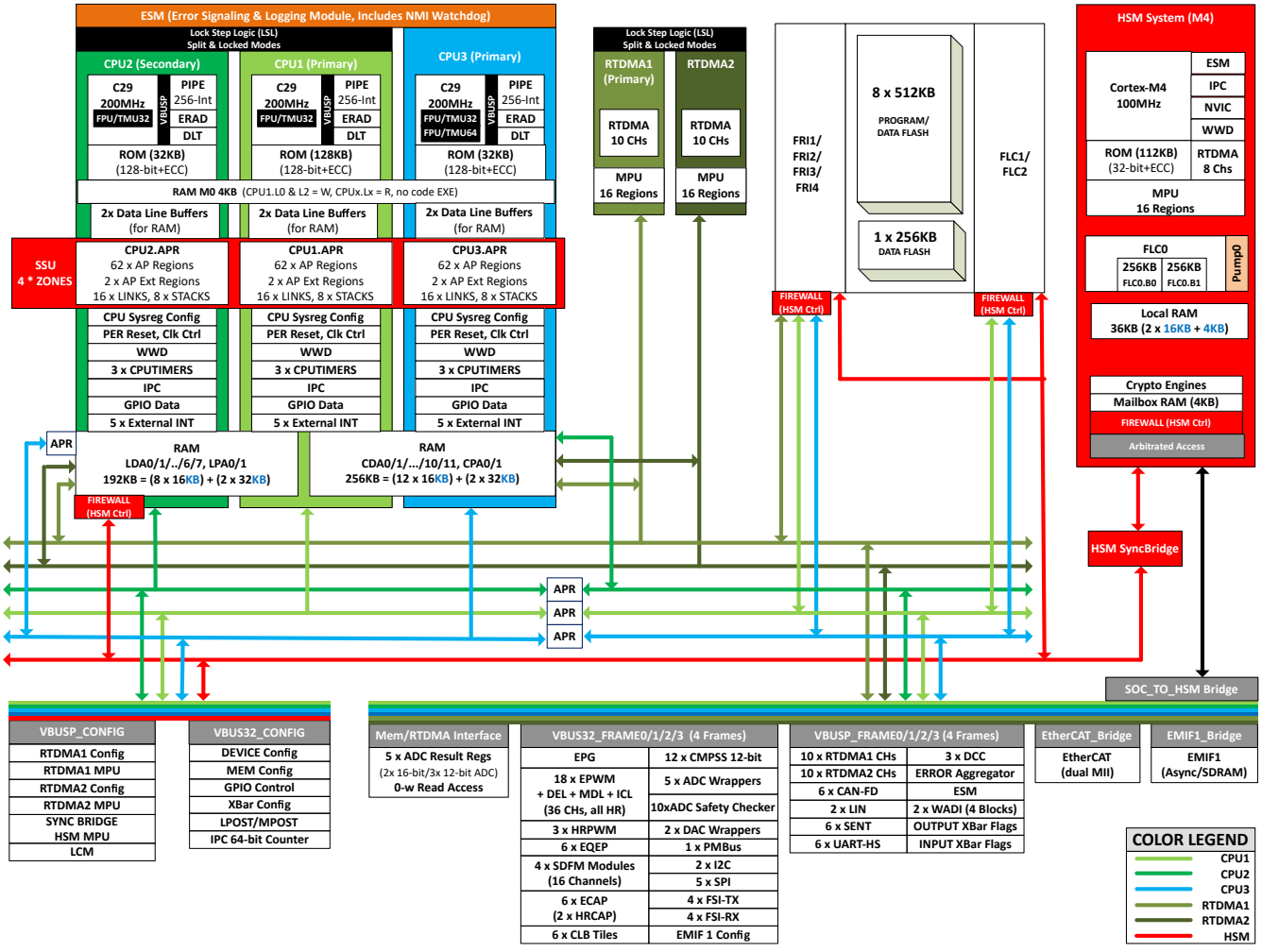

Figure 7-1. Functional Block Diagram

7.3 Error Signaling Module (ESM_C29)

7.3.1 Introduction

The Error Signaling Module (ESM) provides systematic consolidation of responses to error events throughout the device into one location. The Module can signal programmable priority interrupts to the processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore, an external controller is able to reset the device or keep the system in a safe, known state.

7.3.2 ESM Subsystem

The Error Signaling Module Subsystem (ESM-SS) groups error signaling module (ESM) instances as shown in Figure 7-2. ESMSS supports a number of ESM instances that is triggered from common set of error event inputs. Each ESM instance is used to drive interrupts to individual CPU and resets to individual CPU or System. The subsystem combines the ESM instances and output pulse interrupt from each ESM instances are exported at the subsystem boundary for integration at the device level.

ESM subsystem is comprised of the following instances :

- ESM CPU instances one for each CPU
  - **Input's**: The error inputs listed in the *Error Event Inputs* section of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* , common to all ESM Subsystem instances
  - **Output's**:
    - Low Priority Interrupt
    - High Priority Interrupt
    - High Priority WD Event (Event triggered by watchdog timeout on High Priority Interrupt hence also referred to as High Priority Watchdog Interrupt in the later part of the document): Similar functionality as NMIWD on C28x devices
    - Critical Priority Interrupt
- Additional System ESM instance for Error Pin output and monitoring.
  - **Input's**: The error inputs listed in the *Error Event Inputs* section of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* , common to all ESM Subsystem instances
  - **Output's**:
    - Low Priority Interrupt
    - Critical Priority Interrupt
    - Error Pin Output
    - Error Pin Monitor Event : Error pin monitoring and error detection output
- Register Parity Error Aggregator Instance (Safety Aggregator)
  - **Input's**:
    - Input from EDC (Error Detection and Correction) Control Interfaces of all ESM Instances (ESM CPU and SYS ESM)
  - **Output**:
    - Parity Error Interrupt : Interrupt generated by parity error detected on ESM register configurations

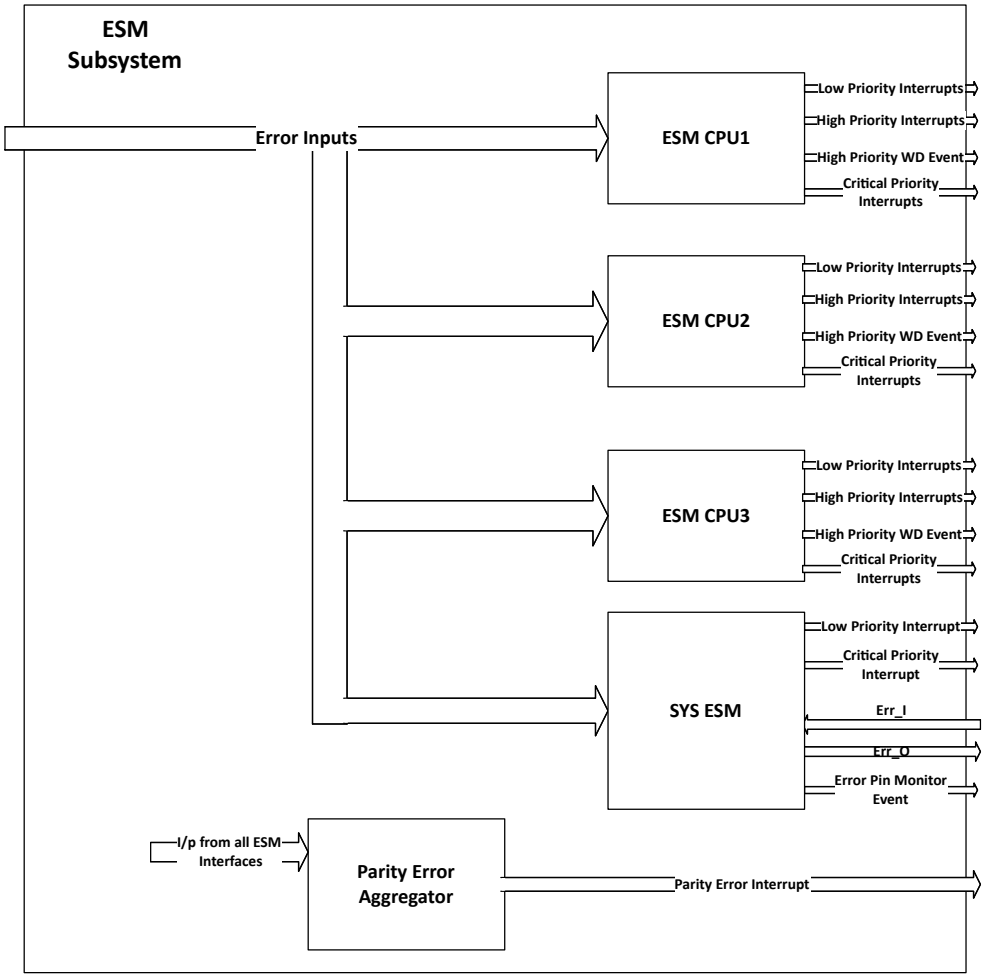

Figure 7-2. ESM-SS Block Diagram

7.3.3 System ESM

Error Pin inputs and outputs are controlled by System ESM instance. The System ESM produces an configurable error pin output (err_o/ERRORSTS) in addition to the set of interrupt outputs. The System ESM generates critical priority interrupt (ESMRESET) output which causes system reset request (XRSn) by default if not disabled by ESMXRSNCTL Register. The System ESM additionally has the Error Pin Monitor feature and associated Error Pin Monitor event which is exported at subsystem as a pulse interrupt. Error Pin Monitor event is also fed back to ESM-SS as an error event input so that the ESM can take appropriate action on the mismatch event.

The low priority interrupt output of System ESM is mapped to XBAR's as ESMGENEVT signal.

7.4 Error Aggregator

7.4.1 Error Aggregator Modules

Each Error Source provides the following information for all Error Aggregator Modules:

- Error - Pulse signal is generated on the occurrence of any error sent to ESM for further action.
- Error Address - System Address at which the error occurred used to detect and debug the error origin.
- Error Type - Multibit signal that indicates the type of error used to classify the error into predefined categories outlined later in the chapter.

All CPU Error Aggregator Modules additionally provide a Program Counter (PC) log for first high-priority error occurrence.

The *Error Aggregator Block Diagram* illustrates the module working and implementation. Each Aggregator module aggregates error from various sources. Upon error occurrence, the corresponding error address and type are logged into Error Address and Error Type registers, respectively.

The errors are classified as high or low priority based on the list in the *Error Type Information* section of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

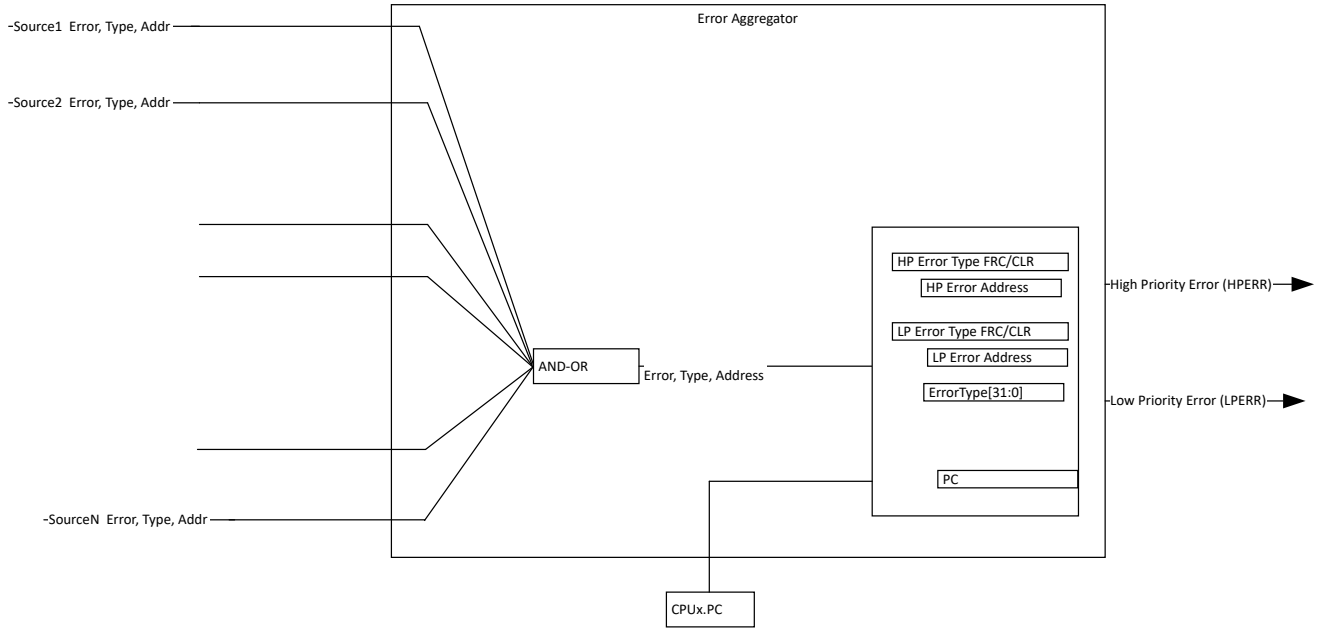

Figure 7-3. Error Aggregator Block Diagram

Error Aggregator modules implemented in the device are:

1. CPUx PR Error Aggregator - Aggregates errors occurred during CPUx program fetch access
2. CPUx DR1 Error Aggregator - Aggregates errors occurred during CPUx Data Read access on DR1 port
3. CPUx DR2 Error Aggregator - Aggregates errors occurred during CPUx Data Read access on DR2 port
4. CPUx DW Error Aggregator - Aggregates errors occurred during CPUx data write access
5. CPUx INT Error Aggregator - Aggregates interrupt related errors from CPUx and associated PIPE module
6. RTDMAx DR Error Aggregator - Aggregates errors occurred during RTDMAx data read access
7. RTDMAx DW Error Aggregator - Aggregates errors occurred during RTDMAx data write access
8. SSU Error Aggregator - Aggregates errors sent out by SSU module
9. EtherCAT Error Aggregator - Aggregates errors occurred during EtherCAT memory access
10. HSM Error Aggregator - Aggregates errors sent out by HSM subsystem

Note

x indicates that each error aggregator is repeated per initiator instance. EtherCAT only provides error and error address information so error type is tied off to uncorrectable error (0x40).

7.4.2 Error Aggregator Interface

This section provides details on how error information is handled and interfaced to the Error Signaling Module (ESM). The error outputs from multiple error aggregators are ORed and applied as single source to ESM. These includes:

- Low-Priority Errors from CPUx PR, CPUx DR1, CPUx DR2, CPUx DW are combined as CPUx LPERR
- High-Priority Errors from CPUx PR, CPUx DR1, CPUx DR2, CPUx DW are combined as CPUx HPERR
- Low-Priority Errors from RTDMAx DR + RTDMAx DW are combined as RTDMAx LPERR
- High-Priority Errors from RTDMAx DR + RTDMAx DW are combined as RTDMAx HPERR

Figure 7-4 shows a conceptual block diagram of the module functionality and how the output flag from each aggregator is combined as described in points above. The block diagram does not show all error aggregator modules available in the system, refer to the detailed list of supported error aggregators.

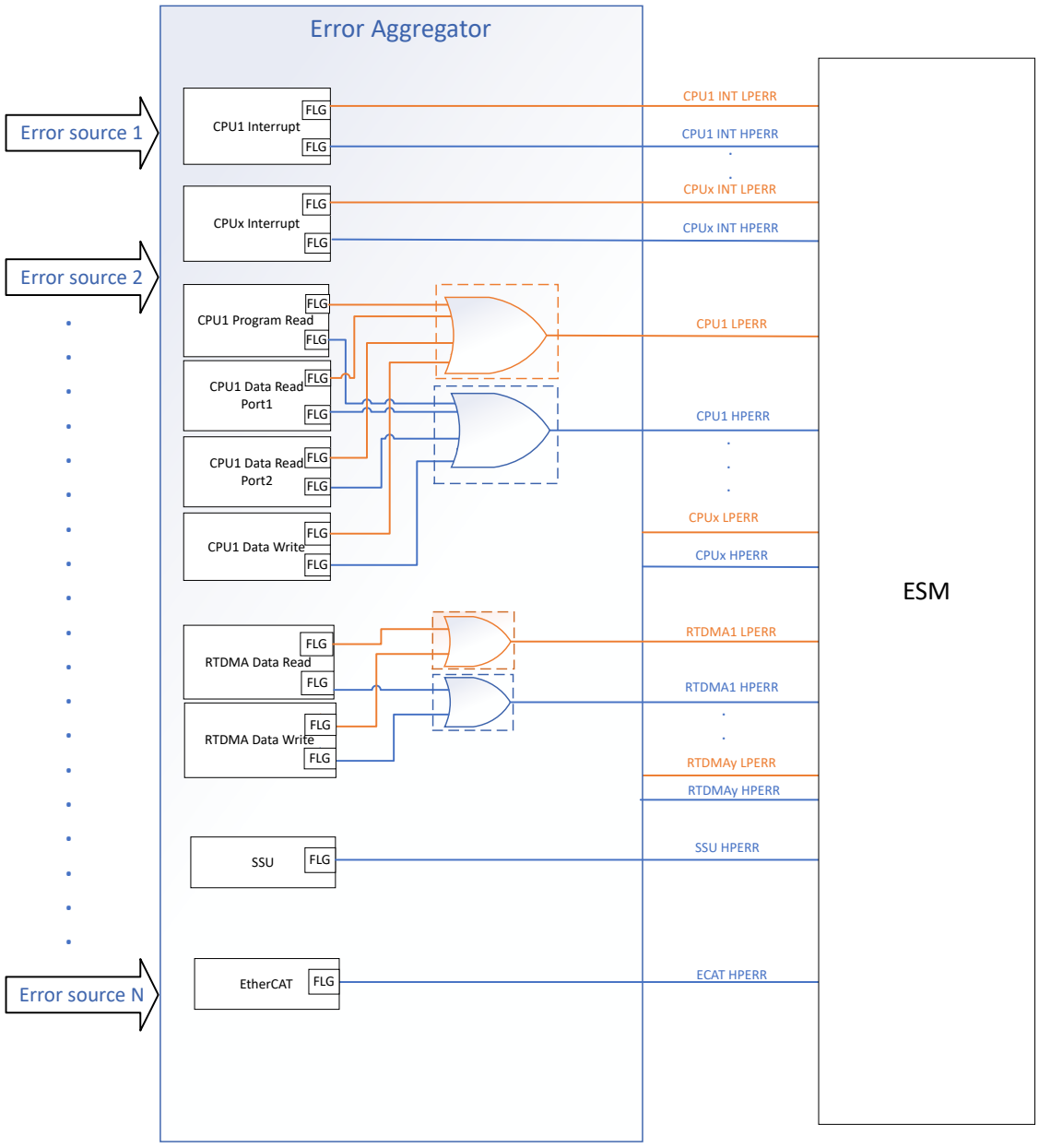

Figure 7-4. Error Aggregator Interface

7.5 Memory

7.5.1 C29x Memory Map

Table 7-1. Memory Map

MEMORY	DESCRIPTION	SIZE (x8)	START ADDRESS	END ADDRESS	RTDMA1 ACCESS	RTDMA2 ACCESS	HSM (M4, RTDMA) ACCESS	ECC/ PARITY
CPU1 ROM		128	0x0000_0000	0x0001_FFFF	-	-	-	ECC
CPU2 ROM		32	0x0000_0000	0x0000_7FFF	-	-	-	ECC
CPU3 ROM		32	0x0000_0000	0x0000_7FFF	-	-	-	ECC
Flash Main Bank	Mapping via FRI-1 RP0	1024	0x1000_0000	0x100F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-1 RP1	1024	0x1010_0000	0x101F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-1 RP2	1024	0x1020_0000	0x102F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-1 RP3	1024	0x1030_0000	0x103F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-2 RP0	1024	0x1040_0000	0x104F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-2 RP1	1024	0x1050_0000	0x105F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-3 RP0	1024	0x1060_0000	0x106F_FFFF	YES	-	YES	ECC
Flash Main Bank	Mapping via FRI-3 RP1	1024	0x1070_0000	0x107F_FFFF	YES	-	YES	ECC
Data Flash 128-bit	Mapping via FRI-4 RP0	256	0x10C0_0000	0x10C3_FFFF	YES	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-1 RP0	4	0x10D8_0000	0x10D8_0FFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-1 RP0	4	0x10D8_1000	0x10D8_1FFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-1 RP1	4	0x10D8_4000	0x10D8_4FFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-1 RP1	4	0x10D8_5000	0x10D8_5FFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-1 RP2	4	0x10D8_8000	0x10D8_8FFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-1 RP2	4	0x10D8_9000	0x10D8_9FFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-1 RP3	4	0x10D8_C000	0x10D8_CFFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-1 RP3	4	0x10D8_D000	0x10D8_DFFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-2 RP0	4	0x10D9_0000	0x10D9_0FFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-2 RP0	4	0x10D9_1000	0x10D9_1FFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-2 RP1	4	0x10D9_4000	0x10D9_4FFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-2 RP1	4	0x10D9_5000	0x10D9_5FFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-3 RP0	4	0x10D9_8000	0x10D9_8FFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-3 RP0	4	0x10D9_9000	0x10D9_9FFF	-	-	YES	ECC
BANKMGMT Sector	Mapping via FRI-3 RP1	4	0x10D9_C000	0x10D9_CFFF	-	-	YES	ECC
SECCFG Sector	Mapping via FRI-3 RP1	4	0x10D9_D000	0x10D9_DFFF	-	-	YES	ECC
Flash Main Bank ECC bits	Mapping via FRI-1 RP0	128	0x10E0_0000	0x10E1_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-1 RP1	128	0x10E2_0000	0x10E3_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-1 RP2	128	0x10E4_0000	0x10E5_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-1 RP3	128	0x10E6_0000	0x10E7_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-2 RP0	128	0x10E8_0000	0x10E9_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-2 RP1	128	0x10EA_0000	0x10EB_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-3 RP0	128	0x10EC_0000	0x10ED_FFFF	YES	-	YES	-
Flash Main Bank ECC bits	Mapping via FRI-3 RP1	128	0x10EE_0000	0x10EF_FFFF	YES	-	YES	-
Data Flash ECC bits	Mapping via FRI-4 RP0	32	0x10F8_0000	0x10F8_7FFF	YES	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-1 RP0	0.5	0x10FB_0000	0x10FB_01FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-1 RP0	0.5	0x10FB_0200	0x10FB_03FF	-	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-1 RP1	0.5	0x10FB_0800	0x10FB_09FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-1 RP1	0.5	0x10FB_0A00	0x10FB_0BFF	-	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-1 RP2	0.5	0x10FB_1000	0x10FB_11FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-1 RP2	0.5	0x10FB_1200	0x10FB_13FF	-	-	YES	-

ADVANCE INFORMATION

Table 7-1. Memory Map (continued)

MEMORY	DESCRIPTION	SIZE (x8)	START ADDRESS	END ADDRESS	RTDMA1 ACCESS	RTDMA2 ACCESS	HSM (M4, RTDMA) ACCESS	ECC/ PARITY
BANKMGMT Sector ECC Bits	Mapping via FRI-1 RP3	0.5	0x10FB_1800	0x10FB_19FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-1 RP3	0.5	0x10FB_1A00	0x10FB_1BFF	-	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-2 RP0	0.5	0x10FB_2000	0x10FB_21FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-2 RP0	0.5	0x10FB_2200	0x10FB_23FF	-	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-2 RP1	0.5	0x10FB_2800	0x10FB_29FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-2 RP1	0.5	0x10FB_2A00	0x10FB_2BFF	-	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-3 RP0	0.5	0x10FB_3000	0x10FB_31FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-3 RP0	0.5	0x10FB_3200	0x10FB_33FF	-	-	YES	-
BANKMGMT Sector ECC Bits	Mapping via FRI-3 RP1	0.5	0x10FB_3800	0x10FB_39FF	-	-	YES	-
SECCFG Sector ECC Bits	Mapping via FRI-3 RP1	0.5	0x10FB_3A00	0x10FB_3BFF	-	-	YES	-
M0	CPU1 Dedicated Stack	4	0x2000_0000	0x2000_0FFF	-	-	-	ECC
LDA7	CPU1 and CPU2 Local SRAM	16	0x200E_0000	0x200E_3FFF	YES	YES	YES	ECC
LDA6	CPU1 and CPU2 Local SRAM	16	0x200E_4000	0x200E_7FFF	YES	YES	YES	ECC
LDA5	CPU1 and CPU2 Local SRAM	16	0x200E_8000	0x200E_BFFF	YES	YES	YES	ECC
LDA4	CPU1 and CPU2 Local SRAM	16	0x200E_C000	0x200E_FFFF	YES	YES	YES	ECC
LDA3	CPU1 and CPU2 Local SRAM	16	0x200F_0000	0x200F_3FFF	YES	YES	YES	ECC
LDA2	CPU1 and CPU2 Local SRAM	16	0x200F_4000	0x200F_7FFF	YES	YES	YES	ECC
LDA1	CPU1 and CPU2 Local SRAM	16	0x200F_8000	0x200F_BFFF	YES	YES	YES	ECC
LDA0	CPU1 and CPU2 Local SRAM	16	0x200F_C000	0x200F_FFFF	YES	YES	YES	ECC
LPA0	CPU1 and CPU2 Local SRAM	32	0x2010_0000	0x2010_7FFF	YES	YES	-	ECC
LPA1	CPU1 and CPU2 Local SRAM	32	0x2010_8000	0x2010_FFFF	YES	YES	-	ECC
CPA0	CPU1 and CPU3 Common SRAM	32	0x2011_0000	0x2011_7FFF	YES	YES	-	ECC
CPA1	CPU1 and CPU3 Common SRAM	32	0x2011_8000	0x2011_FFFF	YES	YES	-	ECC
CDA0	CPU1 and CPU3 Common SRAM	16	0x2012_0000	0x2012_3FFF	YES	YES	-	ECC
CDA1	CPU1 and CPU3 Common SRAM	16	0x2012_4000	0x2012_7FFF	YES	YES	-	ECC
CDA2	CPU1 and CPU3 Common SRAM	16	0x2012_8000	0x2012_BFFF	YES	YES	-	ECC
CDA3	CPU1 and CPU3 Common SRAM	16	0x2012_C000	0x2012_FFFF	YES	YES	-	ECC
CDA4	CPU1 and CPU3 Common SRAM	16	0x2013_0000	0x2013_3FFF	YES	YES	-	ECC
CDA5	CPU1 and CPU3 Common SRAM	16	0x2013_4000	0x2013_7FFF	YES	YES	-	ECC
CDA6	CPU1 and CPU3 Common SRAM	16	0x2013_8000	0x2013_BFFF	YES	YES	-	ECC
CDA7	CPU1 and CPU3 Common SRAM	16	0x2013_C000	0x2013_FFFF	YES	YES	-	ECC

Table 7-1. Memory Map (continued)

MEMORY	DESCRIPTION	SIZE (x8)	START ADDRESS	END ADDRESS	RTDMA1 ACCESS	RTDMA2 ACCESS	HSM (M4, RTDMA) ACCESS	ECC/ PARITY
CDA8	CPU1 and CPU3 Common SRAM	16	0x2014_0000	0x2014_3FFF	YES	YES	-	ECC
CDA9	CPU1 and CPU3 Common SRAM	16	0x2014_4000	0x2014_7FFF	YES	YES	-	ECC
CDA10	CPU1 and CPU3 Common SRAM	16	0x2014_8000	0x2014_BFFF	YES	YES	-	ECC
CDA11	CPU1 and CPU3 Common SRAM	16	0x2014_C000	0x2014_FFFF	YES	YES	-	ECC
HSM MailBox	-	4	0x302C_0800	0x302C_17FF	YES	YES	-	-
EtherCAT RAM	-	16	0x3038_1000	0x3038_4FFF	YES	YES	-	-
EtherCAT RAM - Direct access	-	16	0x303A_1000	0x303A_4FFF	YES	YES	-	-
MCANA Message RAM	-	4	0x6002_0000	0x6002_0FFF	YES	YES	-	-
MCANB Message RAM	-	4	0x6002_8000	0x6002_8FFF	YES	YES	-	-
MCANC Message RAM	-	4	0x6003_0000	0x6003_0FFF	YES	YES	-	-
MCAND Message RAM	-	4	0x6003_8000	0x6003_8FFF	YES	YES	-	-
MCANE Message RAM	-	4	0x6004_0000	0x6004_0FFF	YES	YES	-	-
MCANF Message RAM	-	4	0x6004_8000	0x6004_8FFF	YES	YES	-	-
CPU1 DLT FIFO Regs		8	0x600F_8000	0x600F_9FFF	YES	YES	-	-
CPU2 DLT FIFO Regs		8	0x600F_A000	0x600F_BFFF	YES	YES	-	-
CPU3 DLT FIFO Regs		8	0x600F_C000	0x600F_DFFF	YES	YES	-	-
EMIF1 - SDRAM, CS0	No Burst Mode	262144	0x8000_0000	0x8FFF_FFFF	YES	YES	-	-
EMIF1 - ASYNC, CS2	No Burst Mode	65536	0x9000_0000	0x93FF_FFFF	YES	YES	-	-
EMIF1 - ASYNC, CS3	No Burst Mode	65536	0x9400_0000	0x97FF_FFFF	YES	YES	-	-
EMIF1 - ASYNC, CS4	No Burst Mode	65536	0x9800_0000	0x9BFF_FFFF	YES	YES	-	-
EMIF1 - SDRAM, CS0	With Burst Mode	262144	0xA000_0000	0xAFFF_FFFF	YES	YES	-	-
EMIF1 - ASYNC, CS2	With Burst Mode	65536	0xB000_0000	0xB3FF_FFFF	YES	YES	-	-
EMIF1 - ASYNC, CS3	With Burst Mode	65536	0xB400_0000	0xB7FF_FFFF	YES	YES	-	-
EMIF1 - ASYNC, CS4	With Burst Mode	65536	0xB800_0000	0xBBFF_FFFF	YES	YES	-	-

7.5.2 Flash Memory Map

The F29H85x and F29P58x devices feature up to 4MB of program Flash memory. Program Flash consists of interleaved pairs of 512KB Flash banks, with up to two interleaved pairs (4 banks total) each assigned to Flash Controller 1 (FLC1) and Flash Controller 2 (FLC2). There is also a single 256KB data bank present in FLC1. The Flash banks are notated according to the Flash Controller and bank number. For example, FLC2.B0/B1 refers to the first interleaved pair of banks (B0 and B1) in FLC2, while FLC1.B4 refers to the single data bank in FLC1.

Each Flash bank is made up of 2KB physical sectors. The nominal size (for example, 512KB) denotes the size of the MAIN region. In addition, each Flash bank includes two special regions:

- SECCFG, for storing SSU configuration settings, and
- BANKMGMT, for storing bank mode settings and firmware update metadata.

Flash memory on F29x devices can be addressed through multiple Flash Read Interfaces (FRIs), each with one or more read ports that address up to 1MB of Flash memory. The available FRIs are shown in Table 7-2. The actual Flash memory region that a read port addresses at a given time is dependent on the current system bank mode and swap configurations. For devices with CPU3 present, there are 4 bank modes available (0 to 3). For devices without CPU3 present, there are two bank modes available (0 to 1). CPU2 and CPU4 (if present) are secondary CPUs and cannot execute code directly from Flash.

Table 7-2. F29x Flash Read Interfaces

FLASH READ INTERFACE	DESCRIPTION
FRI-1	CPU1 program memory
FRI-2	CPU3 program memory
FRI-3	Firmware update region (FOTA/LFU)
FRI-4	Data Flash bank

The Flash bank mode is configured by the BANKMODE register in the SSU_GEN_REGS register aperture, and is loaded from the BANKMGMT sector of the active code bank pair in FLC1 during device boot. When CPU3, is present, BANKMODE values of 0 and 1 map all program Flash to CPU1, while BANKMODE values of 2 and 3 map half of the available program Flash to CPU1 and the other half to CPU3. The odd numbered BANKMODE values (1 and 3) enable firmware updates with A/B swap, allowing code to execute from one half of Flash while the other half can be programmed with updated code. When the CPU1SWAP or CPU3SWAP bit in the SSU_GEN_REGS.BANKMAP register is set, the hardware swaps the Flash banks such that the newly programmed banks replace the old banks at the same read port addresses. This feature can be used to implement Firmware-Over-The-Air update (FOTA) or Live Firmware Update (LFU) in the target system application.

Table 7-3. C29 Bank Modes

BANKMODE	Flash Mapping	Swap Enabled	1-CPU Devices
0	All program Flash mapped to CPU1	No	Available
1		Yes	Available
2	Program Flash memory is split between CPU1 and CPU3	No	N/A
3		Yes	N/A

For more information on Flash operation, see the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

7.5.2.1 Flash MAIN Region Address Map (F29H85x, 4MB)

The address mapping tables in this section apply to the following general part numbers: F29H850TU9, F29H859TU8, F29H850DU7, F29H859DU6.

Table 7-4. Flash MAIN Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1
	RP1	1MB	0x10100000	0x101FFFFF	FLC1.B2/B3
	RP2	1MB	0x10200000	0x102FFFFF	FLC2.B0/B1
	RP3	1MB	0x10300000	0x103FFFFF	FLC2.B2/B3
FRI-2 (CPU3 program)	RP0	1MB	0x10400000	0x104FFFFF	N/A
	RP1	1MB	0x10500000	0x105FFFFF	N/A
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	N/A
	RP1	1MB	0x10700000	0x107FFFFF	N/A

Table 7-5. Flash MAIN Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	1MB	0x10100000	0x101FFFFF	FLC2.B0/B1	FLC2.B2/B3
	RP2	1MB	0x10200000	0x102FFFFF	N/A	N/A
	RP3	1MB	0x10300000	0x103FFFFF	N/A	N/A
FRI-2 (CPU3 program)	RP0	1MB	0x10400000	0x104FFFFF	N/A	N/A
	RP1	1MB	0x10500000	0x105FFFFF	N/A	N/A
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	1MB	0x10700000	0x107FFFFF	FLC2.B2/B3	FLC2.B0/B1

Table 7-6. Flash MAIN Region Address Mapping (BANKMODE = 2)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1
	RP1	1MB	0x10100000	0x101FFFFF	FLC1.B2/B3
	RP2	1MB	0x10200000	0x102FFFFF	N/A
	RP3	1MB	0x10300000	0x103FFFFF	N/A
FRI-2 (CPU3 program)	RP0	1MB	0x10400000	0x104FFFFF	FLC2.B0/B1
	RP1	1MB	0x10500000	0x105FFFFF	FLC2.B2/B3
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	N/A
	RP1	1MB	0x10700000	0x107FFFFF	N/A

Table 7-7. Flash MAIN Region Address Mapping (BANKMODE = 3)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	1MB	0x10100000	0x101FFFFF	N/A	N/A
	RP2	1MB	0x10200000	0x102FFFFF	N/A	N/A
	RP3	1MB	0x10300000	0x103FFFFF	N/A	N/A
FRI-2 (CPU3 program)	RP0	1MB	0x10400000	0x104FFFFF	FLC2.B0/B1	FLC2.B2/B3
	RP1	1MB	0x10500000	0x105FFFFF	N/A	N/A
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	1MB	0x10700000	0x107FFFFF	FLC2.B2/B3	FLC2.B0/B1

ADVANCE INFORMATION

7.5.2.2 Flash MAIN Region Address Map (F29H85x, 2MB)

The address mapping tables in this section apply to the following general part numbers: F29H859TM8, F29H850DM7, F29H859DM6.

Table 7-8. Flash MAIN Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	512KB	0x10000000	0x1007FFFF	FLC1.B0/B1
	RP1	512KB	0x10100000	0x1017FFFF	FLC1.B2/B3
	RP2	512KB	0x10200000	0x1027FFFF	FLC2.B0/B1
	RP3	512KB	0x10300000	0x1037FFFF	FLC2.B2/B3
FRI-2 (CPU3 program)	RP0	512KB	0x10400000	0x1047FFFF	N/A
	RP1	512KB	0x10500000	0x1057FFFF	N/A
FRI-3 (Update region)	RP0	512KB	0x10600000	0x1067FFFF	N/A
	RP1	512KB	0x10700000	0x1077FFFF	N/A

Table 7-9. Flash MAIN Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	512KB	0x10000000	0x1007FFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	512KB	0x10100000	0x1017FFFF	FLC2.B0/B1	FLC2.B2/B3
	RP2	512KB	0x10200000	0x1027FFFF	N/A	N/A
	RP3	512KB	0x10300000	0x1037FFFF	N/A	N/A
FRI-2 (CPU3 program)	RP0	512KB	0x10400000	0x1047FFFF	N/A	N/A
	RP1	512KB	0x10500000	0x1057FFFF	N/A	N/A
FRI-3 (Update region)	RP0	512KB	0x10600000	0x1067FFFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	512KB	0x10700000	0x1077FFFF	FLC2.B2/B3	FLC2.B0/B1

Table 7-10. Flash MAIN Region Address Mapping (BANKMODE = 2)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	512KB	0x10000000	0x1007FFFF	FLC1.B0/B1
	RP1	512KB	0x10100000	0x1017FFFF	FLC1.B2/B3
	RP2	512KB	0x10200000	0x1027FFFF	N/A
	RP3	512KB	0x10300000	0x1037FFFF	N/A
FRI-2 (CPU3 program)	RP0	512KB	0x10400000	0x1047FFFF	FLC2.B0/B1
	RP1	512KB	0x10500000	0x1057FFFF	FLC2.B2/B3
FRI-3 (Update region)	RP0	512KB	0x10600000	0x1067FFFF	N/A
	RP1	512KB	0x10700000	0x1077FFFF	N/A

Table 7-11. Flash MAIN Region Address Mapping (BANKMODE = 3)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	512KB	0x10000000	0x1007FFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	512KB	0x10100000	0x1017FFFF	N/A	N/A
	RP2	512KB	0x10200000	0x1027FFFF	N/A	N/A
	RP3	512KB	0x10300000	0x1037FFFF	N/A	N/A
FRI-2 (CPU3 program)	RP0	512KB	0x10400000	0x1047FFFF	FLC2.B0/B1	FLC2.B2/B3
	RP1	512KB	0x10500000	0x1057FFFF	N/A	N/A
FRI-3 (Update region)	RP0	512KB	0x10600000	0x1067FFFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	512KB	0x10700000	0x1077FFFF	FLC2.B2/B3	FLC2.B0/B1

7.5.2.3 Flash MAIN Region Address Map (F29P58x, 4MB)

The address mapping tables in this section apply to the following general part number: F29P589DU5.

Table 7-12. Flash MAIN Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1
	RP1	1MB	0x10100000	0x101FFFFF	FLC1.B2/B3
	RP2	1MB	0x10200000	0x102FFFFF	FLC2.B0/B1
	RP3	1MB	0x10300000	0x103FFFFF	FLC2.B2/B3
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	N/A
	RP1	1MB	0x10700000	0x107FFFFF	N/A

Table 7-13. Flash MAIN Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	1MB	0x10100000	0x101FFFFF	FLC2.B0/B1	FLC2.B2/B3
	RP2	1MB	0x10200000	0x102FFFFF	N/A	N/A
	RP3	1MB	0x10300000	0x103FFFFF	N/A	N/A
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	1MB	0x10700000	0x107FFFFF	FLC2.B2/B3	FLC2.B0/B1

7.5.2.4 Flash MAIN Region Address Map (F29P58x, 2MB)

The address mapping tables in this section apply to the following general part numbers: F29P580DM5, F29P589DM5.

Table 7-14. Flash MAIN Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1
	RP1	1MB	0x10100000	0x101FFFFF	FLC1.B2/B3
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	N/A

Table 7-15. Flash MAIN Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	1MB	0x10000000	0x100FFFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	1MB	0x10100000	0x101FFFFF	N/A	N/A
FRI-3 (Update region)	RP0	1MB	0x10600000	0x106FFFFF	FLC1.B2/B3	FLC1.B0/B1

7.5.2.5 Flash MAIN Region Address MAP (F29P58x, 1MB)

The address mapping tables in this section apply to the following general part numbers: F29P580DM5, F29P589DM5.

Table 7-16. Flash MAIN Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	512KB	0x10000000	0x1007FFFF	FLC1.B0/B1
	RP1	512KB	0x10100000	0x1017FFFF	FLC1.B2/B3
FRI-3 (Update region)	RP0	512KB	0x10600000	0x1067FFFF	N/A

ADVANCE INFORMATION

Table 7-17. Flash MAIN Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	512KB	0x10000000	0x1007FFFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	512KB	0x10100000	0x1017FFFF	N/A	N/A
FRI-3 (Update region)	RP0	512KB	0x10600000	0x1067FFFF	FLC1.B2/B3	FLC1.B0/B1

7.5.2.6 Flash Data Bank Address Map

The following address map table applies to all part numbers.

Table 7-18. Flash Data Bank Address Mapping

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-4	RP0	256KB	0x10C00000	0x10C3FFFF	FLC1.B4

7.5.2.7 Flash BANKMGMT Region Address Map

The following address map tables apply to all part numbers.

Table 7-19. Flash BANKMGMT Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	4KB	0x10D80000	0x10D80FFF	FLC1.B0/B1
	RP1	4KB	0x10D84000	0x10D84FFF	FLC1.B2/B3
	RP2	4KB	0x10D88000	0x10D88FFF	FLC2.B0/B1
	RP3	4KB	0x10D8C000	0x10D8CFFF	FLC2.B2/B3
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D90000	0x10D90FFF	N/A
	RP1	4KB	0x10D94000	0x10D94FFF	N/A
FRI-3 (Update region)	RP0	4KB	0x10D98000	0x10D98FFF	N/A
	RP1	4KB	0x10D9C000	0x10D9CFFF	N/A

Table 7-20. Flash BANKMGMT Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	4KB	0x10D80000	0x10D80FFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	4KB	0x10D84000	0x10D84FFF	FLC2.B0/B1	FLC2.B2/B3
	RP2	4KB	0x10D88000	0x10D88FFF	N/A	N/A
	RP3	4KB	0x10D8C000	0x10D8CFFF	N/A	N/A
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D90000	0x10D90FFF	N/A	N/A
	RP1	4KB	0x10D94000	0x10D94FFF	N/A	N/A
FRI-3 (Update region)	RP0	4KB	0x10D98000	0x10D98FFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	4KB	0x10D9C000	0x10D9CFFF	FLC2.B2/B3	FLC2.B0/B1

Table 7-21. Flash BANKMGMT Region Address Mapping (BANKMODE = 2)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	4KB	0x10D80000	0x10D80FFF	FLC1.B0/B1
	RP1	4KB	0x10D84000	0x10D84FFF	FLC1.B2/B3
	RP2	4KB	0x10D88000	0x10D88FFF	N/A
	RP3	4KB	0x10D8C000	0x10D8CFFF	N/A
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D90000	0x10D90FFF	FLC2.B0/B1
	RP1	4KB	0x10D94000	0x10D94FFF	FLC2.B2/B3
FRI-3 (Update region)	RP0	4KB	0x10D98000	0x10D98FFF	N/A
	RP1	4KB	0x10D9C000	0x10D9CFFF	N/A

ADVANCE INFORMATION

Table 7-22. Flash BANKMGMT Region Address Mapping (BANKMODE = 3)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	4KB	0x10D80000	0x10D80FFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	4KB	0x10D84000	0x10D84FFF	N/A	N/A
	RP2	4KB	0x10D88000	0x10D88FFF	N/A	N/A
	RP3	4KB	0x10D8C000	0x10D8CFFF	N/A	N/A
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D90000	0x10D90FFF	FLC2.B0/B1	FLC2.B2/B3
	RP1	4KB	0x10D94000	0x10D94FFF	N/A	N/A
FRI-3 (Update region)	RP0	4KB	0x10D98000	0x10D98FFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	4KB	0x10D9C000	0x10D9CFFF	FLC2.B2/B3	FLC2.B0/B1

(1) FRI-2/CPU3 not available on F29P58x devices.

7.5.2.8 Flash SECCFG Region Address Map

The following address map tables apply to all part numbers.

Table 7-23. Flash SECCFG Region Address Mapping (BANKMODE = 0)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	4KB	0x10D81000	0x10D81FFF	FLC1.B0/B1
	RP1	4KB	0x10D85000	0x10D85FFF	FLC1.B2/B3
	RP2	4KB	0x10D89000	0x10D89FFF	FLC2.B0/B1
	RP3	4KB	0x10D8D000	0x10D8DFFF	FLC2.B2/B3
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D91000	0x10D91FFF	N/A
	RP1	4KB	0x10D95000	0x10D95FFF	N/A
FRI-3 (Update region)	RP0	4KB	0x10D99000	0x10D99FFF	N/A
	RP1	4KB	0x10D9D000	0x10D9DFFF	N/A

Table 7-24. Flash SECCFG Region Address Mapping (BANKMODE = 1)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	4KB	0x10D81000	0x10D81FFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	4KB	0x10D85000	0x10D85FFF	FLC2.B0/B1	FLC2.B2/B3
	RP2	4KB	0x10D89000	0x10D89FFF	N/A	N/A
	RP3	4KB	0x10D8D000	0x10D8DFFF	N/A	N/A
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D91000	0x10D91FFF	N/A	N/A
	RP1	4KB	0x10D95000	0x10D95FFF	N/A	N/A
FRI-3 (Update region)	RP0	4KB	0x10D99000	0x10D99FFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	4KB	0x10D9D000	0x10D9DFFF	FLC2.B2/B3	FLC2.B0/B1

Table 7-25. Flash SECCFG Region Address Mapping (BANKMODE = 2)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS
FRI-1 (CPU1 program)	RP0	4KB	0x10D81000	0x10D81FFF	FLC1.B0/B1
	RP1	4KB	0x10D85000	0x10D85FFF	FLC1.B2/B3
	RP2	4KB	0x10D89000	0x10D89FFF	N/A
	RP3	4KB	0x10D8D000	0x10D8DFFF	N/A
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D91000	0x10D91FFF	FLC2.B0/B1
	RP1	4KB	0x10D95000	0x10D95FFF	FLC2.B2/B3
FRI-3 (Update region)	RP0	4KB	0x10D99000	0x10D99FFF	N/A
	RP1	4KB	0x10D9D000	0x10D9DFFF	N/A

ADVANCE INFORMATION

Table 7-26. Flash SECCFG Region Address Mapping (BANKMODE = 3)

FRI	READ PORT	SIZE	START ADDRESS	END ADDRESS	FLASH BANKS (SWAP = 0)	FLASH BANKS (SWAP = 1)
FRI-1 (CPU1 program)	RP0	4KB	0x10D81000	0x10D81FFF	FLC1.B0/B1	FLC1.B2/B3
	RP1	4KB	0x10D85000	0x10D85FFF	N/A	N/A
	RP2	4KB	0x10D89000	0x10D89FFF	N/A	N/A
	RP3	4KB	0x10D8D000	0x10D8DFFF	N/A	N/A
FRI-2 (CPU3 program)(1)	RP0	4KB	0x10D91000	0x10D91FFF	FLC2.B0/B1	FLC2.B2/B3
	RP1	4KB	0x10D95000	0x10D95FFF	N/A	N/A
FRI-3 (Update region)	RP0	4KB	0x10D99000	0x10D99FFF	FLC1.B2/B3	FLC1.B0/B1
	RP1	4KB	0x10D9D000	0x10D9DFFF	FLC2.B2/B3	FLC2.B0/B1

(1) FRI-2/CPU3 not available on F29P58x devices.

ADVANCE INFORMATION

7.5.3 Peripheral Registers Memory Map

Table 7-27. Peripheral Registers Memory Map

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
vbusp_config									
RTDMA_REGS	RTDMA1_BASE	0x301C_0000	-	YES	YES	YES	-	-	YES
RTDMA_DIAG_REGS	RTDMA1_DIAG_BASE	0x301C_0800	-	YES	YES	YES	-	-	YES
RTDMA_SELFTEST_REGS	RTDMA1_SELFTEST_BASE	0x301C_0C00	-	YES	YES	YES	-	-	YES
RTDMA_MPU_REGS	RTDMA1_MPU_BASE	0x301C_1000	-	YES	YES	YES	-	-	YES
RTDMA_REGS	RTDMA2_BASE	0x301C_8000	-	YES	YES	YES	-	-	YES
RTDMA_DIAG_REGS	RTDMA2_DIAG_BASE	0x301C_8800	-	YES	YES	YES	-	-	YES
RTDMA_SELFTEST_REGS	RTDMA2_SELFTEST_BASE	0x301C_8C00	-	YES	YES	YES	-	-	YES
RTDMA_MPU_REGS	RTDMA2_MPU_BASE	0x301C_9000	-	YES	YES	YES	-	-	YES
FRI_CTRL_REGS	FRI1_BASE	0x301D_0000	-	YES	YES	YES	-	-	YES
MEMSS_L_CONFIG_REGS	MEMSSLCFG_BASE	0x301D_8000	-	YES	YES	YES	-	-	YES
MEMSS_C_CONFIG_REGS	MEMSSCCFG_BASE	0x301D_8400	-	YES	YES	YES	-	-	YES
MEMSS_M_CONFIG_REGS	MEMSSMCFG_BASE	0x301D_8800	-	YES	YES	YES	-	-	YES
MEMSS_MISCI_REGS	MEMSSMISCI_BASE	0x301D_8E00	-	YES	YES	YES	-	-	YES
SYNCBRIDGEMPU_REGS	SYNCBRIDGEMPU_BASE	0x301E_0000	-	YES	YES	YES	-	-	YES
INPUT_XBAR_REGS	INPUTXBAR_BASE	0x301E_8000	-	YES	YES	YES	-	-	YES
EPWM_XBAR_REGS	EPWMXBAR_BASE	0x301E_9000	-	YES	YES	YES	-	-	YES
CLB_XBAR_REGS	CLBXBAR_BASE	0x301E_A000	-	YES	YES	YES	-	-	YES
OUTPUTXBAR_REGS	OUTPUTXBAR_BASE	0x301E_B000	-	YES	YES	YES	-	-	YES
MDL_XBAR_REGS	MDLXBAR_BASE	0x301E_C000	-	YES	YES	YES	-	-	YES
ICL_XBAR_REGS	ICLXBAR_BASE	0x301E_D000	-	YES	YES	YES	-	-	YES
LCM_REGS	LCM_DMA_BASE	0x301F_4000	-	YES	YES	YES	-	-	YES
c29bus									
ADC_RESULT_REGS	ADCARESULT_BASE	0x303C_0000	-	YES	YES	YES	YES	YES	-
ADC_RESULT_REGS	ADCBRESULT_BASE	0x303C_1000	-	YES	YES	YES	YES	YES	-
ADC_RESULT_REGS	ADCCRESULT_BASE	0x303C_2000	-	YES	YES	YES	YES	YES	-
ADC_RESULT_REGS	ADCDRESULT_BASE	0x303C_3000	-	YES	YES	YES	YES	YES	-
ADC_RESULT_REGS	ADCERESULT_BASE	0x303C_4000	-	YES	YES	YES	YES	YES	-
EMIF_REGS	EMIF1_BASE	0x3080_0000	-	YES	YES	YES	-	-	-
vbus32_config									
DEV_CFG_REGS	DEVCFG_BASE	0x3018_0000	-	YES	YES	YES	-	-	YES
ANALOG_SUBSYS_REGS	ANALOGSUBSYS_BASE	0x3018_2000	-	YES	YES	YES	-	-	YES

ADVANCE INFORMATION

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
GPIO_CTRL_REGS	GPIOCTRL_BASE	0x3019_0000	-	YES	YES	YES	-	-	YES
IPC_COUNTER_REGS	IPCCOUNTER_BASE	0x301B_0000	-	YES	YES	YES	-	-	YES
vbusp_prog									
FLASH_CMD_REGS_FLC1	FLASHCONTROLLER1_BASE	0x3010_0000	-	YES	-	YES	-	-	YES
FLASH_CMD_REGS_FLC2	FLASHCONTROLLER2_BASE	0x3011_0000	-	YES	-	YES	-	-	YES
HSM_ERROR_AGGREGATOR_CONFIG_REGS	HSMERRORAGGREGATOR_BASE	0x3012_0000	-	-	-	-	-	-	YES
vbus32_ethercat									
ESCSS_REGS	ESC_SS_BASE	0x3038_8000	-	YES	YES	YES	YES	YES	-
ESCSS_CONFIG_REGS	ESC_SS_CONFIG_BASE	0x3038_8200	-	YES	YES	YES	YES	YES	-
vbusp_cpu1, vbusp_cpu2, vbusp_cpu3									
C29_RTINT_STACK	C29CPURTINTSTACK_BASE	0x3000_8000	-	YES	YES	YES	-	-	-
C29_SECCALL_STACK	C29CPUSECCALLSTACK_BASE	0x3000_C000	-	YES	YES	YES	-	-	-
C29_SECURE_REGS	C29CPUSECURE_BASE	0x3000_D000	-	YES	YES	YES	-	-	-
C29_DIAG_REGS	C29CPUDIAG_BASE	0x3000_E000	-	YES	YES	YES	-	-	-
C29_SELFTEST_REGS	C29CPUSELFTEST_BASE	0x3000_F000	-	YES	YES	YES	-	-	-
DLT_CORE_REGS	CPUDLT_BASE	0x3001_0000	-	YES	YES	YES	-	-	-
PIPE_REGS	PIPE_BASE	0x3002_0000	-	YES	YES	YES	-	-	-
ERAD_REGS	ERAD_BASE	0x3003_0000	-	YES	YES	YES	-	-	-
vbusp_frame0									
RTDMA_CH_REGS	RTDMA1CH1_BASE	0x6000_0000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH2_BASE	0x6000_1000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH3_BASE	0x6000_2000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH4_BASE	0x6000_3000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH5_BASE	0x6000_4000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH6_BASE	0x6000_5000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH7_BASE	0x6000_6000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH8_BASE	0x6000_7000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH9_BASE	0x6000_8000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA1CH10_BASE	0x6000_9000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH1_BASE	0x6001_0000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH2_BASE	0x6001_1000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH3_BASE	0x6001_2000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH4_BASE	0x6001_3000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH5_BASE	0x6001_4000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH6_BASE	0x6001_5000	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
RTDMA_CH_REGS	RTDMA2CH7_BASE	0x6001_6000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH8_BASE	0x6001_7000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH9_BASE	0x6001_8000	YES	YES	YES	YES	YES	YES	-
RTDMA_CH_REGS	RTDMA2CH10_BASE	0x6001_9000	YES	YES	YES	YES	YES	YES	-
MCANSS_REGS	MCANSSA_BASE	0x6002_4000	YES	YES	YES	YES	YES	YES	-
MCAN_REGS	MCANA_BASE	0x6002_4600	YES	YES	YES	YES	YES	YES	-
MCAN_ERROR_REGS	MCANA_ERROR_BASE	0x6002_4800	YES	YES	YES	YES	YES	YES	-
MCANSS_REGS	MCANBSS_BASE	0x6002_C000	YES	YES	YES	YES	YES	YES	-
MCAN_REGS	MCANB_BASE	0x6002_C600	YES	YES	YES	YES	YES	YES	-
MCAN_ERROR_REGS	MCANB_ERROR_BASE	0x6002_C800	YES	YES	YES	YES	YES	YES	-
MCANSS_REGS	MCANCSS_BASE	0x6003_4000	YES	YES	YES	YES	YES	YES	-
MCAN_REGS	MCANC_BASE	0x6003_4600	YES	YES	YES	YES	YES	YES	-
MCAN_ERROR_REGS	MCANC_ERROR_BASE	0x6003_4800	YES	YES	YES	YES	YES	YES	-
MCANSS_REGS	MCANDSS_BASE	0x6003_C000	YES	YES	YES	YES	YES	YES	-
MCAN_REGS	MCAND_BASE	0x6003_C600	YES	YES	YES	YES	YES	YES	-
MCAN_ERROR_REGS	MCAND_ERROR_BASE	0x6003_C800	YES	YES	YES	YES	YES	YES	-
MCANSS_REGS	MCANESS_BASE	0x6004_4000	YES	YES	YES	YES	YES	YES	-
MCAN_REGS	MCANE_BASE	0x6004_4600	YES	YES	YES	YES	YES	YES	-
MCAN_ERROR_REGS	MCANE_ERROR_BASE	0x6004_4800	YES	YES	YES	YES	YES	YES	-
MCANSS_REGS	MCANFSS_BASE	0x6004_C000	YES	YES	YES	YES	YES	YES	-
MCAN_REGS	MCANF_BASE	0x6004_C600	YES	YES	YES	YES	YES	YES	-
MCAN_ERROR_REGS	MCANF_ERROR_BASE	0x6004_C800	YES	YES	YES	YES	YES	YES	-
LIN_REGS	LINA_BASE	0x6006_0000	YES	YES	YES	YES	YES	YES	-
LIN_REGS	LINB_BASE	0x6006_1000	YES	YES	YES	YES	YES	YES	-
SENT_CFG	SENT1CSENT_BASE	0x6006_8000	YES	YES	YES	YES	YES	YES	-
SENT_MEM	SENT1MEM_BASE	0x6006_8400	YES	YES	YES	YES	YES	YES	-
SENT_MTPG	SENT1MTPG_BASE	0x6006_8800	YES	YES	YES	YES	YES	YES	-
SENT_CFG	SENT2CSENT_BASE	0x6006_9000	YES	YES	YES	YES	YES	YES	-
SENT_MEM	SENT2MEM_BASE	0x6006_9400	YES	YES	YES	YES	YES	YES	-
SENT_MTPG	SENT2MTPG_BASE	0x6006_9800	YES	YES	YES	YES	YES	YES	-
SENT_CFG	SENT3CSENT_BASE	0x6006_A000	YES	YES	YES	YES	YES	YES	-
SENT_MEM	SENT3MEM_BASE	0x6006_A400	YES	YES	YES	YES	YES	YES	-
SENT_MTPG	SENT3MTPG_BASE	0x6006_A800	YES	YES	YES	YES	YES	YES	-
SENT_CFG	SENT4CSENT_BASE	0x6006_B000	YES	YES	YES	YES	YES	YES	-
SENT_MEM	SENT4MEM_BASE	0x6006_B400	YES	YES	YES	YES	YES	YES	-

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
SENT_MTPG	SENT4MTPG_BASE	0x6006_B800	YES	YES	YES	YES	YES	YES	-
SENT_CFG	SENT5CSENT_BASE	0x6006_C000	YES	YES	YES	YES	YES	YES	-
SENT_MEM	SENT5MEM_BASE	0x6006_C400	YES	YES	YES	YES	YES	YES	-
SENT_MTPG	SENT5MTPG_BASE	0x6006_C800	YES	YES	YES	YES	YES	YES	-
SENT_CFG	SENT6CSENT_BASE	0x6006_D000	YES	YES	YES	YES	YES	YES	-
SENT_MEM	SENT6MEM_BASE	0x6006_D400	YES	YES	YES	YES	YES	YES	-
SENT_MTPG	SENT6MTPG_BASE	0x6006_D800	YES	YES	YES	YES	YES	YES	-
UART_REGS, UART_REGS_WRITE	UARTA_BASE, UARTA_WRITE_BASE	0x6007_0000	YES	YES	YES	YES	YES	YES	-
UART_REGS, UART_REGS_WRITE	UARTB_BASE, UARTB_WRITE_BASE	0x6007_2000	YES	YES	YES	YES	YES	YES	-
UART_REGS, UART_REGS_WRITE	UARTC_BASE, UARTC_WRITE_BASE	0x6007_4000	YES	YES	YES	YES	YES	YES	-
UART_REGS, UART_REGS_WRITE	UARTD_BASE, UARTD_WRITE_BASE	0x6007_6000	YES	YES	YES	YES	YES	YES	-
UART_REGS, UART_REGS_WRITE	UARTE_BASE, UARTE_WRITE_BASE	0x6007_8000	YES	YES	YES	YES	YES	YES	-
UART_REGS, UART_REGS_WRITE	UARTF_BASE, UARTF_WRITE_BASE	0x6007_A000	YES	YES	YES	YES	YES	YES	-
DCC_REGS	DCC1_BASE	0x6008_0000	YES	YES	YES	YES	YES	YES	-
DCC_REGS	DCC2_BASE	0x6008_1000	YES	YES	YES	YES	YES	YES	-
DCC_REGS	DCC3_BASE	0x6008_2000	YES	YES	YES	YES	YES	YES	-
ERROR_AGGREGATOR_CONFIG_REGS	ERRORAGGREGATOR_BASE	0x6008_C000	YES	YES	YES	YES	YES	YES	-
ESM_CPU_REGS	ESMCPU1_BASE	0x6009_0000	YES	YES	YES	YES	YES	YES	-
ESM_CPU_REGS	ESMCPU2_BASE	0x6009_1000	YES	YES	YES	YES	YES	YES	-
ESM_CPU_REGS	ESMCPU3_BASE	0x6009_2000	YES	YES	YES	YES	YES	YES	-
ESM_SYSTEM_REGS	ESMSYSTEM_BASE	0x6009_F000	YES	YES	YES	YES	YES	YES	-
ESM_SAFETYAGG_REGS	ESMSAFETYAGG_BASE	0x600A_0000	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI1BLK1CONFIG_BASE	0x600B_0000	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI1BLK2CONFIG_BASE	0x600B_0100	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI1BLK3CONFIG_BASE	0x600B_0200	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI1BLK4CONFIG_BASE	0x600B_0300	YES	YES	YES	YES	YES	YES	-
WADI_OPER_SSS_REGS	WADI1OPERSSS_BASE	0x600B_1000	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI2BLK1CONFIG_BASE	0x600B_2000	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI2BLK2CONFIG_BASE	0x600B_2100	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI2BLK3CONFIG_BASE	0x600B_2200	YES	YES	YES	YES	YES	YES	-
WADI_CONFIG_REGS	WADI2BLK4CONFIG_BASE	0x600B_2300	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
WADI_OPER_SSS_REGS	WADI2OPERSSS_BASE	0x600B_3000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR1_FLAGS_BASE	0x600C_0000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR2_FLAGS_BASE	0x600C_1000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR3_FLAGS_BASE	0x600C_2000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR4_FLAGS_BASE	0x600C_3000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR5_FLAGS_BASE	0x600C_4000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR6_FLAGS_BASE	0x600C_5000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR7_FLAGS_BASE	0x600C_6000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR8_FLAGS_BASE	0x600C_7000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR9_FLAGS_BASE	0x600C_8000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR10_FLAGS_BASE	0x600C_9000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR11_FLAGS_BASE	0x600C_A000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR12_FLAGS_BASE	0x600C_B000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR13_FLAGS_BASE	0x600C_C000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR14_FLAGS_BASE	0x600C_D000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR15_FLAGS_BASE	0x600C_E000	YES	YES	YES	YES	YES	YES	-
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR16_FLAGS_BASE	0x600C_F000	YES	YES	YES	YES	YES	YES	-
XBAR_REGS	XBAR_BASE	0x600E_0000	YES	YES	YES	YES	YES	YES	-
DLT_FIFO_REGS	CPU1DLTFIFO_BASE	0x600F_8000	YES	YES	YES	YES	YES	YES	-
DLT_FIFO_REGS	CPU2DLTFIFO_BASE	0x600F_A000	YES	YES	YES	YES	YES	YES	-
DLT_FIFO_REGS	CPU3DLTFIFO_BASE	0x600F_C000	YES	YES	YES	YES	YES	YES	-
vbus32_ap_cpu1, vbus32_ap_cpu2, vbus32_ap_cpu3									
CPU_SYS_REGS	CPUSYS_BASE	0x3020_0000	-	YES	YES	YES	-	-	-
CPU_PER_CFG_REGS	CPUPERCFG_BASE	0x3020_8000	-	YES	YES	YES	-	-	-
WD_REGS	WD_BASE	0x3020_8C00	-	YES	YES	YES	-	-	-

ADVANCE INFORMATION

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
CPUTIMER_REGS	CPUTIMER0_BASE	0x3021_8000	-	YES	YES	YES	-	-	-
CPUTIMER_REGS	CPUTIMER1_BASE	0x3021_9000	-	YES	YES	YES	-	-	-
CPUTIMER_REGS	CPUTIMER2_BASE	0x3021_A000	-	YES	YES	YES	-	-	-
CPU1_IPC_SEND_REGS	CPU1IPCSEND_BASE	0x3022_0000	-	YES	YES	YES	-	-	-
CPU2_IPC_SEND_REGS	CPU2IPCSEND_BASE	0x3022_8000	-	YES	YES	YES	-	-	-
CPU3_IPC_SEND_REGS	CPU3IPCSEND_BASE	0x3023_0000	-	YES	YES	YES	-	-	-
CPU1_IPC_RCV_REGS	CPU1IPCRCV_BASE	0x3024_0000	-	YES	YES	YES	-	-	-
CPU2_IPC_RCV_REGS	CPU2IPCRCV_BASE	0x3024_8000	-	YES	YES	YES	-	-	-
CPU3_IPC_RCV_REGS	CPU3IPCRCV_BASE	0x3025_0000	-	YES	YES	YES	-	-	-
GPIO_DATA_REGS	GPIODATA_BASE	0x3026_8000	-	YES	YES	YES	-	-	-
GPIO_DATA_READ_REGS	GPIODATAREAD_BASE	0x3026_9000	-	YES	YES	YES	-	-	-
XINT_REGS	XINT_BASE	0x3027_0000	-	YES	YES	YES	-	-	-
vbusp_cpu1									
SECAP_HANDLER_REGS	C29DEBUGSS_BASE	0x3001_8000	-	YES	-	-	-	-	-
LCM_REGS	LCM_CPU_BASE	0x3003_2000	-	YES	-	-	-	-	-
vbus32_frame0									
EPWM_REGS	EPWM1_BASE	0x7000_0000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM1XCMP_BASE	0x7000_0400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM1DE_BASE	0x7000_0800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM1MINDBLUT_BASE	0x7000_0C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM2_BASE	0x7000_1000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM2XCMP_BASE	0x7000_1400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM2DE_BASE	0x7000_1800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM2MINDBLUT_BASE	0x7000_1C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM3_BASE	0x7000_2000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM3XCMP_BASE	0x7000_2400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM3DE_BASE	0x7000_2800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM3MINDBLUT_BASE	0x7000_2C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM4_BASE	0x7000_3000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM4XCMP_BASE	0x7000_3400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM4DE_BASE	0x7000_3800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM4MINDBLUT_BASE	0x7000_3C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM5_BASE	0x7000_4000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM5XCMP_BASE	0x7000_4400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM5DE_BASE	0x7000_4800	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
MINDB_LUT_REGS	EPWM5MINDBLUT_BASE	0x7000_4C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM6_BASE	0x7000_5000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM6XCMP_BASE	0x7000_5400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM6DE_BASE	0x7000_5800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM6MINDBLUT_BASE	0x7000_5C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM7_BASE	0x7000_6000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM7XCMP_BASE	0x7000_6400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM7DE_BASE	0x7000_6800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM7MINDBLUT_BASE	0x7000_6C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM8_BASE	0x7000_7000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM8XCMP_BASE	0x7000_7400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM8DE_BASE	0x7000_7800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM8MINDBLUT_BASE	0x7000_7C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM9_BASE	0x7000_8000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM9XCMP_BASE	0x7000_8400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM9DE_BASE	0x7000_8800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM9MINDBLUT_BASE	0x7000_8C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM10_BASE	0x7000_9000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM10XCMP_BASE	0x7000_9400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM10DE_BASE	0x7000_9800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM10MINDBLUT_BASE	0x7000_9C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM11_BASE	0x7000_A000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM11XCMP_BASE	0x7000_A400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM11DE_BASE	0x7000_A800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM11MINDBLUT_BASE	0x7000_AC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM12_BASE	0x7000_B000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM12XCMP_BASE	0x7000_B400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM12DE_BASE	0x7000_B800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM12MINDBLUT_BASE	0x7000_BC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM13_BASE	0x7000_C000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM13XCMP_BASE	0x7000_C400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM13DE_BASE	0x7000_C800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM13MINDBLUT_BASE	0x7000_CC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM14_BASE	0x7000_D000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM14XCMP_BASE	0x7000_D400	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
DE_REGS	EPWM14DE_BASE	0x7000_D800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM14MINDBLUT_BASE	0x7000_DC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM15_BASE	0x7000_E000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM15XCMP_BASE	0x7000_E400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM15DE_BASE	0x7000_E800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM15MINDBLUT_BASE	0x7000_EC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM16_BASE	0x7000_F000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM16XCMP_BASE	0x7000_F400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM16DE_BASE	0x7000_F800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM16MINDBLUT_BASE	0x7000_FC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM17_BASE	0x7001_0000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM17XCMP_BASE	0x7001_0400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM17DE_BASE	0x7001_0800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM17MINDBLUT_BASE	0x7001_0C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM18_BASE	0x7001_1000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM18XCMP_BASE	0x7001_1400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM18DE_BASE	0x7001_1800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM18MINDBLUT_BASE	0x7001_1C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM1XLINK_BASE	0x7004_0000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM1XCMPXLINK_BASE	0x7004_0400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM1DEXLINK_BASE	0x7004_0800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM1MINDBLUTXLINK_BASE	0x7004_0C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM2XLINK_BASE	0x7004_1000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM2XCMPXLINK_BASE	0x7004_1400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM2DEXLINK_BASE	0x7004_1800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM2MINDBLUTXLINK_BASE	0x7004_1C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM3XLINK_BASE	0x7004_2000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM3XCMPXLINK_BASE	0x7004_2400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM3DEXLINK_BASE	0x7004_2800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM3MINDBLUTXLINK_BASE	0x7004_2C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM4XLINK_BASE	0x7004_3000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM4XCMPXLINK_BASE	0x7004_3400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM4DEXLINK_BASE	0x7004_3800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM4MINDBLUTXLINK_BASE	0x7004_3C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM5XLINK_BASE	0x7004_4000	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
EPWM_XCMP_REGS	EPWM5XCMPXLINK_BASE	0x7004_4400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM5DEXLINK_BASE	0x7004_4800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM5MINDBLUTXLINK_BASE	0x7004_4C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM6XLINK_BASE	0x7004_5000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM6XCMPXLINK_BASE	0x7004_5400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM6DEXLINK_BASE	0x7004_5800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM6MINDBLUTXLINK_BASE	0x7004_5C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM7XLINK_BASE	0x7004_6000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM7XCMPXLINK_BASE	0x7004_6400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM7DEXLINK_BASE	0x7004_6800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM7MINDBLUTXLINK_BASE	0x7004_6C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM8XLINK_BASE	0x7004_7000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM8XCMPXLINK_BASE	0x7004_7400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM8DEXLINK_BASE	0x7004_7800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM8MINDBLUTXLINK_BASE	0x7004_7C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM9XLINK_BASE	0x7004_8000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM9XCMPXLINK_BASE	0x7004_8400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM9DEXLINK_BASE	0x7004_8800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM9MINDBLUTXLINK_BASE	0x7004_8C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM10XLINK_BASE	0x7004_9000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM10XCMPXLINK_BASE	0x7004_9400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM10DEXLINK_BASE	0x7004_9800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM10MINDBLUTXLINK_BASE	0x7004_9C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM11XLINK_BASE	0x7004_A000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM11XCMPXLINK_BASE	0x7004_A400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM11DEXLINK_BASE	0x7004_A800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM11MINDBLUTXLINK_BASE	0x7004_AC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM12XLINK_BASE	0x7004_B000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM12XCMPXLINK_BASE	0x7004_B400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM12DEXLINK_BASE	0x7004_B800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM12MINDBLUTXLINK_BASE	0x7004_BC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM13XLINK_BASE	0x7004_C000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM13XCMPXLINK_BASE	0x7004_C400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM13DEXLINK_BASE	0x7004_C800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM13MINDBLUTXLINK_BASE	0x7004_CC00	YES	YES	YES	YES	YES	YES	-

ADVANCE INFORMATION

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
EPWM_REGS	EPWM14XLINK_BASE	0x7004_D000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM14XCMPXLINK_BASE	0x7004_D400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM14DEXLINK_BASE	0x7004_D800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM14MINDBLUTXLINK_BASE	0x7004_DC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM15XLINK_BASE	0x7004_E000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM15XCMPXLINK_BASE	0x7004_E400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM15DEXLINK_BASE	0x7004_E800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM15MINDBLUTXLINK_BASE	0x7004_EC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM16XLINK_BASE	0x7004_F000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM16XCMPXLINK_BASE	0x7004_F400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM16DEXLINK_BASE	0x7004_F800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM16MINDBLUTXLINK_BASE	0x7004_FC00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM17XLINK_BASE	0x7005_0000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM17XCMPXLINK_BASE	0x7005_0400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM17DEXLINK_BASE	0x7005_0800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM17MINDBLUTXLINK_BASE	0x7005_0C00	YES	YES	YES	YES	YES	YES	-
EPWM_REGS	EPWM18XLINK_BASE	0x7005_1000	YES	YES	YES	YES	YES	YES	-
EPWM_XCMP_REGS	EPWM18XCMPXLINK_BASE	0x7005_1400	YES	YES	YES	YES	YES	YES	-
DE_REGS	EPWM18DEXLINK_BASE	0x7005_1800	YES	YES	YES	YES	YES	YES	-
MINDB_LUT_REGS	EPWM18MINDBLUTXLINK_BASE	0x7005_1C00	YES	YES	YES	YES	YES	YES	-
HRPWMCAL_REGS	HRPWMCAL1_BASE	0x7008_0000	YES	YES	YES	YES	YES	YES	-
HRPWMCAL_REGS	HRPWMCAL2_BASE	0x7008_1000	YES	YES	YES	YES	YES	YES	-
HRPWMCAL_REGS	HRPWMCAL3_BASE	0x7008_2000	YES	YES	YES	YES	YES	YES	-
EQEP_REGS	EQEP1_BASE	0x7008_8000	YES	YES	YES	YES	YES	YES	-
EQEP_REGS	EQEP2_BASE	0x7008_9000	YES	YES	YES	YES	YES	YES	-
EQEP_REGS	EQEP3_BASE	0x7008_A000	YES	YES	YES	YES	YES	YES	-
EQEP_REGS	EQEP4_BASE	0x7008_B000	YES	YES	YES	YES	YES	YES	-
EQEP_REGS	EQEP5_BASE	0x7008_C000	YES	YES	YES	YES	YES	YES	-
EQEP_REGS	EQEP6_BASE	0x7008_D000	YES	YES	YES	YES	YES	YES	-
SDFM_REGS	SDFM1_BASE	0x7009_0000	YES	YES	YES	YES	YES	YES	-
SDFM_REGS	SDFM2_BASE	0x7009_1000	YES	YES	YES	YES	YES	YES	-
SDFM_REGS	SDFM3_BASE	0x7009_2000	YES	YES	YES	YES	YES	YES	-
SDFM_REGS	SDFM4_BASE	0x7009_3000	YES	YES	YES	YES	YES	YES	-
ADC_REGS	ADCA_BASE	0x700A_0000	YES	YES	YES	YES	YES	YES	-
ADC_REGS	ADCB_BASE	0x700A_1000	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
ADC_REGS	ADCC_BASE	0x700A_2000	YES	YES	YES	YES	YES	YES	-
ADC_REGS	ADCD_BASE	0x700A_3000	YES	YES	YES	YES	YES	YES	-
ADC_REGS	ADCE_BASE	0x700A_4000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK1_BASE	0x700B_0000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK2_BASE	0x700B_1000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK3_BASE	0x700B_2000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK4_BASE	0x700B_3000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK5_BASE	0x700B_4000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK6_BASE	0x700B_5000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK7_BASE	0x700B_6000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK8_BASE	0x700B_7000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK9_BASE	0x700B_8000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_REGS	ADCSAFETYCHECK10_BASE	0x700B_9000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_INTEVT_REGS	ADCSAFETYCHECKINTEVT1_BASE	0x700C_0000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_INTEVT_REGS	ADCSAFETYCHECKINTEVT2_BASE	0x700C_1000	YES	YES	YES	YES	YES	YES	-
ADC_SAFECHECK_INTEVT_REGS	ADCSAFETYCHECKINTEVT3_BASE	0x700C_2000	YES	YES	YES	YES	YES	YES	-
ADC_GLOBAL_REGS	ADCGLOBAL_BASE	0x700C_8000	YES	YES	YES	YES	YES	YES	-
DAC_REGS	DACA_BASE	0x700D_0000	YES	YES	YES	YES	YES	YES	-
DAC_REGS	DACB_BASE	0x700D_1000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS1_BASE	0x700E_0000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS2_BASE	0x700E_1000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS3_BASE	0x700E_2000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS4_BASE	0x700E_3000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS5_BASE	0x700E_4000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS6_BASE	0x700E_5000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS7_BASE	0x700E_6000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS8_BASE	0x700E_7000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS9_BASE	0x700E_8000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS10_BASE	0x700E_9000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS11_BASE	0x700E_A000	YES	YES	YES	YES	YES	YES	-
CMPSS_REGS	CMPSS12_BASE	0x700E_B000	YES	YES	YES	YES	YES	YES	-
ECAP_REGS	ECAP1_BASE	0x7010_0000	YES	YES	YES	YES	YES	YES	-
ECAP_SIGNAL_MONITORING	ECAP1SIGNALMONITORING_BASE	0x7010_0080	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
ECAP_REGS	ECAP2_BASE	0x7010_1000	YES	YES	YES	YES	YES	YES	-
ECAP_SIGNAL_MONITORING	ECAP2SIGNALMONITORING_BASE	0x7010_1080	YES	YES	YES	YES	YES	YES	-
ECAP_REGS	ECAP3_BASE	0x7010_2000	YES	YES	YES	YES	YES	YES	-
ECAP_SIGNAL_MONITORING	ECAP3SIGNALMONITORING_BASE	0x7010_2080	YES	YES	YES	YES	YES	YES	-
ECAP_REGS	ECAP4_BASE	0x7010_3000	YES	YES	YES	YES	YES	YES	-
ECAP_SIGNAL_MONITORING	ECAP4SIGNALMONITORING_BASE	0x7010_3080	YES	YES	YES	YES	YES	YES	-
ECAP_REGS	ECAP5_BASE	0x7010_4000	YES	YES	YES	YES	YES	YES	-
HRCAP_REGS	HRCAP5_BASE	0x7010_4040	YES	YES	YES	YES	YES	YES	-
ECAP_SIGNAL_MONITORING	ECAP5SIGNALMONITORING_BASE	0x7010_4080	YES	YES	YES	YES	YES	YES	-
ECAP_REGS	ECAP6_BASE	0x7010_5000	YES	YES	YES	YES	YES	YES	-
HRCAP_REGS	HRCAP6_BASE	0x7010_5040	YES	YES	YES	YES	YES	YES	-
ECAP_SIGNAL_MONITORING	ECAP6SIGNALMONITORING_BASE	0x7010_5080	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONFIG_REGS	CLB1_LOGICCFG_BASE	0x7012_0000	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONTROL_REGS	CLB1_LOGICCTRL_BASE	0x7012_0200	YES	YES	YES	YES	YES	YES	-
CLB_DATA_EXCHANGE_REGS	CLB1_DATAEXCH_BASE	0x7012_0300	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONFIG_REGS	CLB2_LOGICCFG_BASE	0x7012_1000	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONTROL_REGS	CLB2_LOGICCTRL_BASE	0x7012_1200	YES	YES	YES	YES	YES	YES	-
CLB_DATA_EXCHANGE_REGS	CLB2_DATAEXCH_BASE	0x7012_1300	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONFIG_REGS	CLB3_LOGICCFG_BASE	0x7012_2000	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONTROL_REGS	CLB3_LOGICCTRL_BASE	0x7012_2200	YES	YES	YES	YES	YES	YES	-
CLB_DATA_EXCHANGE_REGS	CLB3_DATAEXCH_BASE	0x7012_2300	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONFIG_REGS	CLB4_LOGICCFG_BASE	0x7012_3000	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONTROL_REGS	CLB4_LOGICCTRL_BASE	0x7012_3200	YES	YES	YES	YES	YES	YES	-
CLB_DATA_EXCHANGE_REGS	CLB4_DATAEXCH_BASE	0x7012_3300	YES	YES	YES	YES	YES	YES	-

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
CLB_LOGIC_CONFIG_REGS	CLB5_LOGICCFG_BASE	0x7012_4000	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONTROL_REGS	CLB5_LOGICCTRL_BASE	0x7012_4200	YES	YES	YES	YES	YES	YES	-
CLB_DATA_EXCHANGE_REGS	CLB5_DATAEXCH_BASE	0x7012_4300	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONFIG_REGS	CLB6_LOGICCFG_BASE	0x7012_5000	YES	YES	YES	YES	YES	YES	-
CLB_LOGIC_CONTROL_REGS	CLB6_LOGICCTRL_BASE	0x7012_5200	YES	YES	YES	YES	YES	YES	-
CLB_DATA_EXCHANGE_REGS	CLB6_DATAEXCH_BASE	0x7012_5300	YES	YES	YES	YES	YES	YES	-
PMBUS_REGS	PMBUSA_BASE	0x7014_8000	YES	YES	YES	YES	YES	YES	-
I2C_REGS	I2CA_BASE	0x7015_0000	YES	YES	YES	YES	YES	YES	-
I2C_REGS	I2CB_BASE	0x7015_1000	YES	YES	YES	YES	YES	YES	-
SPI_REGS	SPIA_BASE	0x7015_8000	YES	YES	YES	YES	YES	YES	-
SPI_REGS	SPIB_BASE	0x7015_9000	YES	YES	YES	YES	YES	YES	-
SPI_REGS	SPIC_BASE	0x7015_A000	YES	YES	YES	YES	YES	YES	-
SPI_REGS	SPID_BASE	0x7015_B000	YES	YES	YES	YES	YES	YES	-
SPI_REGS	SPIE_BASE	0x7015_C000	YES	YES	YES	YES	YES	YES	-
FSI_TX_REGS	FSITXA_BASE	0x7018_0000	YES	YES	YES	YES	YES	YES	-
FSI_TX_REGS	FSITXB_BASE	0x7018_1000	YES	YES	YES	YES	YES	YES	-
FSI_TX_REGS	FSITXC_BASE	0x7018_2000	YES	YES	YES	YES	YES	YES	-
FSI_TX_REGS	FSITXD_BASE	0x7018_3000	YES	YES	YES	YES	YES	YES	-
FSI_RX_REGS	FSIRXA_BASE	0x7018_8000	YES	YES	YES	YES	YES	YES	-
FSI_RX_REGS	FSIRXB_BASE	0x7018_9000	YES	YES	YES	YES	YES	YES	-
FSI_RX_REGS	FSIRXC_BASE	0x7018_A000	YES	YES	YES	YES	YES	YES	-
FSI_RX_REGS	FSIRXD_BASE	0x7018_B000	YES	YES	YES	YES	YES	YES	-
EPG_REGS	EPG_BASE	0x701C_0000	YES	YES	YES	YES	YES	YES	-
EPG_MUX_REGS	EPGMUX_BASE	0x701C_0200	YES	YES	YES	YES	YES	YES	-
vbusp_ssu									
SSU_GEN_REGS	SSUGEN_BASE	0x3008_0000	-	YES	YES	YES	-	-	YES
SSU_CPU1_CFG_REGS	SSUCPU1CFG_BASE	0x3008_1000	-	YES	-	-	-	-	-
SSU_CPU2_CFG_REGS	SSUCPU2CFG_BASE	0x3008_2000	-	YES	YES	-	-	-	-
SSU_CPU3_CFG_REGS	SSUCPU3CFG_BASE	0x3008_3000	-	YES	-	YES	-	-	-
SSU_CPU1_AP_REGS	SSUCPU1AP_BASE	0x3008_7000	-	YES	-	-	-	-	-
SSU_CPU2_AP_REGS	SSUCPU2AP_BASE	0x3008_8000	-	YES	YES	-	-	-	-

ADVANCE INFORMATION

Table 7-27. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	Frame Applicable	CPU1	CPU2	CPU3	RTDMA1	RTDMA2	HSM
SSU_CPU3_AP_REGS	SSUCPU3AP_BASE	0x3008_9000	-	YES	-	YES	-	-	-
soc_to_hsm_bridge									
HSM_DTHE_REGS	DTHE_BASE	0x3028_0000	-	YES	YES	YES	YES	YES	-
HSM_DTHE_CRC_S_REGS	CRCS_BASE	0x3028_1000	-	YES	YES	YES	YES	YES	-
HSM_DTHE_CRC_P_REGS	CRCP_BASE	0x3028_2000	-	YES	YES	YES	YES	YES	-
HSM_SHA_S_REGS	SHAS_BASE	0x3028_4000	-	YES	YES	YES	YES	YES	-
HSM_SHA_P_REGS	SHAP_BASE	0x3028_5000	-	YES	YES	YES	YES	YES	-
HSM_AES_S_REGS	AESS_BASE	0x3028_6000	-	YES	YES	YES	YES	YES	-
HSM_AES_P_REGS	AESP_BASE	0x3028_7000	-	YES	YES	YES	YES	YES	-
HSM_SM4_REGS	SM4_BASE	0x3028_8000	-	YES	YES	YES	YES	YES	-
HSM_SM3_REGS	SM3_BASE	0x3028_9000	-	YES	YES	YES	YES	YES	-
HSM_TRNG_REGS	TRNG_BASE	0x3028_A000	-	YES	YES	YES	YES	YES	-
HSM_PKE_REGS	PKE_BASE	0x3029_0000	-	YES	YES	YES	YES	YES	-

7.6 Identification

Table 7-28 lists the Device Identification Registers. Additional information on these device identification registers can be found in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*. See the register descriptions of PARTIDH and PARTIDL for identification of production status and other device information.

Table 7-28. Device Identification Registers

NAME	ADDRESS	SIZE (x8)	DESCRIPTION	
PARTIDH	0x3018 0024	4	Device part identification number	
			F29H850TU9	0x08FF 0C00
			F29H859TU8	0x08FD 0C00
			F29H859TM8	0x08ED 0C00
			F29H850DU7	0x08DF 0C00
			F29H859DU6	0x08DD 0C00
			F29H850DM7	0x08CF 0C00
			F29H859DM6	0x08CD 0C00
			F29P589DU5	0x087E 0C00
			F29P580DM5	0x086F 0C00
			F29P589DM5	0x086E 0C00
REVID	0x3018 0028	4	Silicon revision number	
			Revision 0	0x0000 0000

ADVANCE INFORMATION

7.7 Boot ROM

The purpose of this section is to explain the boot read-only memory (ROM) code functionality for the C29x CPU core's, including the boot procedure. This section also discusses the functions and features of the boot ROM code, and provides details about the ROM memory-map contents. On every reset, the device executes a boot sequence in the ROM depending on the reset type and boot configuration. This sequence initializes the device to run the application code. For the CPU, the boot ROM also contains peripheral bootloaders that can be used to load an application into RAM. These bootloaders can be disabled for safety or security purposes.

See Table 7-29 for details on available boot features for the C29x CPU. Additionally, Table 7-30 shows the sizes of the various ROMs on the device.

Table 7-29. Boot System Overview

BOOT FEATURE	CPU
Initial boot process	Device reset
Boot mode selection	GPIOs
Boot modes supported	Flash boot RAM boot Wait boot Parallel IO CAN CAN-FD I2C SPI UART

Table 7-30. ROM Memory

ROM	SIZE
CPU1 boot ROM	128KB
CPU2 boot ROM	32KB
CPU3 boot ROM	32KB

7.7.1 Device Boot Sequence

Table 7-31 describes the general boot ROM procedure each time the CPU1 core is reset.

During boot, boot ROM code updates a boot status location in RAM that details the actions taken during this process. Refer to the *Boot Status Information* section in the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for more details.

Table 7-31. CPU1 Boot ROM Sequence

STEP	CPU1 ACTION
1	Flash Read Interface (FRI) wait state configuration
2	Enable Watchdog
3	Zone0 full debug password configured from OTP into SSU registers
4	UID (Unique ID) is configured from OTP into SSU registers
5	On PORESETn only, All CPU RAMs (LPAx,LDAx, CPAx and CDAx) are initialized
6	Critical Trims (APLL, PMM, OSC, Flash) are loaded from OTP and device configuration registers are programmed
7	ESM configurations are performed for Group0 events
8	SIC (Safe Interconnect) is enabled
9	UPP (User Protection Policy) revision from User-OTP is configured into SSU register
10	Error status pin configuration input from User-OTP is configured
11	External crystal power-up if enabled in User-OTP
12	Reading the Device Configurations from OTP into DCx Registers
13	Load non-critical (ADC, DAC) trims
14	SSU configurations based on User-OTP inputs which include: 1. SSU register self-test 2. SSU register configurations
15	Lock DCx (Device Configuration), PARTID, MCUCNF26 and PERxSYSCONFIG (Peripheral System Configuration) registers
16	Wait for RAM initialization, done only on PORESETn
17	Clear PORRESETn and XRSn reset cause on PORESETn and only clear XRSn reset cause on XRSn
18	Pull-ups are enabled on unbonded IOs
19	The boot mode GPIO pins are polled to determine the boot mode to run. Boot loader is executed based on boot mode/configurations. Refer to Section 7.7.4.2 for a flow chart of the boot sequences.
20	RAMOPEN for LINK1 which includes: LPA0 and LDA0-7
21	Lock and Commit LINK1 RAMPOPEN by writing to SSU registers based on User-OTP inputs
22	APR's (Access Protection Regions) are set from User-OTP configurations
23	Disable watchdog for Link1 bootloaders execution
24	Bootloader process under Link1 execution
25	Clear Link1 RAMOPEN
26	Jump to C29 Application Link2

ADVANCE INFORMATION

7.7.2 Device Boot Modes

This section explains the default boot modes, as well as all the available custom boot modes supported on this device. The boot ROM uses the boot mode select, general purpose input/output (GPIO) pins to determine the boot mode configuration.

7.7.2.1 Default Boot Modes

Table 7-32 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used. Default BMSP (Boot Mode Select Pin) used are GPIO72 (BMSP1) and GPIO84 (BMSP0).

Table 7-32. Device Default Boot Modes

BOOT MODE	GPIO72 (DEFAULT BOOT MODE SELECT PIN 1)	GPIO84 (DEFAULT BOOT MODE SELECT PIN 0)
Parallel IO	0	0
UART	0	1
CAN	1	0
Flash	1	1

Refer to Section 7.7.3 for details of boot configurations.

Refer to the *Bootloaders* section in the ROM Code and Peripheral Booting chapter of the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual* for details of the boot modes that use a peripheral boot loader.

Refer to Section 7.7.5 for GPIOs used for selecting the boot modes.

Note

All the peripheral boot modes that are supported use the first instance of the peripheral module (SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this section, such as SPI boot, the mode is actually referring to the first module instance, which means the SPI boot on the SPIA port. The same applies to the other peripheral boot modes.

7.7.2.2 Custom Boot Modes

Once the user programs a custom boot table in user OTP, an entry in the custom table is used for booting. Users can customize the boot mode select pins in the end system design by programming the BOOTPIN_CONFIG location in user OTP. This allows customers to use 0, 1, 2, or 3 boot mode select pins as needed. You can also customize the boot definition table and indicate which location to boot from by programming the boot mode definition table in the BOOTDEF location of user OTP. Table 7-33 show the options for various boot modes.

Note

All peripheral boot modes supported in Table 7-33 use the first instance of the peripheral modules (that is SPIA, I2CA, and so on).

Table 7-33. CPU1 Boot Modes

BOOT MODE NUMBER	BOOT MODES
0	Parallel
1	UART
2	CAN
3	Flash
4	Wait
5	RAM
6	SPI
7	I2C
8	CAN-FD

7.7.3 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from zero boot mode select pins up to three boot mode select pins and from one configured boot mode up to eight configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SPI boot for debugging, and so on.)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: Two BMSPs are required to select between three boot mode options.)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default that is disabled.). Refer to Section 7.7.3.1 for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0 = Boot to Flash, BOOTDEF1 = CAN Boot, BOOTDEF2 = SPI Boot; all other BOOTDEFx remain as default/nothing). Refer to Section 7.7.3.2 for all the details on setting up and configuring the custom boot mode table.

7.7.3.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins are customized by the user, by programming the BOOTPIN_CONFIG location (refer to Table 7-34), in the user-configurable OTP. The location in the OTP is BOOTPIN-CONFIG. When debugging, EMU_BOOTPIN_CONFIG register in SSU_GEN_REGS is the emulation equivalent of BOOTPIN_CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use **zero**, **one**, **two**, or **three** boot mode select pins as needed.

BMSP configuration and boot definition table is either read from User-OTP or SSU registers based on debugger connection status as explained below:

- If the debugger is connected, then the emulation boot flow is followed, where the following SSU registers are used to determine GPIO to be used:
  - EMU_BOOTPIN_CONFIG
  - EMU_BOOTDEF_LOW
  - EMU_BOOTDEF_HIGH
- If the debugger is not connected, then the following User-OTP locations are used to determine the boot modes:
  - BOOTPIN_CONFIG
  - BOOTDEF_LOW
  - BOOTDEF_HIGH

Table 7-34. BOOTPIN-CONFIG Bit Fields

BIT	NAME	DESCRIPTION
31:24	Key	Write 0x5A to these 8-bits to tell the boot ROM code that the bits in this register are valid.
23:16	Boot Mode Select Pin 2 (BMSP2)	Refer to BMSP0 description.
15:8	Boot Mode Select Pin 1 (BMSP1)	Refer to BMSP0 description.
7:0	Boot Mode Select Pin 0 (BMSP0)	Set to the GPIO pin to be used during boot (GPIO0 up to GPIO254). 0x0 = GPIO0 0x01 = GPIO1, and so on. Writing 0xFF disables this BMSP and this pin is no longer used to select the boot mode.

Note

GPIO that can be either digital and analog type pins, digital type inputs are possible on these pins provided the software writes to the GPIOHAMSEL register bits.

The following GPIOs that are not available on any package cannot be used as a boot mode select pin. If selected for a particular BMSP, the boot ROM automatically selects the factory default GPIOs for BMSP0 and BMSP1. Factory default for BMSP2 is 0xFF, which disables the BMSP.

Table 7-35. Stand-alone Boot Mode Select Pin Decoding

BOOTPIN_CONFIG KEY	BMSP0	BMSP1	BMSP2	REALIZED BOOT MODE
!= 0x5A	Don't Care	Don't Care	Don't Care	Boot as defined by the factory default BMSPs.
= 0x5A	0xFF	0xFF	0xFF	Boot as defined in the boot table for boot mode 0 (All BMSPs disabled).
	Valid GPIO	0xFF	0xFF	Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled).
	0xFF	Valid GPIO	0xFF	Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled).
	0xFF	0xFF	Valid GPIO	Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled)
	Valid GPIO	Valid GPIO	0xFF	Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled).
	Valid GPIO	0xFF	Valid GPIO	Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled).
	0xFF	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled).
	Valid GPIO	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP0, BMSP1, and BMSP2.
	Invalid GPIO	Valid GPIO	Valid GPIO	BMSP0 is reset to the factory default BMSP0 GPIO. Boot as defined by the values of BMSP0, BMSP1, and BMSP2.
	Valid GPIO	Invalid GPIO	Valid GPIO	BMSP1 is reset to the factory default BMSP1 GPIO. Boot as defined by the values of BMSP0, BMSP1, and BMSP2.
	Valid GPIO	Valid GPIO	Invalid GPIO	BMSP2 is reset to the factory default state, which is disabled. Boot as defined by the values of BMSP0 and BMSP1.

Note

When decoding the boot mode, BMSP0 is the least-significant bit and BMSP2 is the most-significant bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 are selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

ADVANCE INFORMATION

7.7.3.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options (refer to Table 7-36). The 64-bit location is located in user-configurable OTP in the BOOTDEF_LOW and BOOTDEF_HIGH locations. When debugging, EMU_BOOTDEF_LOW and EMU_BOOTDEF_HIGH are the emulation equivalents of BOOTDEF_LOW and BOOTDEF_HIGH, and can be programmed to experiment with different boot mode options without writing to OTP.

The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries.

Table 7-36. BOOTDEF Bit Fields

BOOTDEF NAME	BYTE POSITION	NAME	DESCRIPTION
BOOT_DEF0	7:0	[3:0] BOOT_DEF0 Mode	Set the boot mode number from Section 7.7.2.2. Any unsupported boot mode causes the device to either go to wait boot (debugger connected) or boot to Flash (stand-alone).
		[7:4] BOOT_DEF0 Options	Set alternate/additional boot options. This can include changing the GPIOs for a particular boot peripheral or specifying a different Flash entry point. Refer to Section 7.7.5 for valid BOOTDEF values to set in the table.
BOOT_DEF1	15:8	BOOT_DEF1 Mode/Options	Refer to BOOT_DEF0 description.
BOOT_DEF2	23:16	BOOT_DEF2 Mode/Options	
BOOT_DEF3	31:24	BOOT_DEF3 Mode/Options	
BOOT_DEF4	39:32	BOOT_DEF4 Mode/Options	
BOOT_DEF5	47:40	BOOT_DEF5 Mode/Options	
BOOT_DEF6	55:48	BOOT_DEF6 Mode/Options	
BOOT_DEF7	63:56	BOOT_DEF7 Mode/Options	

7.7.4 Device Boot Flow Diagrams

This section details the C29 CPU boot flow diagrams for stand-alone and emulation boot flows.

7.7.4.1 Device Boot Flow

The following flow diagrams describe how the device boots up after PORESETn. HSM starts up first and then releases reset to CPU1. Detailed CPU1 boot flow is explained in later sections and for detailed HSM boot flow refer to HSM User Guide.

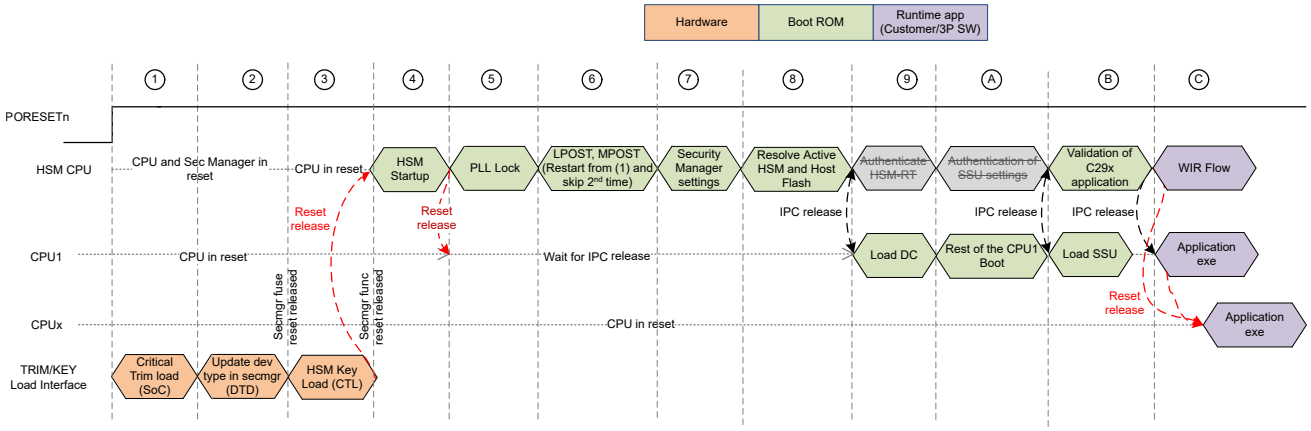

Figure 7-5. HS-FS Device Boot Flow Diagram

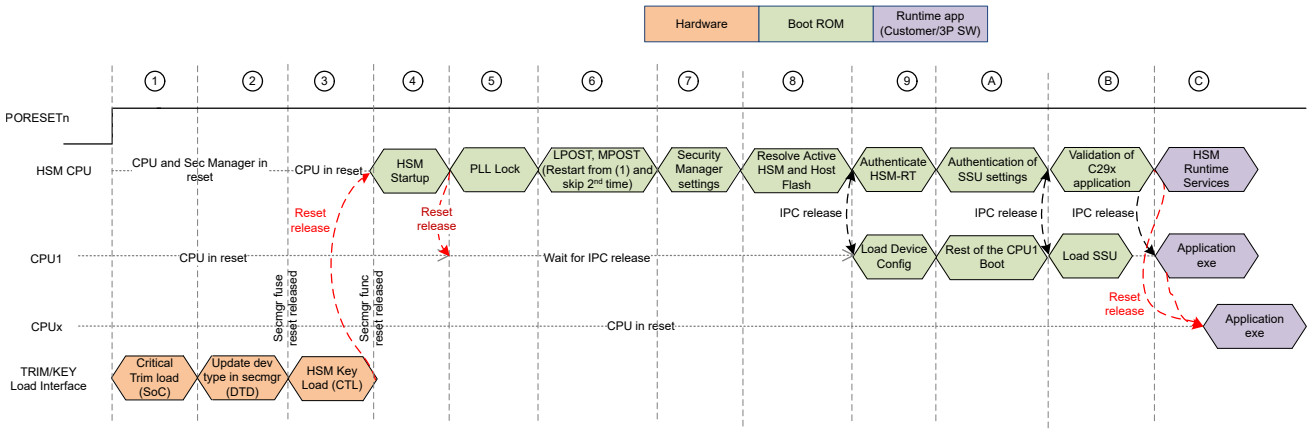

Figure 7-6. HS-SE Secure Boot Flow Diagram

ADVANCE INFORMATION

7.7.4.2 CPU1 Boot Flow

Upon reset, CPU1 follows the boot flow shown in Figure 7-7. Depending on whether a JTAG debugger is connected to the device, the CPU1 either continues booting following the emulation boot flow or the stand-alone boot flow.

Note

Boot on reset (BOR) follows same flow as power on reset (POR).

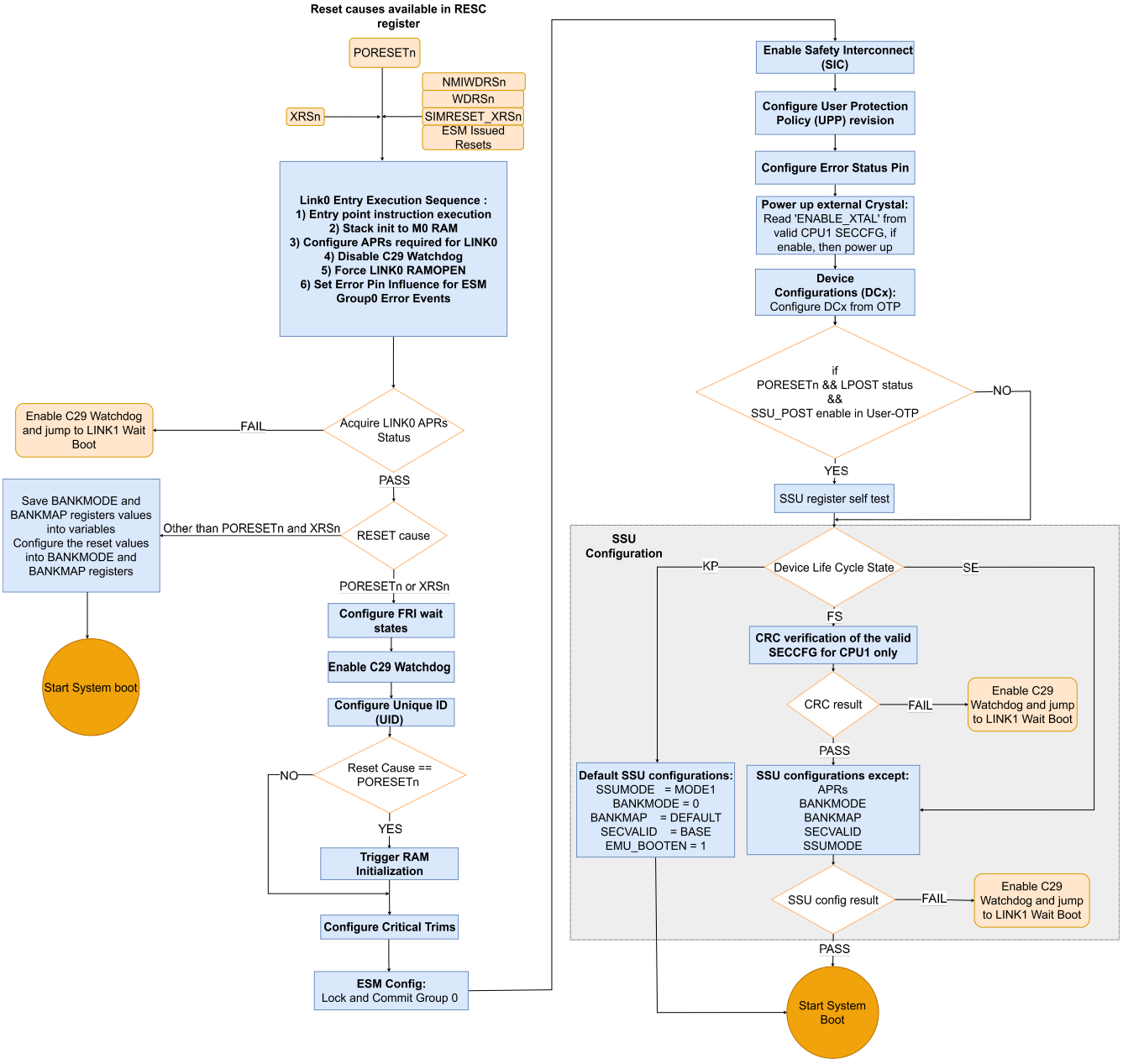

Figure 7-7. Device Boot Flow from Reset to System Boot

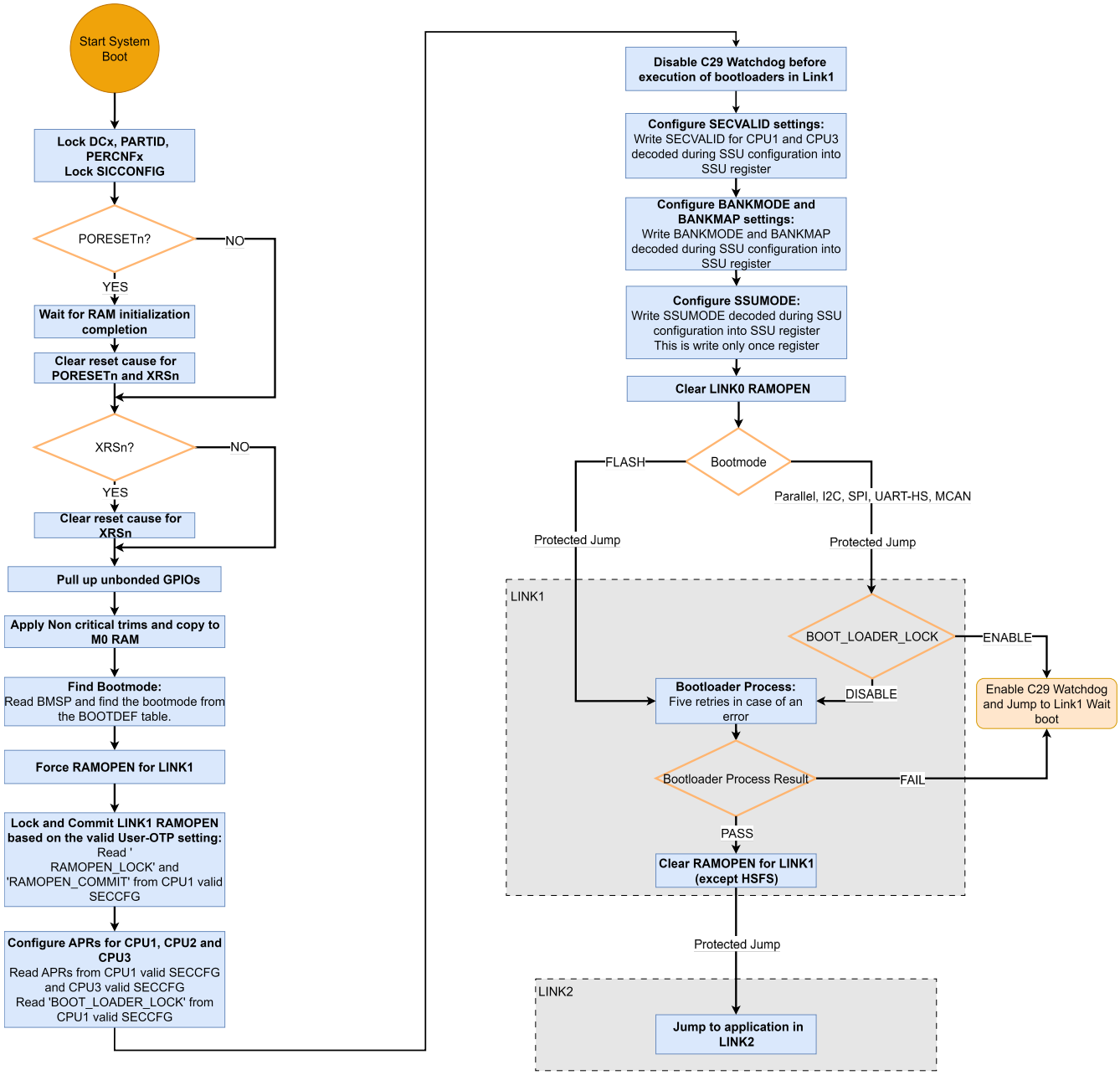

Figure 7-8. System Boot Flow to Application Code

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7.7.4.3 Emulation Boot Flow

Figure 7-9 shows the emulation boot flow when JTAG debugger is connected and emulation boot is enabled in SECCFG User OTP.

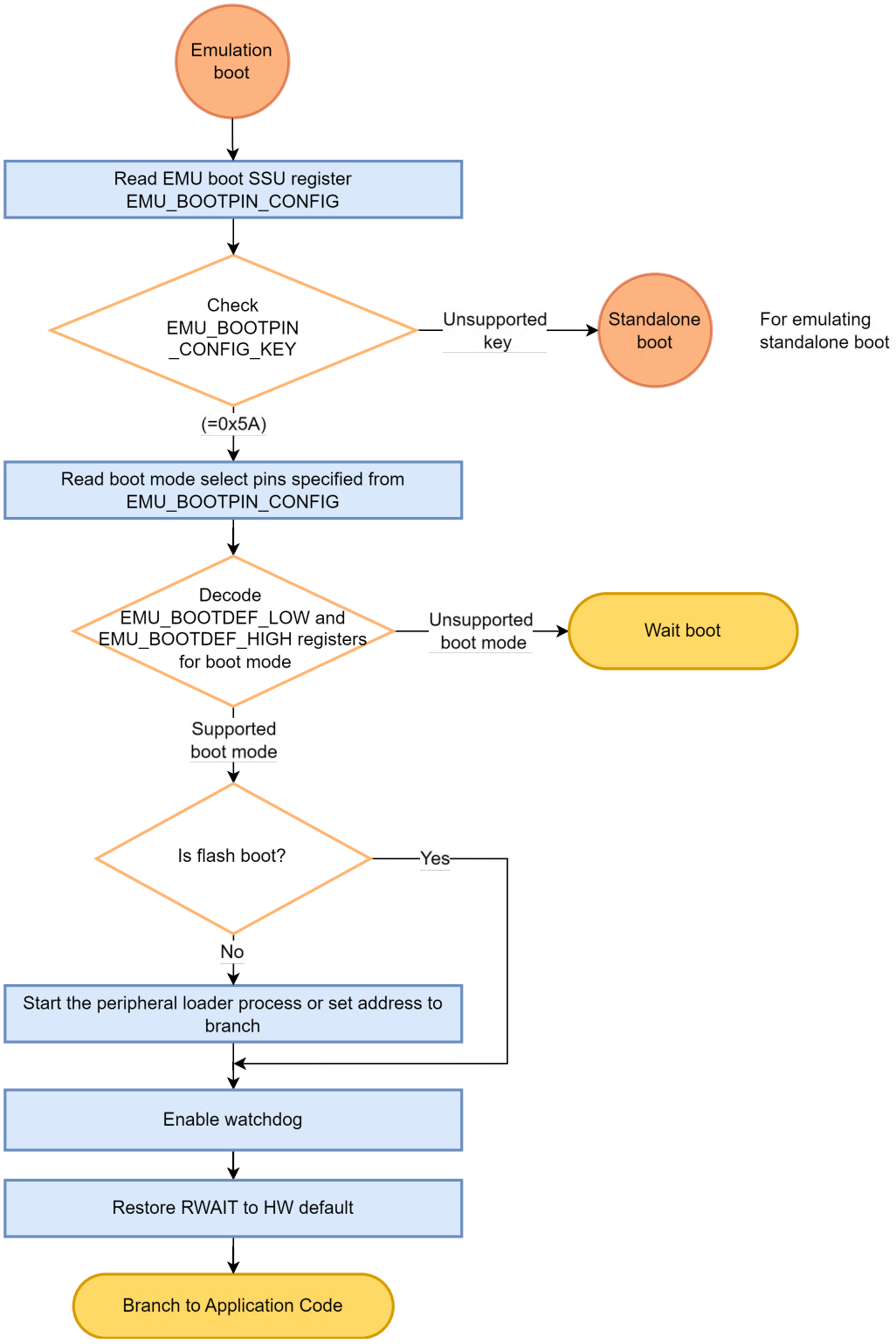


Figure 7-9. Emulation Boot Flow

7.7.4.4 Stand-alone Boot Flow

Figure 7-10 shows the stand-alone boot flow for CPU1 when no JTAG debugger is connected to the device.

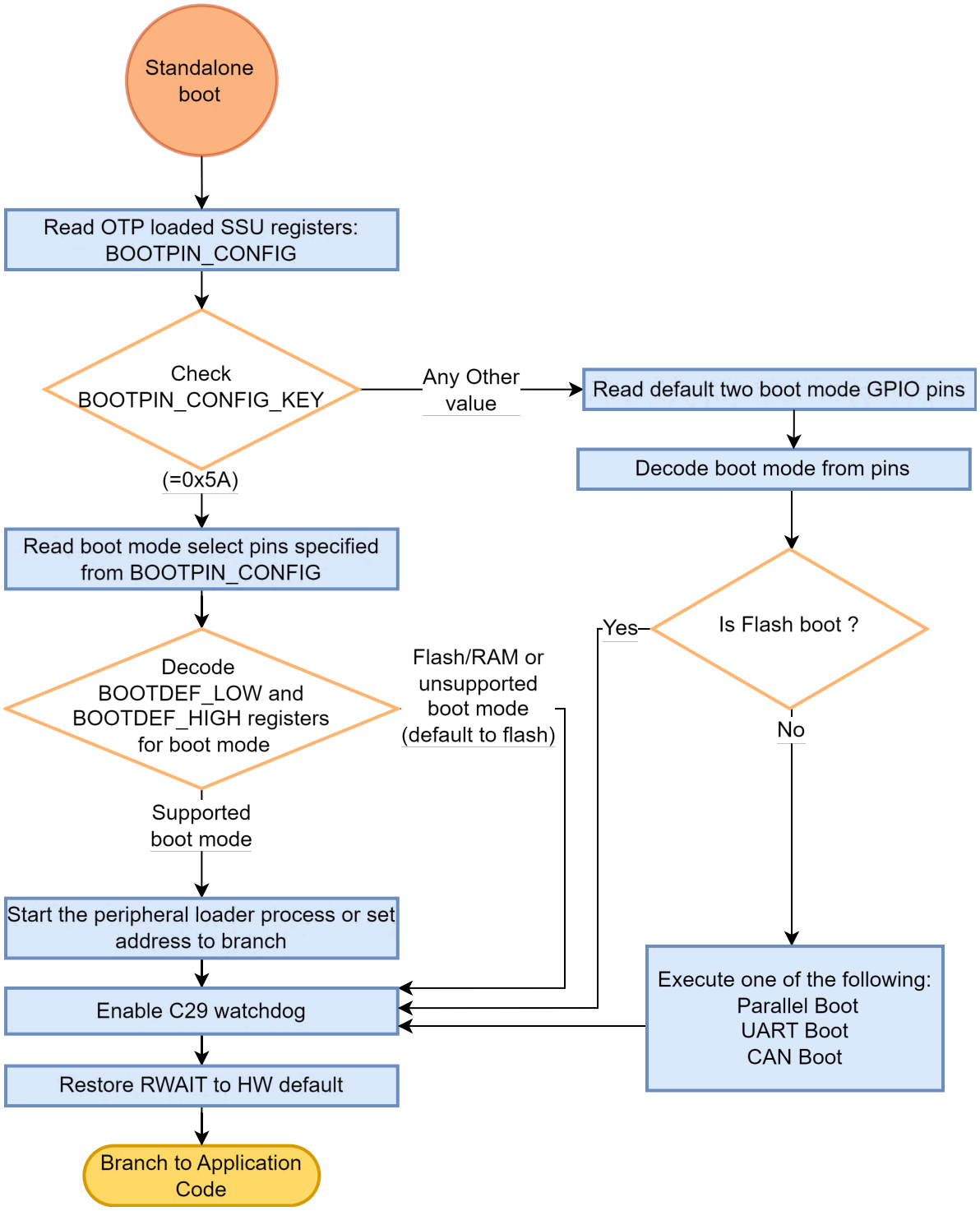


Figure 7-10. Stand-alone Boot Flow

ADVANCE INFORMATION

7.7.5 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at BOOTDEF_LOW and BOOTDEF_HIGH. Refer to Section 7.7.3.2 on how to configure BOOT_DEFx. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Default boot mode GPIO pins:

- Boot mode pin 0 - GPIO84
- Boot mode pin 1 - GPIO72

Guidelines on boot pin selection:

- Avoid pins that have PWM functionality.
- Cannot be analog or USB pins.
- Boot mode select pins and default boot peripheral pins can be available on all packages.
- Avoid JTAG emulation pins and crystal pins.
- Boot mode select pins can be inputs.
- Pins cannot have PHY bootstrap functionality.

Table 7-37. Parallel Boot Options

OPTION	BOOTDEF VALUE	D0–D7 GPIO	C29x (DSP) CONTROL GPIO	HOST CONTROL GPIO	PACKAGE SUPPORTED
0 (default)	0x00	D0 - GPIO0 D1 - GPIO1 D2 - GPIO2 D3 - GPIO3 D4 - GPIO4 D5 - GPIO10 D6 - GPIO11 D7 - GPIO12	GPIO15	GPIO16	All
1	0x20	D0 - GPIO17 D1 - GPIO18 D2 - GPIO22 D3 - GPIO23 D4 - GPIO25 D5 - GPIO26 D6 - GPIO29 D7 - GPIO30	GPIO4	GPIO5	All

Table 7-38. UART Boot Options

OPTION	BOOTDEF VALUE	TX	RX	PACKAGE SUPPORTED
0	0x01	GPIO42	GPIO43	All
1	0x21	GPIO38	GPIO39	176-QFP, 256-BGA
2	0x41	GPIO2	GPIO3	All
3	0x61	GPIO38	GPIO3	All
4	0x81	GPIO84	GPIO85	256-BGA

Table 7-39. CAN Boot Options

OPTION	BOOTDEF VALUE	CANTXA GPIO	CANRXA GPIO	PACKAGE SUPPORTED
0 (default)	0x02	GPIO64	GPIO65	All
1	0x22	GPIO234	GPIO235	144-QFP, 176-QFP, 256-BGA
3	0x42	GPIO64	GPIO235	144-QFP, 176-QFP, 256-BGA
4	0x62	GPIO234	GPIO65	144-QFP, 176-QFP, 256-BGA

Table 7-40. SPI Boot Options

OPTION	BOOTDEF VALUE	SPIPICOA	SPIPOCIA	SPICLKA	SPISTEA	PACKAGE SUPPORTED
0	0x06	GPIO58	GPIO59	GPIO60	GPIO61	All
1	0x26	GPIO16	GPIO17	GPIO60	GPIO19	144-QFP, 176-QFP, 256-BGA
2	0x46	GPIO32	GPIO33	GPIO34	GPIO35	256-BGA
3	0x66	GPIO54	GPIO55	GPIO56	GPIO57	176-QFP, 256-BGA

Table 7-41. I2C Boot Options

OPTION	BOOTDEF VALUE	SDAA GPIO	SCLA GPIO	PACKAGE SUPPORTED
0	0x07	GPIO0	GPIO1	All
1	0x27	GPIO32	GPIO33	256-BGA
2	0x47	GPIO42	GPIO43	All
3	0x67	GPIO56	GPIO57	144-QFP, 176-QFP, 256-BGA

Table 7-42. CAN-FD Boot Options

OPTION	BOOTDEF VALUE	MCAN TX	MCAN RX	PACKAGE SUPPORTED
0	0x08	GPIO64	GPIO65	All
1	0x28	GPIO234	GPIO235	144-QFP, 176-QFP, 256-BGA
2	0x48	GPIO64	GPIO235	144-QFP, 176-QFP, 256-BGA
3	0x68	GPIO234	GPIO65	144-QFP, 176-QFP, 256-BGA

ADVANCE INFORMATION

7.8 Security Modules and Cryptographic Accelerators

7.8.1 Security Modules

This chapter explains security modules for the C29x cores found on this MCU.

7.8.1.1 Hardware Security Module (HSM)

The Hardware Security Module (HSM) is a self-contained subsystem within the device that provides security and cryptographic functions. The host C29x subsystem interfaces with the HSM subsystem to perform the cryptographic operations required for code authentication, secure boot, secure firmware upgrades and encrypted run-time communications. A high-level view of the various subsystems in this device, with the HSM subsystem highlighted, is shown in Figure 7-11.

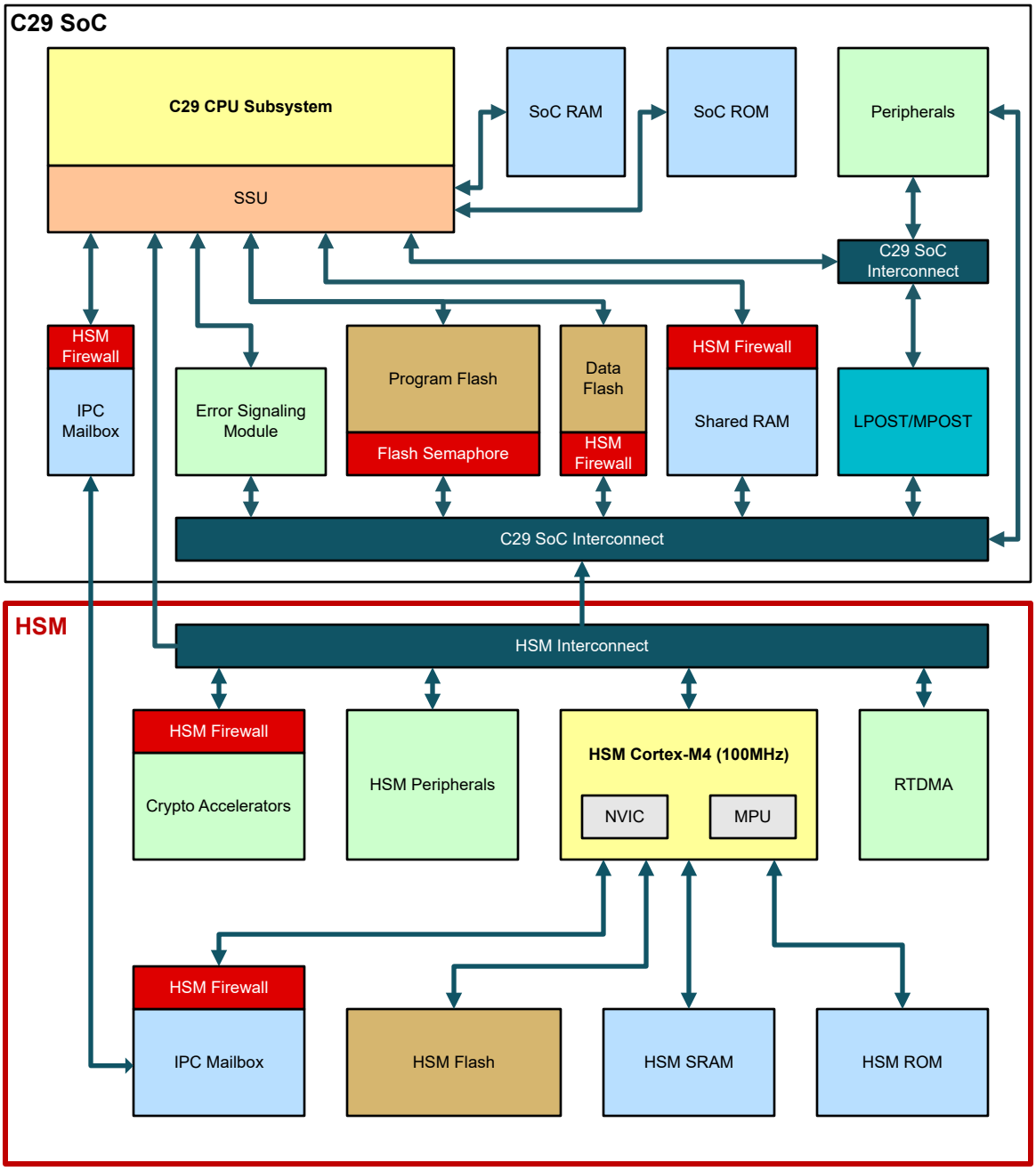


Figure 7-11. Device High-Level Block Diagram

At the center of the HSM is an ARM® Cortex®-M4 CPU running at 100MHz, with embedded SRAM, ROM, and up to 512KB of Flash memory. The Real-Time DMA (RTDMA) module enables fast data transfers between the HSM CPU and SRAM, HSM and application Flash memory banks, secure mailbox, and cryptographic engines.

The Security Manager module hosts the root-of-trust keys, defines the secure access mechanisms, controls the debug firewalls, and performs the security override sequences to establish protection of security assets if debug or failure-analysis operation is required.

The HSM includes a set of accelerator engines for executing cryptographic algorithms. These engines enable fast execution of symmetric encryption algorithms, hash functions, asymmetric encryption algorithms for public key infrastructure, and a true random number generator (TRNG). The Data Transform and Hashing Engine (DTHE) interfaces between the CPU and the cryptographic accelerators, providing interrupt and RTDMA trigger management and essential functions such as CRC and checksum computation.

In addition, the HSM provides peripheral modules to aid various security functions: timers, a real-time counter, a watchdog, DCC for clock monitoring, and ESM for error handling.

Communication between the HSM and the host application cores happens over a secure mailbox interface. The HSM controls various secure firewalls in the device, including the secure mailbox, cryptographic engines, shared RAM, and device Flash memory.

7.8.1.2 Cryptographic Accelerators

The Hardware Security Manager (HSM) includes several hardware accelerators to enable fast execution of key cryptographic algorithms. These engines are described in Table 7-43. For a hardware description and usage instructions for the cryptographic accelerator engines and the Data Transform and Hash Engine (DTHE), see the *Cryptographic Hardware Accelerators User's Guide*.

Table 7-43. List of Cryptographic Accelerator Engines

Engine	Algorithms Supported
AES (Advanced Encryption Standard)	Symmetric Algorithms: AES-128, AES-192, AES-256 Cipher modes: ECB, CTR, CBC, CFB, OFB, CCM, GCM Authentication: CBC-MAC
SM4	Symmetric Algorithms: SM4
PKE (Public Key Engine)	High-performance PKE for large-vector math/modulus operation Ciphers: RSA-2048, RSA-3092, RSA-4096, ECC (Curve25519, X25519, SecP256r1, secP256k1, secP384r1, secP384k1, Brain Pool, and more), SM2 Supports cryptographic operations: ECDSA, EdDSA, ECDH, EdDH, SM2DSA Side-channel protection (DPA, FIA)
SHA	Hash Algorithms: SHA-256, SHA-384, SHA-512 Keyed hashing: HMAC-SHA256, HMAC-SHA512
SM3	Hash Algorithms: SM3 (256 bits, 384 bits, 512 bits)
TRNG	True random number generator Deterministic random bit generator (DRBG)

ADVANCE INFORMATION

7.8.2 Safety and Security Unit (SSU)

7.8.2.1 System View

A simplified view of the F29x Real-Time Security architecture in this device is shown in Figure 7-12. At the heart of the architecture is the Safety and Security Unit (SSU). The SSU acts as a firewall between the C29 CPUs and the memory and peripherals. The primary role of the SSU is to enforce user access protection policy every time the C29 CPU performs accesses to peripherals and memory on the chip. In addition, the SSU governs debug access and Flash Controller operations in the C29 application subsystem (note: the SSU has no control over the HSM Flash, or any other HSM resources). While the Hardware Security Module (HSM) provides cryptographic services and governs authentication, secure boot and secure key/code provisioning, the SSU is responsible for run-time safety and security protections in application CPU subsystems. Both the HSM and SSU govern debug access authorization; both must enable access to a specific resource for debug to be authorized.

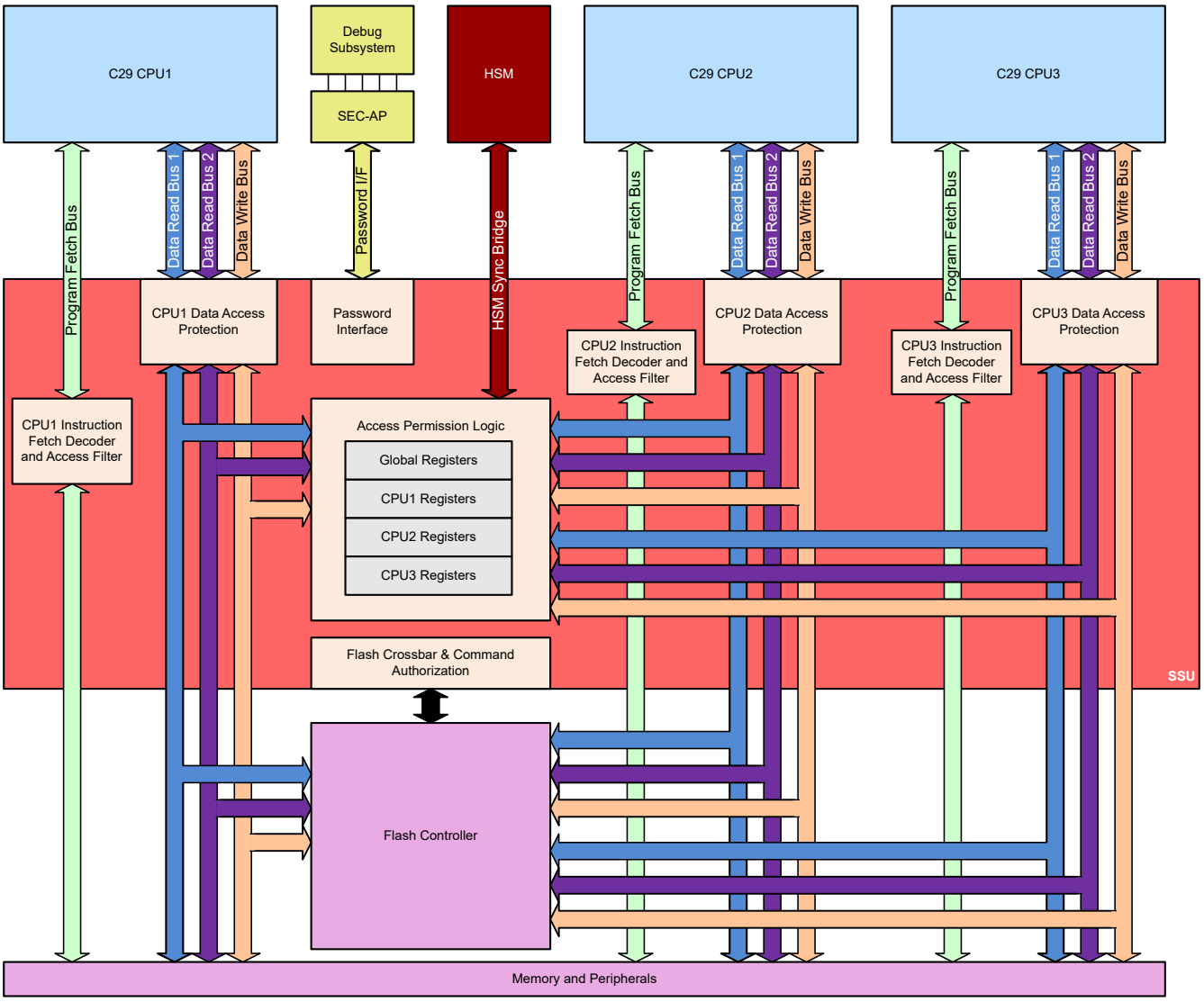


Figure 7-12. C29 Real-Time Security Architectural Block Diagram

The SSU is tightly coupled to the C29 CPUs and the Flash Controller. Each C29 CPU is designed to support hardware function isolation and protections using memory protection identifiers (LINKs), safety and security isolation contexts (STACKs), and debug access ZONEs. An example of a system SSU configuration, showing the relationship between access protection ranges, LINKs, STACKs and ZONEs is shown in Figure 7-13. When

the CPU requests an instruction fetch, the SSU first decodes the instruction address to a LINK, STACK, and ZONE, and then passes that information back to the CPU along with the fetched data. The CPU retains this security context information together with the instruction throughout the execution pipeline, and passes the context along to the SSU when making a data memory read or write access.

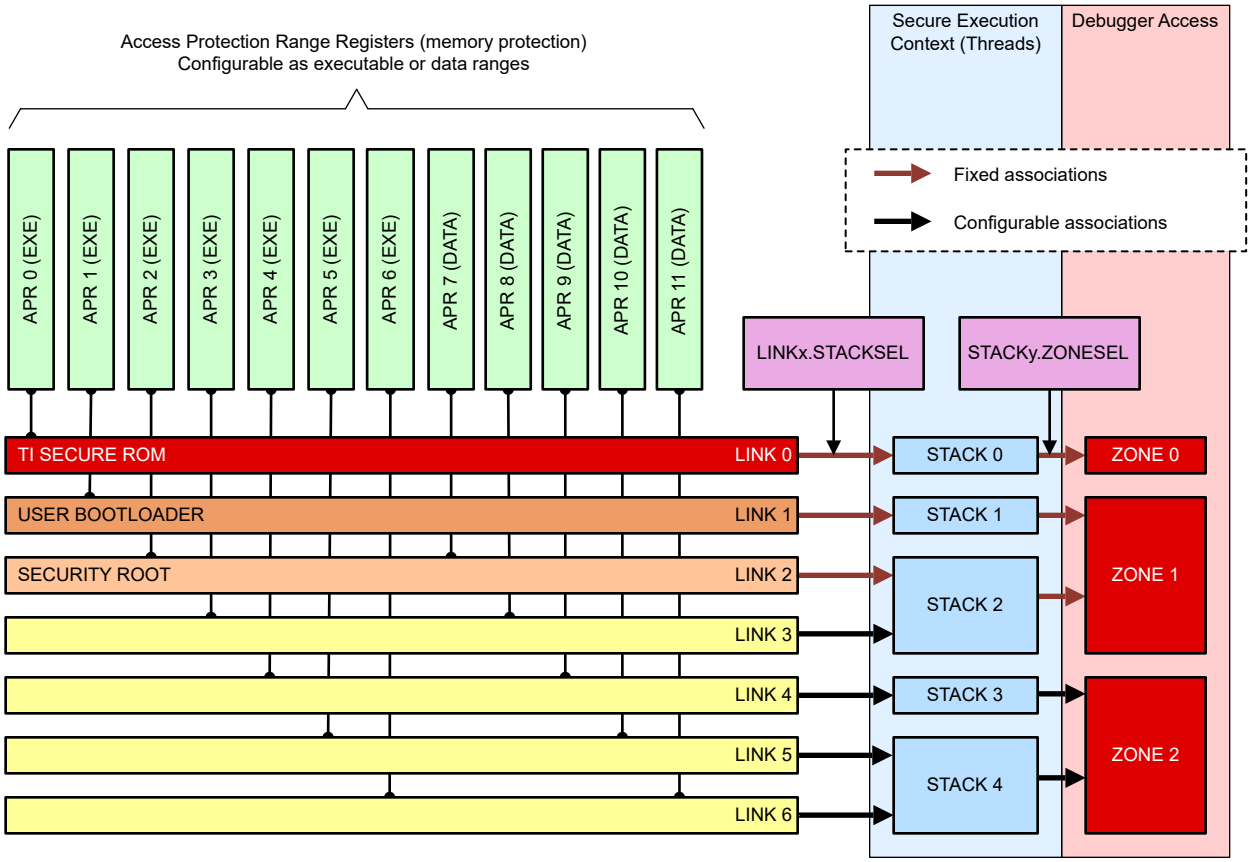


Figure 7-13. SSU Concept Diagram (Simplified)

ADVANCE INFORMATION

7.9 C29x Subsystem

7.9.1 C29 CPU Architecture

The C29 CPU is a VLIW (Very Long Instruction Word) architecture with a fully protected pipeline. The CPU supports multiple instruction sizes (16/32/48 bits). The CPU also supports variable instruction packet size, with each packet able to contain up to eight instructions that execute in parallel. For example, the CPU architecture can execute up to eight 16-bit instructions in parallel. This is enabled by multiple functional units inside the CPU which can execute concurrently. A total of 64 working registers, broken into three different categories (Ax, Dx and Mx Register banks) support the parallel operations in the CPU. In addition to the working registers, the CPU contains multiple status registers (DSTS, ESTS and ISTS) which maintain execution-related and interrupt-context-related information.

Following are the list of C29 CPU major features:

- **Ease of use:**
  - Byte addressable CPU.
  - Linear and unified memory map with 4GB address range.
  - Fully Protected Pipeline: 9 stage pipeline that prevents writes and reads from same location from occurring out of order.
  - Deterministic execution and maximum performance without cached memories.
- **Improved parallelism:**
  - Execute from 1 to 8 instructions in parallel.
  - Execute fixed-point, floating-point, and addressing operations in parallel.
  - Multiple parallel functional units.
  - Specialized operations to minimize discontinuities and accelerate decision making code (for example, if-then-else statements and switch statements).
  - Specialized operations targeting real-time control (for example, trigonometric operations and multiphase vector translation operations).
- **Improved bus throughput:**
  - Capable of fetching up to 128-bit instruction packet every cycle.
  - Capable of performing 8/16/32/64-bit dual reads and single writes per cycle.
  - Improved addressing modes reduce overhead in accessing memory and peripheral resources.
  - Improved pipeline allows for additional 0-wait memory to be accessible to CPU for max performance.
- **Code efficiency:**
  - Supports variable length instruction set (16-bit, 32-bit and 48-bit instructions).
  - Rich instruction set optimizes the most common operations in smallest instructions.
- **ASIL-D safety capability with code isolation in hardware:**
  - Lock step core capable of independent execution in split-lock mode (acting as a separate core) or lock step execution (for redundancy).
  - Integrated ECC logic
  - Integrated memory management (MPU) and protection mechanisms in hardware to maximize MIPS.
  - Separate code threads are fully isolated and protected (including software stacks).
- **Enhanced debug and trace capabilities:**
  - Specialized data logging and code flow trace instructions.
  - Trace data capable of being logged in on-chip RAM or exported through serial communication peripherals.

7.9.2 Peripheral Interrupt Priority and Expansion (PIPE)

7.9.2.1 Introduction

Each PIPE module instance arbitrates peripheral interrupts for the respective CPU. All asserted interrupts are arbitrated each clock cycle, with the highest priority interrupt asserted to the corresponding CPU interrupt line (NMI, RTINT, or INT). The PIPE module is responsible for providing vector addresses to the CPU for NMI, RTINT, INT and RESET. The PIPE is capable of custom ordering of interrupts, prioritization, and nesting.

7.9.2.1.1 Features

The PIPE module has the following features:

- Hardware support for interrupt prioritization, arbitration, grouping, software hand-shake, and nesting.
- Dynamic arbitration of interrupts in hardware on every clock.
- Selectable priority level to choose interrupts as either RTINT and INT.
- Interrupt grouping of adjacent-prioritized interrupts to block nesting within groups.
- Default index-based priority order for interrupts used in arbitration.
- Vector fetch support for RESET, NMI, RTINT, and INT.
- User access to the stack configured for INT.
- Contexts used by a software task manager system or operating system.
- Link-based protection verifies only legal code from the assigned interrupt owner services the interrupt.
- Device level protection validates only legal code source updates interrupt configuration and vector tables.
- Automatic context save and restore for RTINT and NMI.
- RTINT stack overflow protection always provides NMI a block of reserved stack space for execution.
- ECC protection for interrupt vector table.
- Parity protection for configuration registers.
- Optional locking capability of interrupt configurations.

7.9.2.1.2 Interrupt Concepts

An interrupt is a signal that causes the CPU to pause the currently running process and branch to a different piece of code known as an interrupt service routine (ISR). This is a useful mechanism for handling peripheral events, and involves less CPU overhead and program complexity than register polling. However, because interrupts are asynchronous to the program flow, care must be taken to avoid conflicts over resources that are accessed both in interrupts and in the main program code.

Interrupts propagate to the CPU through a series of flag and enable registers. The flag registers store the interrupt until the interrupt is processed. The enable registers allow or block the propagation of the interrupt. When an interrupt signal reaches the CPU, the CPU fetches the appropriate ISR address from the vector table.

7.9.2.2 Interrupt Architecture

The PIPE module has three primary functional blocks:

1. Dynamic Priority Arbitration Circuit
2. Post Processing Block
3. Memory-Mapped Registers (includes vector table and bus interface)

These three blocks are explained in detail in the following subsections.

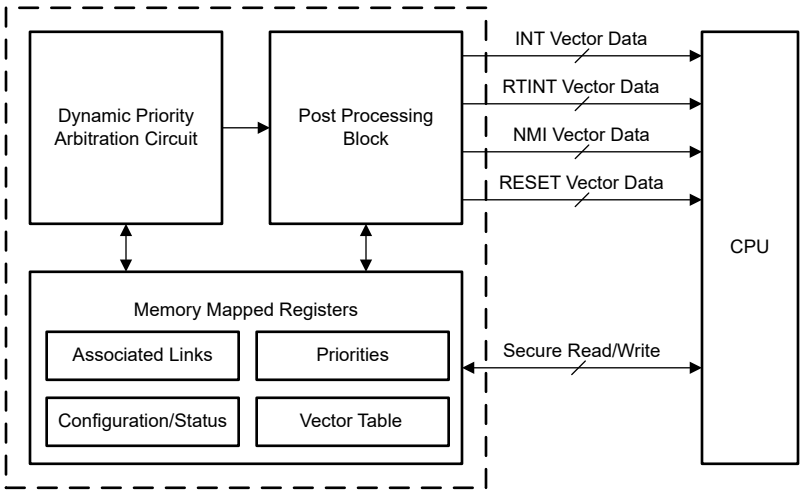


Figure 7-14. PIPE Architecture

7.9.2.2.1 Dynamic Priority Arbitration Block

The dynamic priority arbitration block provides the CPU with the highest priority interrupt vector that is available every clock cycle. The CPU processes the highest priority interrupt at the provided vector address.

7.9.2.2.2 Post Processing Block

The post processing block takes the highest priority interrupt that won the arbitration process and selects which interrupt line (INT or RTINT) to forward the interrupt to. The post processing block also automatically checks which link is accessing an interrupt line and whether a secure link is accessing protected registers.

Note

The NMI line provided to the CPU is an independent line that overrides any other interrupt (INT or RTINT) ready for assertion.

7.9.2.2.3 Memory Mapped Registers

The memory mapped registers (MMR) contain the interrupt configuration registers. Below are the type of registers available in the memory mapped registers:

- Link associated with each interrupt.
- Priority configured for each interrupt.
- Interrupt configurations.
- Interrupt status.
- Vector table.

Accesses are controlled by the same security rules that apply to all registers.

7.9.2.3 Interrupt Propagation

Interrupts propagate to the CPU through several steps. Peripheral interrupts set the corresponding FLAG bit in the INT_CTL_REG_L_y register of a given interrupt. If the EN bit of the interrupt's INT_CTL_REG_L_y register is set, the interrupt propagates to the dynamic priority arbitration circuit. Next, the dynamic priority arbitration block and post processing block arbitrate the highest priority interrupt and assert this to the CPU on one of the two interrupt lines (RTINT or INT). Finally, the CPU chooses the highest priority interrupt line that is asserted (amongst NMI, RTINT, and INT) and begins execution of that interrupt.

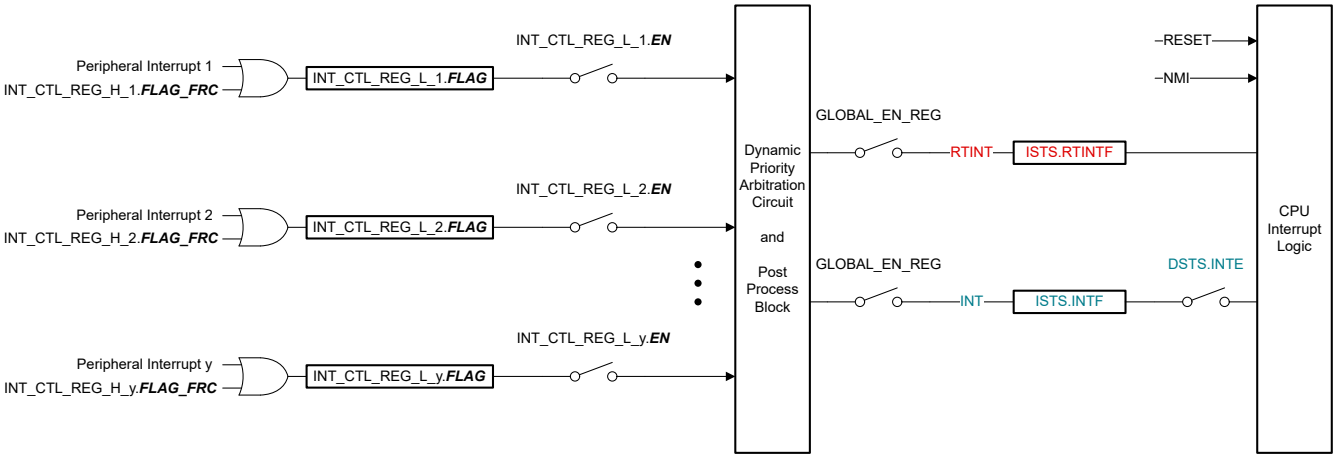


Figure 7-15. Interrupt Propagation

Note

NMI is an independent line that overrides any other interrupts ready for assertion. An NMI event asserted to PIPE is forwarded to the CPU, including NMI in service. CPU can select a new NMI at any time, but the PIPE module does not forward the new NMI until the in-service NMI interrupt service routine is complete.

The same rule is applicable to RESET. Once the CPU receives the RESET, there are no conditions to meet before reset assertion to CPU.

ADVANCE INFORMATION

7.9.3 Data Logging and Trace (DLT)

7.9.3.1 Introduction

For critical CPU run-time content the data logger and trace (DLT) module has the ability to control what data gets logged, when to start data-logging, and the size of the data to capture. Critical run-time content can include any information that needs to be monitored as the content is computed. When data-logging the DLT is non-intrusive meaning there is no impact to run-time or CPU core behavior. The ability to view intermediate values of computation in a critical task, such as a control loop, can help users fine-tune the loop. The DLT module can generate interrupts to the interrupt controller, issue RTDMA transfer requests, and interact with ERAD event triggers.

The DLT can collect, time-stamp, prefilter, export, and do real-time and post analysis of data.

7.9.3.1.1 Features

The DLT has the following capabilities:

- Logging critical run-time content referred to as data logging
- Analyze program execution sequence using tags referred to as trace
- Logging is non-intrusive to run-time/CPU core behavior
- Flexible logging capability for extended period of time by transferring data to external memory or short period of time to on-chip memory
- Logging of registers can be up to 32-bit size, depending on the size on the variable to be logged
- Each CPU has DLT support
- Time stamping records time difference from last logged variable and can time stamp the IPC timer's count
- RTDMA triggering
- Global, FIFO and timer interrupt generation

7.9.3.1.1.1 Block Diagram

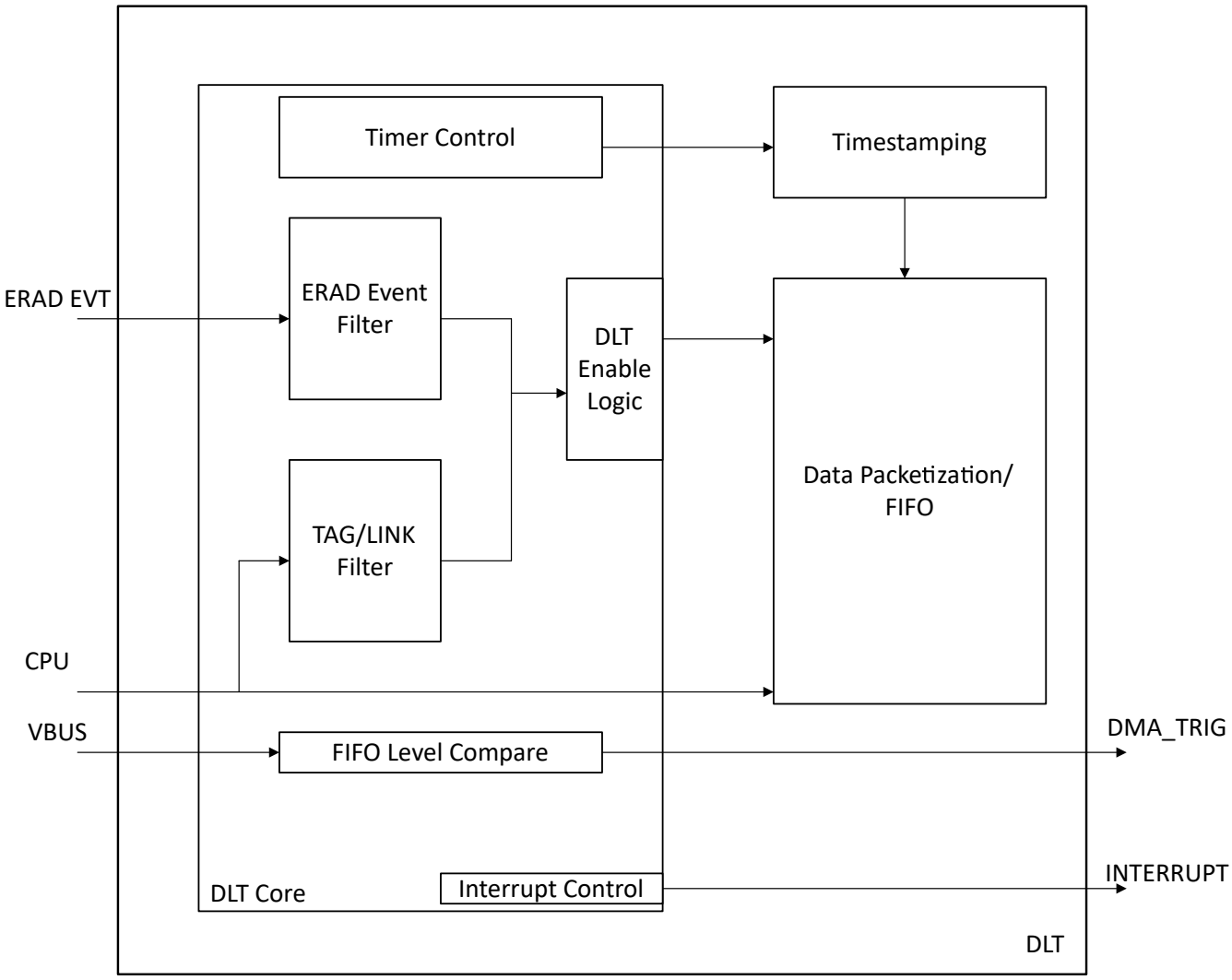


Figure 7-16. DLT Block Diagram

7.9.4 Waveform Analyzer Diagnostics (WADI)

7.9.4.1 WADI Overview

The waveform analyzer and diagnostic (WADI) peripheral consists of many useful built in signal analysis support and provides a safety mechanism for the signals. WADI is primarily useful for safety applications where driving switches or capturing signals require an action or a linking of actions to occur if the signal analysis reports any misbehavior.

7.9.4.1.1 Features

- Ability to select an input signal from multiple sources (CMPSS, ePWM, Input-XBAR, CLB, ADC) to WADI block and configure trigger to start analysis and perform safety diagnostics on the signals
- Ability to perform different checks as configured:
  - Pulse width measurement
  - Frequency measurement
  - Phase Overlap measurement
  - Dead-band measurement
- Ability to perform checks on individual signal or perform checks between two signals
- Ability to override outputs to a certain state or define a link of output combination based on analysis of signals
- Registers with parity support
- Support for RTDMA trigger and RTDMA acknowledgment

7.9.4.1.2 Block Diagram

Figure 7-17 shows a block diagram of the WADI.

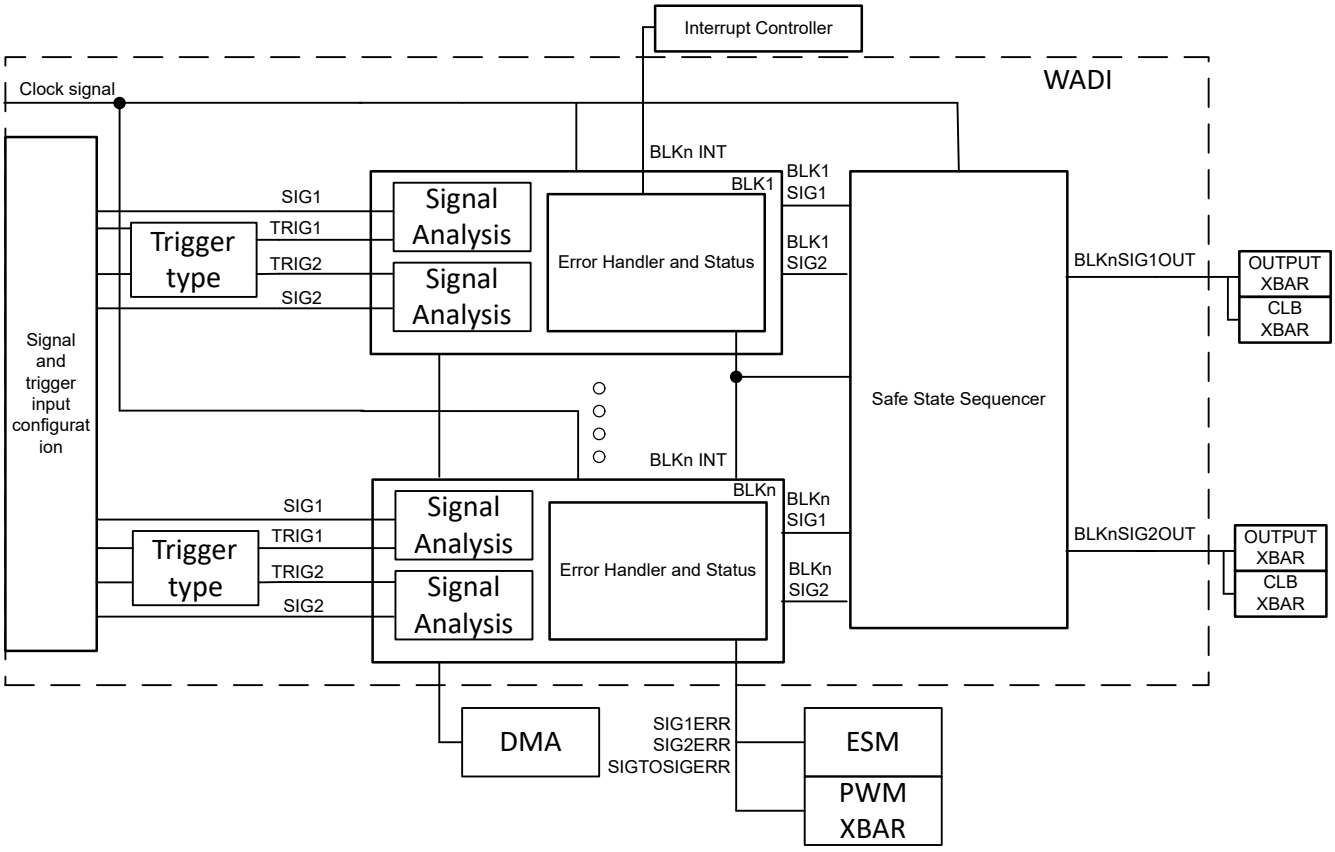


Figure 7-17. WADI Block Diagram

7.9.4.1.3 Description

The waveform analyzer diagnostic (WADI) determines the correctness and quality of the underlying real time control system by performing measurements, aggregation and comparison on the input signals. Each input signal is characterized for certain attributes of pulse width, frequency, phase, dead-band and so on. WADI validates the measurements for each signal against a compare value with some error of margin that the signal can still be considered valid. WADI allows comparison of individual signals or signal to signal analysis within a WADI block. There are four WADI blocks for each WADI instance. Each WADI block can monitor up to two signals and perform signal analysis on each.

ADVANCE INFORMATION

7.9.5 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the System Event Counter units. The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software, which significantly increases the debug capabilities of many real-time systems, especially in situations where debuggers are not connected.

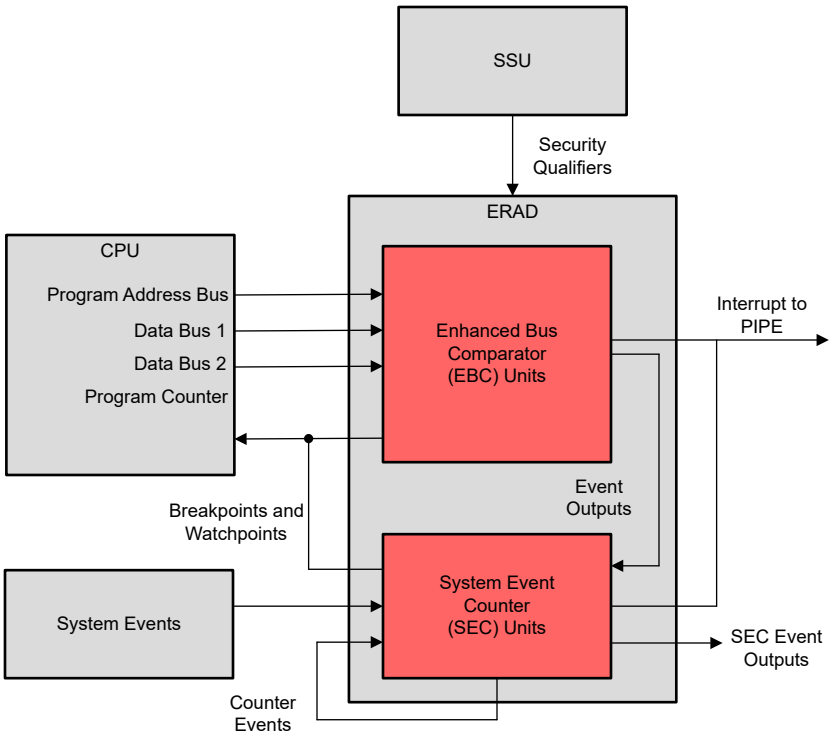


Figure 7-18. ERAD System Overview

7.9.6 Inter-Processor Communications (IPC)

7.9.6.1 Introduction

This section details the IPC features that each CPU can use to request and share information. The IPC features are:

- IPC flags and interrupts
- IPC command registers
- Free-running counter

All IPC features are independent of each other, and most do not require any specific data format.

The *IPC Module Architecture* figure shows the design structure of the IPC module. The functionality is the same between any two CPUs.

There is no message RAM for devices with C29x processors, since it is possible to designate any memory as readable or writable by the various CPUs.

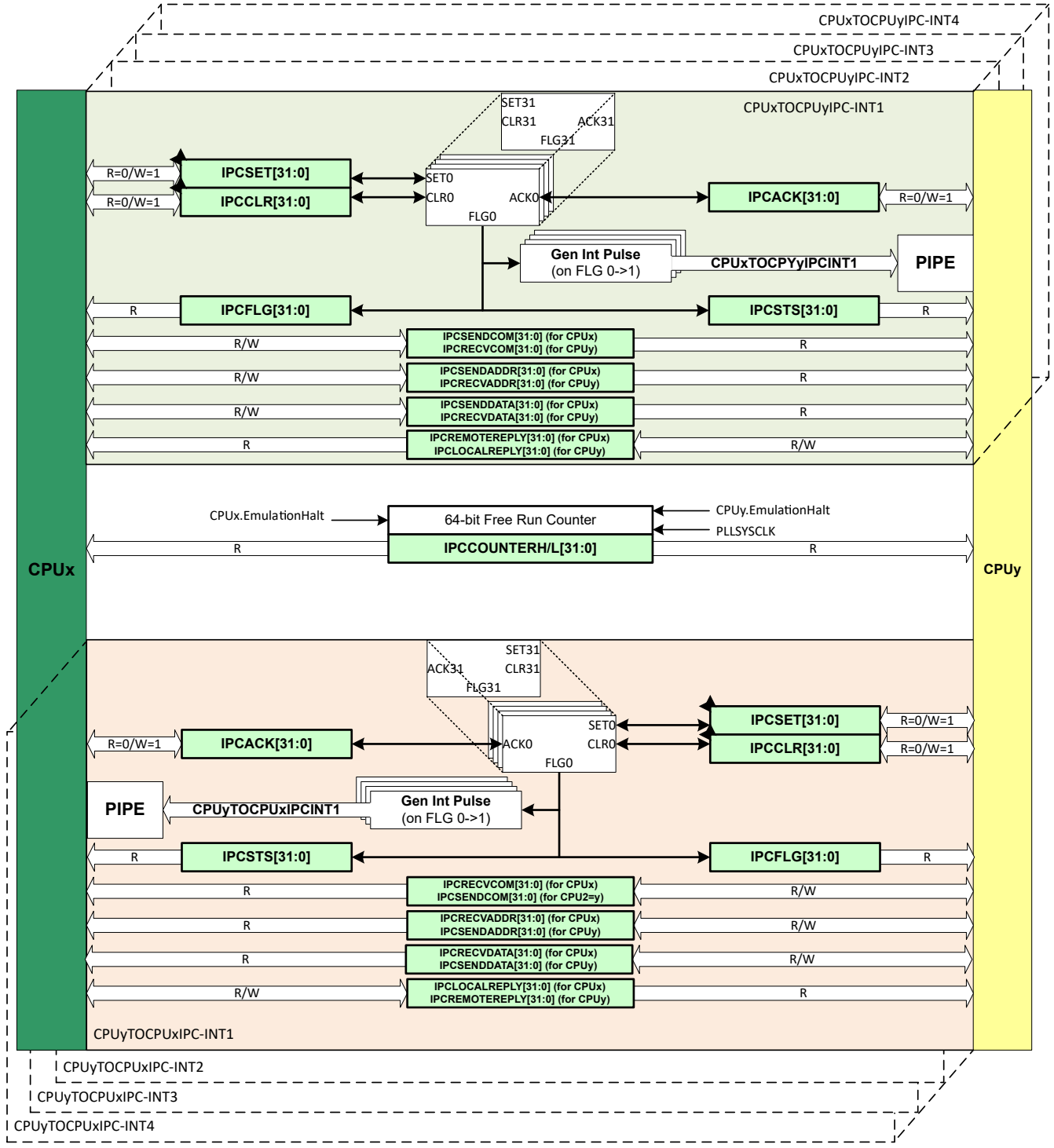


Figure 7-19. IPC Module Architecture

7.9.7 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ microcontrollers, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-20 shows the various functional blocks within the watchdog module.

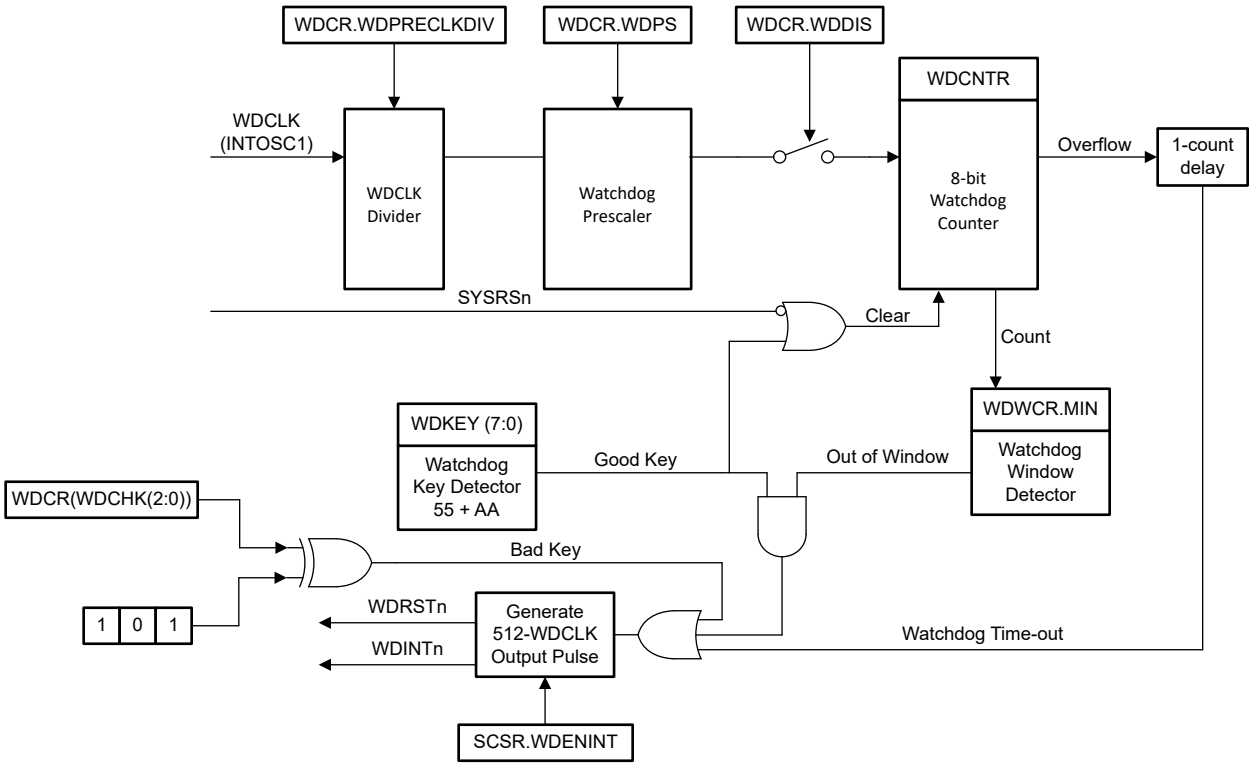


Figure 7-20. Windowed Watchdog

ADVANCE INFORMATION

7.9.8 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.9.8.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.9.8.2 Mapping of DCCx Clock Source Inputs

Table 7-44. DCCx Clock Source0 Table

DCCxCLKSRC0[3:0]	CLOCK NAME
0x0	XTAL/X1
0x1	INTOSC1
0x2	INTOSC2
0x4	TCK
0x5	CPU1.SYSCLK
0x8	AUXCLKIN
0xC	INPUT XBAR (Output16 of input-xbar)
others	Reserved

Table 7-45. DCCx Clock Source1 Table

DCCxCLKSRC1[4:0]	CLOCK NAME
0x0	PLLRAWCLK
0x2	INTOSC1
0x3	INTOSC2
0x6	CPU1.SYSCLK
0x9	Input XBAR (Output15 of the input-xbar)
0xA	AUXCLKIN
0xB	EPWMCLK
0xC	LSPCLK
0xD	ADCCLK
0xE	WDCLK
0xF	CAN0BITCLK
others	Reserved

7.9.9 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application notes and users guide, please refer to the following location in your C2000Ware for C2000 MCUs package (C2000Ware_2_00_00_03 and higher):

- **C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc**
- *CLB Tool User's Guide*
- *Designing With the C2000™ Configurable Logic Block (CLB)* Application Note
- *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers* Application Note

The CLB module and its interconnections are shown in Figure 7-21.

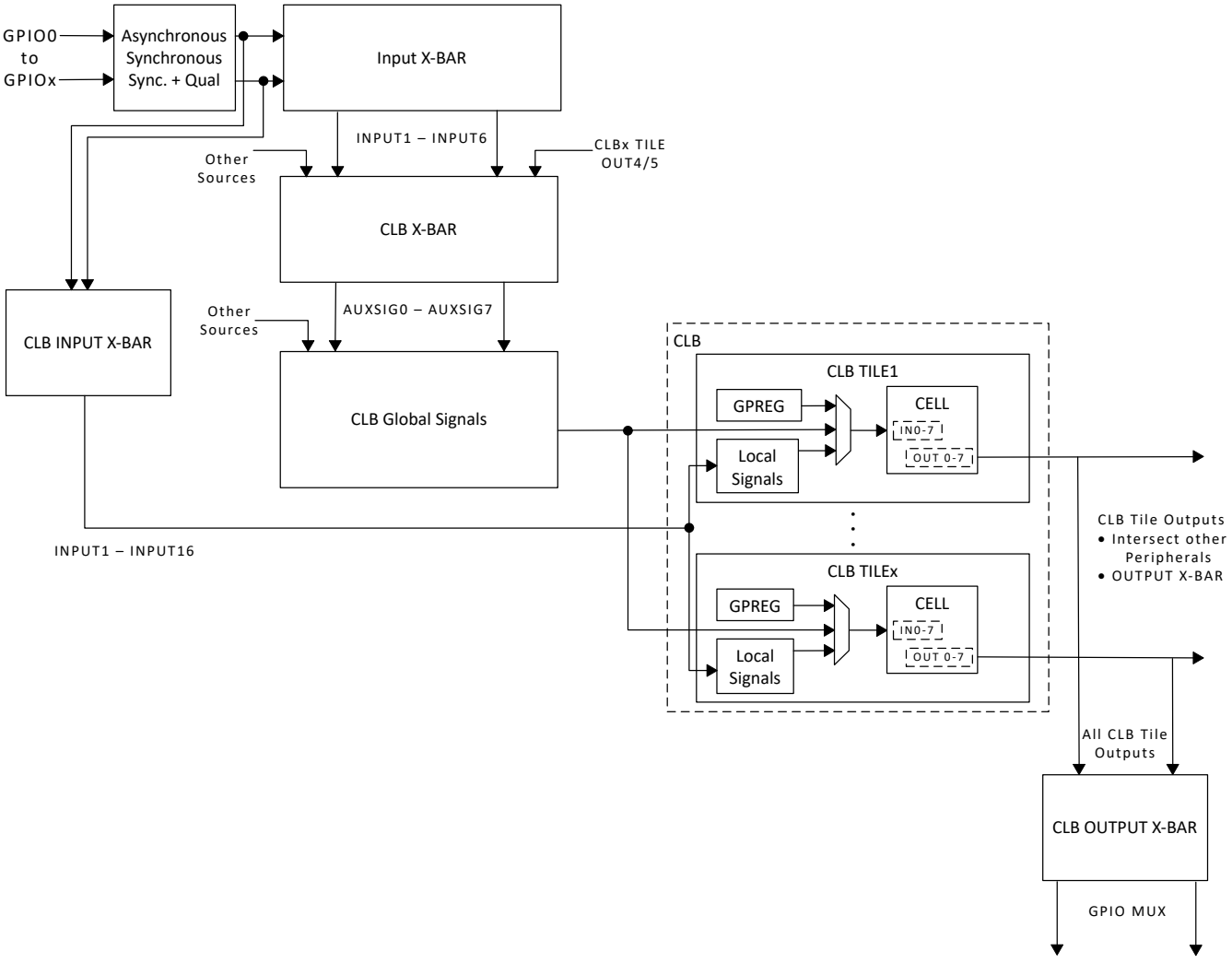


Figure 7-21. GPIO to CLB Tile Connections

Absolute encoder protocol interfaces are now provided as Position Manager solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with C2000Ware MotorControl SDK. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality.

7.10 Lockstep Compare Module (LCM)

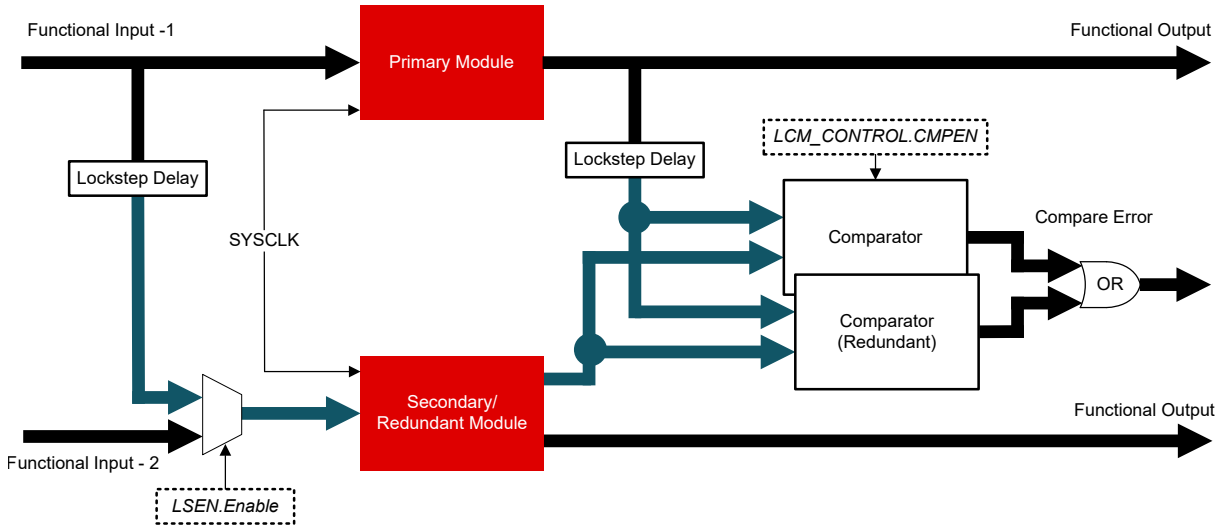
Hardware module integrity during run-time is a critical functional safety requirement. Hardware Redundancy implemented by the lockstep CPU architecture (two CPUs executing the same function and the output of the CPUs are continuously compared) is a proven method for achieving high diagnostic coverage for both permanent and transient faults. The Lockstep Comparator Module (LCM) is implemented to compare output from the CPU to detect permanent and transient faults.

The LCM implements the following features:

- Pipelined architecture
- Redundant comparison
- Self-test capability
  - Match and mismatch test
  - Error forcing capability
- Temporal redundancy: The operation of the two modules is skewed by two cycles to address the issue of common cause failures like failure of clock, power, and so on. This makes sure of temporal redundancy.
- Spatial redundancy: In the lockstep architecture, module instances are redundantly instantiated and the outputs are compared. Redundant instantiation provides spatial redundancy.
- Non-delayed functional output path to provide non-delayed CPU execution for the system (while still having temporal redundancy).
- Register protection of critical memory mapped registers of the module, using a parity scheme.

Figure 7-22 shows the LCM block diagram.

Figure 7-22. LCM Block Diagram



Note

The *Module* described in this block diagram can be either a CPU (for example, CPU1) or a peripheral (for example, RTDMA) depending on availability for the device.

ADVANCE INFORMATION

8 Applications, Implementation, and Layout

8.1 Reference Design

The TI Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all reference designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

Search and download TI reference designs at Select TI reference designs.

9 Device and Documentation Support

9.1 Device Nomenclature

Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

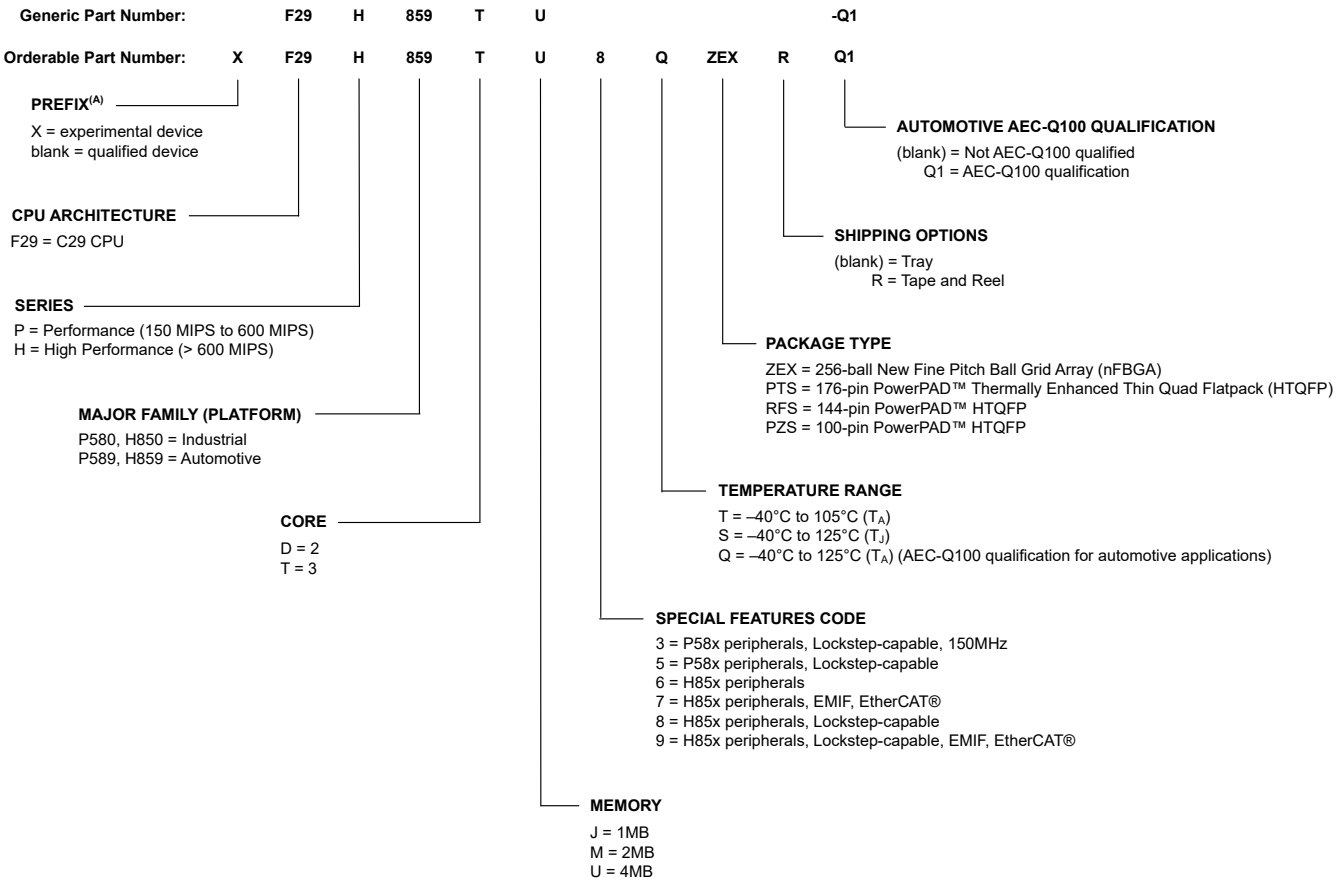
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZEX).

For device part numbers and further ordering information, contact your TI sales representative.

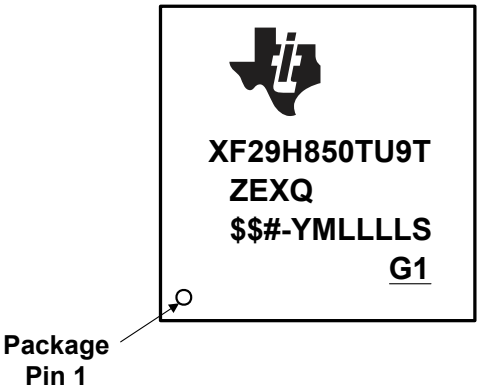


A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.2 Markings

Figure 9-2, Figure 9-3, Figure 9-4, and Figure 9-5 show the package symbolization. Table 9-1 lists the silicon revision codes.

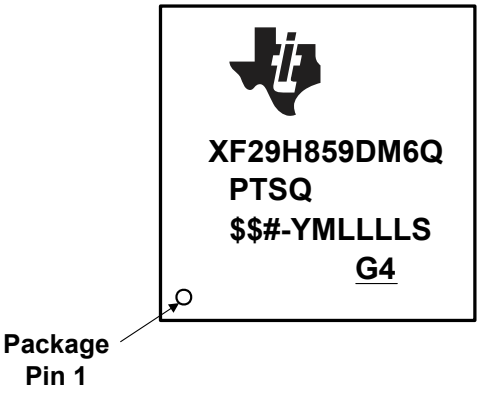


YMLLLLS = Lot Trace Code

$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code

G1 = Green (Low Halogen and RoHS-compliant)

Figure 9-2. Package Symbolization for ZEX Package

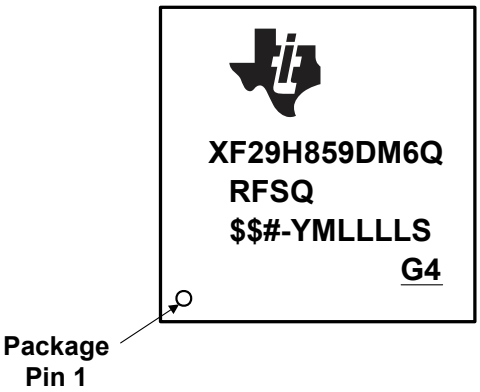


YMLLLLS = Lot Trace Code

$$ = Wafer Fab Code (one or two characters) as applicable
# = Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-3. Package Symbolization for PTS Package

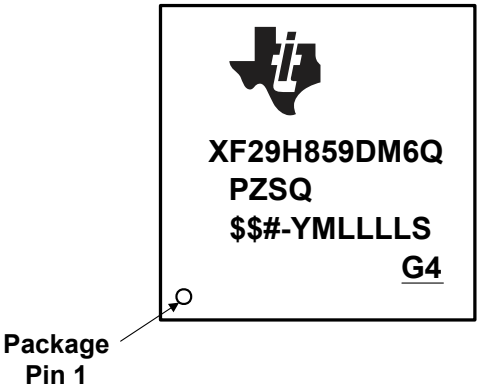


YMLLLLS = Lot Trace Code

$$ = Wafer Fab Code (one or two characters) as applicable
# = Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-4. Package Symbolization for RFS Package



YMLLLLS = Lot Trace Code

$$ = Wafer Fab Code (one or two characters) as applicable
# = Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-5. Package Symbolization for PZS Package

Table 9-1. Revision Identification

SILICON REVISION CODE	SILICON REVISION	REVID(1) Address: 0x5D00C	COMMENTS(2)
Blank	0	0x0000 0000	This silicon revision is available as pre-production.

(1) Silicon Revision ID
(2) For orderable device numbers, see the Packaging Information tables at the end of this data sheet.

ADVANCE INFORMATION

9.3 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

Development Tools

TI Resource Explorer
To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

SDK for C29 MCUs
TBD

DigitalPower SDK
DigitalPower SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI reference designs, which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

MotorControl SDK
MotorControl SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI reference designs, which are targeted for industrial drive and other motor control, MotorControl SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

CCS Theia
TBD

SysConfig System configuration tool
SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a stand-alone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the System configuration tool page.

C2000 Third-party search tool
TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

UniFlash flash programming tool
UniFlash is a software tool for programming on-chip flash on TI microcontrollers and wireless connectivity devices and on-board flash for TI processors. UniFlash provides both graphical and command-line interfaces.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL)

Models. To view all available models, visit the *Design tools & simulation* section of the *Design & development* page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site.

9.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Errata

F29H85x and F29P58x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F29H85x and F29P58x real-time microcontrollers.

User's Guides

F29x Hardware Security Manager (HSM) User’s Guide The Hardware Security Module (HSM) is a self-contained subsystem within the device that provides security and cryptographic functions. The host C29x subsystem interfaces with the HSM subsystem to perform the cryptographic operations required for code authentication, secure boot, secure firmware upgrades, and encrypted run-time communications.

F29x Cryptographic Hardware Accelerators User’s Guide The Hardware Security Manager (HSM) includes several hardware accelerators to enable fast execution of key cryptographic algorithms. These engines include a Data Transform and Hashing Engine (DTHE), an Advanced Encryption Standard Accelerator, a Public Key Engine (PKE), a Hash Algorithms, and a True Random Number Generator (TRNG).

C29x CPU and Instruction Set Reference Guide describes the CPU architecture, interrupt, pipeline, addressing modes, safety and security aspects of C29x CPU architecture. This manual also describes emulation features available on these devices.

Peripheral Guides

C2000 Real-Time Microcontrollers Peripherals Reference Guide describes all the peripherals available for TMS320x28x and F29x devices. This reference guide shows the peripherals used by each device and provides descriptions of the peripherals.

Tools Guides

TBD

ADVANCE INFORMATION

Application Notes

The SMT & packaging application notes website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

The Essential Guide for Developing With C2000™ Real-Time Microcontrollers provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

Migrating Software From 8-Bit (Byte) Addressable CPUs to C28x CPU discusses common scenarios of migrating software from 8-bit (byte) addressable CPUs to C28x CPU, and provides a guide on how to develop application irrespective of the addressability.

The *Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note* is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

9.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.6 Trademarks

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9.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

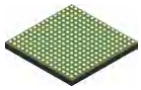
DATE	REVISION	NOTES
November 2024	*	Initial Release TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas. For SPI, all instances of legacy terminology have been changed to controller and peripheral. All instances of legacy pin names have been changed to: POCI (Peripheral OUT Controller IN); PICO (Peripheral IN Controller OUT); and CS (Chip Select). For the I2C Bus Interface, all instances of legacy terminology have been changed to controller and target. For the CAN and LIN Interface/BUS, all instances of legacy terminology have been changed to commander and responder. For the EtherCAT Controller, all instances of legacy terminology have been changed to MainDevice (or MDevice) and SubordinateDevice (or SubDevice).

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging website.

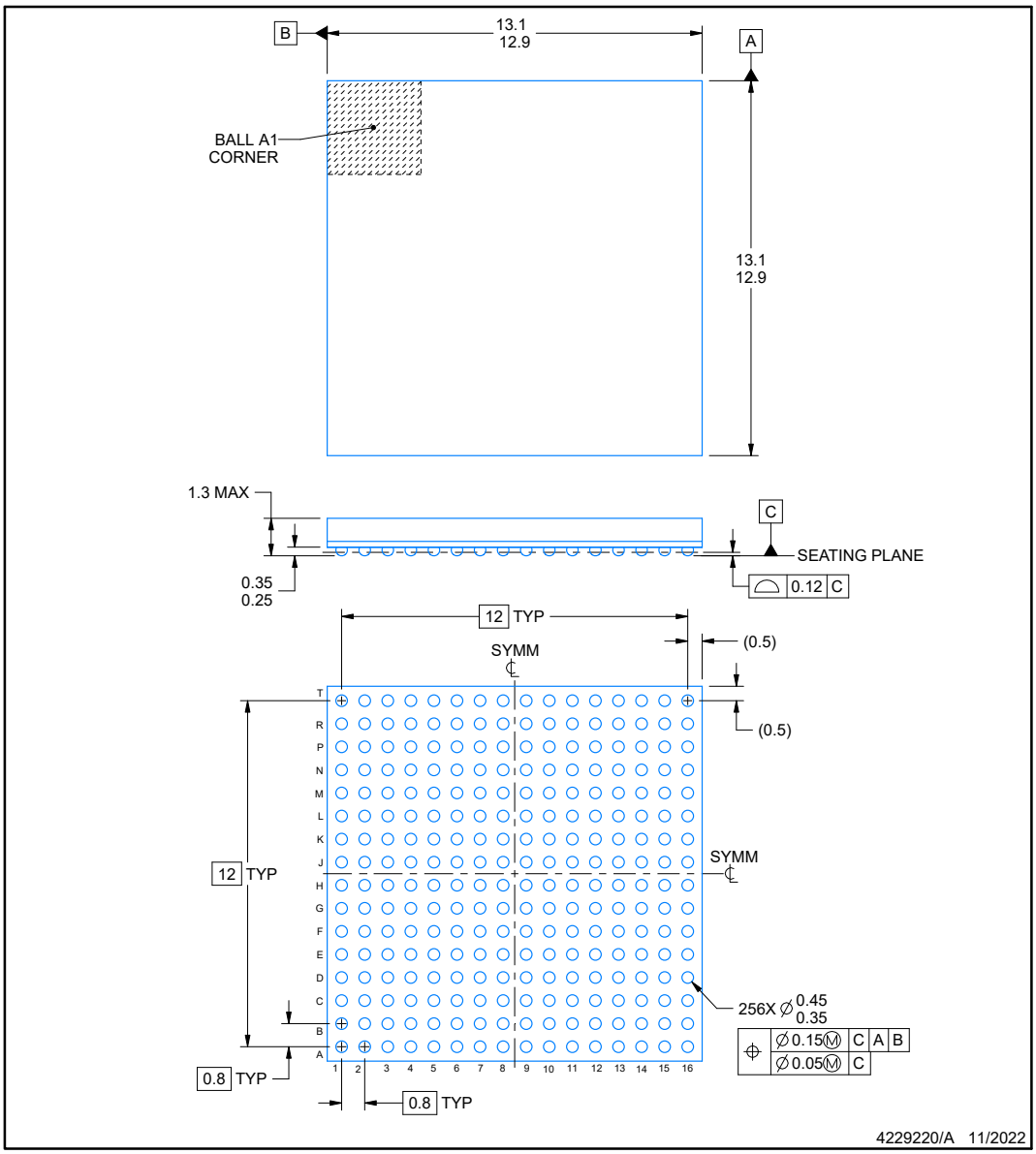


PACKAGE OUTLINE

ZEX0256A

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

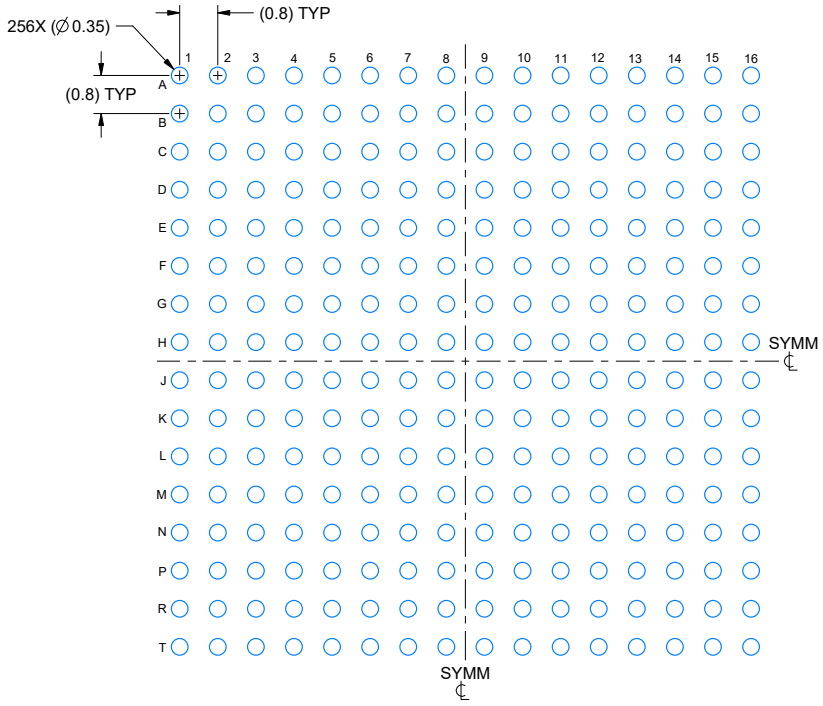
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

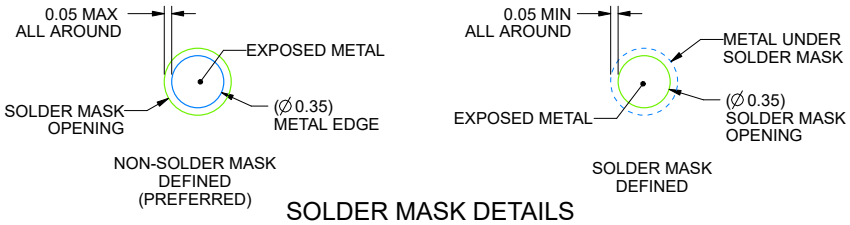
EXAMPLE BOARD LAYOUT

ZEX0256A — **NFBGA - 1.3 mm max height**

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4229220/A 11/2022

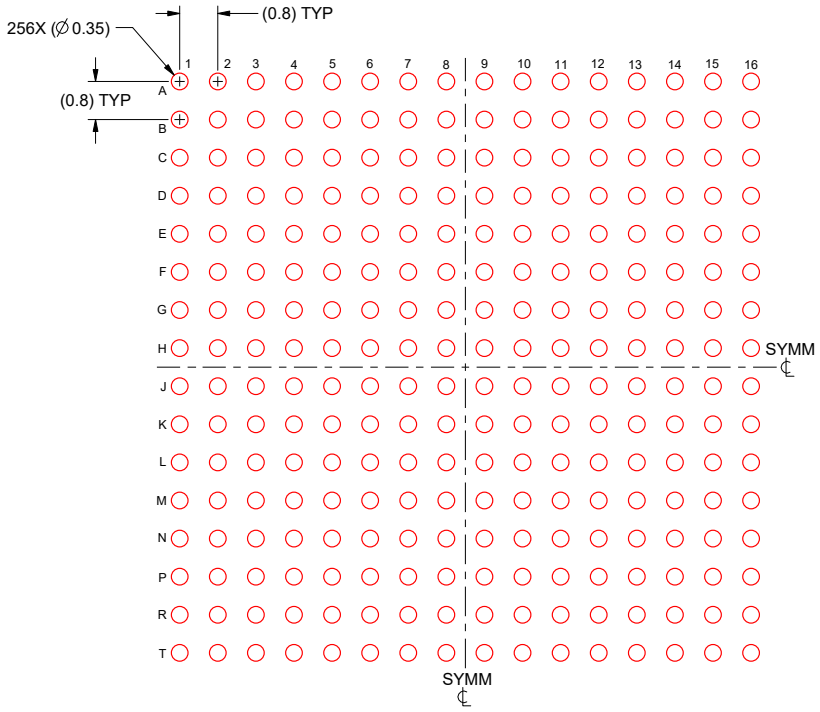
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZEX0256A **NFBGA - 1.3 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4229220/A 11/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ADVANCE INFORMATION

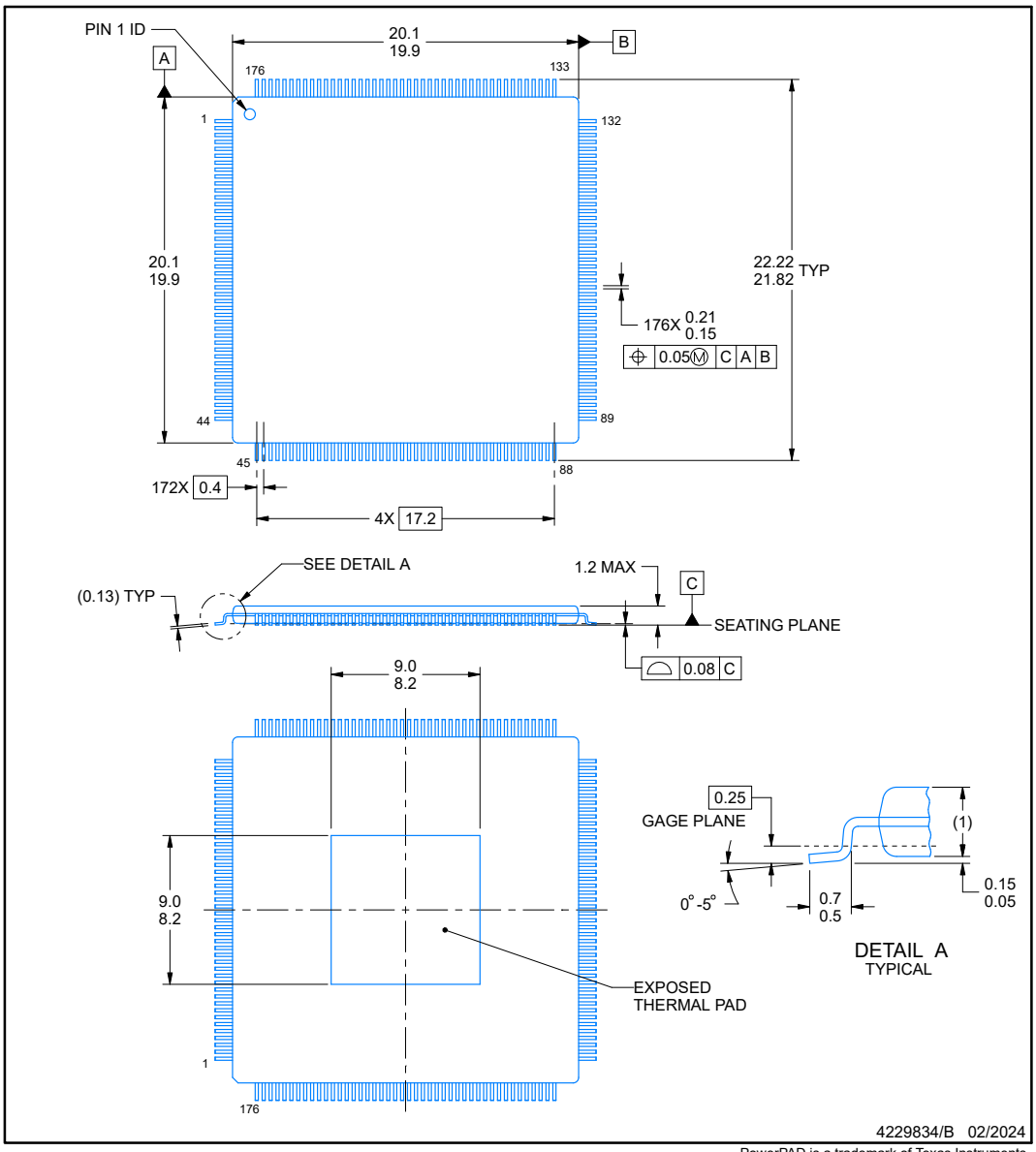
ADVANCE INFORMATION

PACKAGE OUTLINE

PTS0176A

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

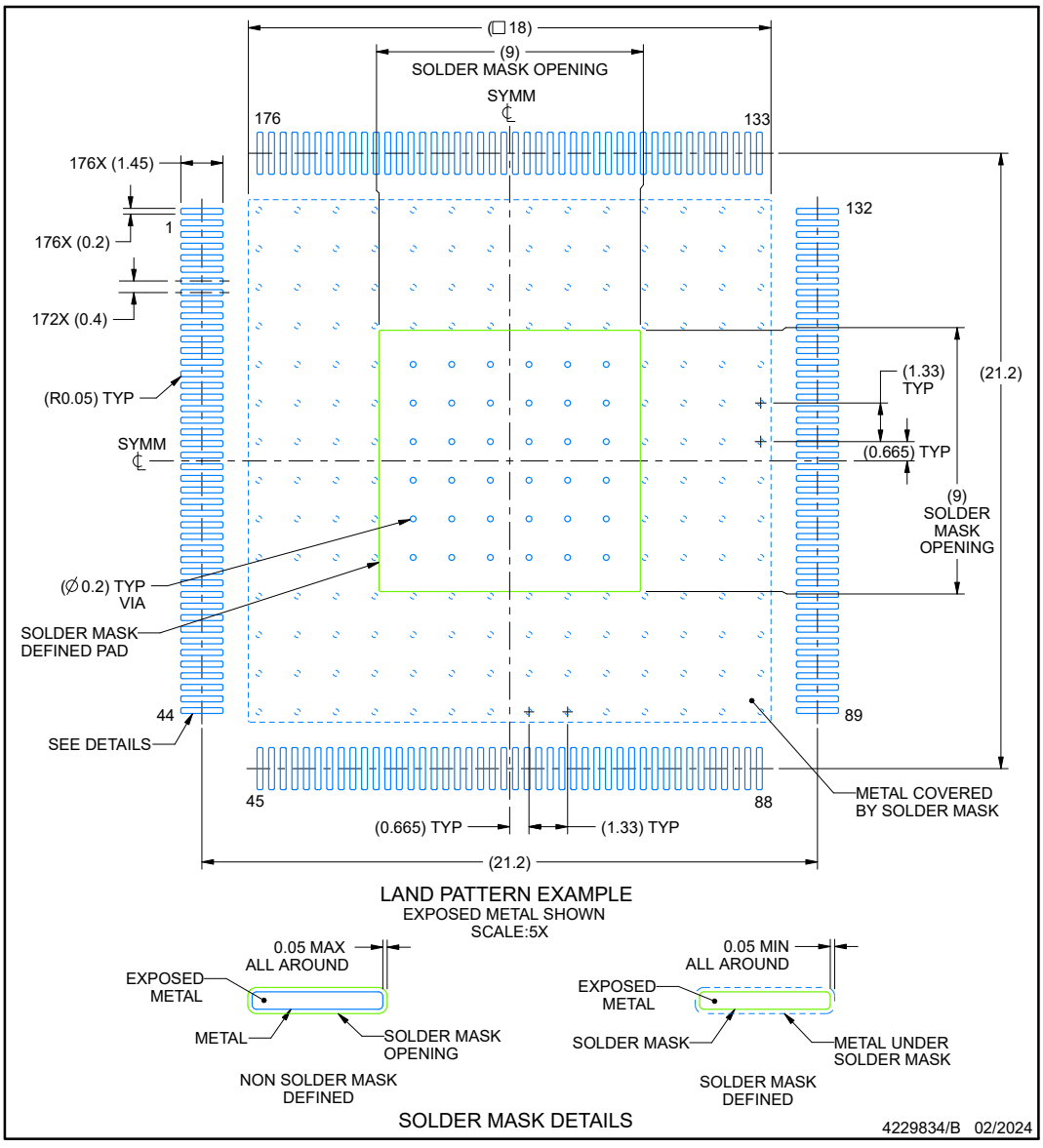
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. Strap features may not be present,

EXAMPLE BOARD LAYOUT

PTS0176A — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

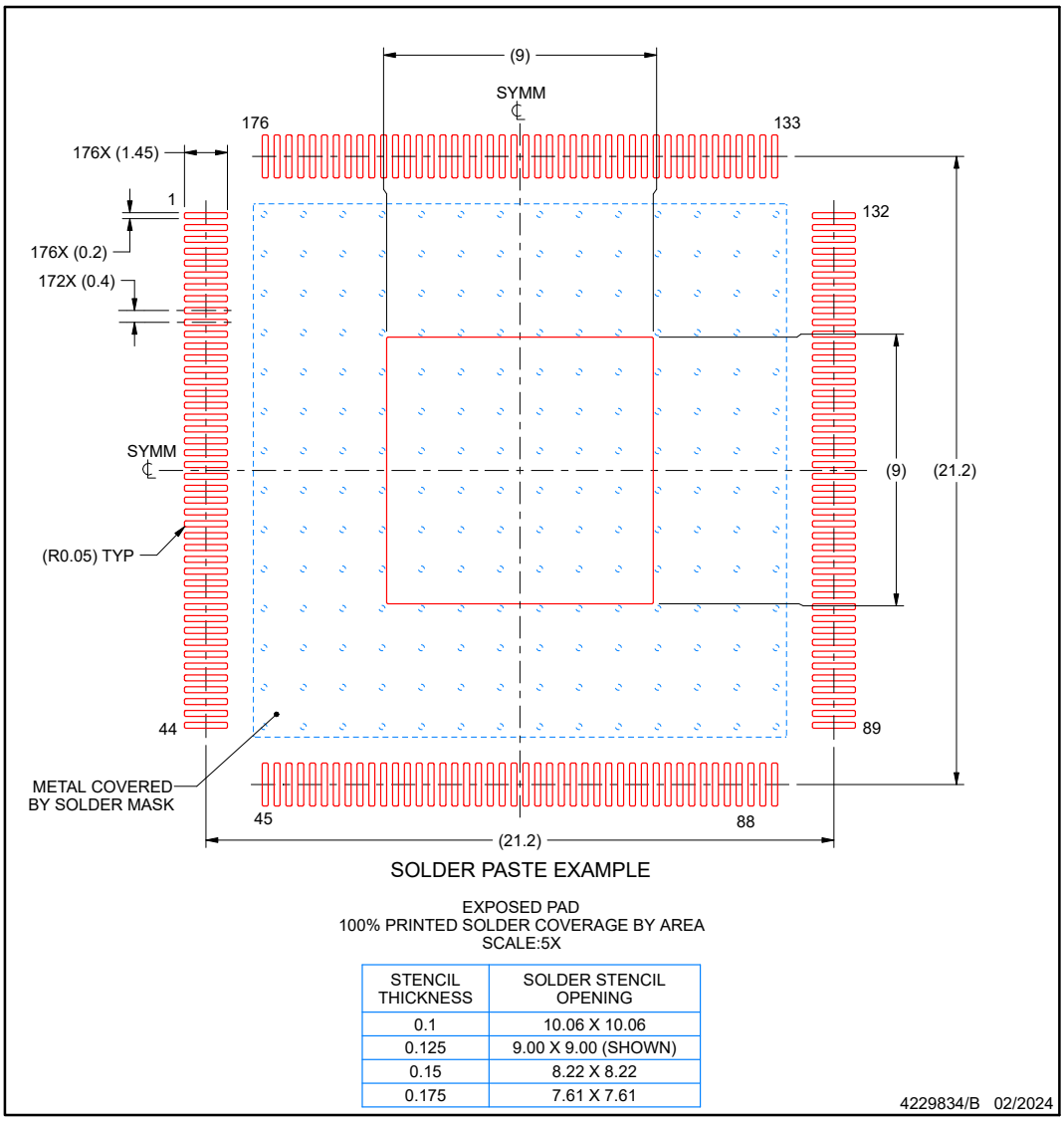
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PTS0176A — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE

EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:5X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	10.06 X 10.06
0.125	9.00 X 9.00 (SHOWN)
0.15	8.22 X 8.22
0.175	7.61 X 7.61

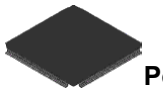
4229834/B 02/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

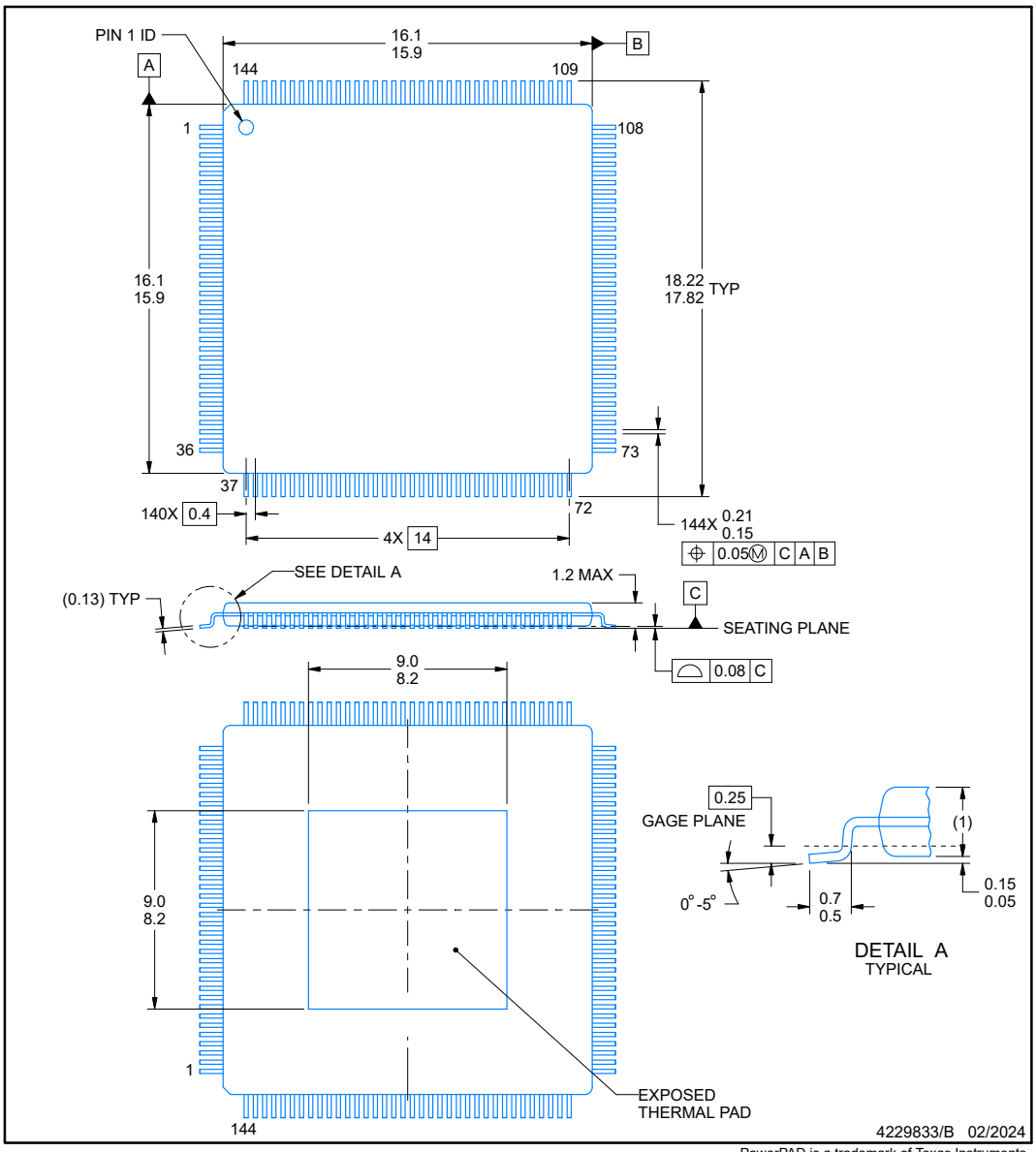
PACKAGE OUTLINE

RFS0144A



PowerPAD ™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

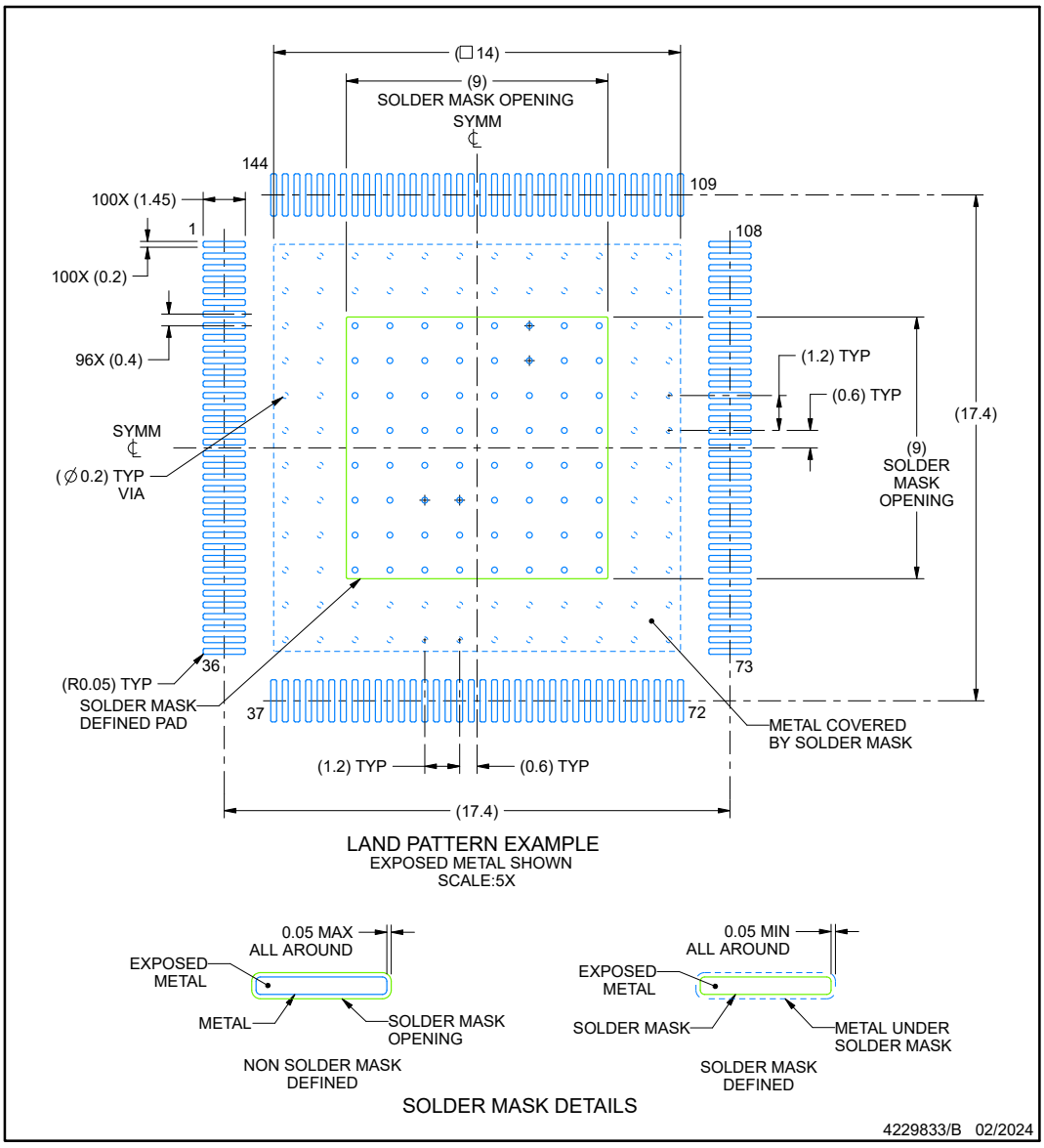
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. Strap features may not be present,

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RFS0144A — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



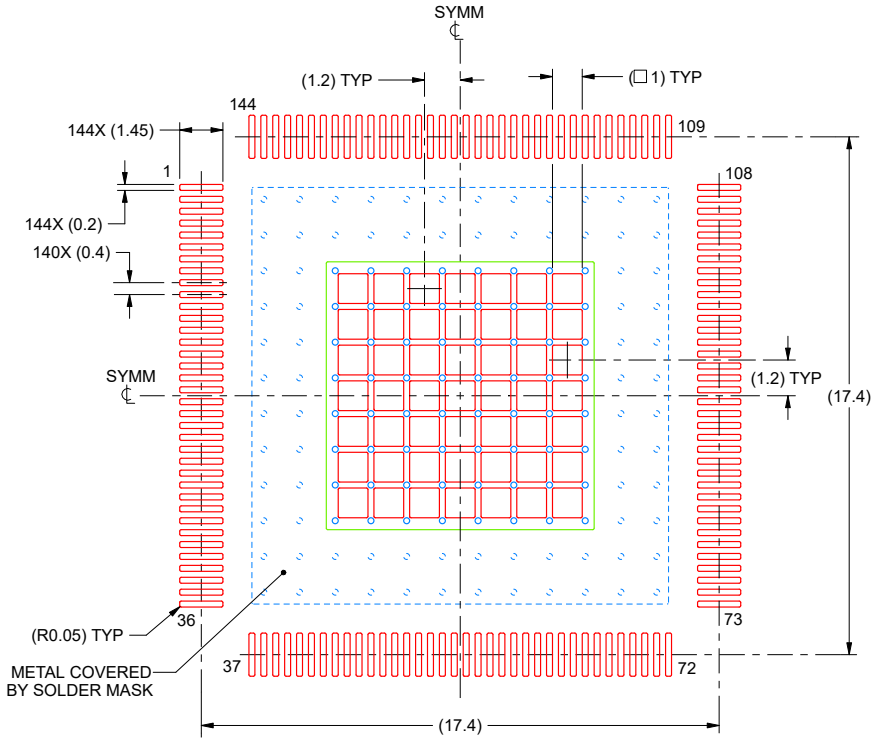
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

RFS0144A — **PowerPAD ™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
(BASED ON 0.125mm STENCIL THICKNESS)

SCALE:5X

4229833/B 02/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

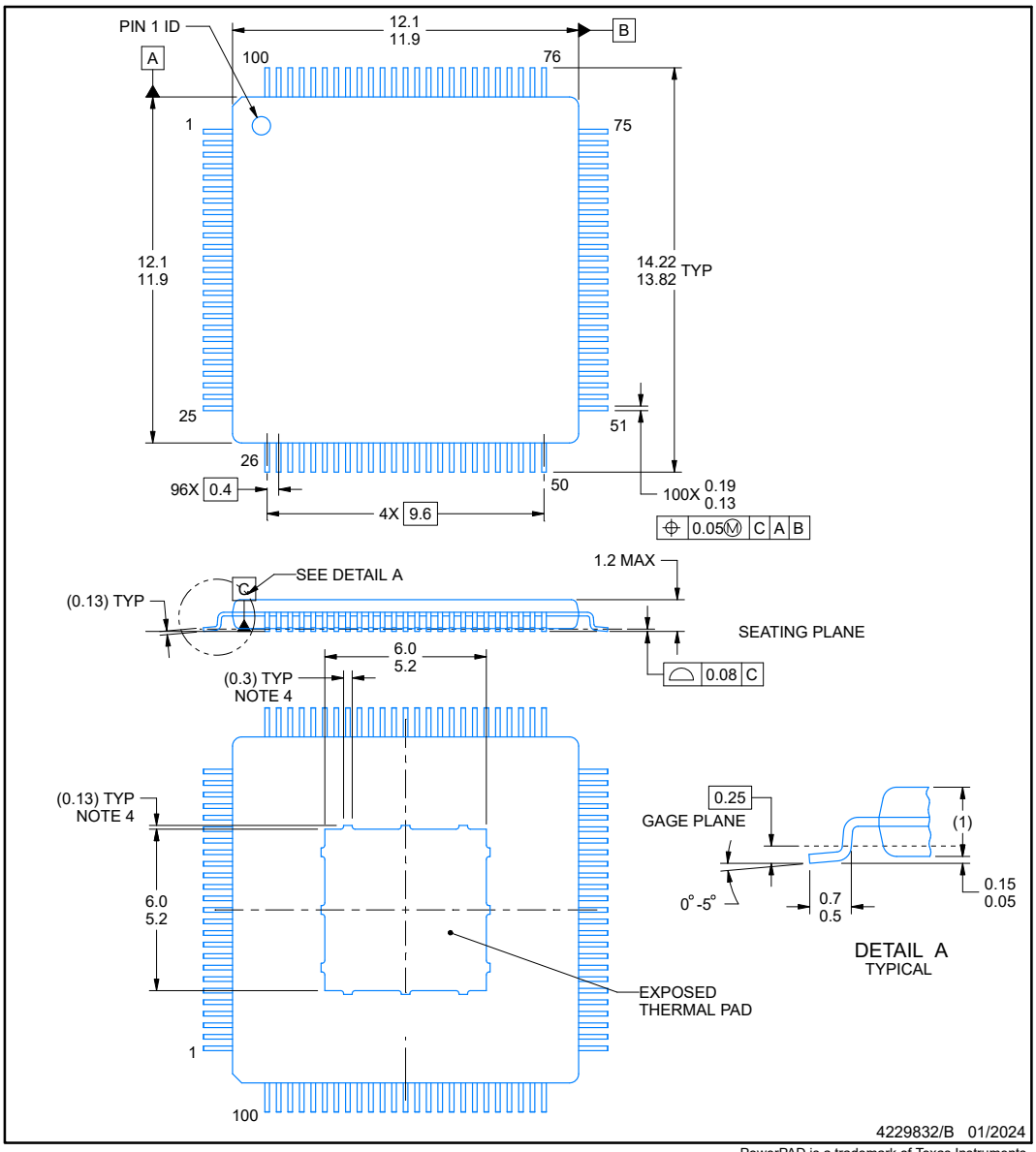
ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

PZS0100A — **PowerPAD ™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

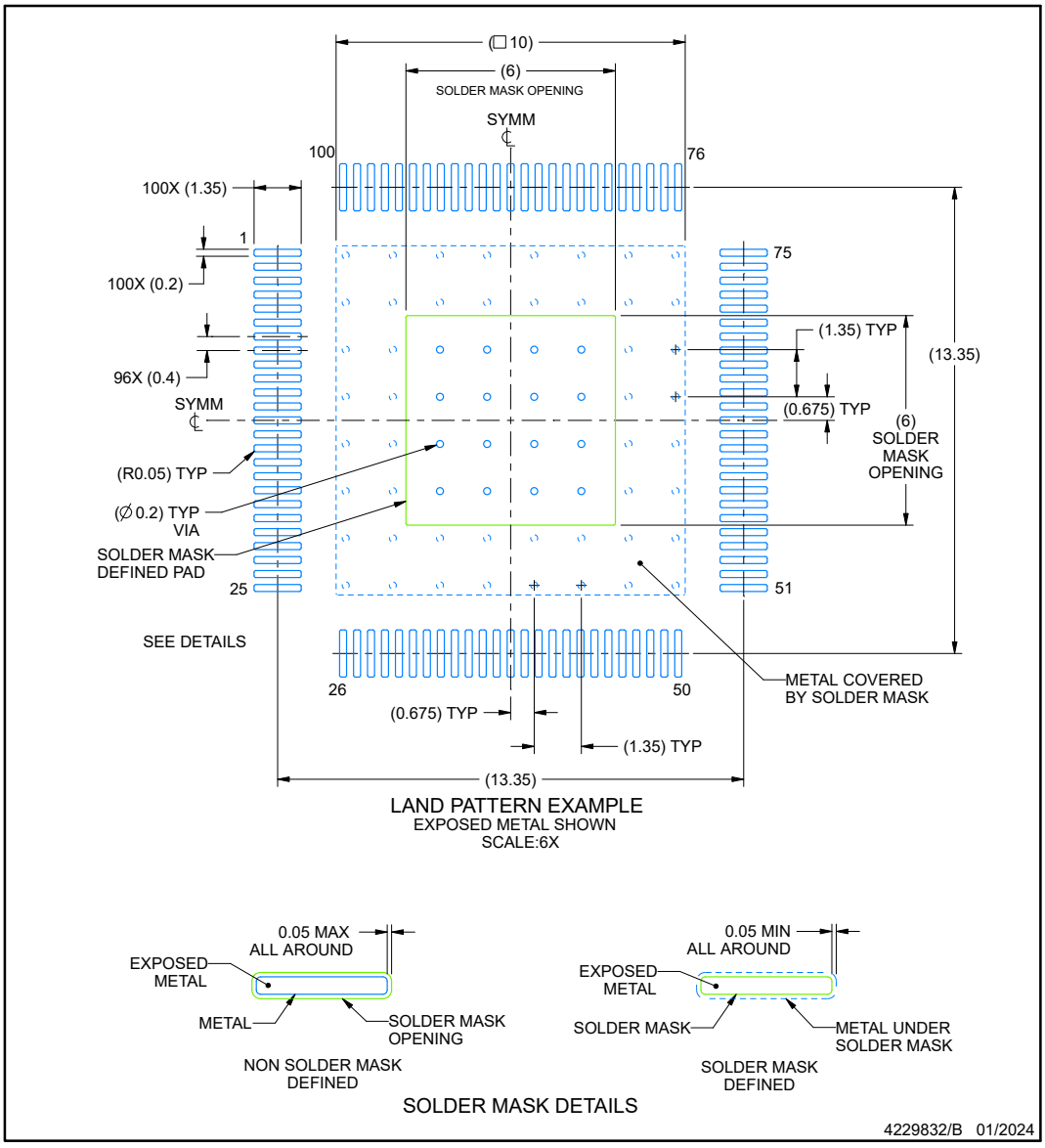
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. Strap features may not be present,

EXAMPLE BOARD LAYOUT

PZS0100A — **PowerPAD ™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

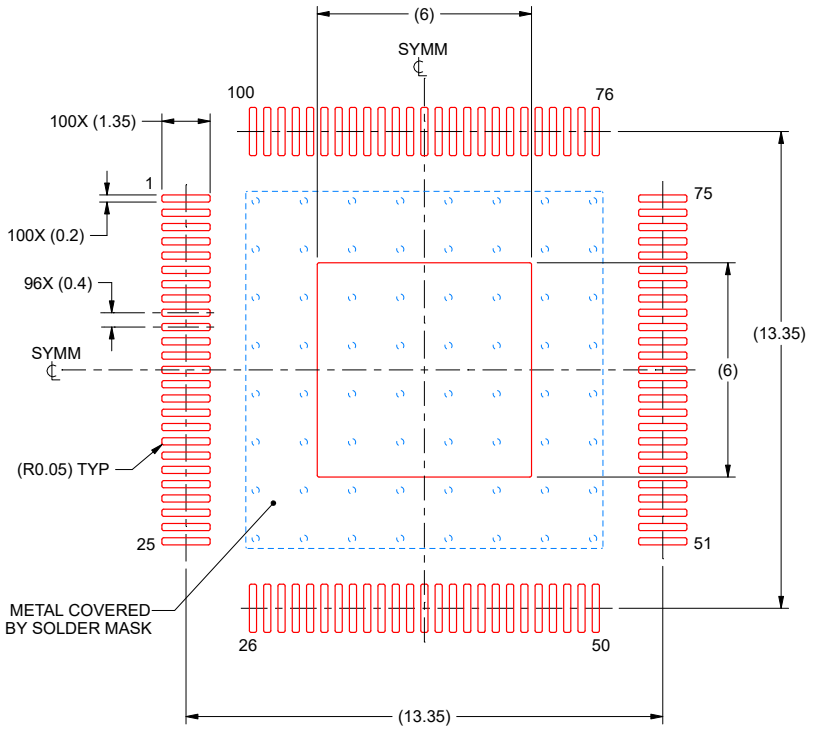
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PZS0100A — **PowerPAD ™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE

EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

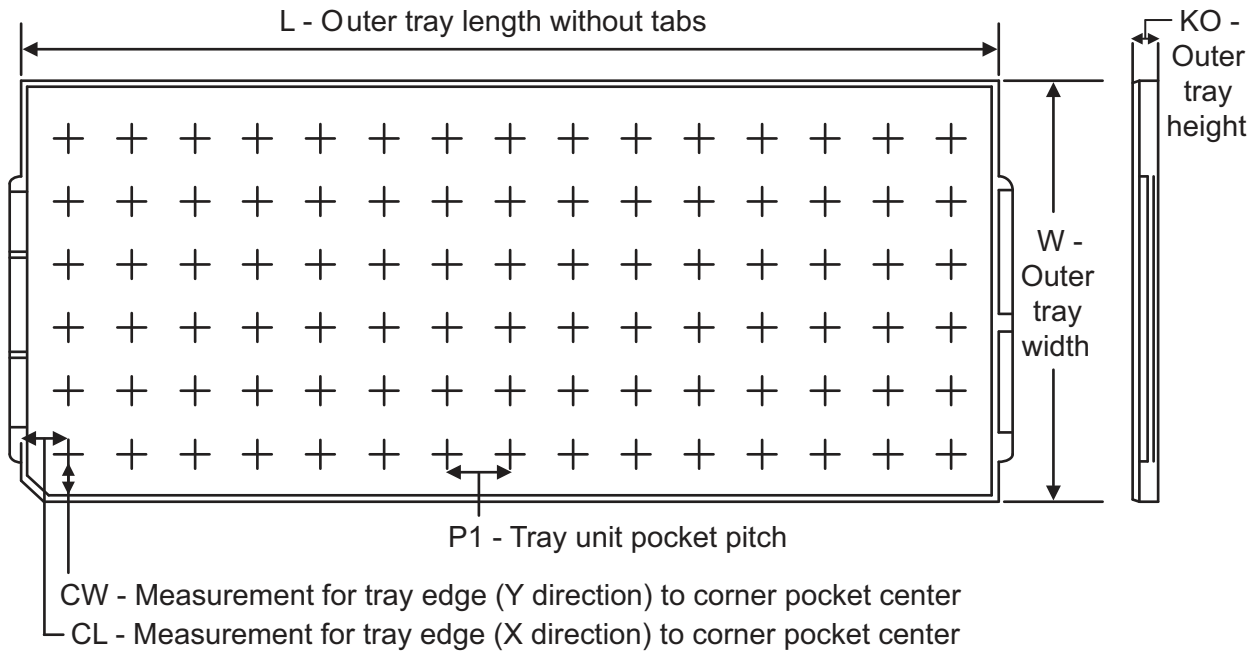
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.71 X 6.71
0.125	6.00 X 6.00 (SHOWN)
0.15	5.48 X 5.48
0.175	5.07 X 5.07

4229832/B 01/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

All dimensions are nominal.

Device	Package Type	Package Name	Pins	SPQ	Unit Array Matrix	Max Temp. (Deg C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
F29H85x												
XF29H859TU8QZEXQ1	nFBGA	ZEX	256	119	7 x 17	150	315	135.9	7620	18.1	12.7	12.9
XF29H850TU9TZEX	nFBGA	ZEX	256	119	7 x 17	150	315	135.9	7620	18.1	12.7	12.9
XF29H859TU8QPTSQ1	HTQFP	PTS	176	96	6 x 16	150	315	135.9	7620	20.7	30.4	20.7
XF29H850TU9SPTS	HTQFP	PTS	176	96	6 x 16	150	315	135.9	7620	20.7	30.4	20.7
XF29H859TU8QRFSQ1	HTQFP	RFS	144	84	6 x 14	150	315	135.9	7620	22	14.5	14.45
XF29H850TU9SRFS	HTQFP	RFS	144	84	6 x 14	150	315	135.9	7620	22	14.5	14.45
XF29H859TU8QPZSQ1	HTQFP	PZS	100	90	6 x 15	150	315	135.9	7620	15.4	20.3	21
F29P58x												
XF29P589DU5QZEXQ1	nFBGA	ZEX	256	119	7 x 17	150	315	135.9	7620	18.1	12.7	12.9
XF29P589DU5QPTSQ1	HTQFP	PTS	176	96	6 x 16	150	315	135.9	7620	20.7	30.4	20.7
XF29P589DU5QRFSQ1	HTQFP	RFS	144	84	6 x 14	150	315	135.9	7620	22	14.5	14.45
XF29P580DM5SRFS	HTQFP	RFS	144	84	6 x 14	150	315	135.9	7620	22	14.5	14.45
XF29P589DU5QPZSQ1	HTQFP	PZS	100	90	6 x 15	150	315	135.9	7620	15.4	20.3	21

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XF29H850TU9SPTS	PREVIEW	HTQFP	PTS	176	60	TBD	Call TI	Call TI	-40 to 125		
XF29H850TU9SRFS	PREVIEW	HTQFP	RFS	144	84	TBD	Call TI	Call TI	-40 to 125		
XF29H850TU9TZEX	ACTIVE	NFBGA	ZEX	256	119	TBD	Call TI	Call TI	-40 to 125		Samples
XF29H859TU8QPTSQ1	PREVIEW	HTQFP	PTS	176	60	TBD	Call TI	Call TI	-40 to 125		
XF29H859TU8QPZSQ1	PREVIEW	HTQFP	PZS	100	480	TBD	Call TI	Call TI	-40 to 125		
XF29H859TU8QRFSQ1	PREVIEW	HTQFP	RFS	144	420	TBD	Call TI	Call TI	-40 to 125		
XF29H859TU8QZEXQ1	PREVIEW	NFBGA	ZEX	256	119	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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