ISO644x General-Purpose, Reinforced, Quad-Channel Digital Isolators With Robust EMC

1 Features

- Up to 100Mbps data rate
- Robust SiO_2 isolation barrier:
  - Wide temperature range: –40°C to 125°C
  - Up to $5000V_{RMS}$ isolation rating
  - Up to 10.4kV surge capability
  - ±100kV/µs typical CMTI
- Supply range: 2.25V to 5.5V
- Default output *high* (ISO644x) and *low* (ISO644xF) options
- Low propagation delay: 6.2ns typical at 5V
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Wide-SOIC (DW-16) Package
- Safety-Related Certifications (Planned):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1 certifications

2 Applications

- Power supplies
- Grid, Electricity meter
- Motor drives
- Factory automation
- Building automation
- Lighting
- Appliances

3 Description

The ISO644x devices are high-performance, quad-channel digital isolators designed for cost-sensitive applications requiring up to $5000V_{RMS}$ isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO644x devices provide high electromagnetic immunity and low emissions at low power consumption while isolating CMOS or LVCMOS digital I/Os. ISO644x uses SiO_2 as the isolation barrier. Each isolation channel has a logic input and output buffer separated by the insulation barrier. These devices come with enable pins that can be used to put the respective outputs in high impedance for parallel (multiple) control driving applications.

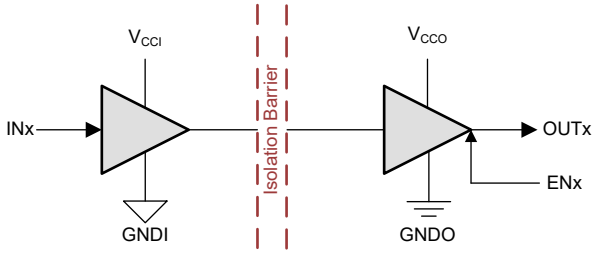
The ISO6441 and ISO6441F devices have one reverse-direction channel.

In the event of input power or signal loss, the default output is *high* for devices without the suffix F and *low* for devices with the suffix F. See the *Device Functional Modes* section for further details.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)
ISO6441	Wide-SOIC (DW-16)	10.30mm × 10.30mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

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4 Pin Configuration and Functions

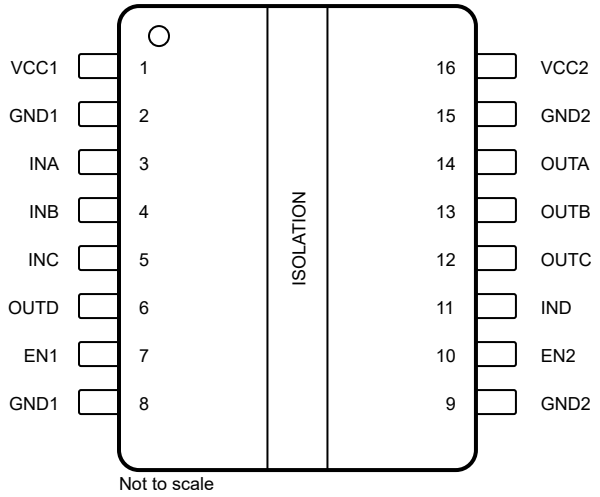

Figure 4-1. ISO6441 and ISO6441F Top View

Table 4-1. Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	ISO6441 , ISO6441F		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2,8	—	Ground connection for V_{CC1}
GND2	9,15	—	Ground connection for V_{CC2}
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

(1) I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Digital Input Voltage	INx to GNDx	-0.5	6	V
Digital Input Voltage	ENx to GNDx	-0.5	6	V
Digital Output Voltage	OUTx to GNDx	-0.5	V_{CCX} + 0.5 (3)	V
Digital Output current	I_O	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC_RO} (1)	Supply Voltage Side 1 (Recommended Operating Range)	V_{CC1} = 2.5V to 5V (3)	2.25		5.5	V
	Supply Voltage Side 2 (Recommended Operating Range)	V_{CC2} = 2.5V to 5V (3)	2.25		5.5	V
V_{CC_UVLO+}	V_{CC} UVLO threshold when supply voltage is rising				2.24	V
V_{CC_UVLO-}	V_{CC} UVLO threshold when supply voltage is falling		1.6			V
$V_{CC\_UVLO\_HYS}$	V_{CC} Supply voltage UVLO hysteresis		0.1			V
$V_{IH(ENx)}$	Enable: High level Input voltage	Enable: High level Input voltage	0.7 x V_{CCI} (2)		V_{CCI}	V
$V_{IL(ENx)}$	Enable: Low level Input voltage	Enable: Low level Input voltage	0		0.3 x V_{CCI}	V
$V_{IH(INx)}$	Input: High level Input voltage		0.7 x V_{CCI} (2)		V_{CCI}	V
$V_{IL(INx)}$	Input: Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	Output: High level output current	V_{CCO} = 5V (2)	-4			mA
		V_{CCO} = 3.3V (2)	-2			mA
		V_{CCO} = 2.5V (2)	-1			mA
I_{OL}	Output: Low level output current	V_{CCO} = 5V (2)			4	mA
		V_{CCO} = 3.3V (2)			2	mA
		V_{CCO} = 2.5V (2)			1	mA
DR	Data Rate		0		100	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) The channel outputs are in undetermined state when $V_{CC\_UVLO-} \le V_{CC1}$, $V_{CC2} < V_{CC\_RO(MIN)}$.

5.4 Thermal Information

		THERMAL METRIC(1)						UNIT
PACKAGE	PINS	$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DW (Wide-SOIC)	16	83	48.5	49	28	48.4	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6441 (default high) and ISO6441F (default low, with F suffix)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L =15pF, Input a 50MHz 50% duty cycle square wave			201.9	mW
P_{D1}	Maximum power dissipation (side-1)				79.8	mW
P_{D2}	Maximum power dissipation (side-2)				122.1	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			16-DW	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t= 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	V_{IOSM} ≥ 1.3 x V_{IMP}; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input-output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 x V_{IORM}, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 x V_{IORM}, t_m = 10s	≤ 5	
		Method b: At routine test (100% production); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	≅2.4	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

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5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1, IEC 61010-1 and IEC 60601	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 83°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			273.8	mA
		$R_{\theta JA}$ = 83°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			418.3	mA
		$R_{\theta JA}$ = 83°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			547.6	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 83°C/W, T_J = 150°C, T_A = 25°C			1506	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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5.9 Electrical Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -4mA; See Section 6	V_{CCO} - 0.4 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 4mA; See Section 6			0.4	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 x V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 x V_{CCI}			V
$V_{I\_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.1 x V_{CCI}			V
$I_{IH(INx)}$	INx (input) high-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
$I_{IL(INx)}$	INx (input) low-level input current	V_{IL} = 0V at INx	-10			µA
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 x V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 x V_{CCI}			V
$V_{I\_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.1 x V_{CCI}			V
$I_{IH(ENx)}$	ENx (enable) high-level input current	V_{IH} = V_{CCI} (1) at ENx			10	µA
$I_{IL(ENx)}$	ENx (enable) low-level input current	V_{IL} = 0V at ENx	-10			µA
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 5V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.10 Supply Current Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6441 (default high) and ISO6441F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0 V (default low, with F suffix)		I_{CC1}		3.5	4.6	mA
			I_{CC2}		2.3	3	
	V_I = 0 V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		9.8	11.5	
			I_{CC2}		4.4	5.1	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1Mbps	I_{CC1}		6.8	8	
			I_{CC2}		3.5	4.1	
		10Mbps	I_{CC1}		7.3	8.5	
			I_{CC2}		5	5.7	
		100Mbps	I_{CC1}		12.6	14.5	
			I_{CC2}		19	22.2	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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5.11 Electrical Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -2mA; See Section 6	V_{CCO} - 0.2 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 2mA; See Section 6			0.2	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 x V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 x V_{CCI}			V
$V_{I\_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.1 x V_{CCI}			V
$I_{IH(INx)}$	INx (input) high-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
$I_{IL(INx)}$	INx (input) low-level input current	V_{IL} = 0V at INx	-10			µA
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 x V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 x V_{CCI}			V
$V_{I\_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.1 x V_{CCI}			V
$I_{IH(ENx)}$	ENx (enable) high-level input current	V_{IH} = V_{CCI} (1) at ENx			10	µA
$I_{IL(ENx)}$	ENx (enable) low-level input current	V_{IL} = 0V at ENx	-10			µA
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 3.3V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.12 Supply Current Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6441 (default high) and ISO6441F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0 V (default low, with F suffix)		I_{CC1}		3.6	4.6	mA
			I_{CC2}		2.3	2.9	
	V_I = 0 V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		10	11.4	
			I_{CC2}		4.4	5	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		6.8	7.9	
			I_{CC2}		3.4	4	
		10Mbps	I_{CC1}		7.2	8.2	
			I_{CC2}		4.4	5	
		100Mbps	I_{CC1}		10.7	12.1	
			I_{CC2}		13.7	15.6	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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5.13 Electrical Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -1mA; See Section 6	V_{CCO} - 0.1 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 1mA; See Section 6			0.1	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 x V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 x V_{CCI}			V
$V_{I\_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.1 x V_{CCI}			V
$I_{IH(INx)}$	INx (input) high-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
$I_{IL(INx)}$	INx (input) low-level input current	V_{IL} = 0V at INx	-10			µA
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 x V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 x V_{CCI}			V
$V_{I\_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.1 x V_{CCI}			V
$I_{IH(ENx)}$	ENx (enable) high-level input current	V_{IH} = V_{CCI} (1) at ENx			10	µA
$I_{IL(ENx)}$	ENx (enable) low-level input current	V_{IL} = 0V at ENx	-10			µA
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 2.5V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.14 Supply Current Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6441 (default high) and ISO6441F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0 V (default low, with F suffix)		I_{CC1}		3.6	4.5	mA
			I_{CC2}		2.3	2.9	
	V_I = 0 V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		10	11.3	
			I_{CC2}		4.3	5	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		6.8	7.8	
			I_{CC2}		3.4	4	
		10Mbps	I_{CC1}		7.1	8.2	
			I_{CC2}		4.1	4.9	
		100Mbps	I_{CC1}		10.1	11.2	
			I_{CC2}		11.3	12.8	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

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5.15 Switching Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	@100kbps See Section 6		6.2	10	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.03	2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	ns
t_r	Output signal rise time	See Section 6			3	ns
t_f	Output signal fall time				3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6			9	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				8	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO644x				7	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO644x				8	ns
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			90	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC\_UVLO-(MIN)}$. See Section 6		0.055	0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.21		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

5.16 Switching Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	@100kbps See Section 6		7	12	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.26	2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	ns
t_r	Output signal rise time	See Section 6			4	ns
t_f	Output signal fall time				4	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6			14	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				12	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO644x				11	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO644x				10	ns
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			70	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC\_UVLO-(MIN)}$. See Section 6		0.06	0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.2		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

5.17 Switching Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	@100kbps See Section 6		8.4	14.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	ns
t_r	Output signal rise time	See Section 6			5	ns
t_f	Output signal fall time				5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 6			19	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				17	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO644x				17	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO644x				12	ns
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			80	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC\_UVLO-(MIN)}$. See Section 6		0.06	0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.22		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ADVANCE INFORMATION

5.18 Insulation Characteristics Curves

Insulation Characteristics Curves for Wide-SOIC (DW-16) Package

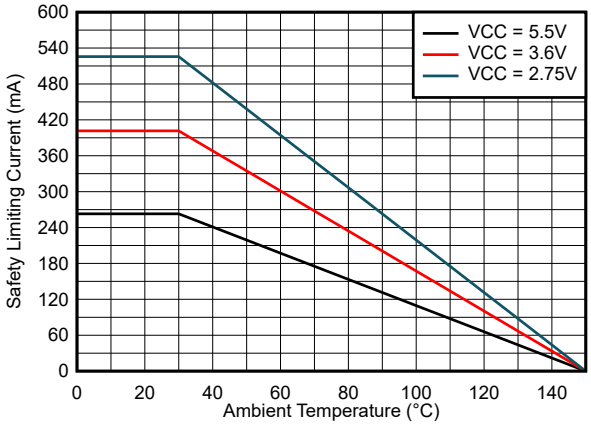


Figure 5-1. Thermal Derating Curve for Safety Limiting Current for Wide-SOIC (DW-16) Package

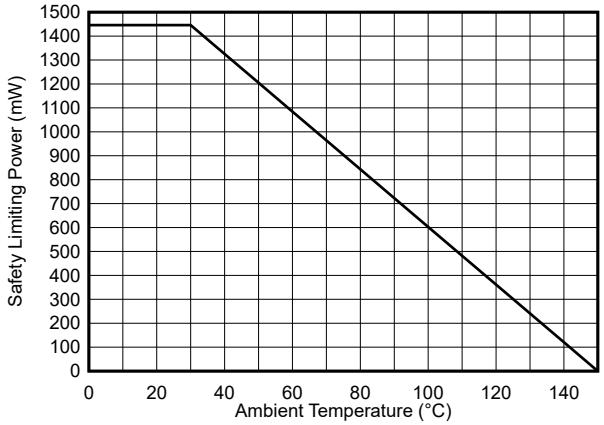
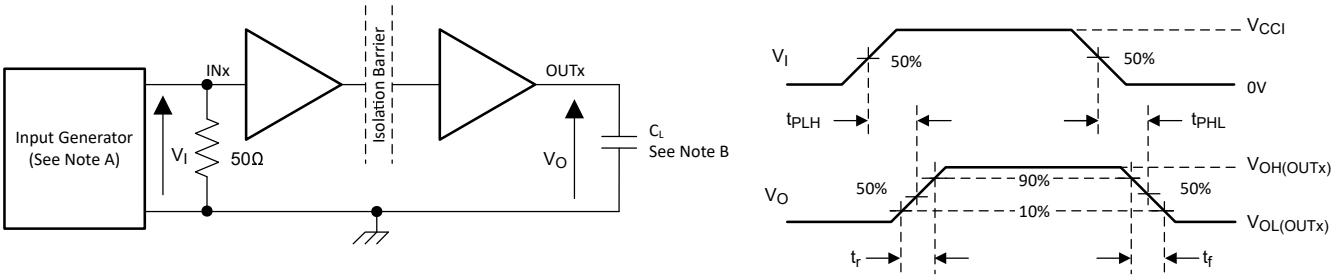


Figure 5-2. Thermal Derating Curve for Safety Limiting Power for Wide-SOIC (DW-16) Package

ADVANCE INFORMATION

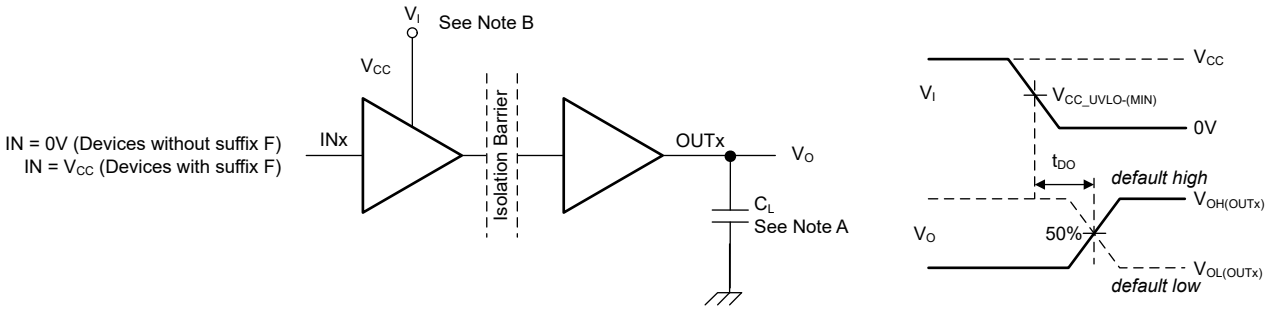
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 1ns, t_f ≤ 1ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate INx (input) generator signal. The 50Ω resistor is not needed in the actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

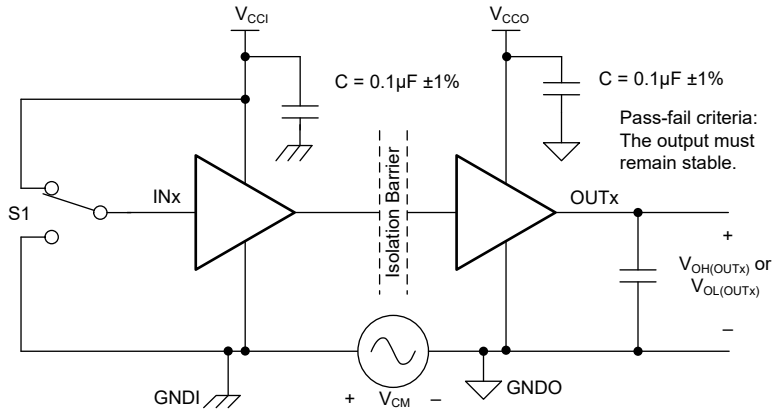
Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10mV/ns

Figure 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. ENx = V_{CC}, channels are enabled during CMTI test.

Figure 6-3. Common-Mode Transient Immunity Test Circuit

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The ISO644x family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier.

The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO644x devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching.

The conceptual block diagram of the digital isolator, Figure 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

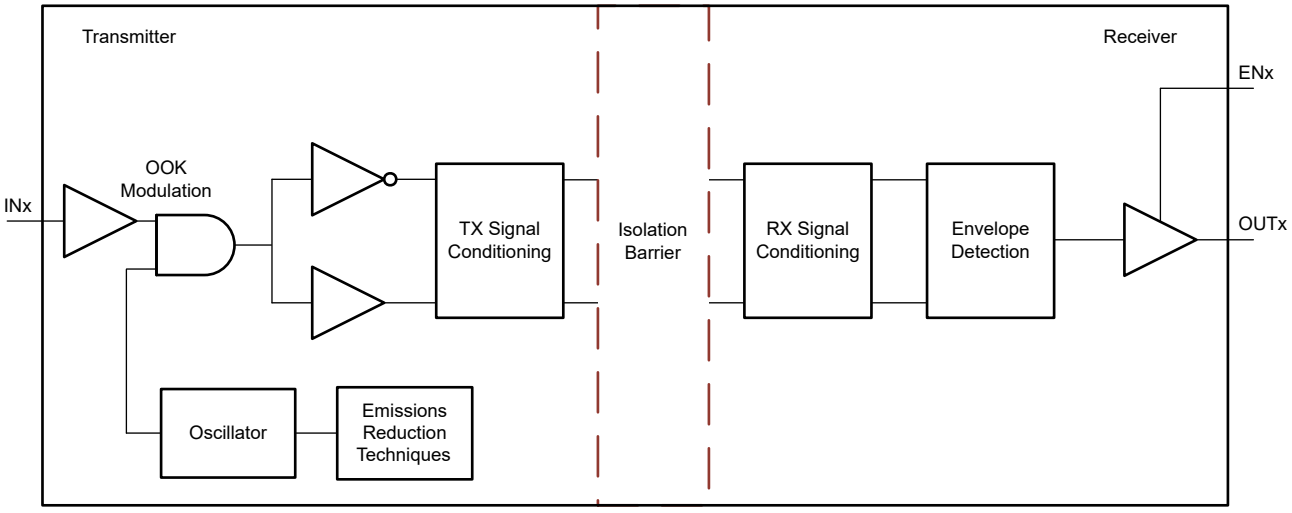


Figure 7-1. Conceptual Block Diagram of an OOK Based Digital Isolator

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

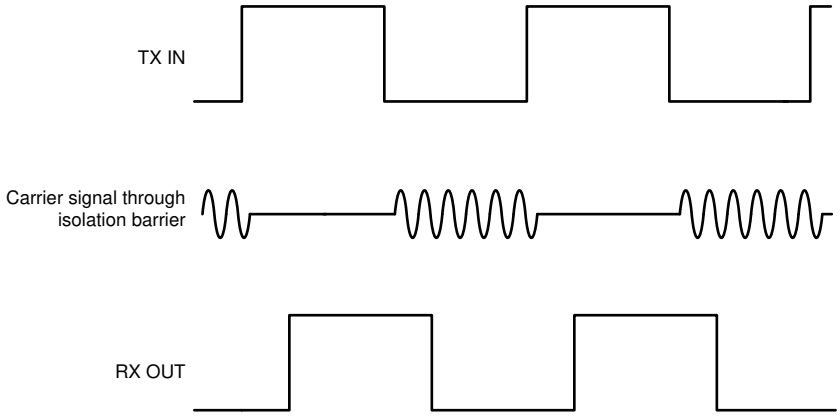


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE
ISO6441	3 Forward 1 Reverse	100Mbps	High	DW-16
ISO6441F	3 Forward 1 Reverse	100Mbps	Low	DW-16

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO644x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Higher on-chip decoupling capacitance to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by confirming purely differential internal operation.

7.4 Device Functional Modes

Table 7-2 lists the functional modes for the ISO644x devices.

Table 7-2. Function Table

V_{CCI}(1)	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is *High* for ISO644x and *Low* for ISO644xF (with F suffix).
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO644x and *Low* for ISO644xF (with F suffix). When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq V_{CC\_RO(MIN)}$); PD = Powered down ($V_{CC} \leq V_{CC\_UVLO-}$); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance

(2) The outputs are in undetermined state when $V_{CC\_UVLO-} \leq V_{CCI}$ or $V_{CCO} < V_{CC} \geq V_{CC\_RO(MIN)}$.

ADVANCE INFORMATION

7.5 Device I/O Schematics

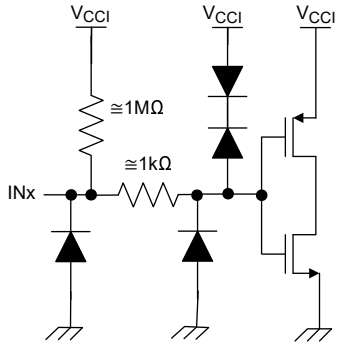


Figure 7-3. Input (INx) Default High (Device Without F Suffix Device) Schematics

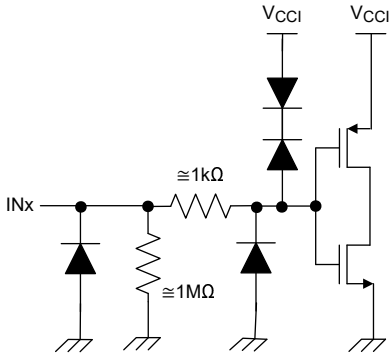


Figure 7-4. Input (INx) Default Low (Device With F Suffix Device) Schematics

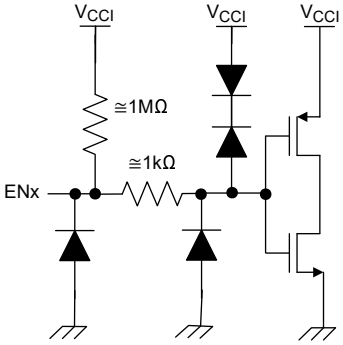


Figure 7-5. Enable (ENx) Schematics

ADVANCE INFORMATION

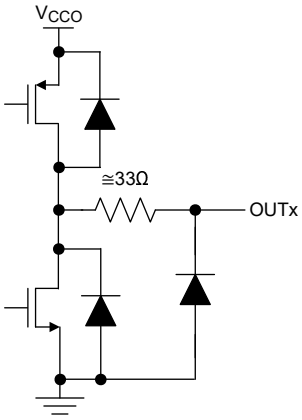


Figure 7-6. Output (OUTx) Schematics

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO644x devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for parallel (multiple) driver applications. The ISO644x devices use single-ended CMOS-logic switching technology.

The supply voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, supplying ISO644x V_{CC1} with 3.3V (which is within2.25V to 5.5V) and V_{CC2} with 5V (which is also within 2.25V to 5.5V) is possible. You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

Figure 8-1 shows the isolated serial peripheral interface (SPI).

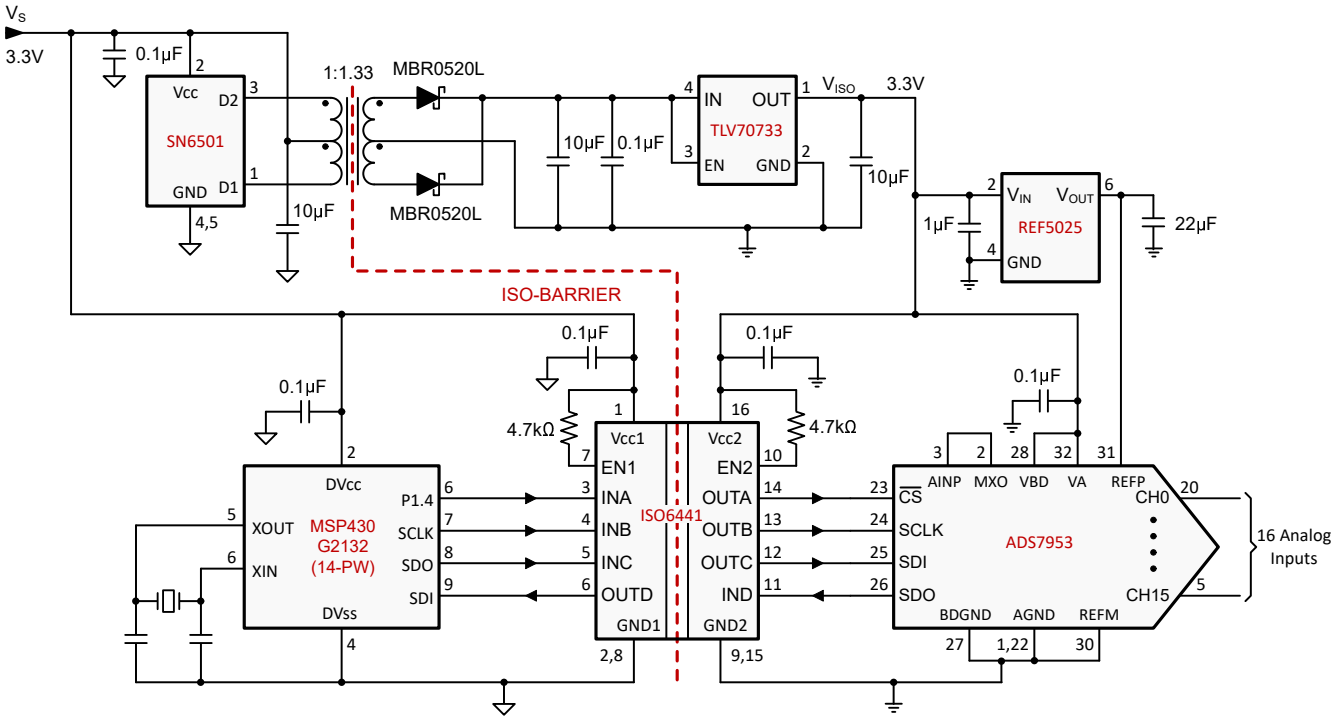


Figure 8-1. Isolated SPI for an Analog Input Module With 16 Inputs

8.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO644x family of devices only require two external bypass capacitors to operate.

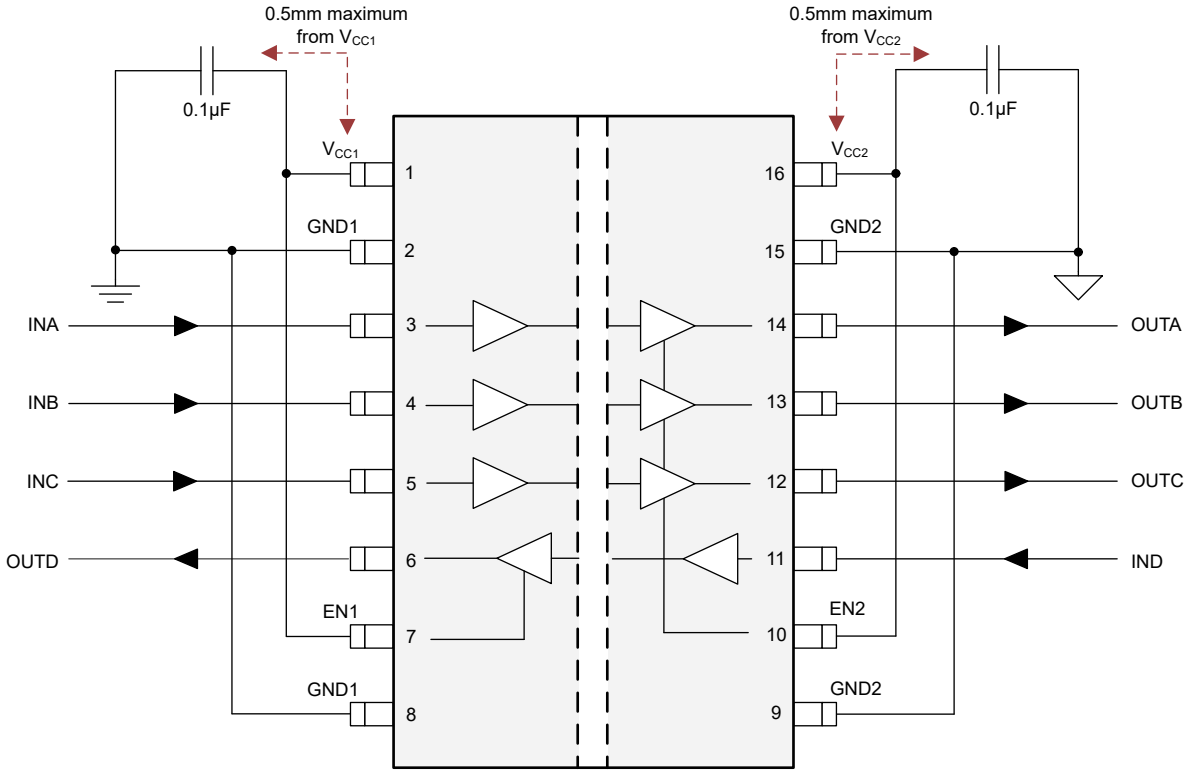
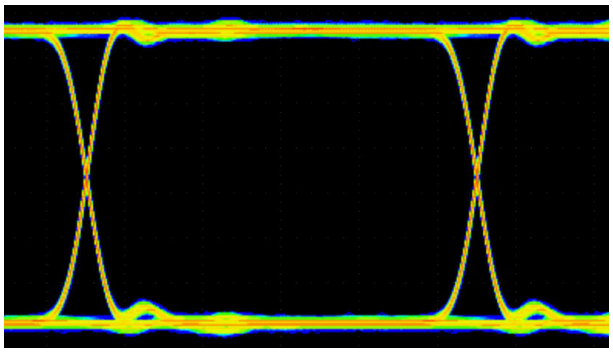


Figure 8-2. Typical ISO644x Circuit

ADVANCE INFORMATION

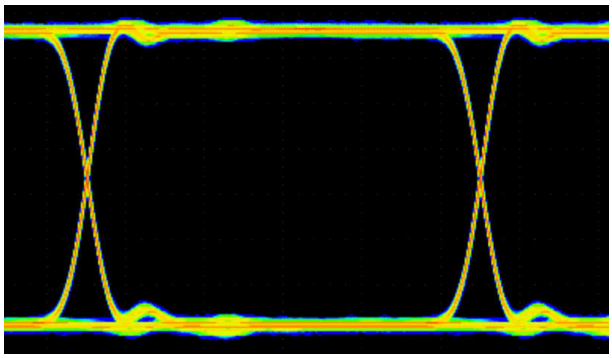
8.2.3 Application Curve

The following typical eye diagrams of the ISO644x family of devices indicates low jitter and wide open eye at the maximum data rate of 100Mbps.



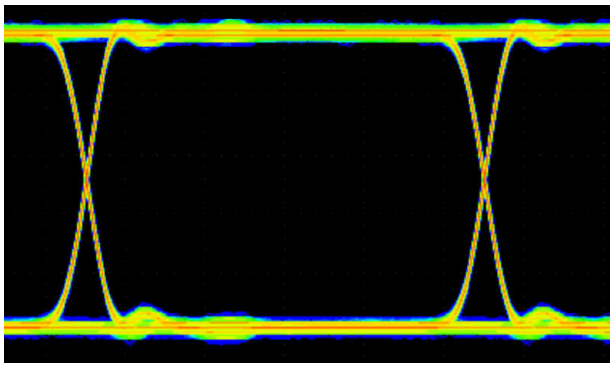
Horizontal 2ns / division, Vertical 1V / division.

Figure 8-3. ISO644x Eye Diagram at 100Mbps PRBS 2^{16} – 1, 5V and 25°C



Horizontal 2ns / division, Vertical 500mV / division.

Figure 8-4. ISO644x Eye Diagram at 100Mbps PRBS 2^{16} – 1, 3.3V and 25°C



Horizontal 2ns / division, Vertical 500mV / division.

Figure 8-5. ISO644x Eye Diagram at 100Mbps PRBS 2^{16} – 1, 2.5V and 25°C

8.3 Power Supply Recommendations

To provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' SN6501 or SN6505B. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505B Low-noise, 1-A Transformer Drivers for Isolated Power Supplies* .

8.4 Layout

8.4.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Layout Example). Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide* application note.

ADVANCE INFORMATION

8.4.2 Layout Example

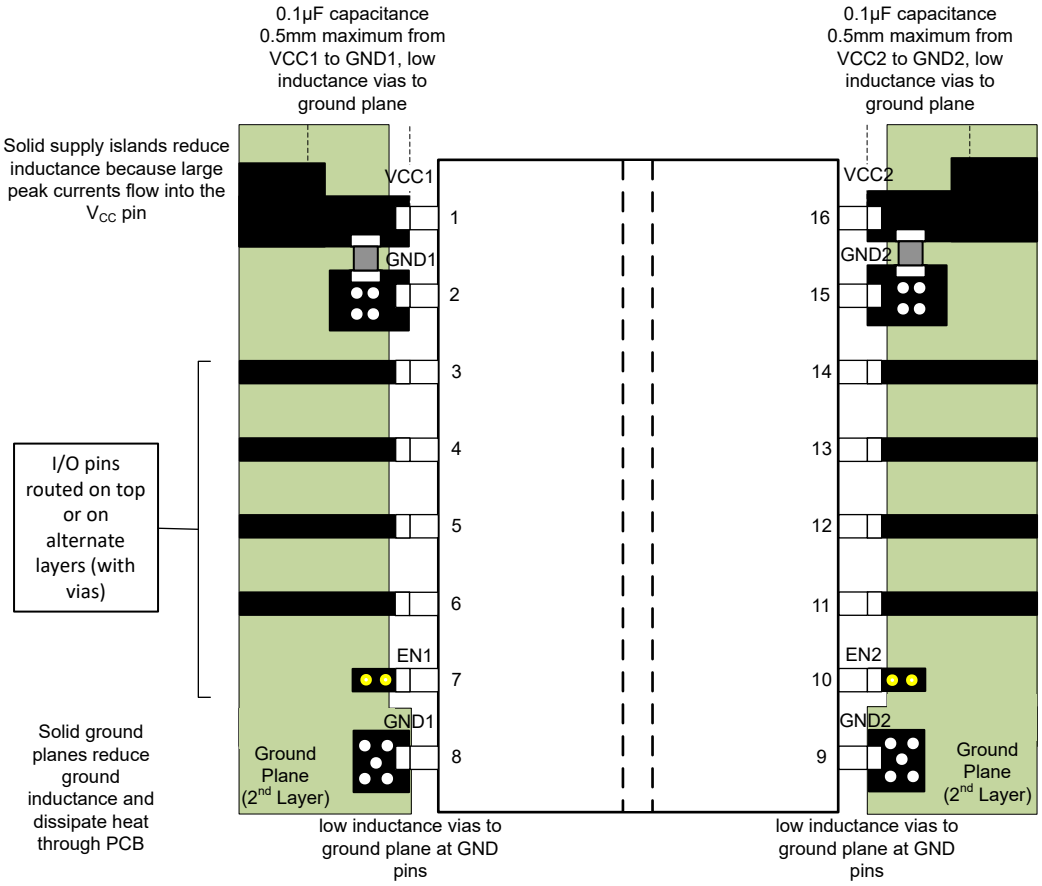


Figure 8-6. Layout Example

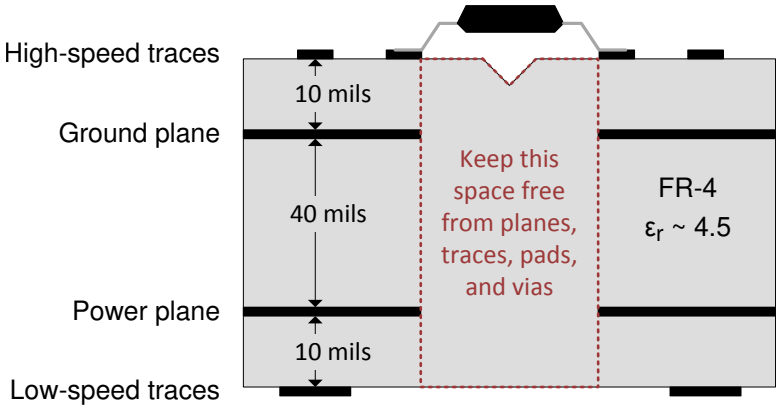


Figure 8-7. Layout Example PCB cross section

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*, application note
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*, data sheet
- Texas Instruments, *TPS76333 Low-Power 150-mA Low-Dropout Linear Regulators*, data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

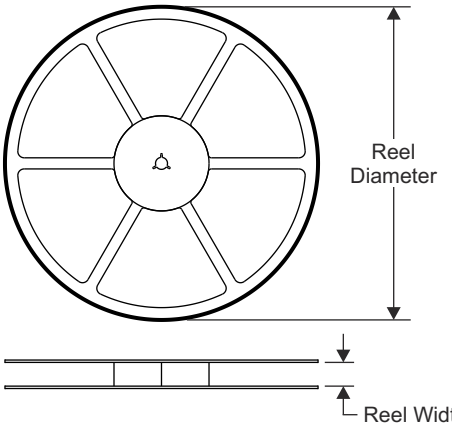
11.1 Package Option Addendum

Packaging Information

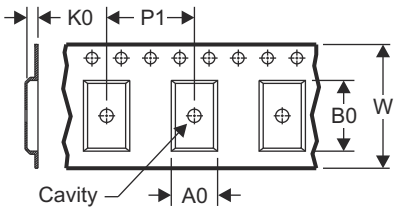
Orderable Device	Status[1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan[2]	Lead/Ball Finish[6]	MSL Peak Temp[3]	Op Temp (°C)	Device Marking[4] [5]
ISO6441DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6441

11.2 Tape and Reel Information

REEL DIMENSIONS

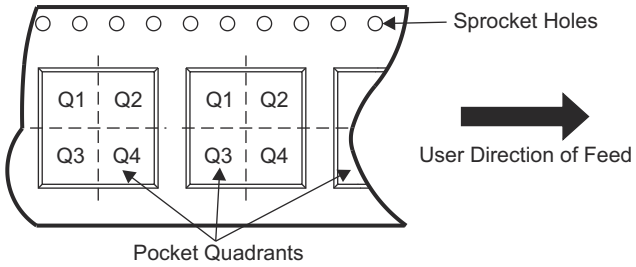


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6441DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

ADVANCE INFORMATION

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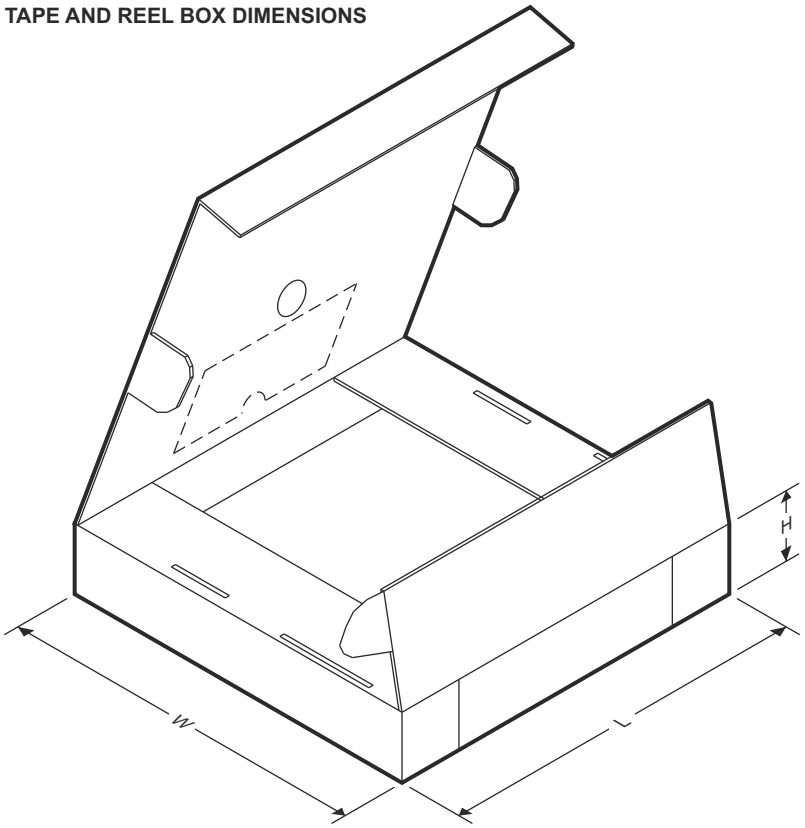
TAPE AND REEL BOX DIMENSIONS



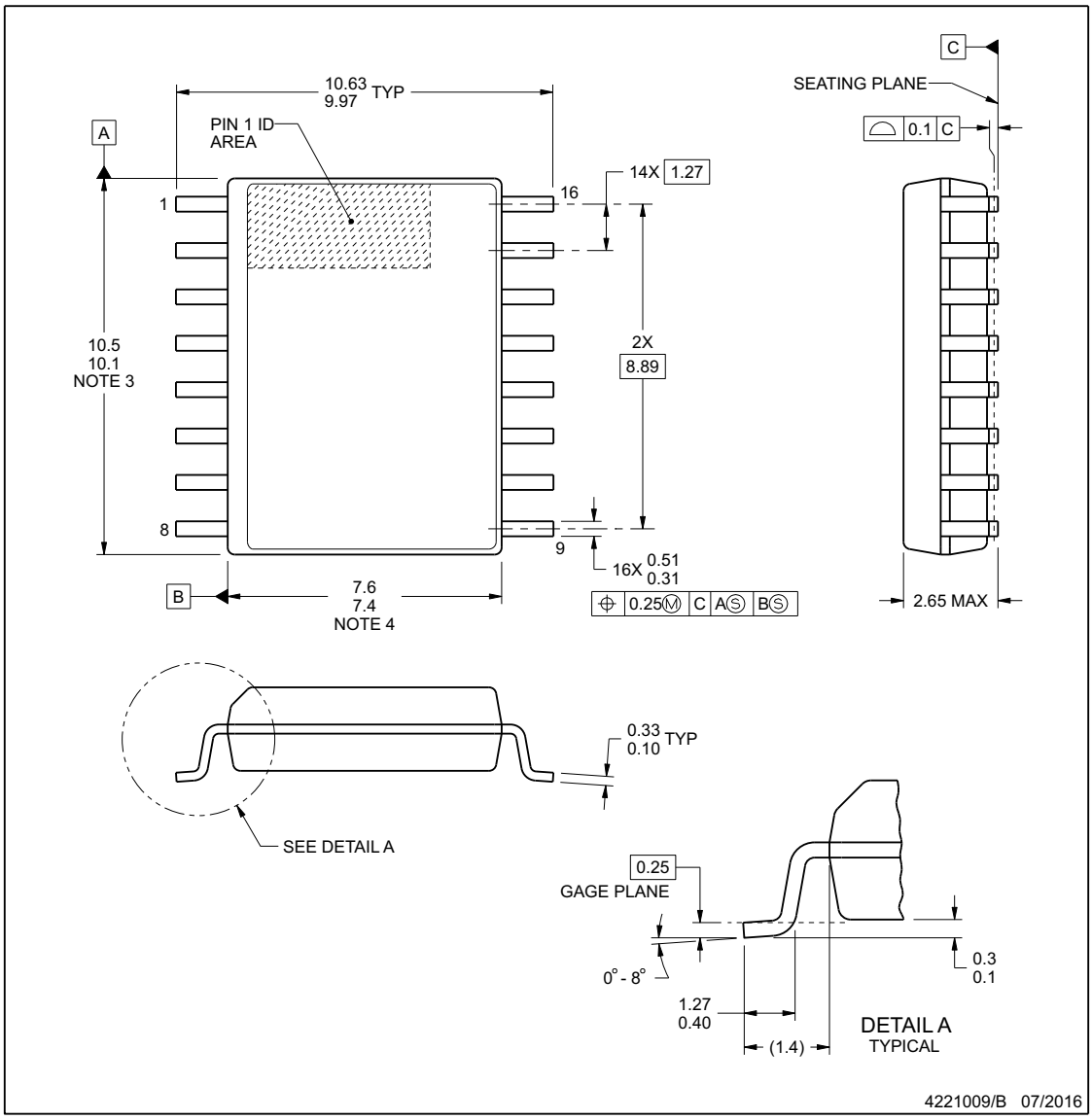
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6441DWR	SOIC	DW	16	2000	367.0	367.0	45.0

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

ADVANCE INFORMATION

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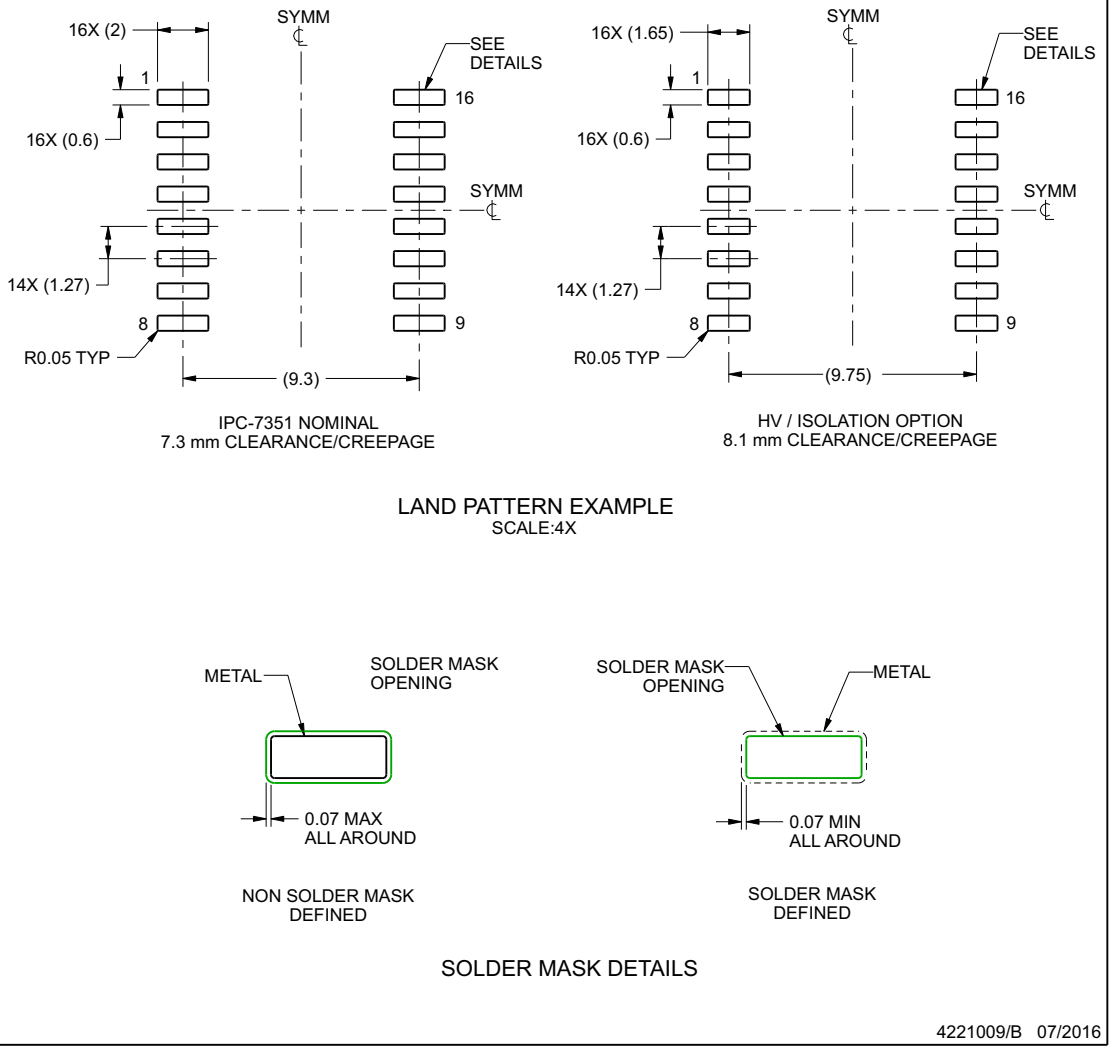
EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

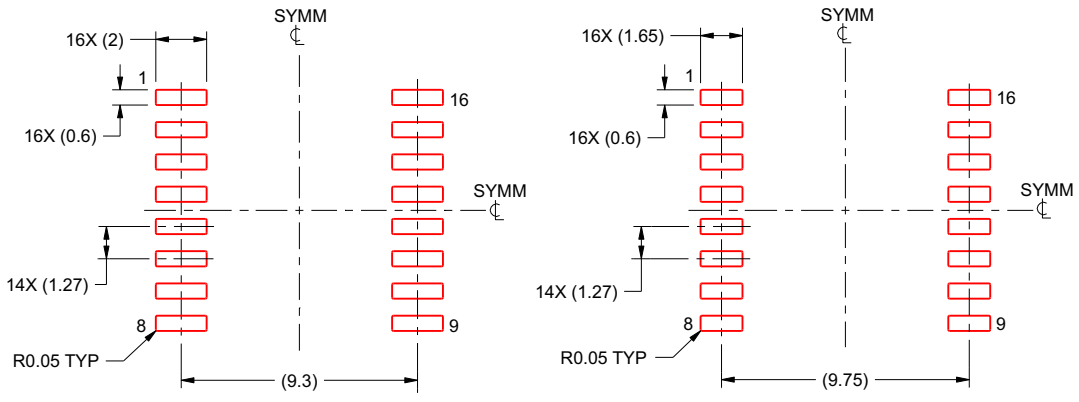
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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