LF356-MIL JFET Input Operational Amplifier

1 Features

- Advantages
  - Replace Expensive Hybrid and Module FET Op Amps
  - Rugged JFETs Allow Blow-Out Free Handling Compared With MOSFET Input Devices
  - Excellent for Low Noise Applications Using Either High or Low Source Impedance—Very Low 1/f Corner
  - Offset Adjust Does Not Degrade Drift or Common-Mode Rejection as in Most Monolithic Amplifiers
  - New Output Stage Allows Use of Large Capacitive Loads (5,000 pF) Without Stability Problems
  - Internal Compensation and Large Differential Input Voltage Capability
- Common Features
  - Low Input Bias Current: 30 pA
  - Low Input Offset Current: 3 pA
  - High Input Impedance: 10^{12} Ω
  - Low Input Noise Current: 0.01 pA/√Hz
  - High Common-Mode Rejection Ratio: 100 dB
  - Large DC Voltage Gain: 106 dB
- Uncommon Features
  - Extremely Fast Settling Time to 0.01%: 1.5 μs
  - Fast Slew Rate: 12 V/μs
  - Wide Gain Bandwidth: 5 MHz
  - Low Input Noise Voltage: 12 nV/√Hz

2 Applications

- Precision High-Speed Integrators
- Fast D/A and A/D Converters
- High Impedance Buffers
- Wideband, Low Noise, Low Drift Amplifiers
- Logarithmic Amplifiers
- Photocell Amplifiers
- Sample and Hold Circuits

3 Description

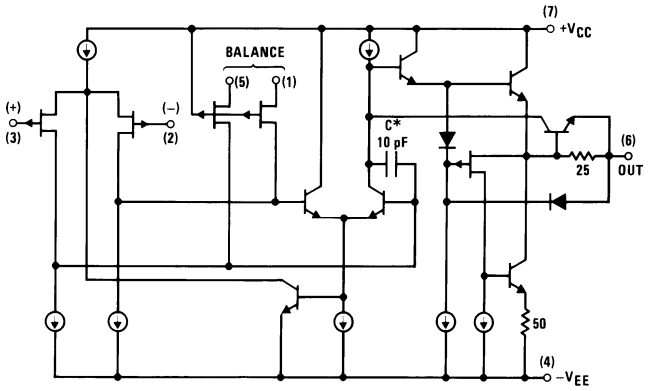
The LF356-MIL device are the first monolithic JFET input operational amplifiers to incorporate well-matched, high-voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust, which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF356-MIL	SOIC (8)	4.90 mm × 3.91 mm
	TO-CAN (8)	9.08 mm × 9.08 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



3 pF in LF357 series

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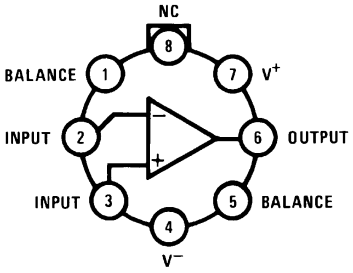
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2017	*	Initial release.

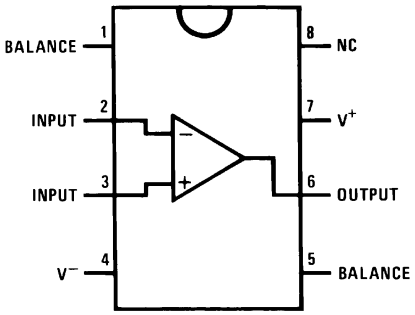
5 Pin Configuration and Functions

LMC Package
8-Pin TO-99
Top View



Available per JM38510/11401 or JM38510/11402

D or P Package
8-Pin SOIC or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BALANCE	1, 5	I	Balance for input offset voltage
+INPUT	3	I	Noninverting input
–INPUT	2	I	Inverting input
NC	8	—	No connection
OUTPUT	6	O	Output
V+	7	—	Positive power supply
V–	4	—	Negative power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

			MIN	MAX	UNIT
Supply voltage				±18	V
Differential input voltage				±30	V
Input voltage (4)				±16	V
Output short circuit duration			Continuous		—
T_{JMAX}		LMC package		115	°C
		P package		100	
		D package		100	
Soldering information (lead temp.)	TO-99 package	Soldering (10 sec.)		300	°C
	PDIP package	Soldering (10 sec.)		260	
	SOIC package	Vapor phase (60 sec.)		215	
		Infrared (15 sec.)		220	
Storage temperature, T_{stg}			−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.
(3) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(4) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) 100 pF discharged through 1.5-kΩ resistor

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S			±15	V
T_A	0	T_A	70	°C

6.4 Thermal Information

THERMAL METRIC (1)		LF356-MIL		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.5	55.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	44.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.8	32.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	21.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.3	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 AC Electrical Characteristics, $T_A = T_J = 25°C$, $V_S = ±15$ V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew Rate	$A_V = 1$			12		V/μs
GBW	Gain Bandwidth Product				5		MHz
t_s	Settling Time to 0.01% (1)				1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\ \Omega$	f = 100 Hz		15		nV/√Hz
			f = 1000 Hz		12		nV/√Hz
i_n	Equivalent Input Current Noise	f = 100 Hz			0.01		pA/√Hz
		f = 1000 Hz			0.01		pA/√Hz
C_{IN}	Input Capacitance				3		pF

(1) Settling time is defined here, for a unity gain inverter connection using 2-kΩ resistors for the LF15x. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10-V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10 V (See *Settling Time Test Circuit*).

6.6 DC Electrical Characteristics, $T_A = T_J = 25°C$, $V_S = ±15$ V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current			5	10	mA

6.7 DC Electrical Characteristics

See (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	R_S = 50 Ω	T_A = 25°C		3	10	mV
			Over temperature			13	
$\Delta V_{OS}/\Delta T$	Average TC of input offset voltage	R_S = 50 Ω			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in average TC with V_{OS} adjust	R_S = 50 Ω(2)			0.5		µV/°C per mV
I_{OS}	Input offset current	T_J = 25°C(1) (3)			3	50	pA
		$T_J \le T_{HIGH}$				2	nA
I_B	Input bias current	T_J = 25°C(1) (3)			30	200	pA
		$T_J \le T_{HIGH}$				8	nA
R_{IN}	Input resistance	T_J = 25°C			10^{12}		Ω
A_{VOL}	Large signal voltage gain	V_S = ±15 V, V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Over temperature	15			
V_O	Output voltage swing	V_S = ±15 V, R_L = 10 kΩ		±12	±13		V
		V_S = ±15 V, R_L= 2 kΩ		±10	±12		
V_{CM}	Input common-mode voltage range	V_S = ±15 V	$V_{CM, High}$	10	15.1		V
			$V_{CM, Low}$		−12	–10	
CMRR	Common-mode rejection ratio			80	100		dB
PSRR	Supply voltage rejection ratio(1)			80	100		dB

(1) Unless otherwise stated, these test conditions apply:

Supply Voltage, V_S	V_S = ±15 V
T_A	0°C ≤ T_A ≤ +70°C
T_{HIGH}	+70°C

and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

(2) The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open-loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(1) Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

6.8 Power Dissipation Ratings

		MIN	MAX	UNIT
Power Dissipation at T_A = 25°C (1) (2)	LMC Package (Still Air)		400	mW
	LMC Package (400 LF/Min Air Flow)		1000	
	P Package		670	
	D Package		380	

(1) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.

(2) Maximum power dissipation is defined by the package characteristics. Operating the part near the maximum power dissipation may cause the part to operate outside specified limits.

6.9 Typical Characteristics

6.9.1 Typical AC Performance Characteristics

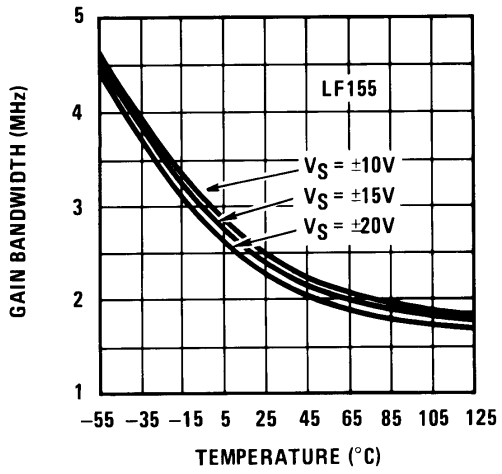


Figure 1. Gain Bandwidth

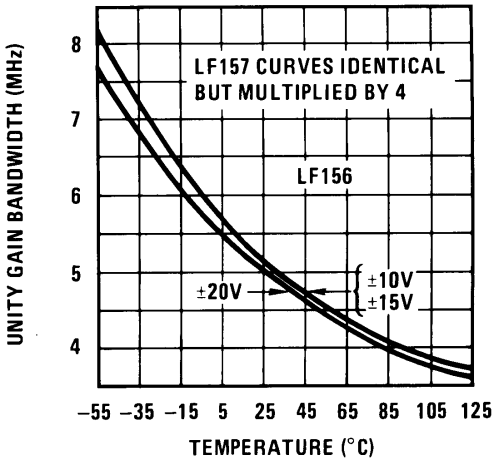


Figure 2. Gain Bandwidth

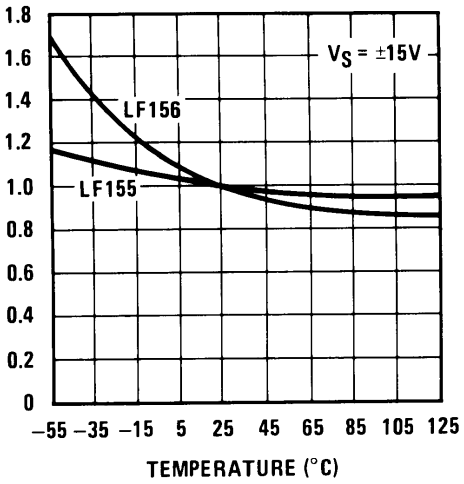


Figure 3. Normalized Slew Rate

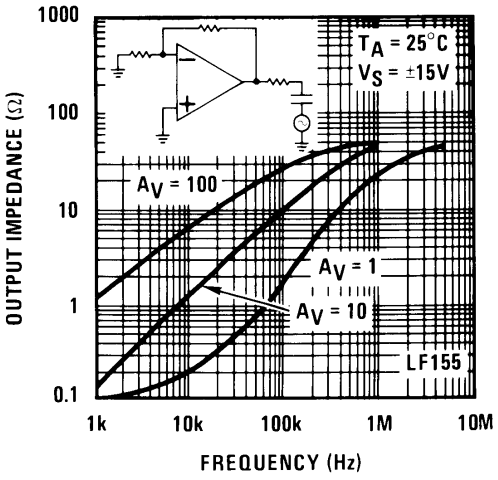


Figure 4. Output Impedance

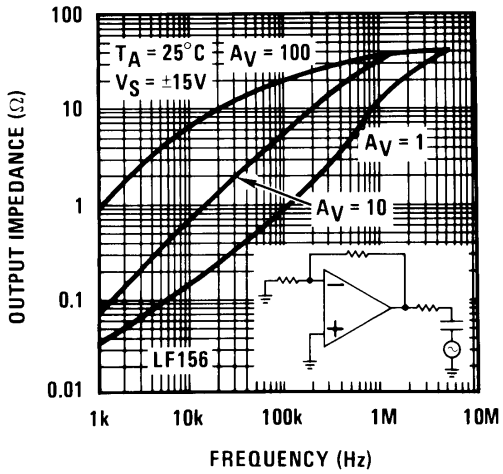


Figure 5. Output Impedance

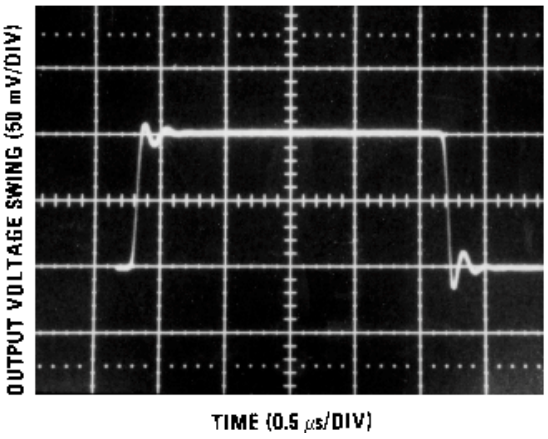


Figure 6. LF155 Small Signal Pulse Response, A_V = +1

Typical AC Performance Characteristics (continued)

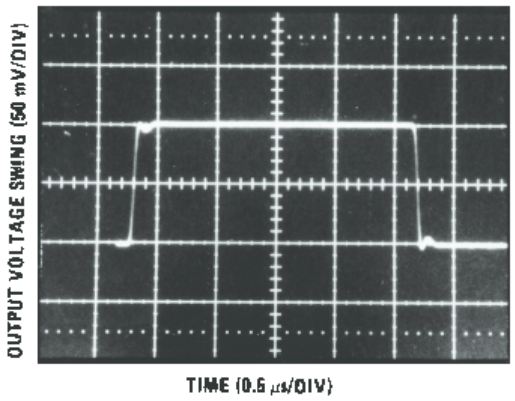


Figure 7. LF156 Small Signal Pulse Response, A_V = +1

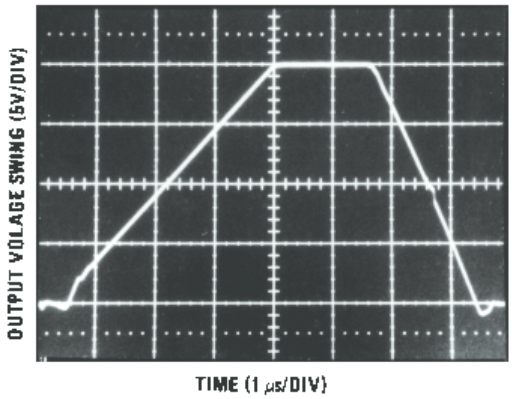


Figure 8. LF155 Large Signal Pulse Response, A_V = +1

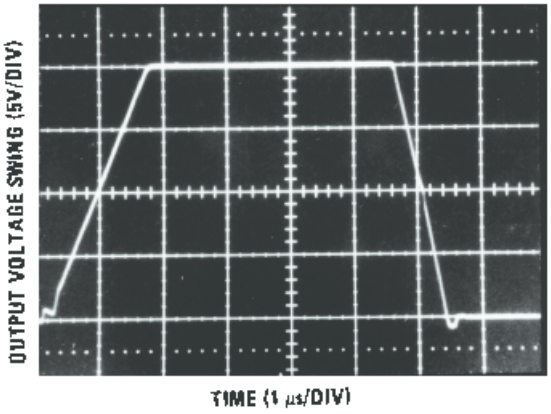


Figure 9. LF156 Large Signal Puls Response, A_V = +1

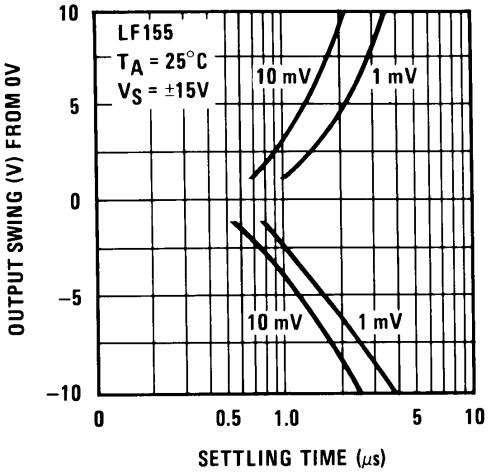


Figure 10. Inverter Settling Time

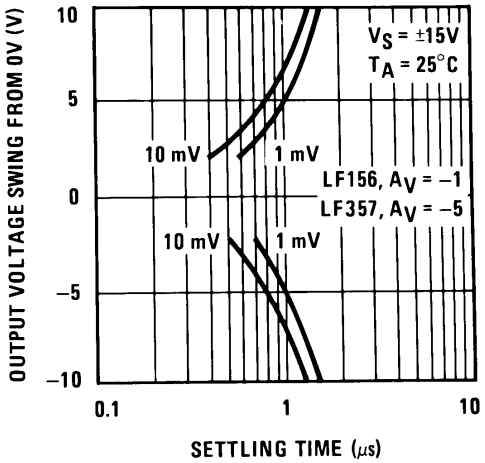


Figure 11. Inverter Settling Time

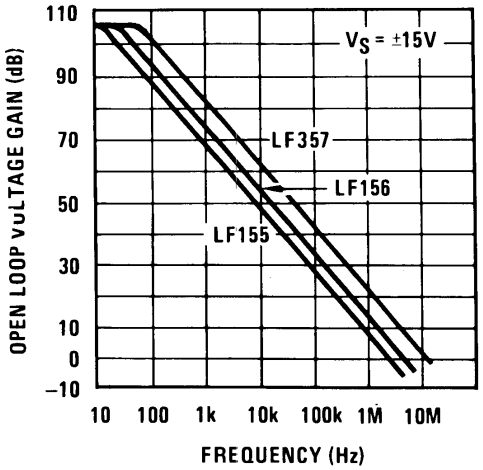


Figure 12. Open-Loop Frequency Response

Typical AC Performance Characteristics (continued)

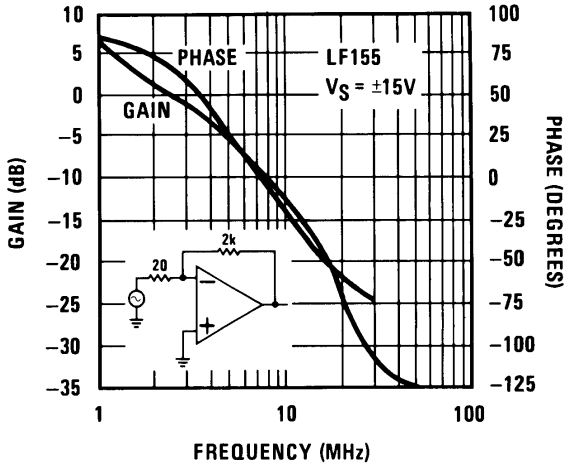


Figure 13. Bode Plot

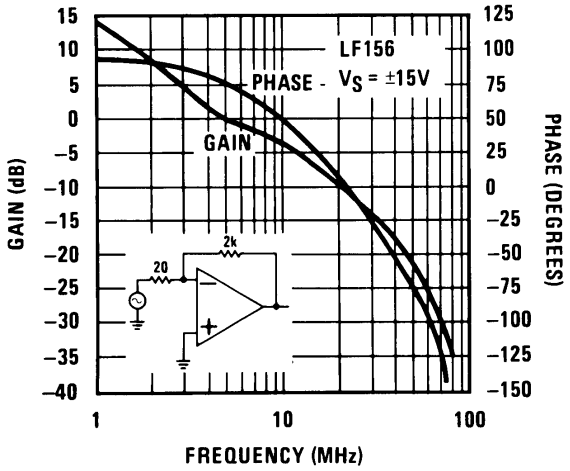


Figure 14. Bode Plot

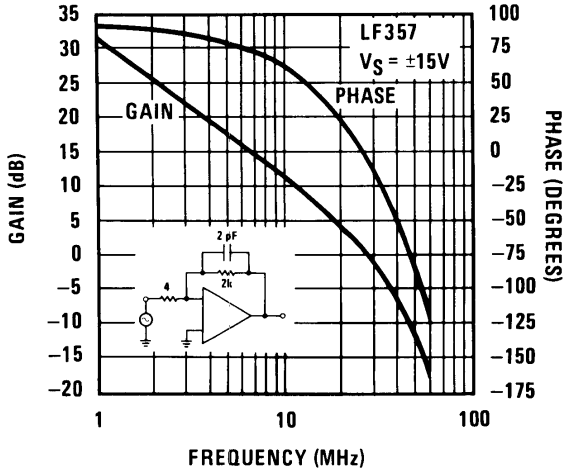


Figure 15. Bode Plot

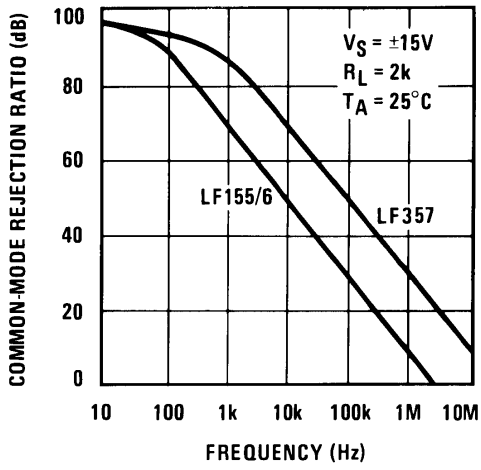


Figure 16. Common-Mode Rejection Ratio

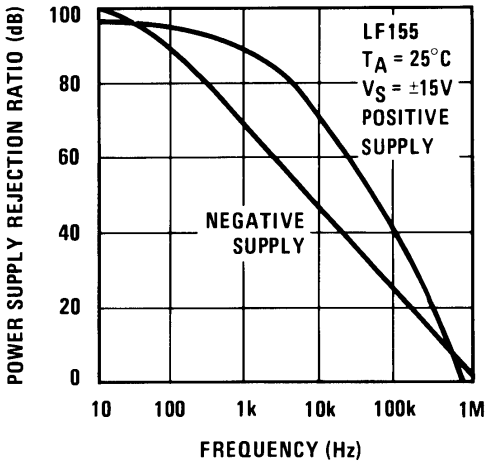


Figure 17. Power Supply Rejection Ratio

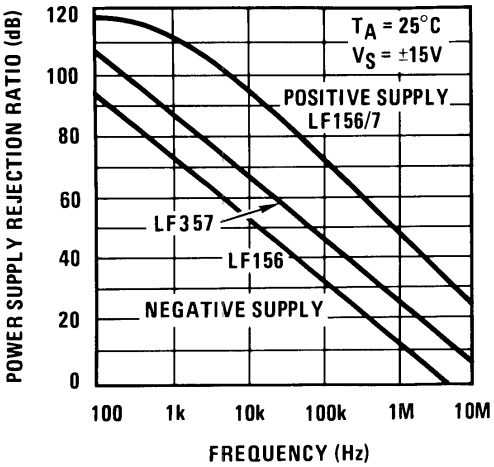


Figure 18. Power Supply Rejection Ratio

Typical AC Performance Characteristics (continued)

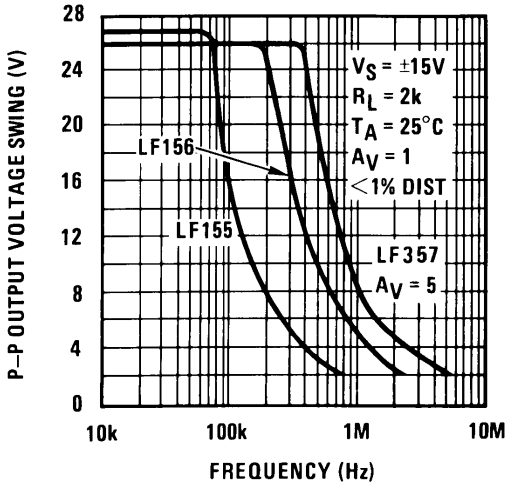


Figure 19. Undistorted Output Voltage Swing

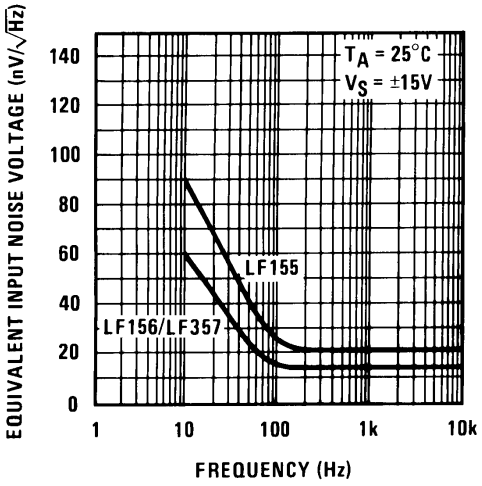


Figure 20. Equivalent Input Noise Voltage

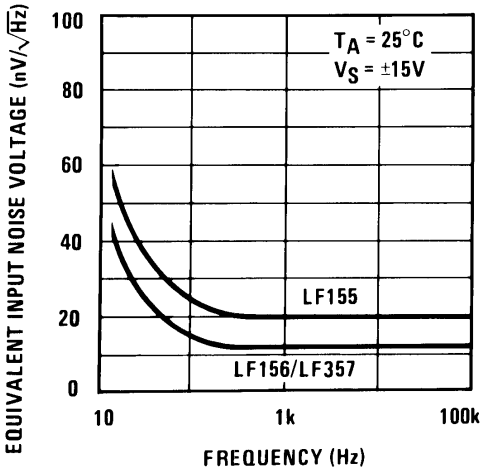


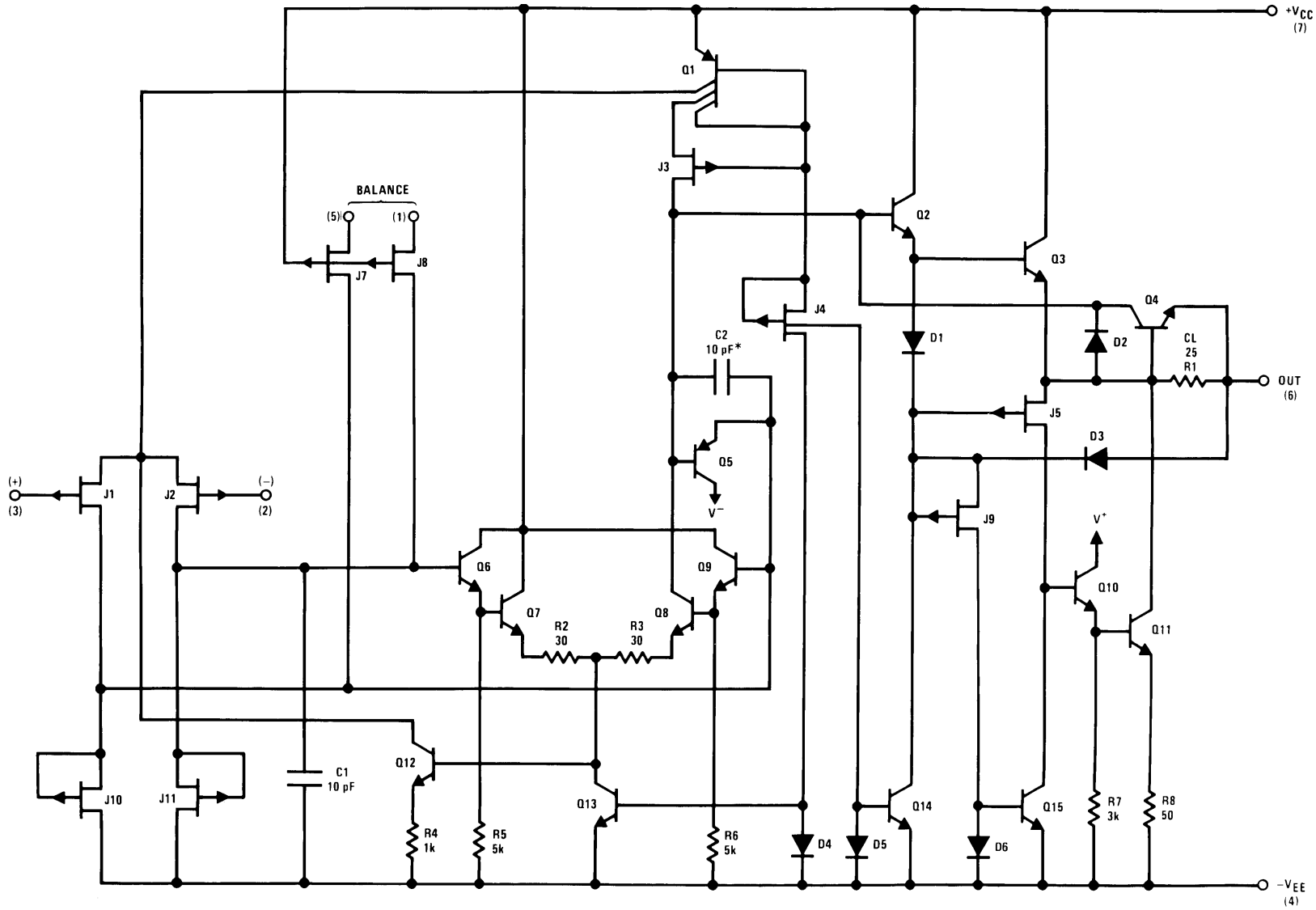
Figure 21. Equivalent Input Noise Voltage (Expanded Scale)

7 Detailed Description

7.1 Overview

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, as well as low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. These devices can replace expensive hybrid and module FET operational amplifiers. Designed for low voltage and current noise and a low 1/f noise corner, these devices are excellent for low noise applications using either high or low source impedance.

7.2 Functional Block Diagram



*C = 3 pF in LF357 series.

Figure 22. Detailed Schematic

7.3 Feature Description

7.3.1 Large Differential Input Voltage

These are operational amplifiers with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

7.3.2 Large Common-Mode Input Voltage

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

7.4 Device Functional Modes

The LF356-MIL has a single functional mode and operates according to the conditions listed in the *Recommended Operating Conditions*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize pick-up and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3-dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3-dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

8.2 Typical Application

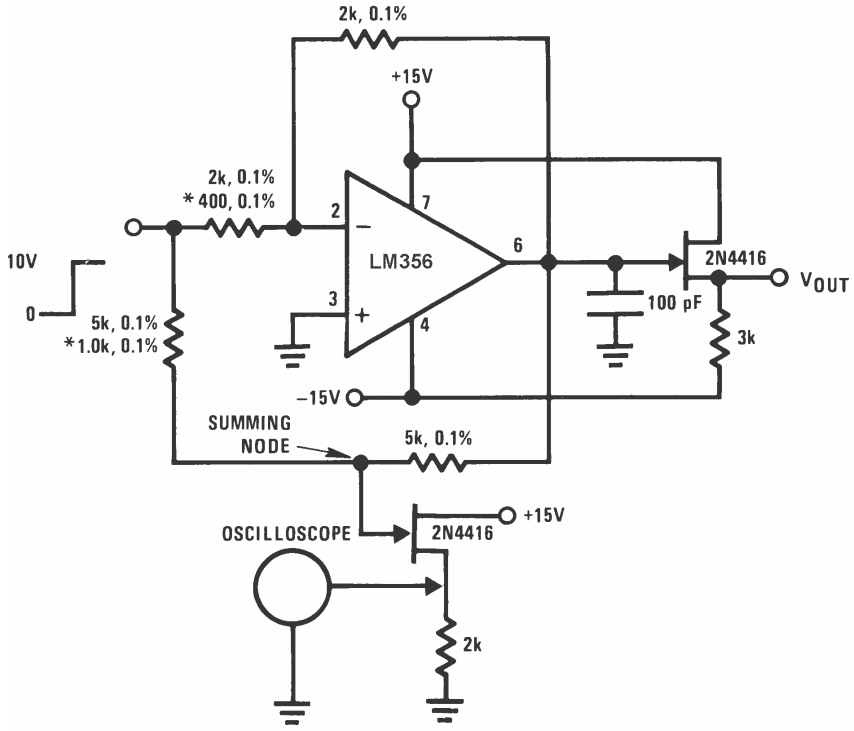


Figure 23. Settling Time Test Circuit

8.2.1 Design Requirements

Settling time is tested with the LF35x connected as unity gain inverter and LF357 connected for $A_V = -5$

8.2.2 Detailed Design Procedure

Connect the circuit components as shown in Figure 23. In particular, use FET to isolate the probe capacitance.

Apply a 10-V step function to the input.

Use an oscilloscope to probe the circuit as shown in Figure 23.

8.2.3 Application Curve

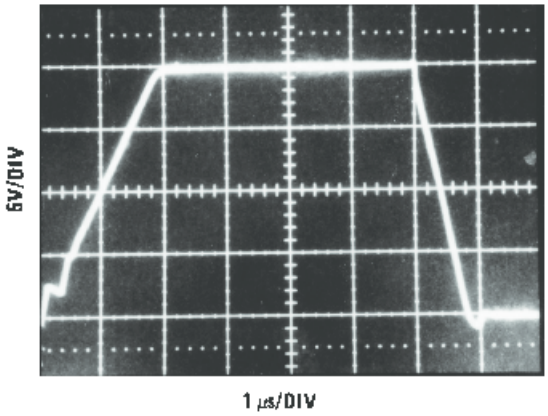


Figure 24. Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

8.3 System Examples

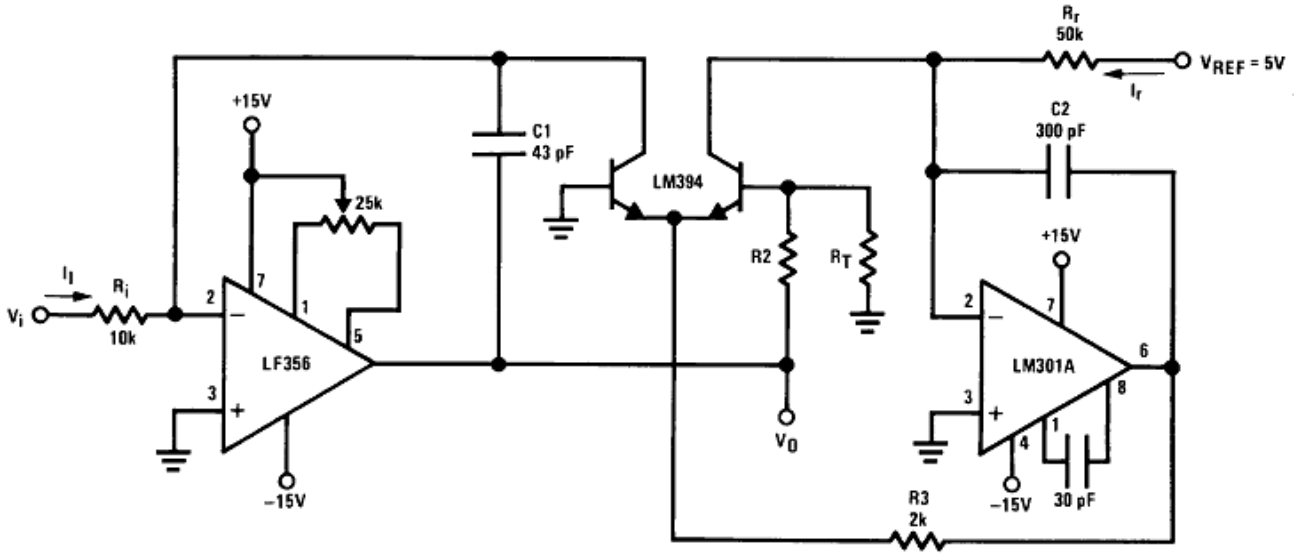


Figure 25. Fast Logarithmic Converter

- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1 V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)} \tag{1}$$

System Examples (continued)

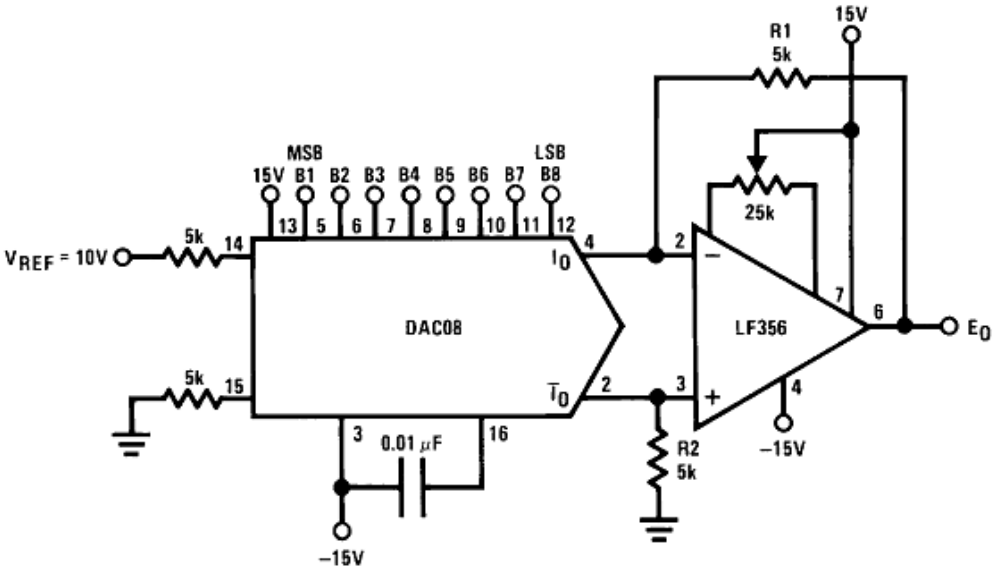


Figure 26. 8-Bit D/A Converter With Symmetrical Offset Binary Operation

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

Table 1. Bit Illustration of the 8-Bit D/A Converter

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

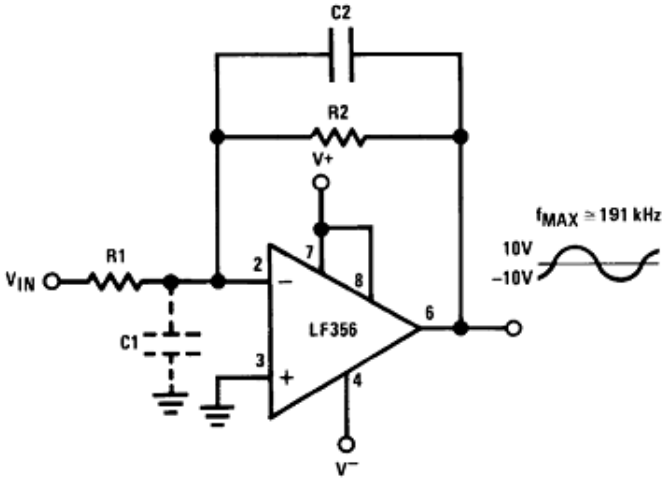


Figure 27. Wide BW Low Noise, Low Drift Amplifier

- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_p} \cong 191\,kHz$ (2)

Parasitic input capacitance C1 ≃ (3 pF for LF155, LF156 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

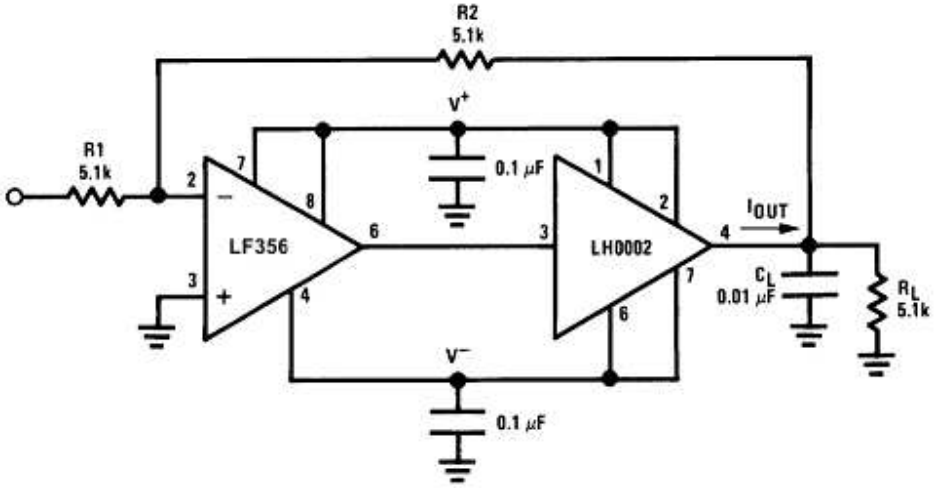


Figure 28. Boosting the LF156 With a Current Amplifier

- $I_{OUT(MAX)}$ ≃ 150 mA (will drive $R_L \geq 100\ \Omega$)
  - $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s$ (with C_L shown) (3)
- No additional phase shift added by the current amplifier

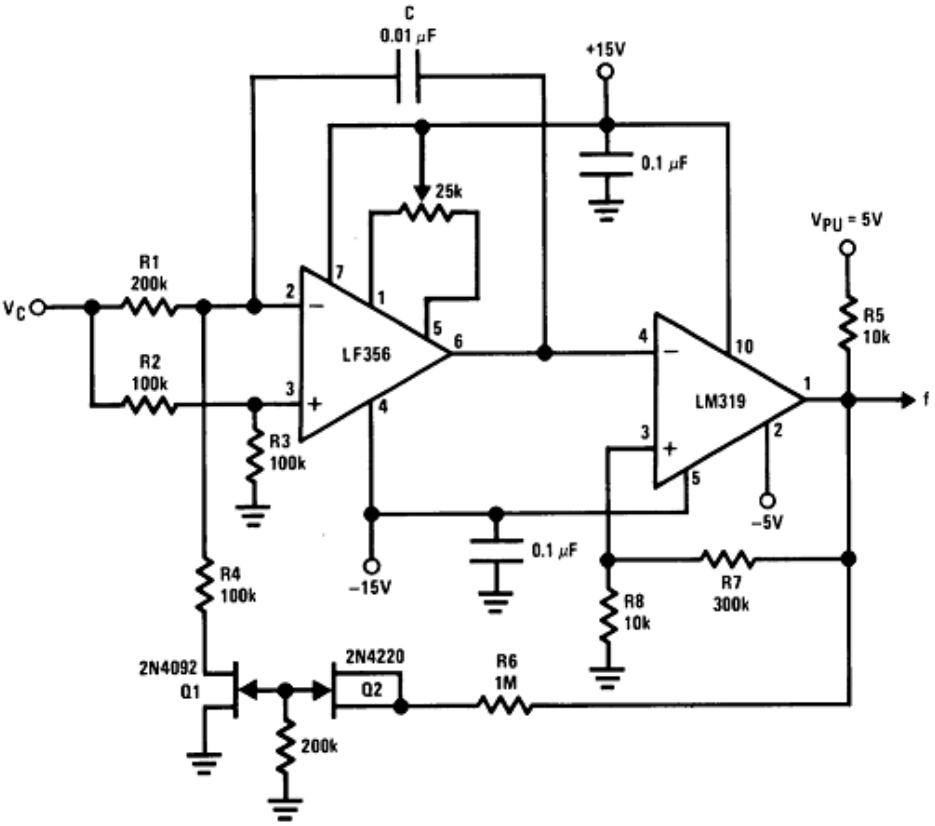


Figure 29. Decades VCO

R1, R4 matched. Linearity 0.1% over 2 decades.

$$f = \frac{V_C\,(R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \le V_C \le 30V,\ 10\,Hz \le f \le 10\,kHz \tag{4}$$

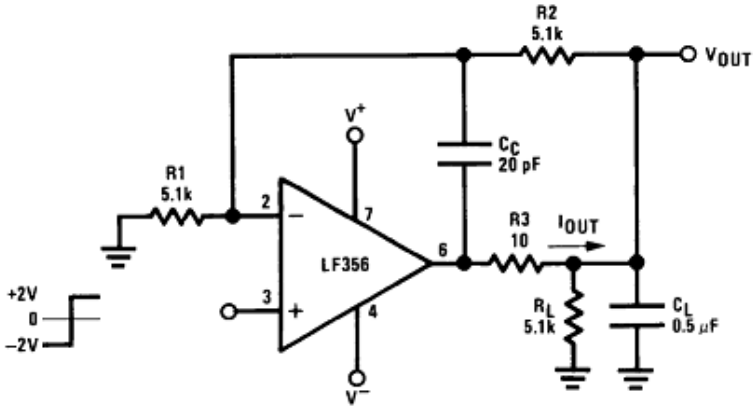


Figure 30. Isolating Large Capacitive Loads

- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\,V/\mu s = 0.04\,V/\mu s \text{ (with } C_L \text{ shown)} \tag{5}$$

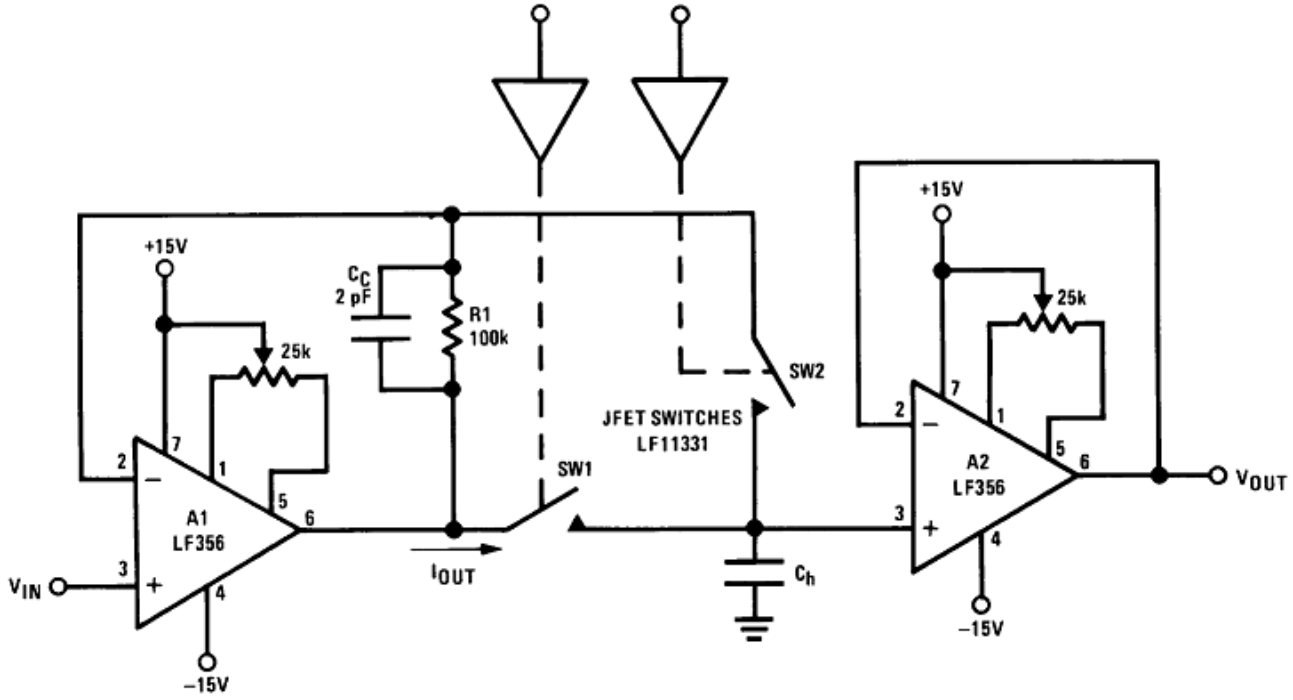


Figure 31. Fast Sample and Hold

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right] 1/2 \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA} \quad (6)$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1$ V
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

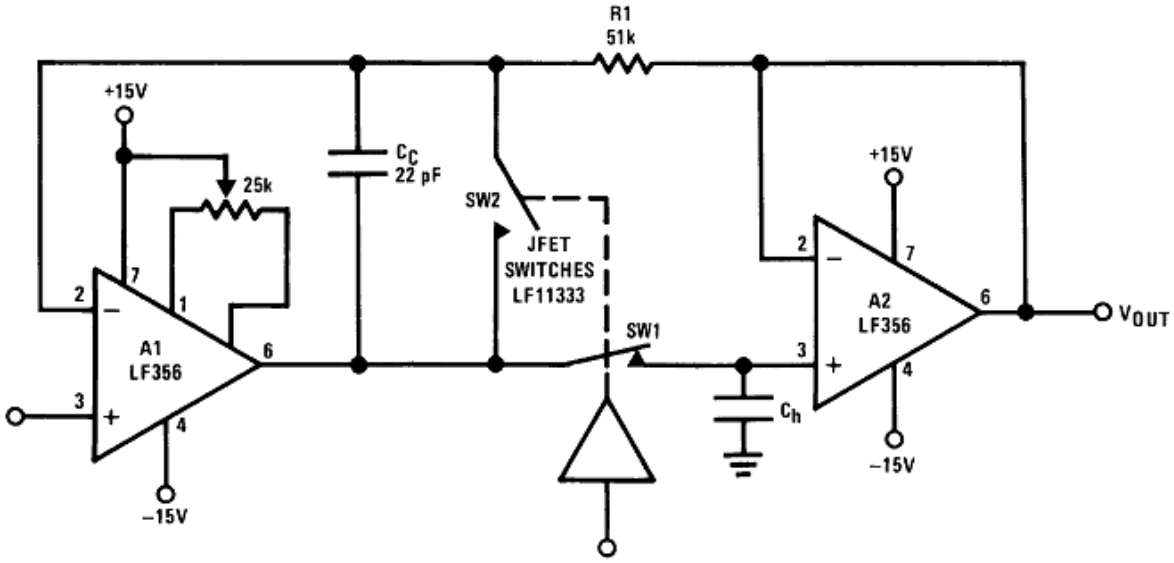


Figure 32. High Accuracy Sample and Hold

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.
  - No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added
  - propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

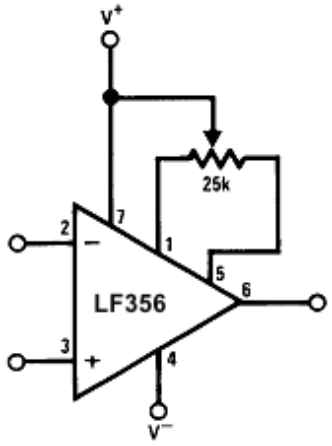


Figure 33. V_{OS} Adjustment

- V_{OS} is adjusted with a 25-k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

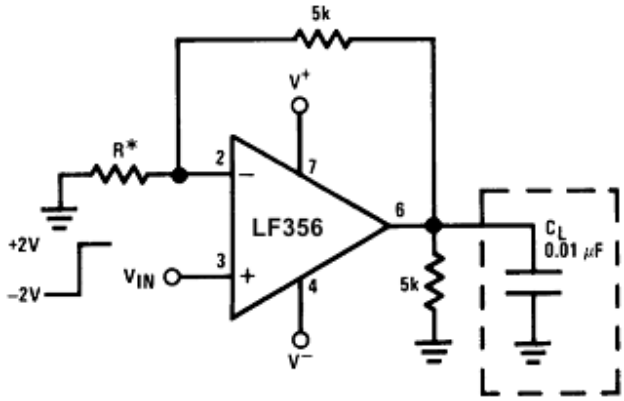


Figure 34. Driving Capacitive Loads

- *LF15x R = 5k, LF357 R = 1.25 k
- Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\ \mu F$.
- Overshoot ≤ 20%, Settling time (t_s) ≈ 5 µs

9 Power Supply Recommendations

See the *Recommended Operating Conditions* for the minimum and maximum values for the supply input voltage and operating junction temperature.

10 Layout

10.1 Layout Guidelines

10.1.1 Printed-Circuit-Board Layout For High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PCB. When one wishes to take advantage of the low input bias current of the LF356-MIL, typically less than 30 pA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PCB, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the inputs of the LF356-MIL and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth, connected to the inputs of the op amp, as in Figure 39. To have a significant effect, guard rings must be placed on both the top and bottom of the PCB. This PC foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10 TΩ, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input. If a guard ring is used and held close to the potential of the amplifier inputs, it will significantly reduce this leakage current.

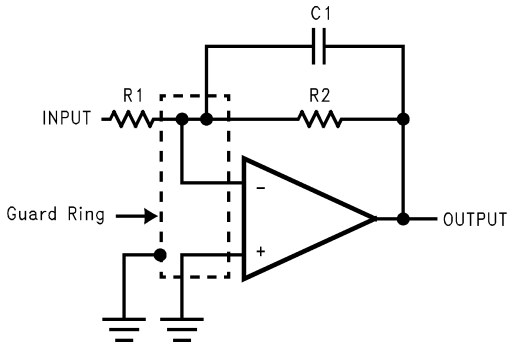


Figure 35. Inverting Amplifier

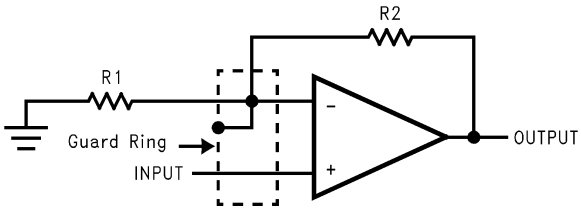


Figure 36. Noninverting Amplifier

Layout Guidelines (continued)

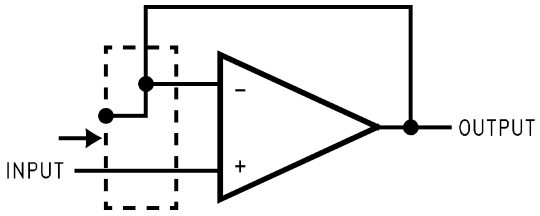
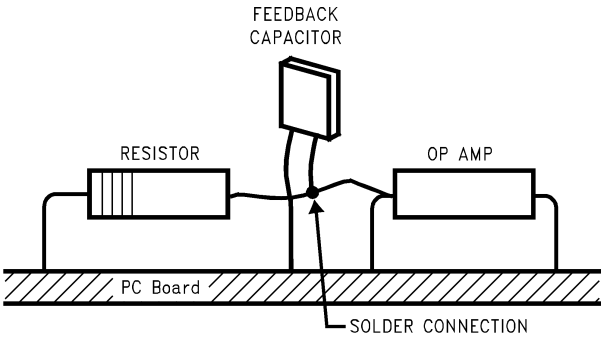


Figure 37. Typical Connections Of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 38.



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB).

Figure 38. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LF356-MIL is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

10.2 Layout Example

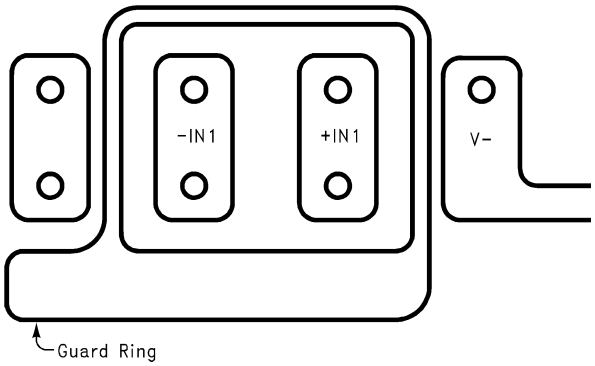


Figure 39. Examples Of Guard Ring In PCB Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF356 MWC	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LF356H	ACTIVE	TO-99	LMC	8	500	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	(LF356H, LF356H)	Samples
LF356H/NOPB	ACTIVE	TO-99	LMC	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	(LF356H, LF356H)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

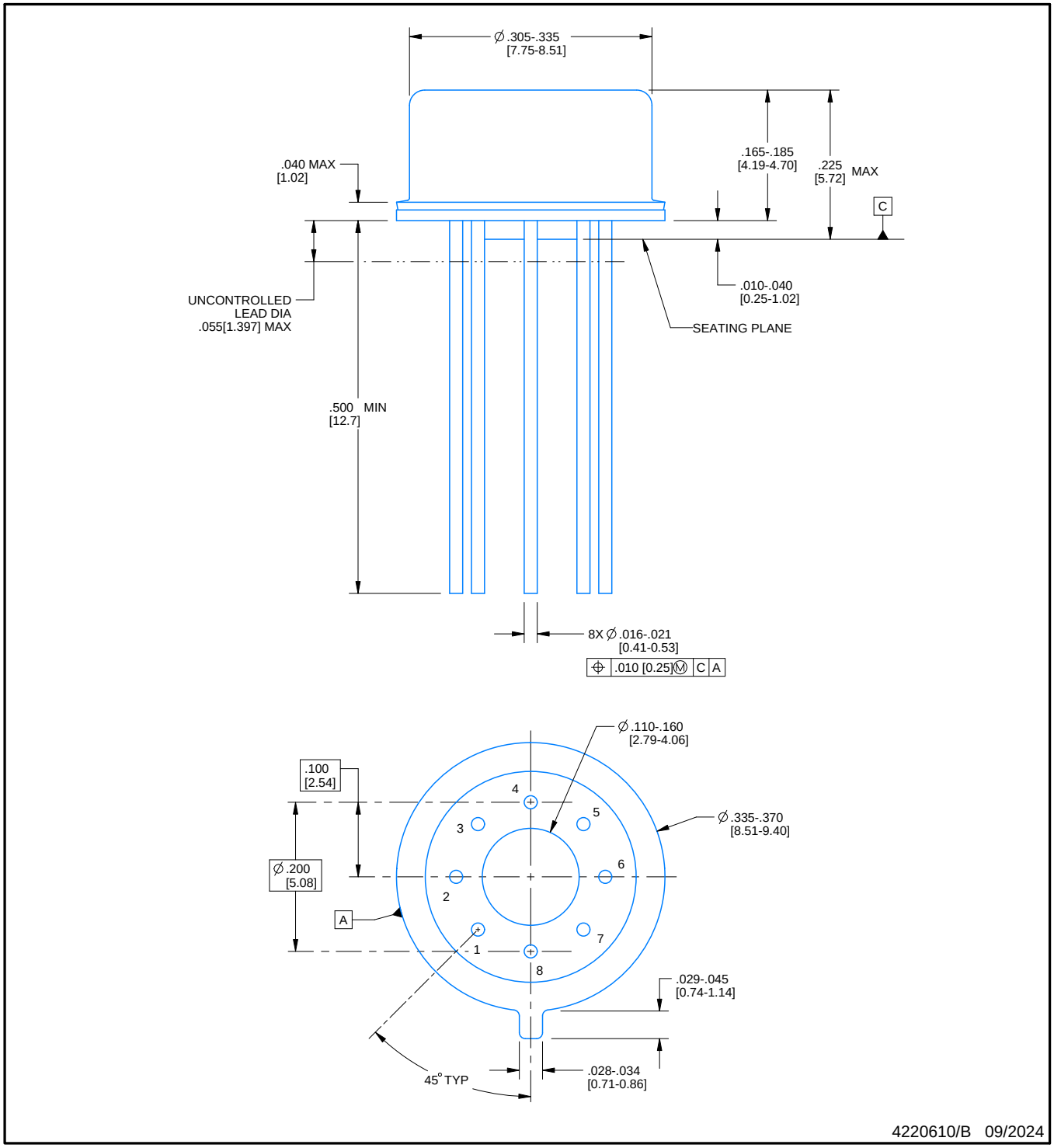
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

LMC0008A

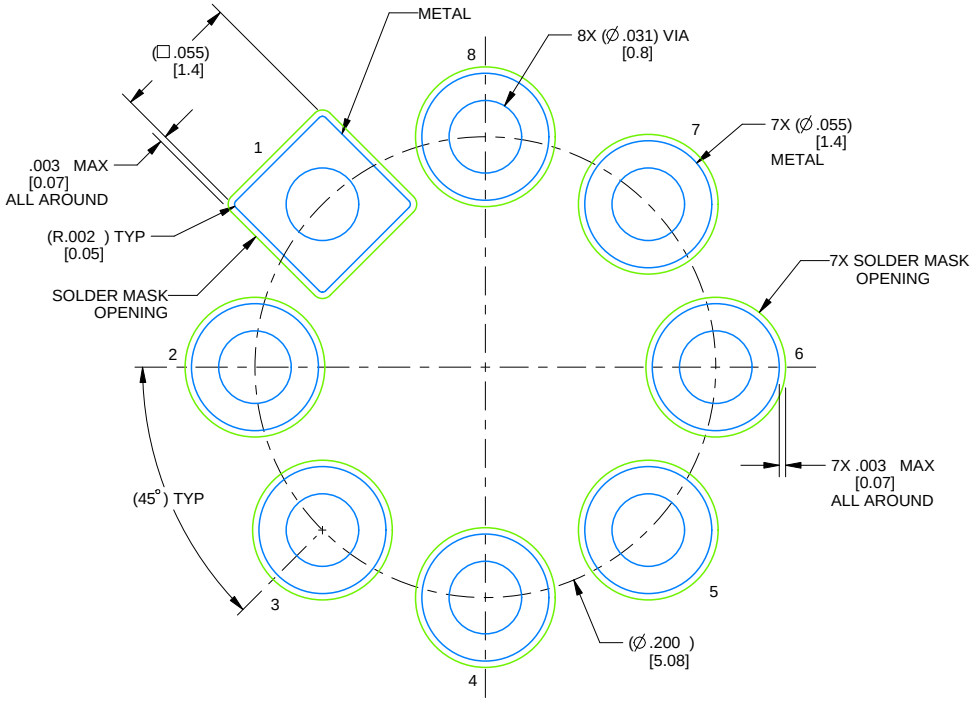
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

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