OPAx241, OPAx251 Single-Supply, MicroPower Operational Amplifiers

1 Features

- OPAx241 family optimized for 5V supply
- OPAx251 family optimized for ±15V supply
- Micro power: I_Q = 25μA
- Single-supply operation
- Rail-to-rail output (within 50mV)
- Wide supply range
  - Single supply: 2.7V to 36V
  - Dual supply: ±1.35V to ±18V
- Low offset voltage: ±250μV max
- High common-mode rejection: 124dB
- High open-loop gain: 128dB
- Single, dual, and quad

2 Applications

- Battery operated instruments
- Portable devices
- Medical instruments
- Test equipment

3 Description

The OPA241, OPA2241, OPA4241 (OPAx241), and OPA251, OPA2251, OPA4251 (OPAx251) devices are specifically designed for battery-powered, portable applications. In addition to very low power consumption (25μA), these amplifiers feature low offset voltage, rail-to-rail output swing, high common-mode rejection, and high open-loop gain.

The OPAx241 series is optimized for operation at low power supply voltage while the OPAx251 series is optimized for high-power supplies. Both series can operate from either single (2.7V to 36V) or dual supplies (±1.35V to ±18V). The input common-mode voltage range extends 200mV less than the negative supply—an excellent choice for single-supply applications.

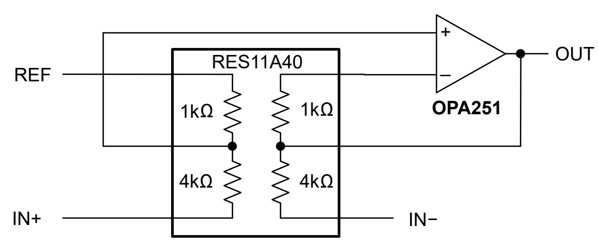
The OPAx241 and OPAx251 are unity-gain stable and can drive large capacitive loads. Special design considerations makes sure that these products are easy to use. High performance is maintained as the amplifiers swing to the specified limits. Because the initial offset voltage (±250μV max) is so low, user adjustment is usually not required. However, external trim pins are provided for special applications (single versions only).

The OPAx241 and OPAx251 are fully specified from −40°C to +85°C and operate from −55°C to +125°C.

Device Information

PART NUMBER	CHANNELS	PACKAGE[1]
OPA241	Single	D (SOIC, 8)
		P (PDIP, 8)
OPA2241	Dual	D (SOIC, 8)
		P (PDIP, 8)
OPA4241	Quad	N (PDIP, 14)
		D (SOIC, 14)
OPA251	Single	D (SOIC, 8)
OPA2251	Dual	P (PDIP, 8)
		D (SOIC, 8)
OPA4251	Quad	D (SOIC, 14)

(1) For more information, see Section 9.



High-Common-Mode, Low-Power Difference Amplifier

Table of Contents

4 Pin Configuration and Functions

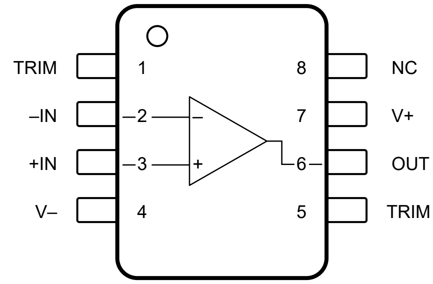


Figure 4-1. OPA241 and OPA251: D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

Table 4-1. Pin Functions: OPA241 and OPA251

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	2	Input	Inverting input
NC	8	—	No internal connection (can be left floating)
OUT	6	Output	Output
TRIM	1, 5	—	External offset voltage adjustment. See Section 6.1.2.
V+	7	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

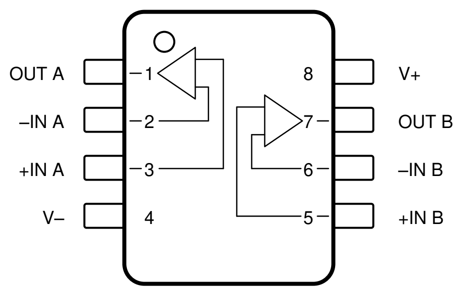


Figure 4-2. OPA2241 and OPA2251: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

Table 4-2. Pin Functions: OPA2241 and OPA2251

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

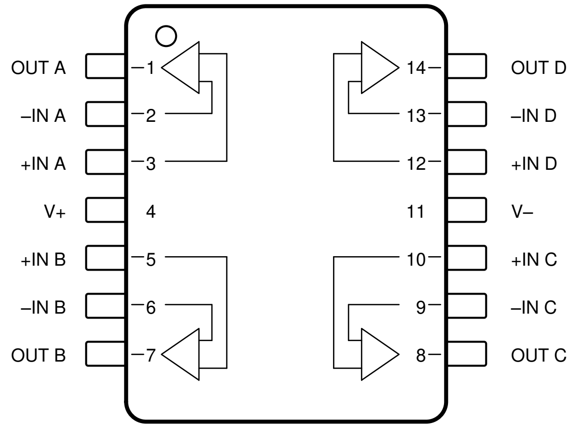


Figure 4-3. OPA4241 and OPA4251: D Package, 14-Pin SOIC (Top View)

Pin Functions: OPA4241 and OPA4251

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply		36	V
		Dual supply		±18	
	Signal input pin voltage	Common-mode[2]	(V–) – 0.5	(V+) + 0.5	V
		Differential[3]		±0.5	
	Output short-circuit[4]		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C
	Lead temperature (soldering, 10s)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power supply rails. Current-limit input signals that can swing more that 0.5V beyond the supply rails to 5mA or less.
(3) Input terminals are anti-parallel diode-clamped to each other. Current-limit input signals that cause differential voltage swings of more than ±0.5V to 5mA or less.
(4) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	2.7	30	36	V
		Dual supply	±1.35	±15	±18	
T_A	Operating temperature		–40		+85	°C

5.3 Thermal Information for OPA241 and OPA251

THERMAL METRIC[(1)]		OPA241 AND OPA251		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	100	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.4	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.1	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	74.2	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information for OPA2241 and OPA2251

THERMAL METRIC[(1)]		OPA2241 AND OPA2251		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	100	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.0	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.3	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.8	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.4	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information for OPA4241 and OPA4251

THERMAL METRIC[(1)]		OPA4241 AND OPA4251		UNIT
		D (SOIC)	P (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100	80	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics for V_S = 2.7V to 5V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx241			±50	±250	μV
			T_A = –40°C to +85°C		±100	±400	
		OPAx251			±100		
			T_A = –40°C to +85°C		±130		
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	OPAx241		±0.4		μV/°C
			OPAx251		±0.6		
PSRR	Power supply rejection ratio	V_S = 2.7V to 36V			±3	±30	μV/V
			T_A = –40°C to +85°C			±30	
	Channel separation, (dual, quad)				0.3		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				–4	–20	nA
		T_A = –40°C to +85°C				–25	
I_{OS}	Input offset current				±0.1	±2	nA
		T_A = –40°C to +85°C				±2	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.7		$μV_{PP}$
e_n	Input voltage noise density	f = 1kHz			65		nV/√Hz
i_n	Input current noise density	f = 1kHz			40		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			–0.2		(V+) – 0.8	V
CMRR	Common-mode rejection ratio	–0.2V < V_{CM} < (V+) – 0.8V		80	106		dB
		0V < V_{CM} < (V+) – 0.8V, T_A = –40°C to +85°C		80			
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			10 || 3.75		MΩ || pF
		Common-mode			1 || 4		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 100mV < V_O < (V+) – 100mV		100	120		dB
			T_A = –40°C to +125°C	100			
		(V–) + 200mV < V_O < (V+) – 200mV, R_L = 10kΩ		100	120		
			T_A = –40°C to +125°C	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				35		kHz
SR	Slew rate	V_S = 5V, G = 1V/V			0.01		V/μs
	Overload recovery time	V_S = V_{IN} × G			80		μs

5.6 Electrical Characteristics for V_S = 2.7V to 5V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail[2]	A_{OL} > 70dB			50		mV
		A_{OL} > 100dB			75	100	
			T_A = –40°C to +85°C			100	
		A_{OL} > 100dB, R_L = 10kΩ,			100	200	
			T_A = –40°C to +85°C			200	
I_{SC}	Short-circuit current	Source, V_S = 5V	Single		4		mA
			Dual and Quad		4		
		Sink, V_S = 5V	Single		–24		
			Dual and Quad		–24		
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			±25	±30	µA
			T_A = –40°C to +85°C			±36	

(1) The negative sign indicates input bias current flows out of the input terminals.
(2) Output voltage swings are measured between the output and power supply rails.

5.7 Electrical Characteristics for V_S = ±15V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx241			±100		µV
			T_A = –40°C to +85°C		±150		
		OPAx251			±50	±250	
			T_A = –40°C to +85°C		±100	±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	OPAx241		±0.6		µV/°C
			OPAx251		±0.5		
PSRR	Power supply rejection ratio	V_S = 2.7V to 36V			±3	±30	µV/V
			T_A = –40°C to +85°C			±30	
	Channel separation, (dual, quad)				0.3		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				–4	–20	nA
		T_A = –40°C to +85°C				–25	
I_{OS}	Input offset current				±0.1	±2	nA
		T_A = –40°C to +85°C				±2	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.7		μV_{PP}
e_n	Input voltage noise density	f = 1kHz			65		nV/√Hz
i_n	Input current noise density	f = 1kHz			40		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) – 0.8	V
CMRR	Common-mode rejection ratio	–15.2V < V_{CM} < (V+) – 14.2V		100	124		dB
		–15V < V_{CM} < (V+) – 14.2V	T_A = –40°C to +85°C	100			
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			10 || 3.75		MΩ || pF
		Common-mode			1 || 4		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 250mV < V_O < (V+) – 250mV		100	128		dB
			T_A = –40°C to +85°C	100			
		(V–) + 300mV < V_O < (V+) – 300mV, R_L = 20kΩ		100	128		
			T_A = –40°C to +85°C	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				30		kHz
SR	Slew rate	V_S = 5V, G = 1V/V			0.01		V/µs
	Overload recovery time	V_S = V_{IN} × G			75		µs

5.7 Electrical Characteristics for V_S = ±15V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 100kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail[2]	A_{OL} > 100dB			50		mV
		A_{OL} > 100dB			75	250	
			T_A = –40°C to +85°C			250	
		A_{OL} > 100dB, R_L = 20kΩ,			100	300	
			T_A = –40°C to +85°C			300	
I_{SC}	Short-circuit current	Source	Single		4		mA
			Dual		4		
		Sink	Single		–21		
			Dual		–27		
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			±27	±38	μA
			T_A = –40°C to +85°C			±45	

(1) The negative sign indicates input bias current flows out of the input terminals.
(2) Output voltage swings are measured between the output and power supply rails.

5.8 Typical Characteristics

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

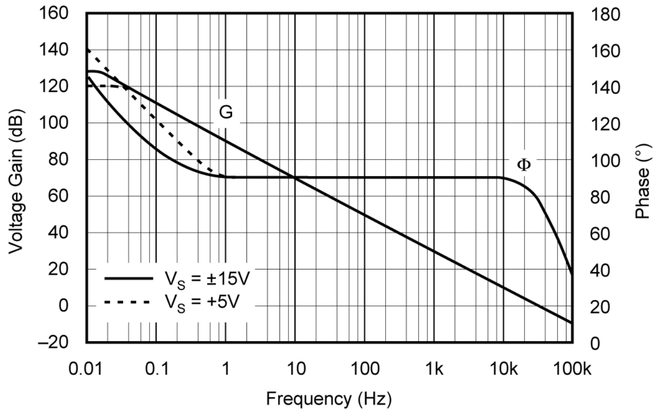


Figure 5-1. Open-Loop Gain and Phase vs Frequency

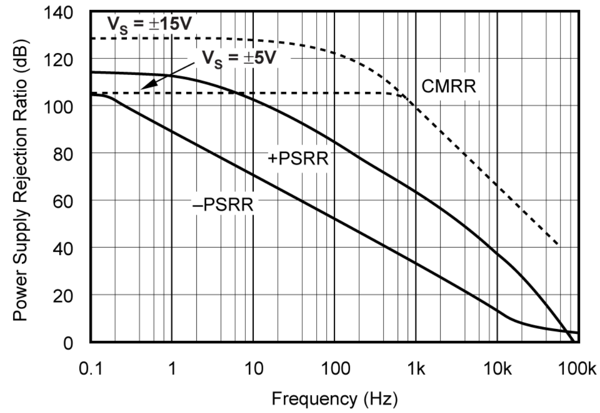


Figure 5-2. Power Supply and Common-mode Rejection Ratio vs Frequency

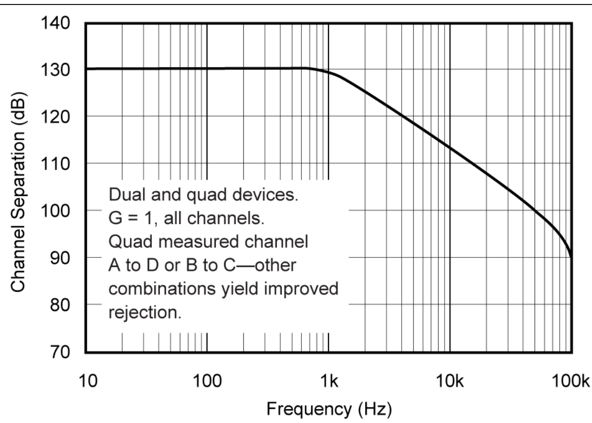


Figure 5-3. Channel Separation vs Frequency

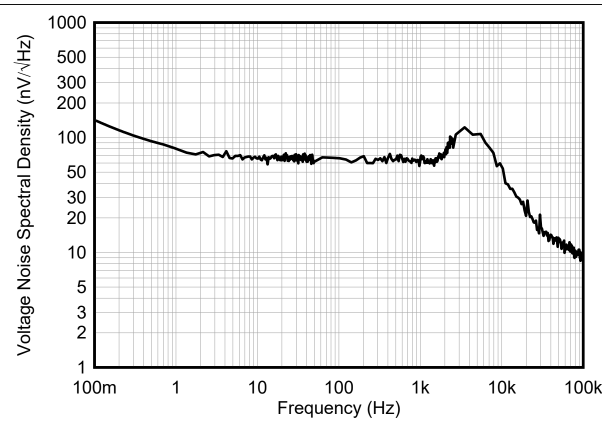


Figure 5-4. Input Voltage Noise Spectral Density vs Frequency

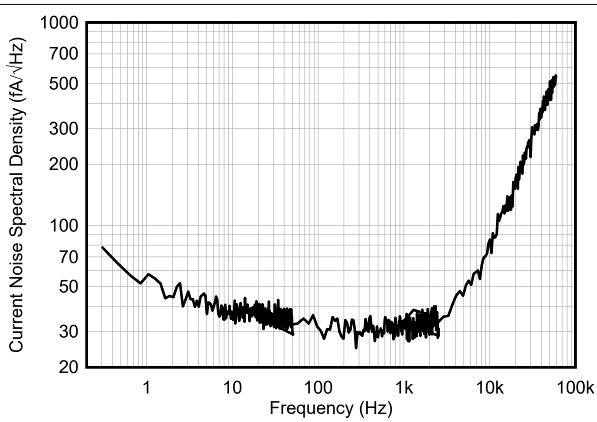


Figure 5-5. Input Current Noise Spectral Density vs Frequency

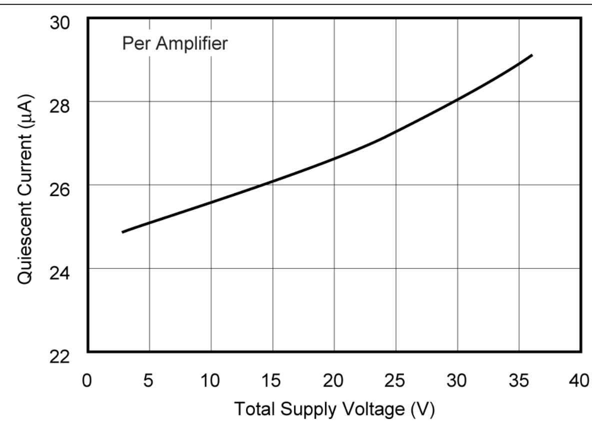


Figure 5-6. Quiescent Current vs Supply Voltage

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

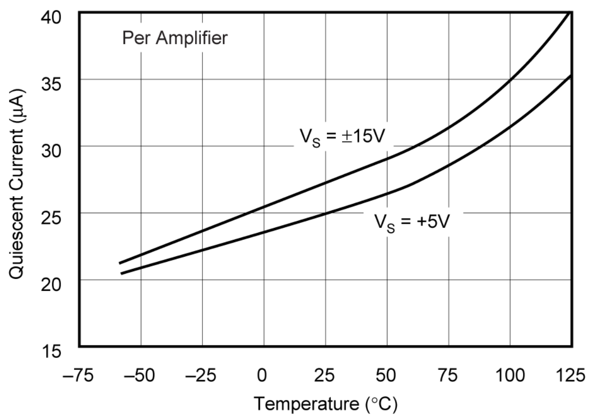


Figure 5-7. Quiescent Current vs Temperature

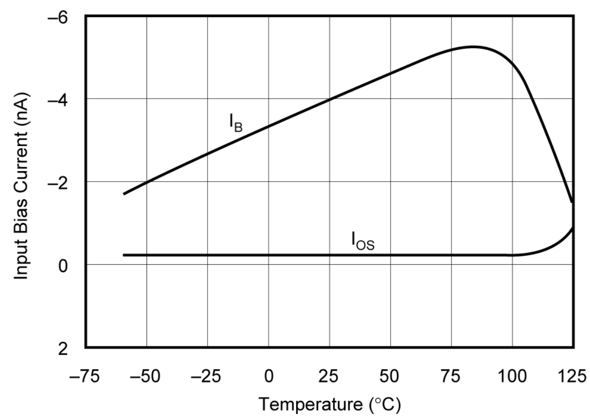


Figure 5-8. Input Bias Current vs Temperature

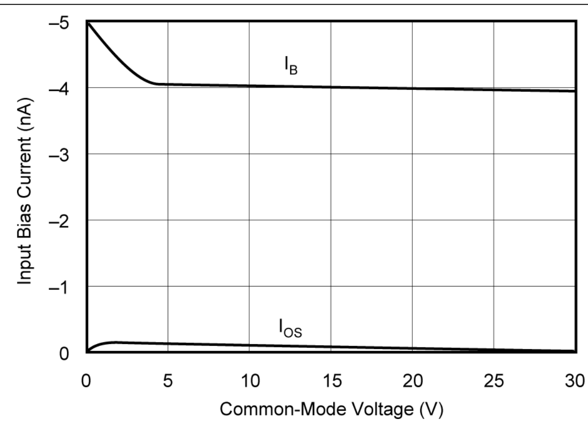


Figure 5-9. Input Bias Current vs Input Common-mode Voltage

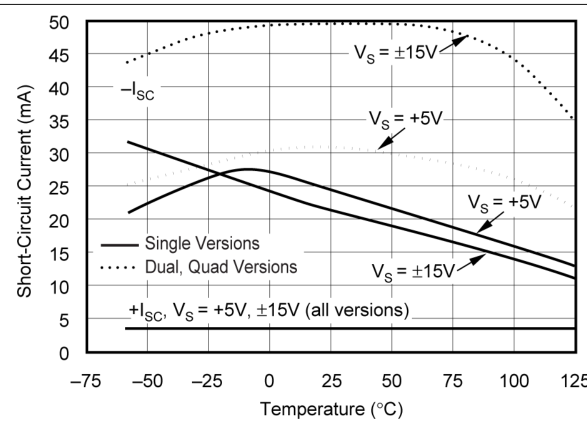


Figure 5-10. Short-circuit Current vs Temperature

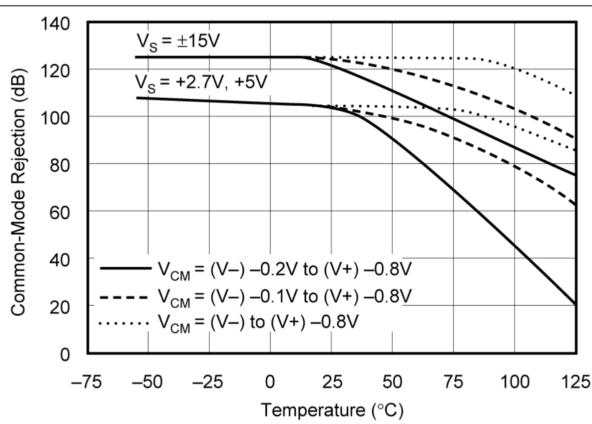


Figure 5-11. Common-mode Rejection vs Temperature

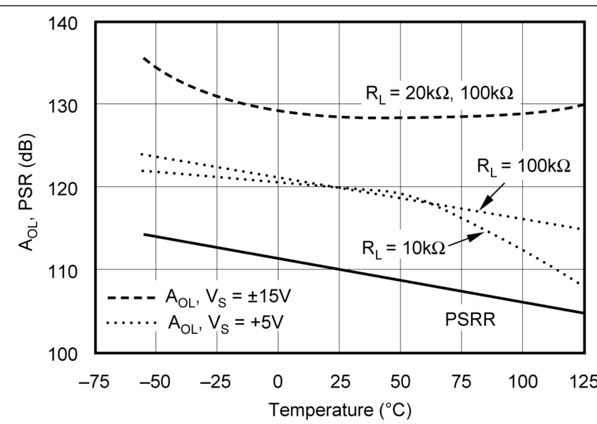


Figure 5-12. Open-loop Gain and Power Supply Rejection vs Temperature

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

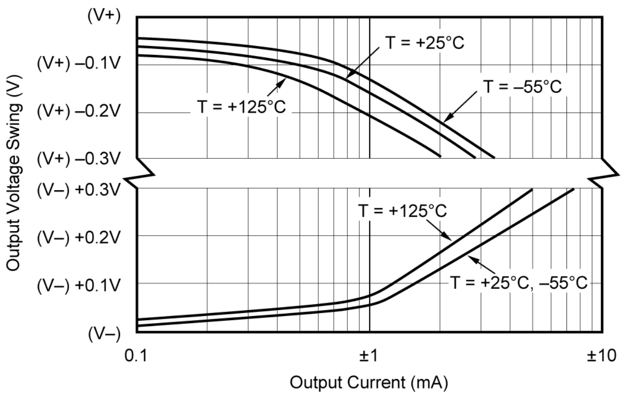


Figure 5-13. Output Voltage Swing vs Output Current

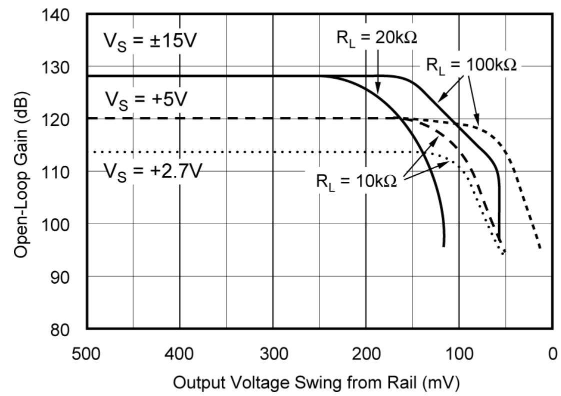


Figure 5-14. Open-loop Gain vs Output Voltage Swing

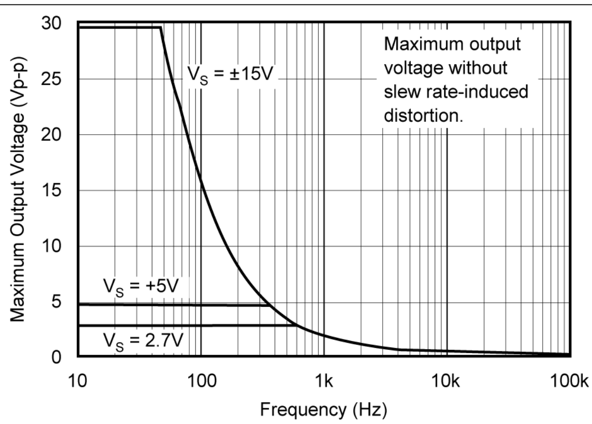


Figure 5-15. Maximum Output Voltage vs Frequency

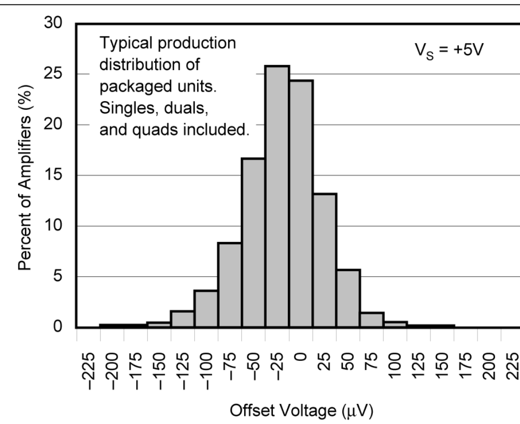


Figure 5-16. OPA241 Series Offset Voltage Production Distribution

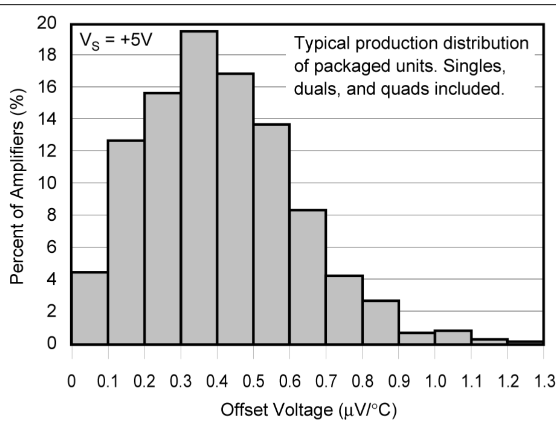


Figure 5-17. OPA241 Series Offset Voltage Drift Production Distribution

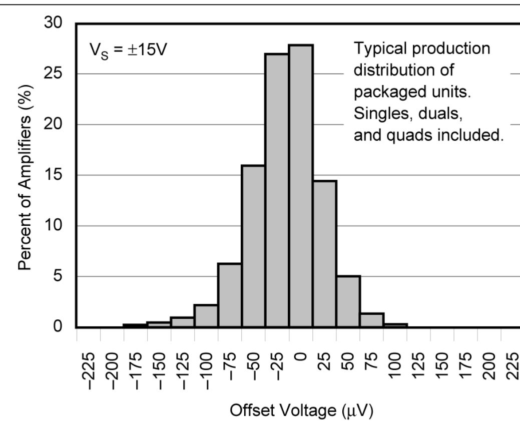


Figure 5-18. OPA251 Series Offset Voltage Production Distribution

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)

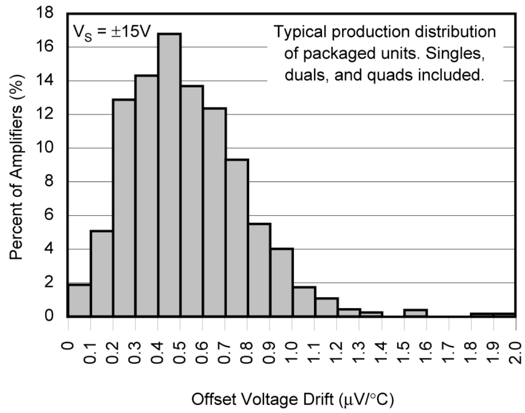


Figure 5-19. OPA251 Series Offset Voltage Drift Production Distribution

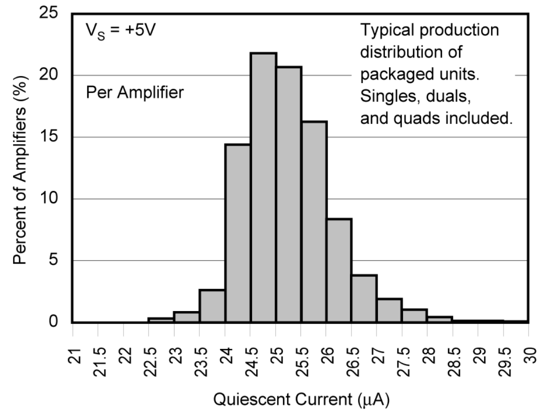


Figure 5-20. Quiescent Current Product Distribution

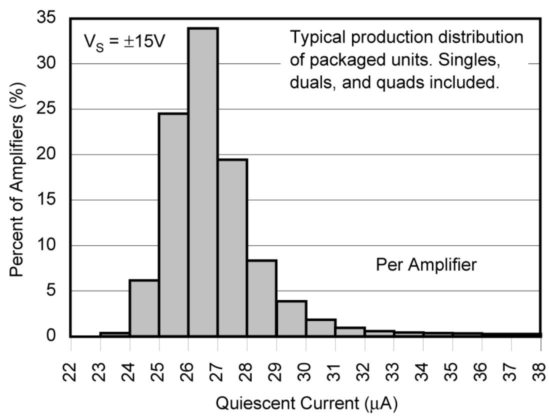
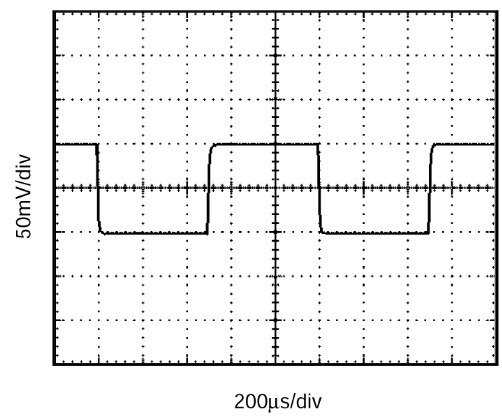
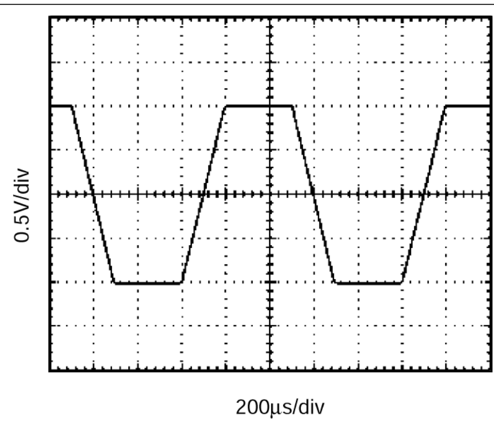


Figure 5-21. Quiescent Current Production Distribution



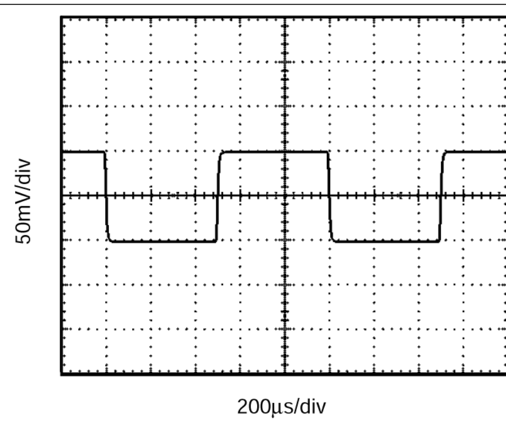
V_S = 5V, G = +1, R_L = 100kΩ, C_L = 100pF

Figure 5-22. OPA241 Small-Signal Step Response



V_S = 5V, G = + 1, R_L = 100kΩ, C_L = 100pF

Figure 5-23. OPA241 Large-Signal Step Response

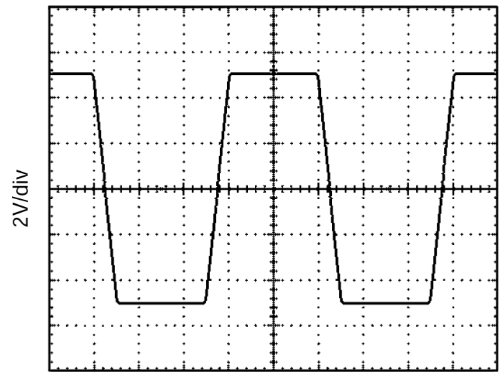


V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF

Figure 5-24. OPA251 Small-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = +25°C, R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), and curves apply to OPA241 and OPA251 (unless otherwise specified)



V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF

Figure 5-25. OPA251 Large-Signal Step Response

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Applications Information

The OPAx241 and OPAx251 series are unity-gain stable and designed for a wide range of general-purpose applications. Bypass power-supply pins with 0.01µF ceramic capacitors.

6.1.1 Operating Voltage

The OPAx241 series is laser-trimmed for low offset voltage and drift at a low supply voltage (V_S = 5V). The OPAx251 series is trimmed for ±15V operation. Both series operate over the full voltage range (2.7V to 36V or ±1.35V to ±18V) with some compromises in offset voltage and drift performance. However, all other parameters have similar performance. Key parameters are production tested over the specified temperature range of −40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. The typical characteristics curves show parameters that vary significantly with operating voltage or temperature.

6.1.2 Offset Voltage Trim

As previously mentioned, the OPAx241 series offset voltage is laser-trimmed at 5V. The OPAx251 series is trimmed at ±15V. The initial offset is so low that user adjustment is usually not required. However, the OPA241 and OPA251 (single op-amp versions) provide offset voltage trim connections on pins 1 and 5. Figure 6-1shows how the offset voltage can be adjusted by connecting a potentiometer. Only use this adjustment to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset can degrade the offset drift behavior of the op amp. While predicting the exact change in drift is not possible, the effect is usually small.

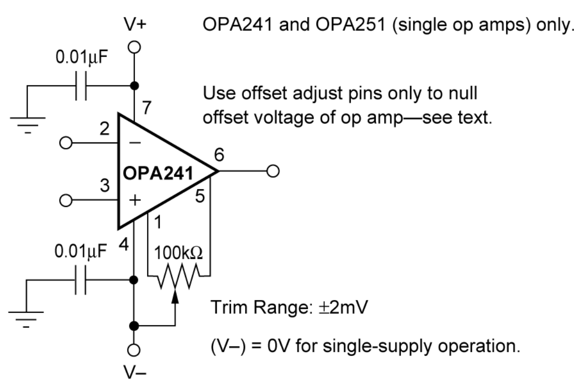


Figure 6-1. OPA241 and OPA251 Offset Voltage Trim Circuit

6.1.3 Capacitive Load and Stability

The OPAx241 series and OPAx251 series can drive a wide range of capacitive loads. However, all op amps under certain conditions can be unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

Figure 6-2 and Figure 6-3 show the regions where the OPAx241 series and OPAx251 series have the potential for instability. As shown, the unity gain configuration with low supplies is the most susceptible to the effects of capacitive load. With V_S = 5V, G = 1, and I_{OUT} = 0, operation remains stable with load capacitance up to approximately 200pF. Increasing a combination of supply voltage, output current, and gain significantly improves capacitive load drive. For example, increasing the supplies to ±15V and gain to 10 drives approximately 2700pF.

Figure 6-4 shows one method to improve capacitive load drive in the unity gain configuration by inserting a resistor inside the feedback loop. This reduces ringing with large capacitive loads while maintaining dc accuracy. For example, with V_S = ±1.35V and R_S = 5kΩ, the OPAx241 series and OPAx251 series perform well with capacitive loads in excess of 1000pF. Without the series resistor, the capacitive load drive is typically 200pF for these conditions. However, this method results in a slight reduction of output voltage swing.

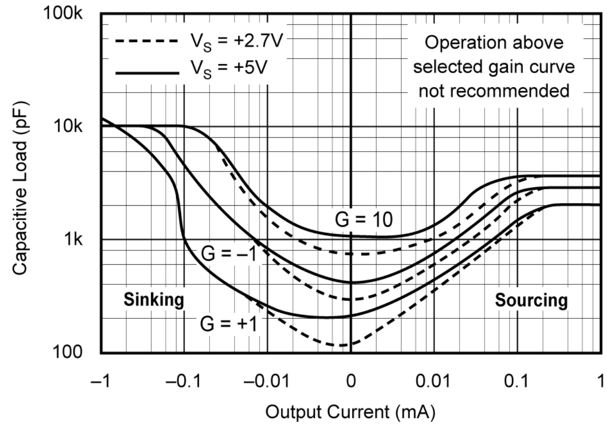


Figure 6-2. Stability—Capacitive Load vs Output Current for Low Supply Voltage

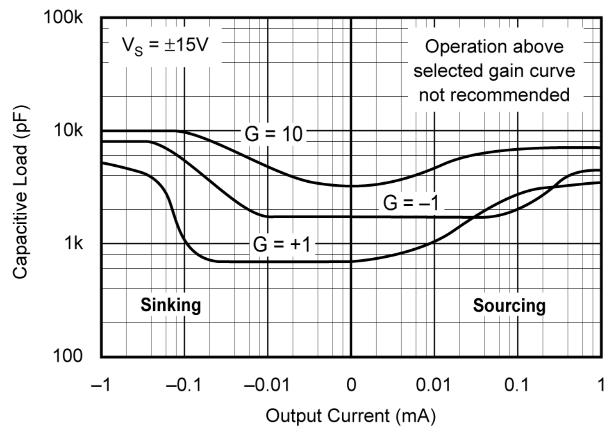


Figure 6-3. Stability—Capacitive Load vs Output Current for ±15V Supplies

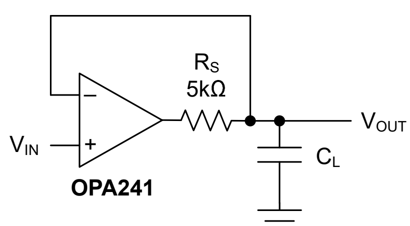
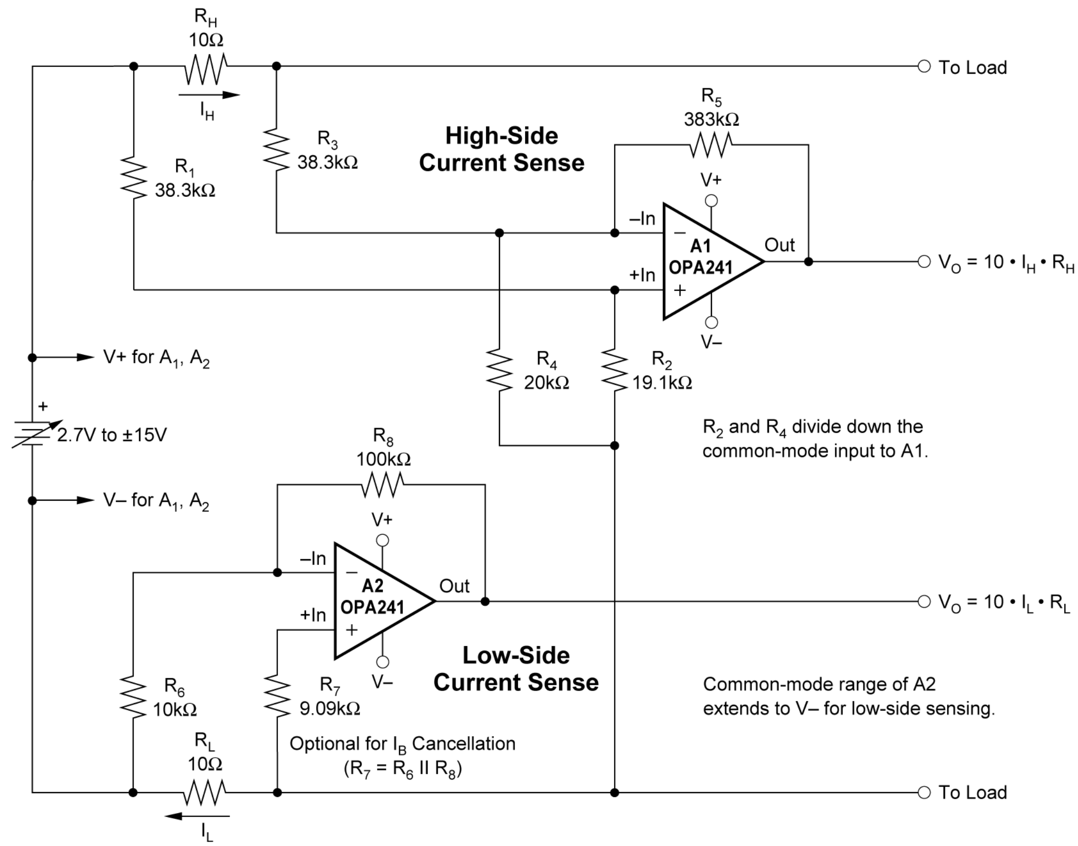


Figure 6-4. Series Resistor in Unity Gain Configuration Improves Capacitive Load Drive



NOTE: Low and high-side sensing circuits can be used independently.

Figure 6-5. Low-Side and High-Side Battery Current Sensing

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2000) to Revision A (June 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout document....................... 1
- Added the *Device Information* table, and the *Pin Configuration and Functions*, *Recommended Operating Conditions*, *Thermal Information*, *Electrical Characteristics*, *Application and Implementation*, *Device and Documentation Support*, *Revision History*, and *Mechanical, Packaging, and Orderable Information* sections..1
- Added new figure to *Description* 1
- Updated pin names.. 3
- Changed input voltage noise from 1µV_{PP} to 1.7µV_{PP} 7
- Changed input voltage noise density from 45nV/√Hz to 65nV/√Hz 7
- Changed input impedance differential capacitance from 2pF to 3.75pF.. 7
- Changed overload recovery from 60µs to 80µs... 7
- Changed short-circuit current from –30mA to –24mA for dual and quad.. 7
- Changed short-circuit current sink from –50mA to –27mA...9
- Deleted *Input Voltage and Current Noise Spectral Density vs Frequency* from *Typical Characteristics* 11
- Added Figure 5-4, *Input Voltage Noise Spectral Density vs Frequency* and Figure 5-5, *Input Current Noise Spectral Density vs Frequency* 11

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2241PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2241PA	Samples
OPA2241PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2241PA	Samples
OPA2241UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 2241UA	
OPA2241UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2251PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2251PA	Samples
OPA2251PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2251PA	Samples
OPA2251UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 2251UA	
OPA2251UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA241PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA241PA	Samples
OPA241UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 241UA	
OPA241UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA251UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 251UA	
OPA251UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA	Samples
OPA4241PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4241PA	Samples
OPA4241UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4241UA	Samples
OPA4241UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4241UA	Samples
OPA4251UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples
OPA4251UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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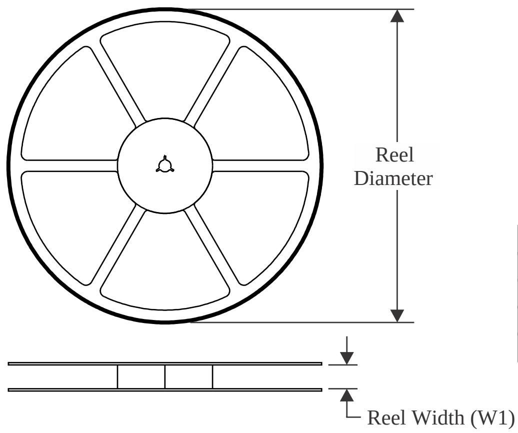
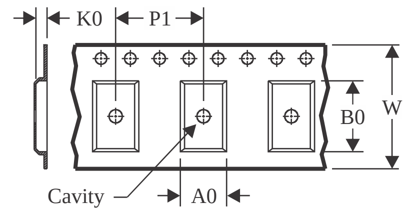
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

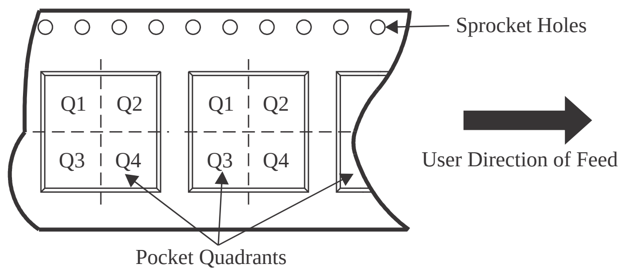


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

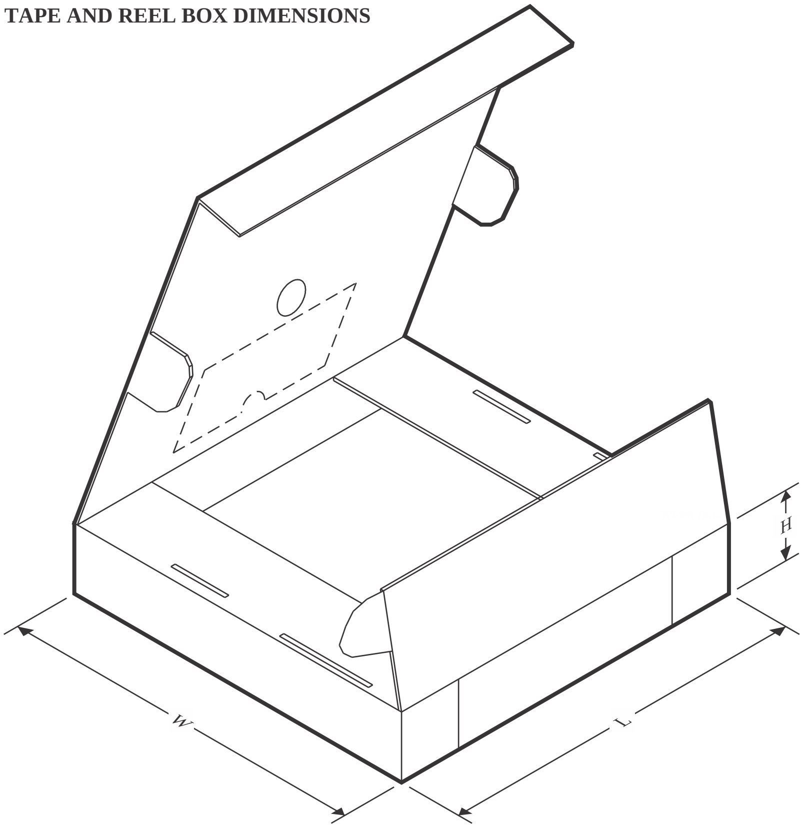
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4241UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4251UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

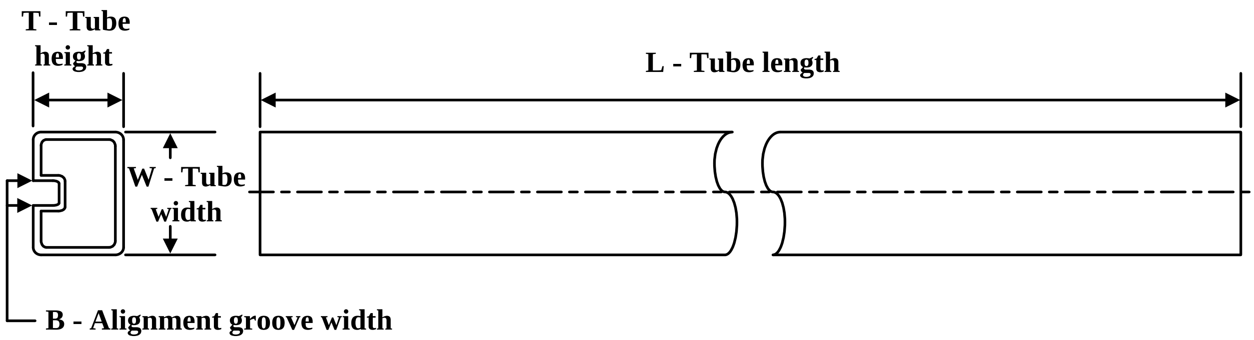
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

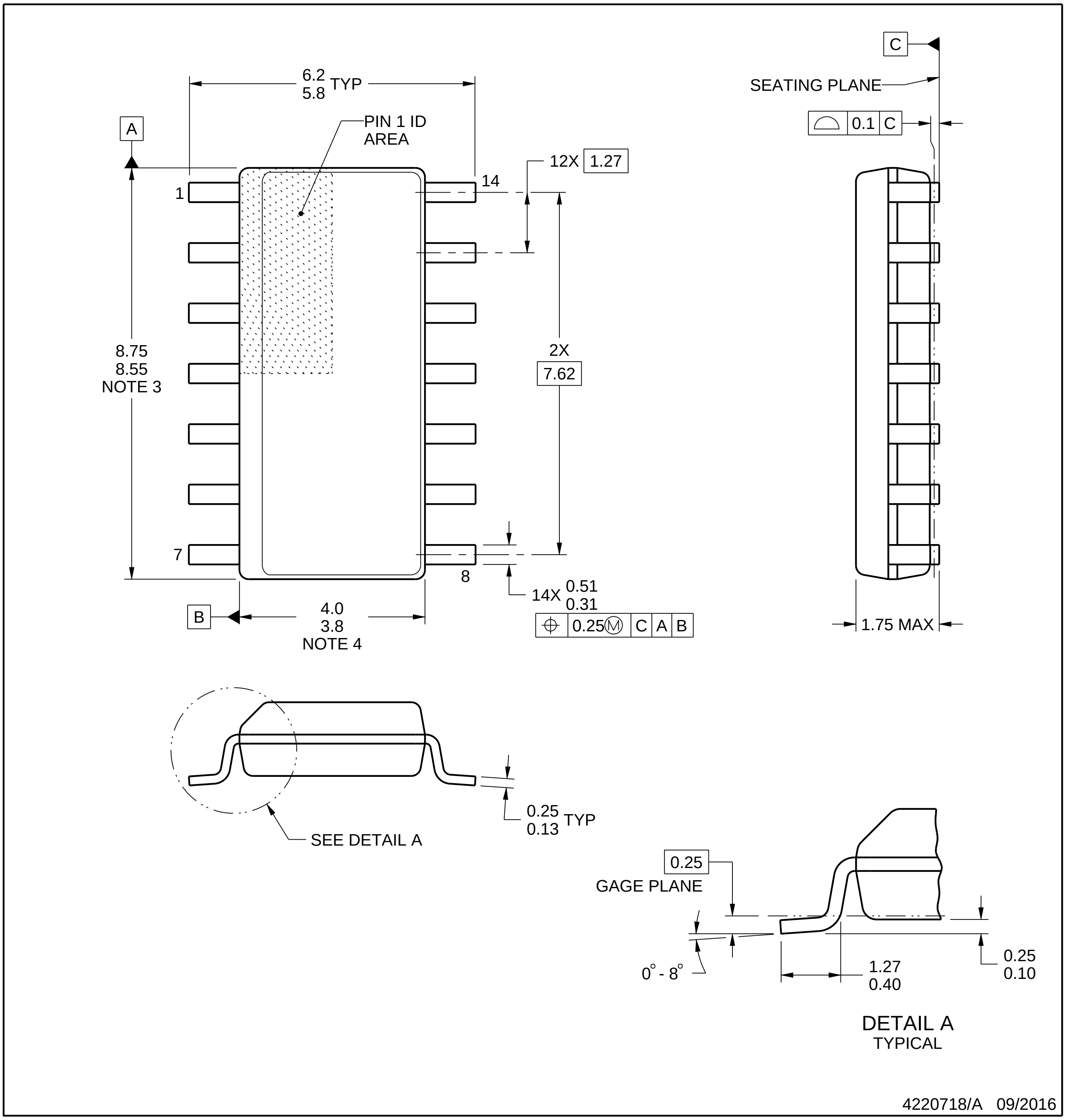
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2241UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2251UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA241UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA251UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4241UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0
OPA4251UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



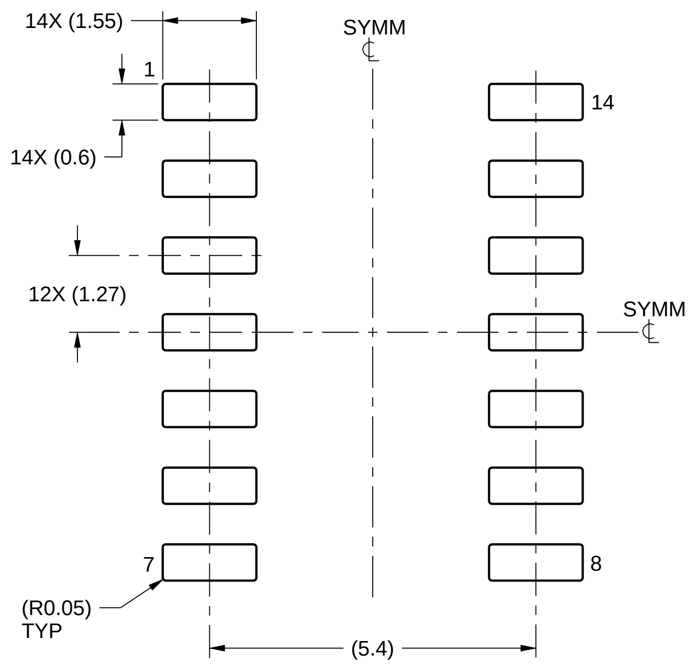
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA4241PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4241UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4251UA	D	SOIC	14	50	506.6	8	3940	4.32

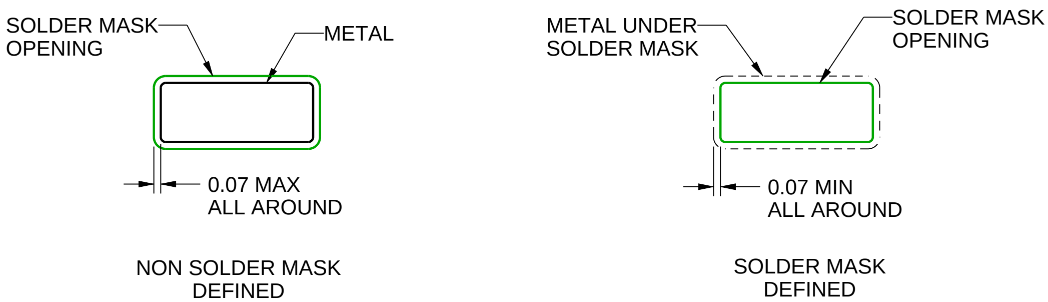


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

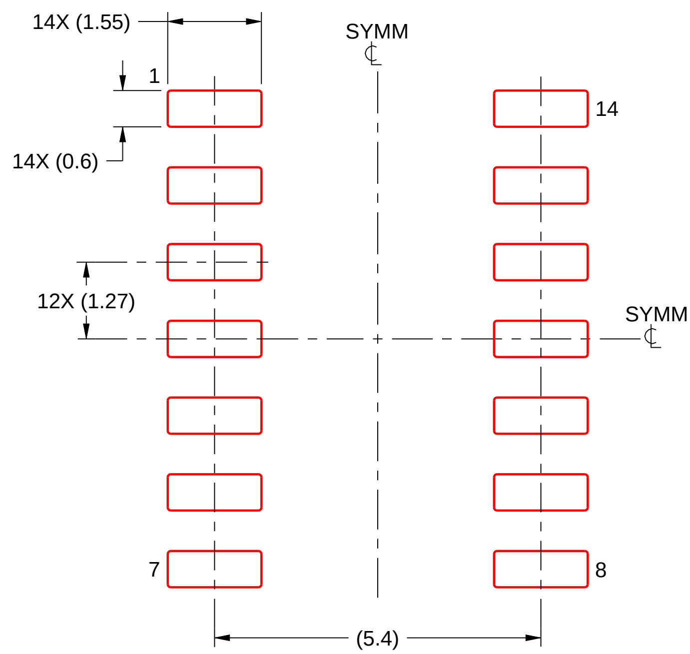


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

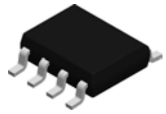


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

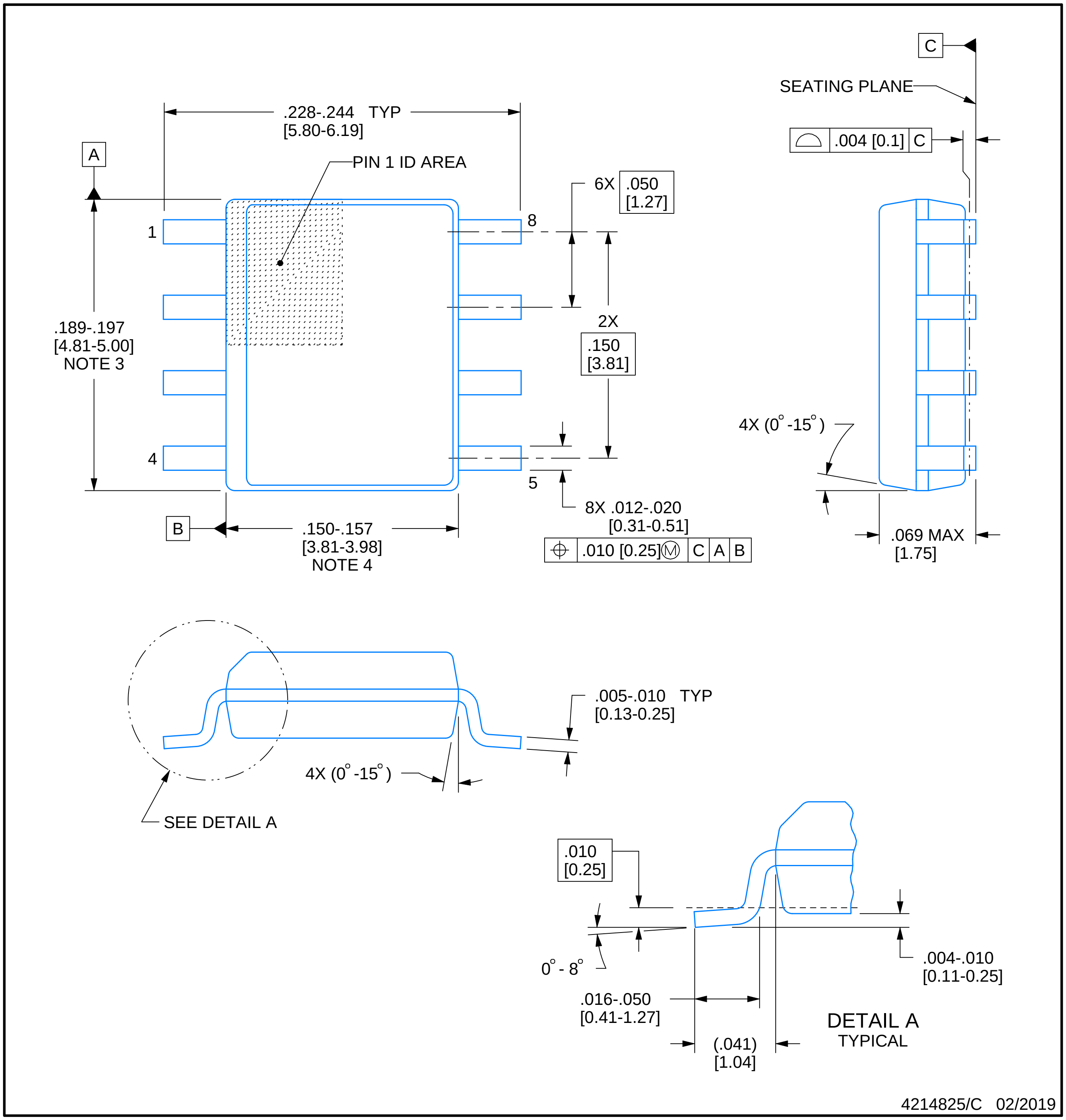
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

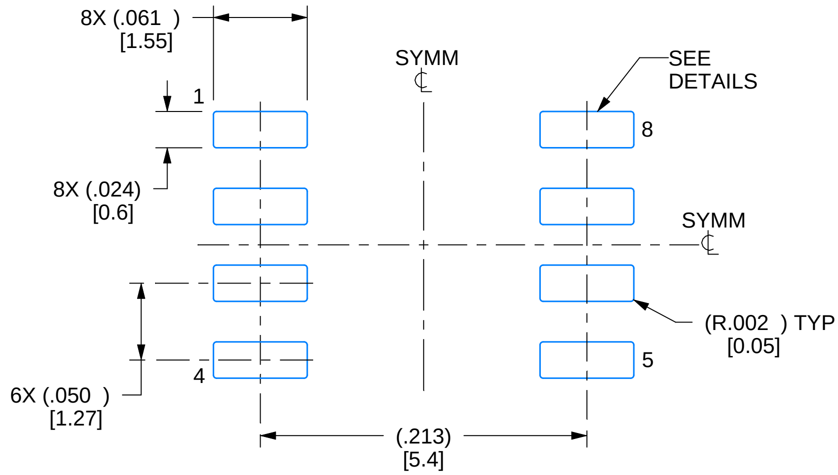
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

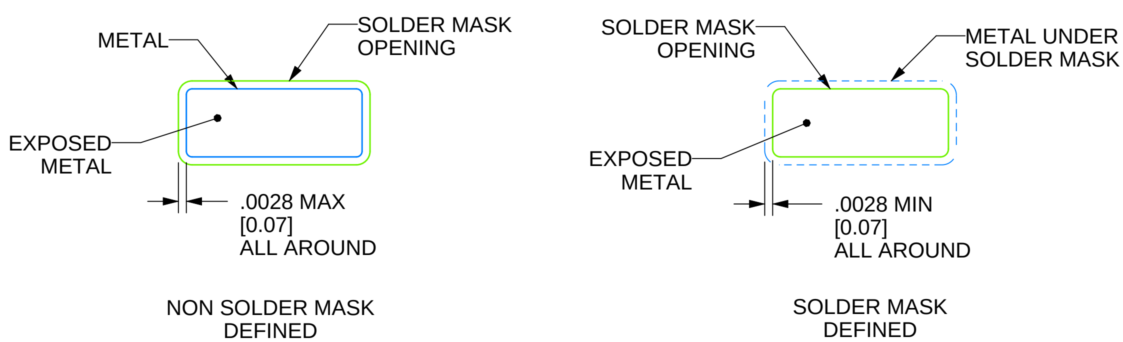


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

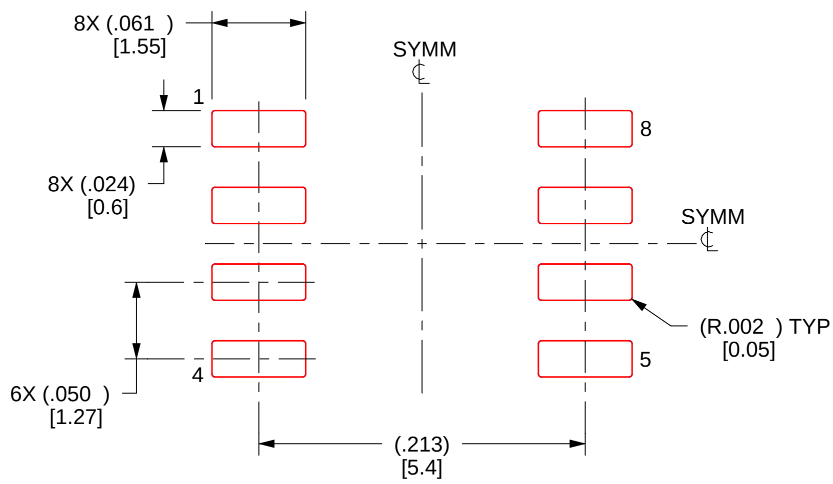


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



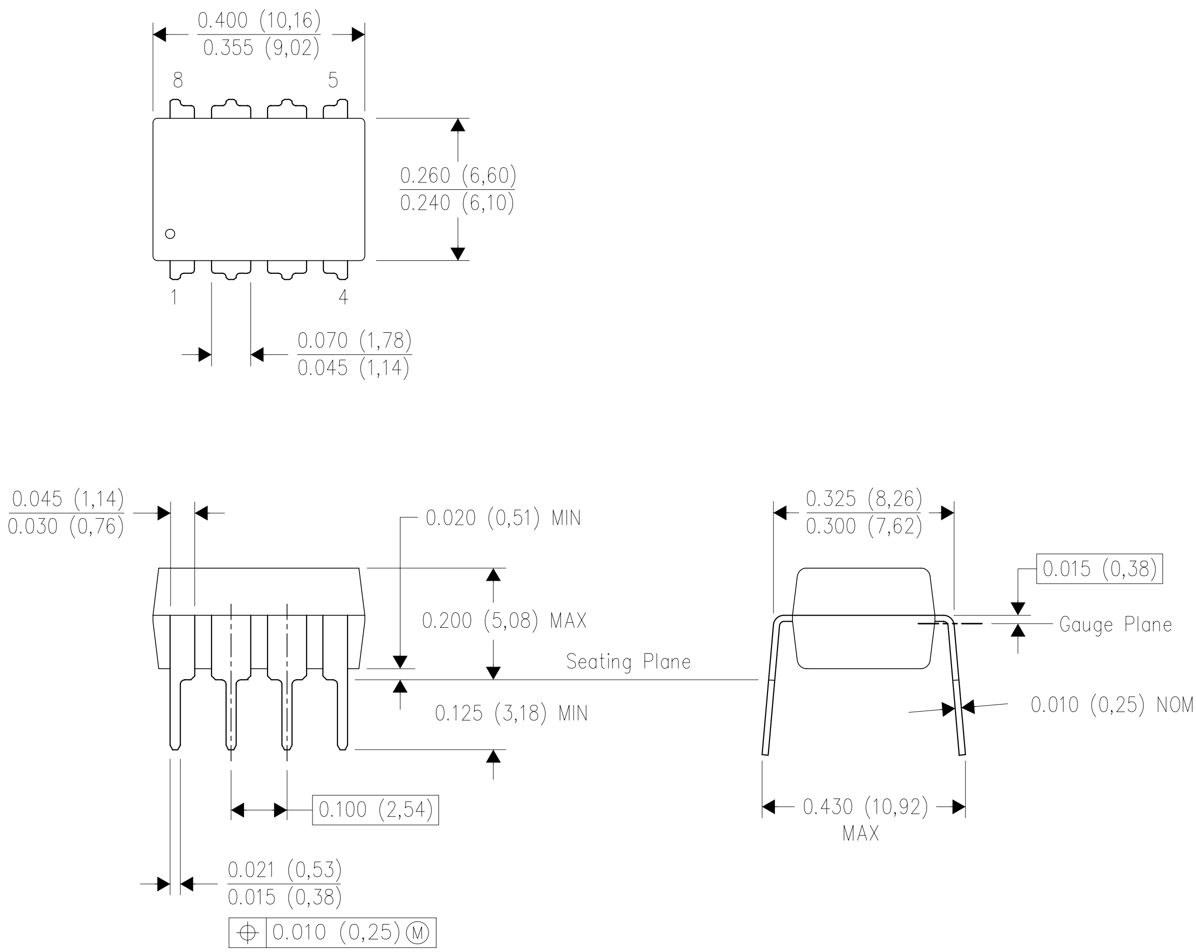
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

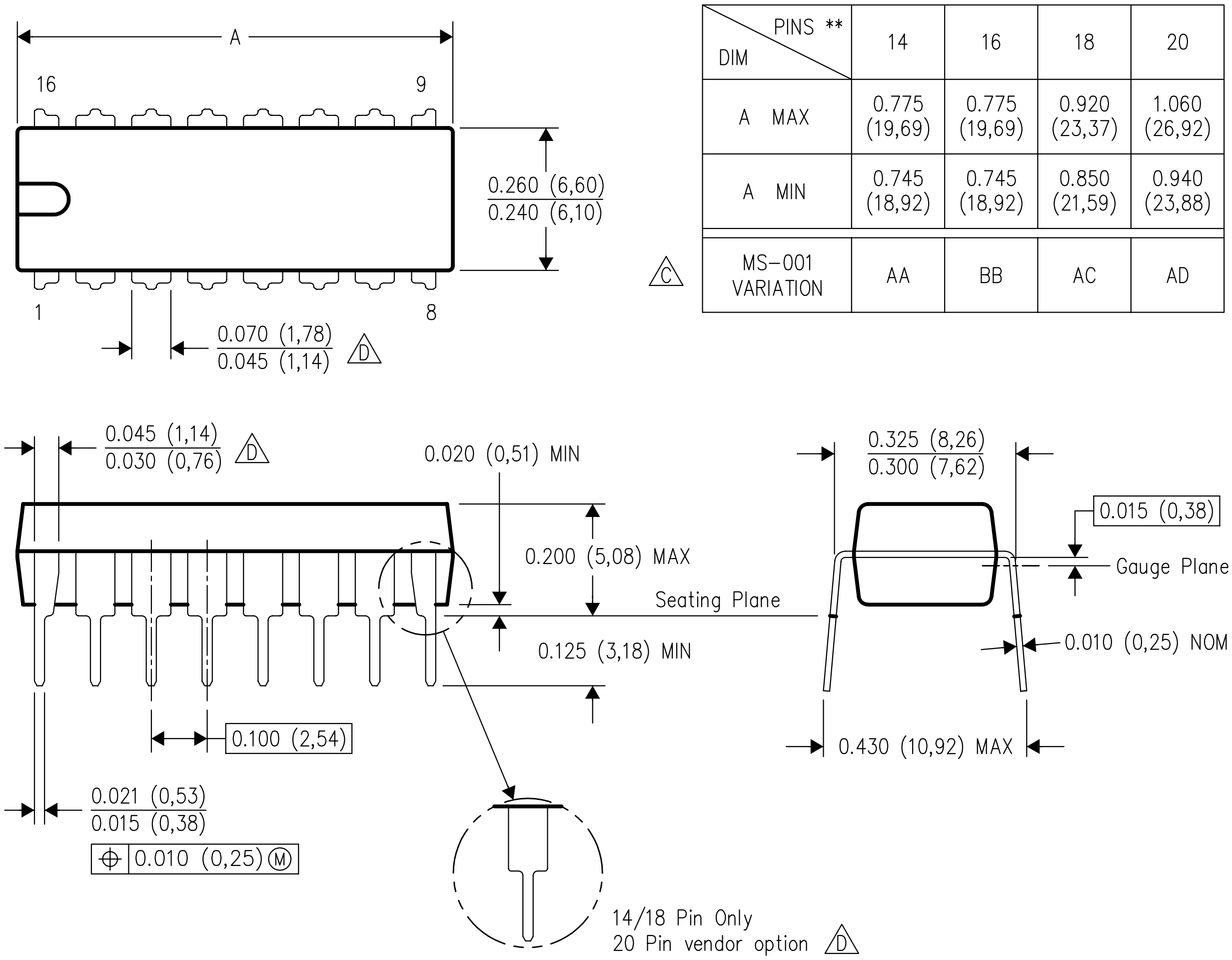


4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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