OPA4277-EP High Precision Operational Amplifier

1 Features

- Ultra-Low Offset Voltage: 10 µV
- Ultra-Low Drift: ±0.1 µV/°C
- High Open-Loop Gain: 134 dB
- High Common-Mode Rejection: 140 dB
- High-Power Supply Rejection: 130 dB
- Low Bias Current: 1-nA Max
- Wide Supply Range: ±2 to ±18 V
- Low Quiescent Current: 800 µA/Amplifier
- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military (–55°C to 125°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

2 Applications

- Transducer Amplifier
- Bridge Amplifier
- Temperature Measurements
- Strain Gage Amplifier
- Precision Integrator
- Battery Powered Instruments
- Test Equipment

3 Description

The OPA4277-EP precision operational amplifier replaces the industry standard OP-177. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

The OPA4277-EP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-EP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage (±20-µV max) is so low, user adjustment is usually not required.

The OPA4277-EP is easy to use and free from phase inversion and overload problems found in some operational amplifiers. It is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. The OPA4277-EP features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA4277MDTEP	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

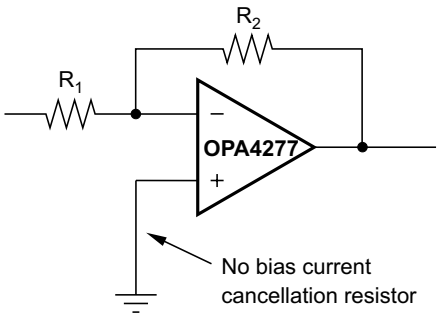


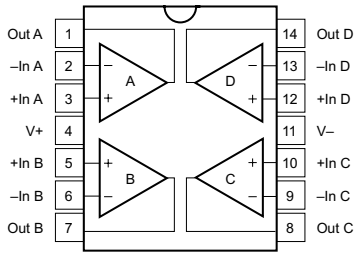
Table of Contents

4 Revision History

DATE	REVISION	NOTES
November 2014	*	Initial release.

5 Pin Configuration and Functions

D Package
14 Pins
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT A	1	O	Amplifier output A
–IN A	2	I	Inverting amplifier input A
+IN A	3	I	Noninverting amplifier input A
V+	4	P	Positive amplifier power supply input
+IN B	5	I	Noninverting amplifier input B
–IN B	6	I	Inverting amplifier input B
OUT B	7	O	Amplifier output B
OUT C	8	O	Amplifier output C
–IN C	9	I	Inverting amplifier input C
+IN C	10	I	Noninverting amplifier input C
V–	11	P	Negative amplifier power supply input
+IN D	12	I	Noninverting amplifier input D
–IN D	13	I	Inverting amplifier input D
OUT D	14	O	Amplifier output D

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage		36	V
Input voltage	(V–) – 0.7	(V+) + 0.7	V
Output short circuit	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Machine model (MM)	–100	100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Dual supply voltage	±5	±15	V
T_J	Operating junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA4277-EP D (14 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	26.8	
ψ_{JT}	Junction-to-top characterization parameter	2.1	
ψ_{JB}	Junction-to-board characterization parameter	26.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = 25°C, and R_L = 2 kΩ, V_S = ±5 to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±20	±65	µV
	Input offset voltage over temperature	T_J = –55°C to 125°C			±140	
dV_{OS}/d_T	Input offset voltage drift			±0.15		µV/°C
PSRR	Input offset voltage	vs time		0.2		µV/mo
		vs power supply, V_S = ±2 to ±18 V		±0.3	±1	µV/V
		T_J = –55°C to 125°C; V_S = ±2 to ±18 V			±1	µV/V
	Channel separation	dc		0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±0.5	±2.8	nA
		T_J = –55°C to 125°C			±7.5	
I_{OS}	Input offset current			±0.5	±2.8	nA
		T_J = –55°C to 125°C			±7.5	
NOISE						
	Input voltage noise	f = 0.1 to 10 Hz		0.22		μV_{pp}
e_n	Input voltage noise density	f = 10 Hz		12		$nV/\sqrt{Hz}$
		f = 100 Hz		8		
		f = 1 kHz		8		
		f = 10 kHz		8		
$_{in}$	Current noise density	f = 1 kHz		0.2		$pA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = (V–) + 2 V to (V+) – 2 V	115	140		dB
		T_J = –55°C to 125°C; V_{CM} = (V–) + 2 V to (V+) – 2 V	115			
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common mode	V_{CM} = (V–) + 2 V to (V+) – 2 V		250 || 3		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_O = (V–) + 0.5 V to (V+) – 1.2 V, R_L = 10 kΩ		140		dB
		V_O = (V–) + 1.5 V to (V+) – 1.5 V, R_L = 2 kΩ	126	134		
		T_J = –55°C to 125°C; V_O = (V–) + 1.5 V to (V+) – 1.5 V, R_L = 2 kΩ	126			
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.8		V/µs
	Setting time	0.1%, V_S = ±15 V, G = 1, 10-V step		14		µs
		0.01%, V_S = ±15 V, G = 1, 10-V step		16		
THD + N	Total harmonic distortion + noise	1 kHz, G = 1, V_O = 3.5 Vrms		0.002%		

Electrical Characteristics (continued)

At T_J = 25°C, and R_L = 2 kΩ, V_S = ±5 to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output	T_J = –55°C to 125°C; R_L = 10 kΩ	(V–) + 0.5		(V+) – 1.2	V
		T_J = –55°C to 125°C; R_L = 2 kΩ	(V–) + 1.5		(V+) – 1.5	
I_{SC}	Short-circuit current			±35		mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
POWER SUPPLY						
V_S	Specified voltage		±5		±15	V
	Operating voltage		±2		±18	V
I_Q	Quiescent current (per amplifier)	I_O = 0		±790	±825	µA
		T_J = –55°C to 125°C; I_O = 0			±900	

6.6 Typical Characteristics

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

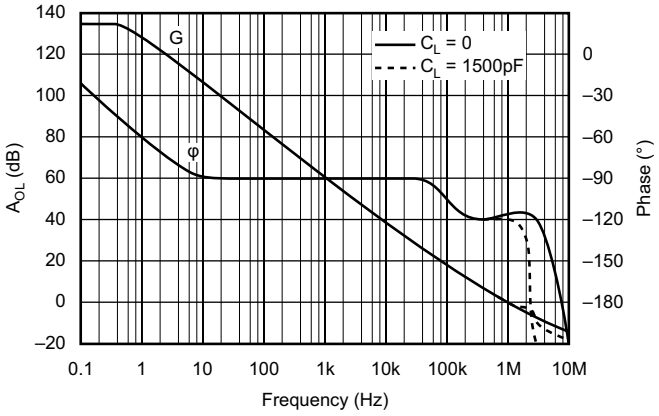


Figure 1. Open-Loop Gain/Phase vs Frequency

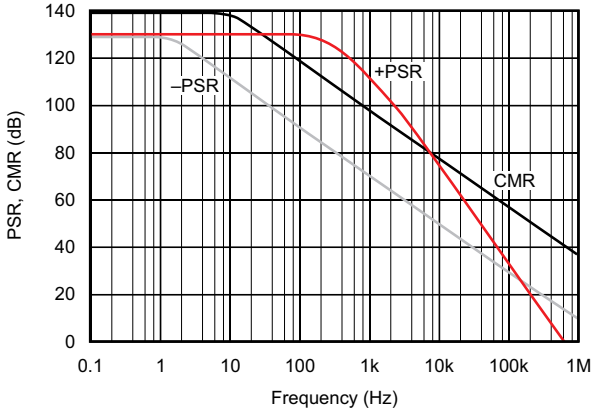


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

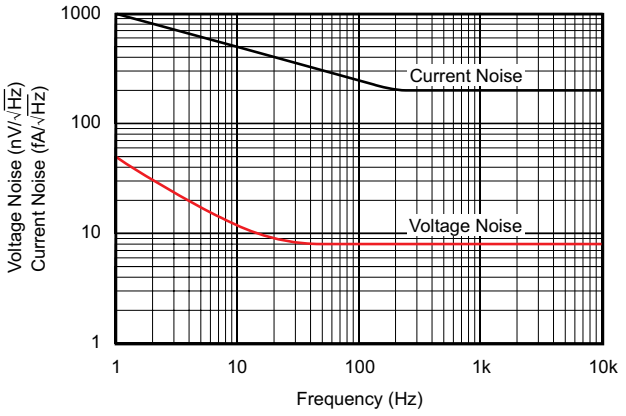


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency

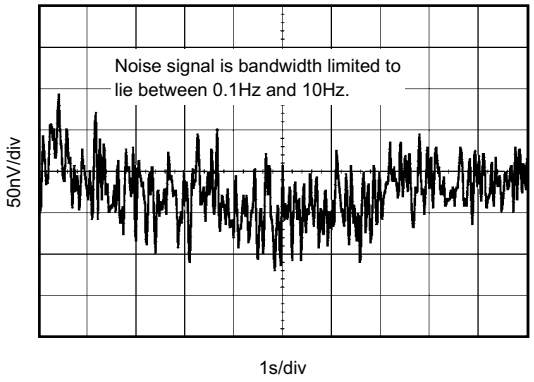


Figure 4. Input Noise Voltage vs Time

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

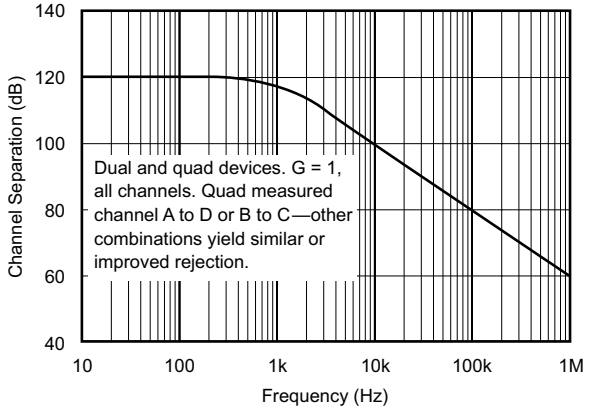
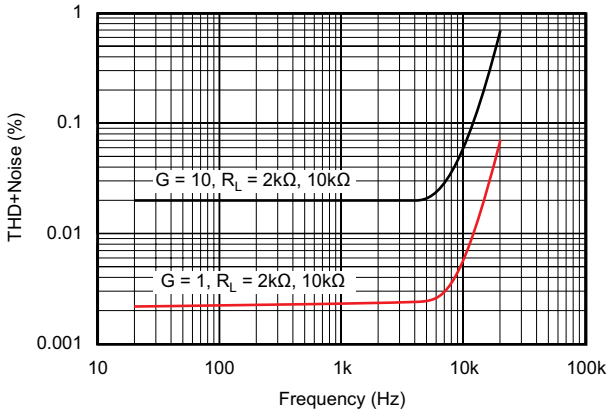


Figure 5. Channel Separation vs Frequency



V_{OUT} = 3.5 Vrms

Figure 6. Total Harmonic Distortion + Noise vs Frequency

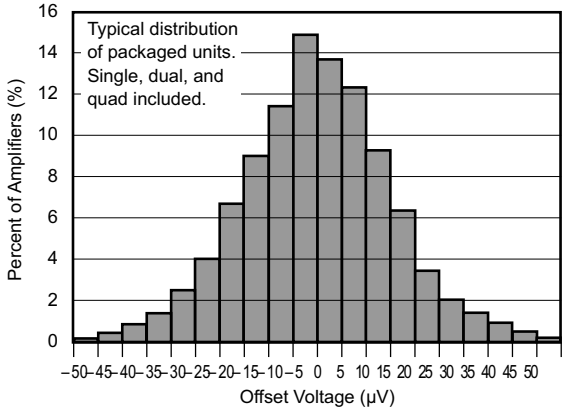


Figure 7. Offset Voltage Production Distribution

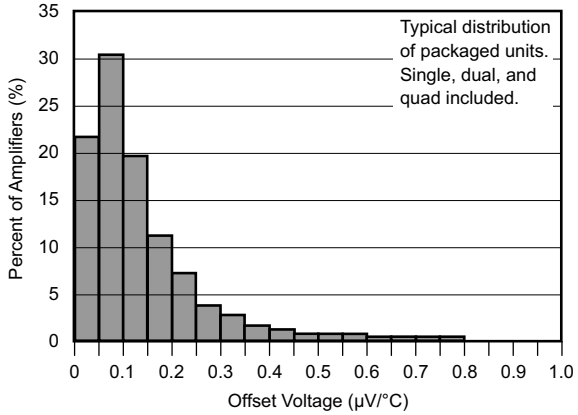


Figure 8. Offset Voltage Drift Production Distribution

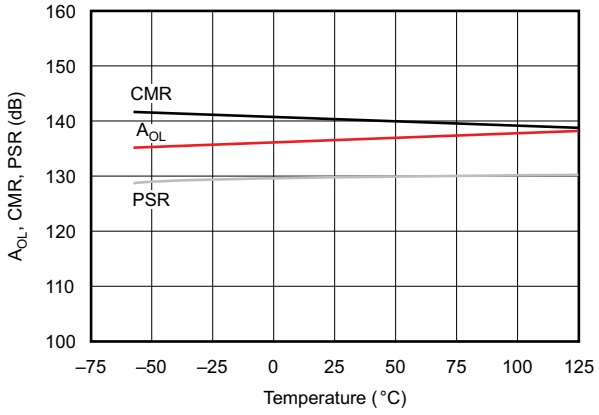


Figure 9. A_{OL}, CMR, PSR vs Temperature

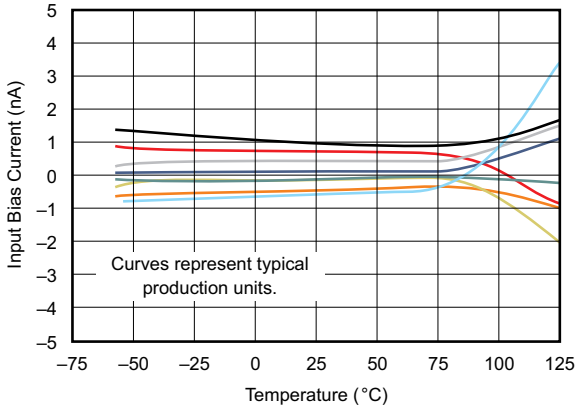


Figure 10. Input Bias Current vs Temperature

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

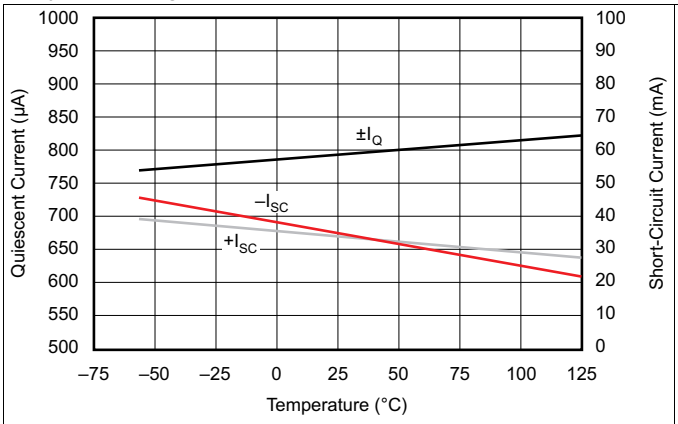


Figure 11. Quiescent Current and Short-Circuit Current vs Temperature

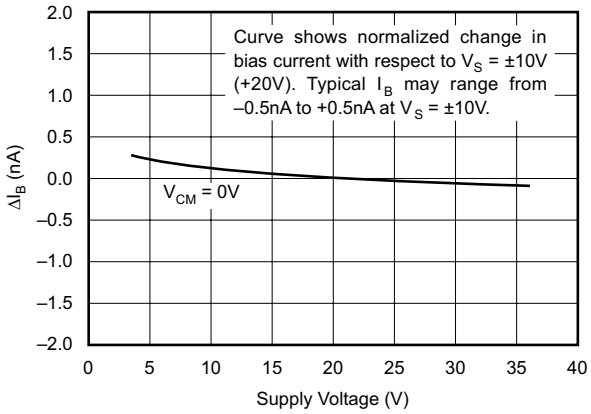


Figure 12. Change in Input Bias Current vs Power Supply Voltage

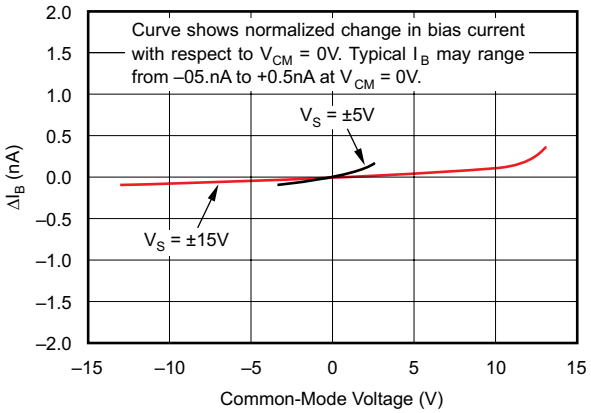


Figure 13. Change in Input Bias Current vs Common-Mode Voltage

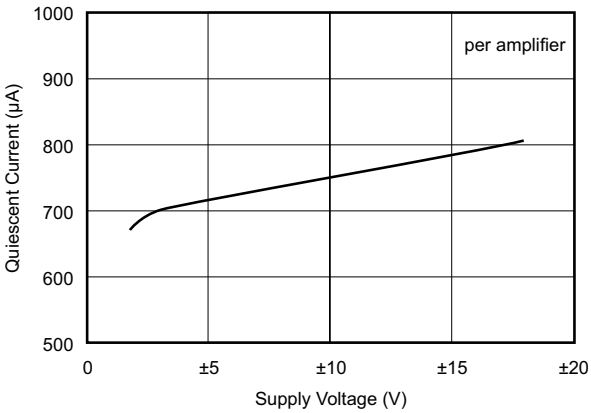


Figure 14. Quiescent Current vs Supply Voltage

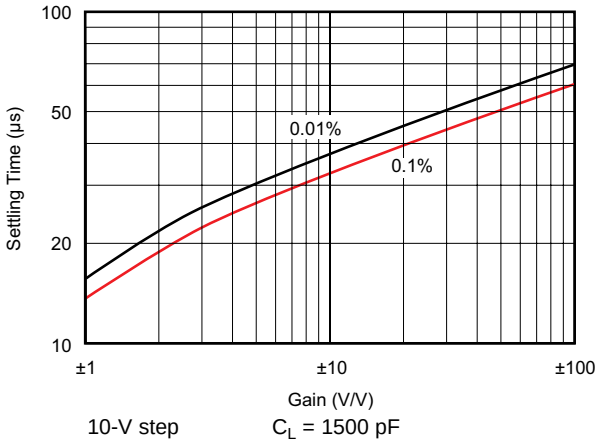


Figure 15. Settling Time vs Closed-Loop Gain

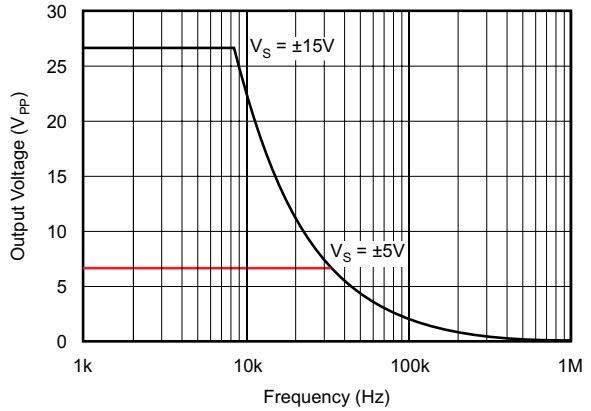


Figure 16. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

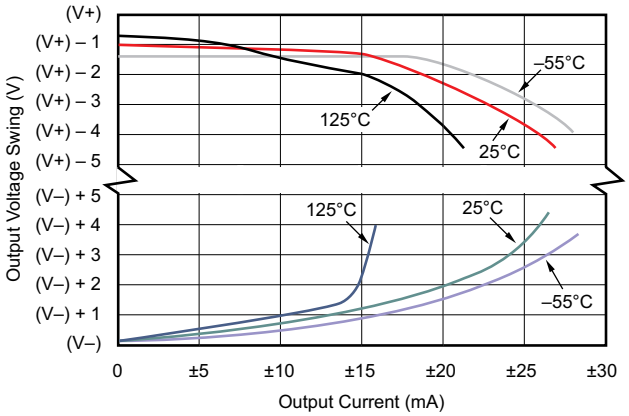


Figure 17. Output Voltage Swing vs Output Current

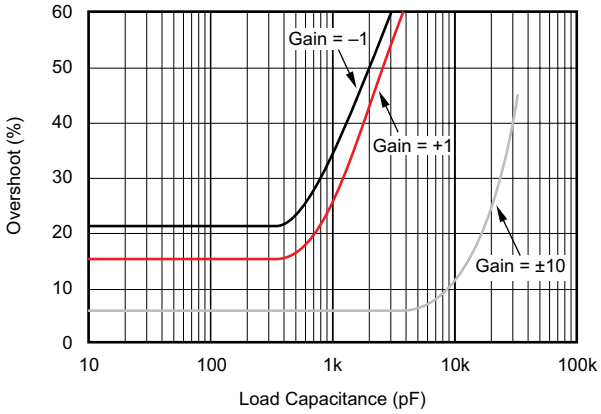
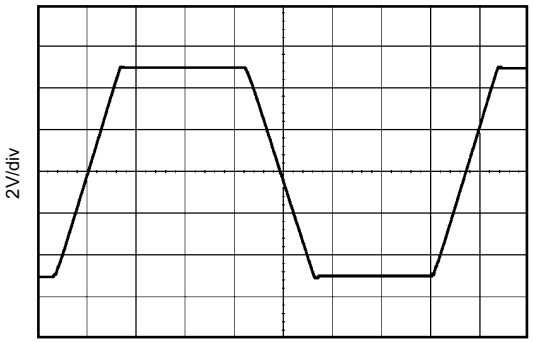
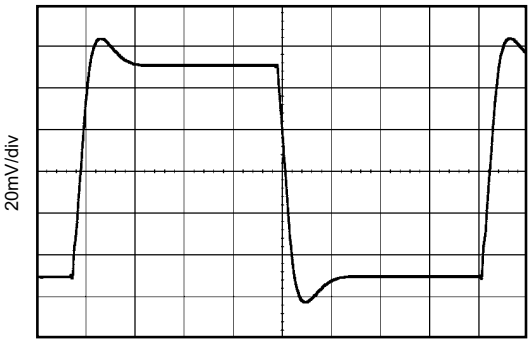


Figure 18. Small-Signal Overshoot vs Load Capacitance



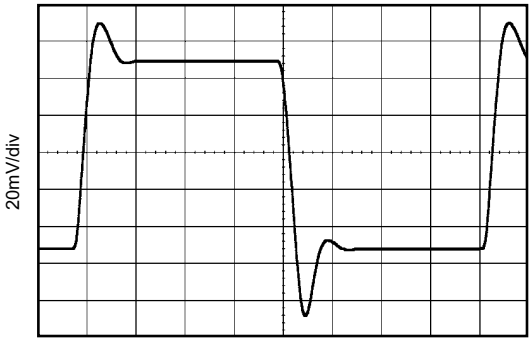
G = 1 C_L = 1500 pF V_S = 15 V

Figure 19. Large-Signal Step Response



G = 1 C_L = 0 pF V_S = 15 V

Figure 20. Small-Signal Step Response



G = 1 C_L = 1500 pF V_S = 15 V

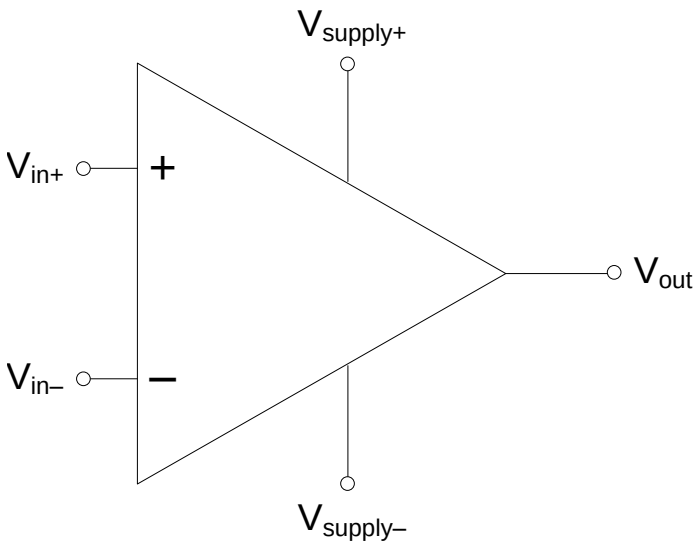
Figure 21. Small-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA4277-EP precision operational amplifier replaces the industry standard OP-177. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA4277-EP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-EP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage (±50 µV max) is so low, user adjustment is usually not required.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA4277 is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

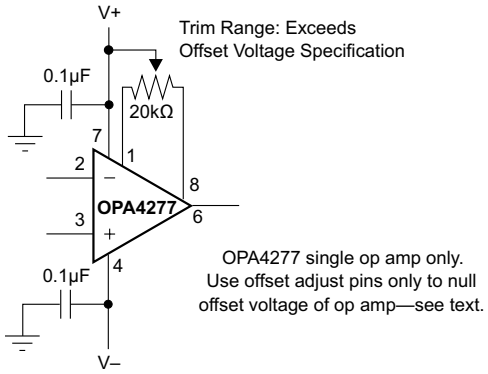


Figure 22. OPA4277 Offset Voltage Trim Circuit

8.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation (see Figure 25), Table 1 lists the design parameters needed with gain = 50.

$$G = 1 + \frac{2R_F}{R} = 50 \quad (1)$$

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_F	10 kΩ
R	412 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Offset Voltage Adjustment

The OPA27 is laser-trimmed for very-low offset voltage and drift so most circuits do not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. The user can adjust offset voltage by connecting a potentiometer as shown in Figure 22. Only use this adjustment to null the offset of the operational amplifier. This adjustment should not be used to compensate for offsets created elsewhere in a system because this can introduce additional temperature drift.

8.2.2.2 Input Protection

The inputs of the OPA4277 are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

8.2.2.3 Input Bias Current Cancellation

The input stage base current of the OPA4277 is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see Figure 23). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

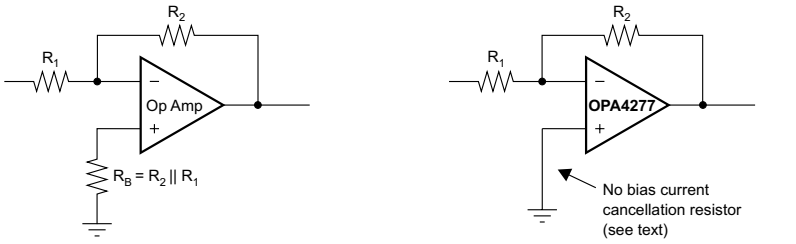
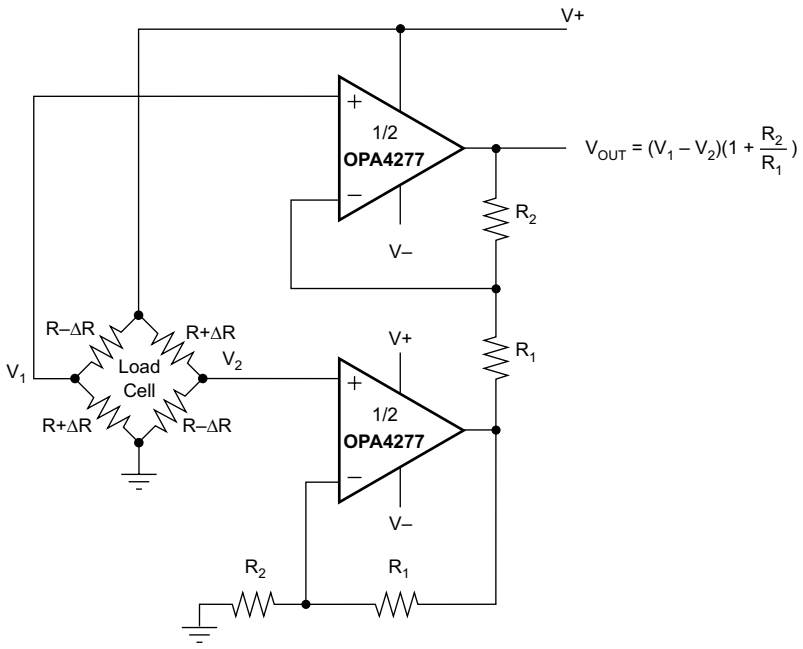


Figure 23. Input Bias Current Cancellation



For integrated solution see: INA126, INA2126 (dual)
INA125 (on-board reference)
INA122 (single-supply)

Figure 24. Load Cell Amplifier

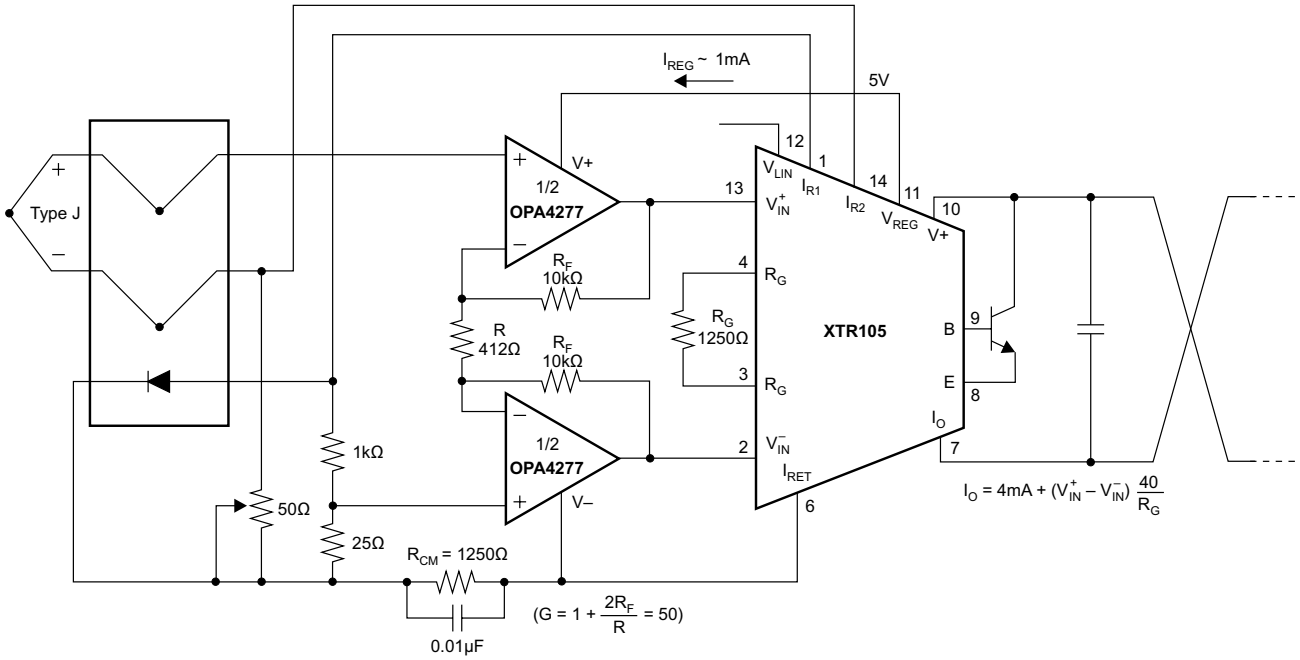


Figure 25. Thermocouple Low Offset, Low Drift Loop Measurement With Diode Cold Junction Compensation

8.2.3 Application Curve

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

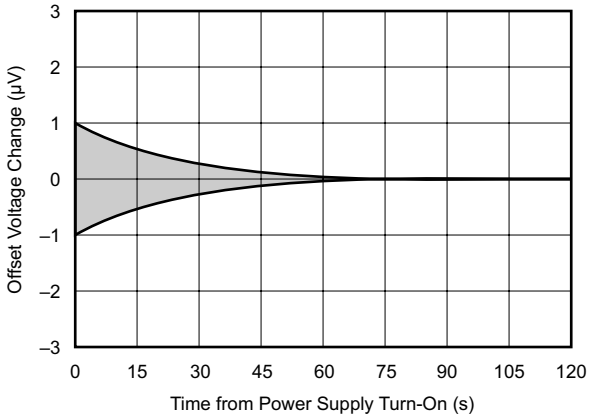


Figure 26. Warm-Up Offset Voltage Drift

9 Power Supply Recommendations

OPA4277 operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277 is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. This allows a customer operating at V_S = ±10 V to have the same assured performance as a customer using ±15-V supplies. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Most behavior remains unchanged through the full operating voltage range (±2 to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in the typical performance curves.

10 Layout

10.1 Layout Guidelines

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located in *Mechanical, Packaging, and Orderable Information* show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA4277 has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA4277. Cancel these thermal potentials by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

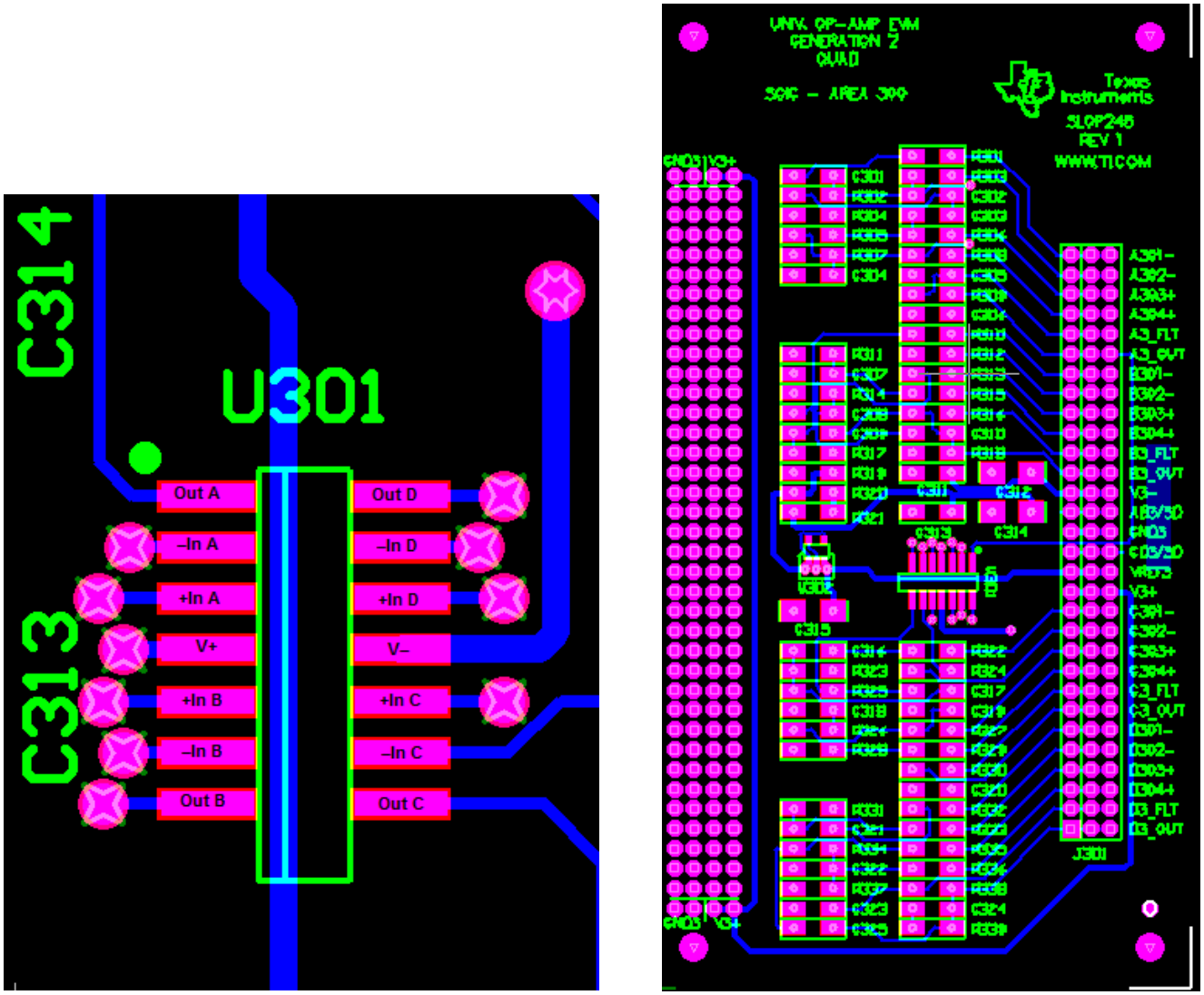


Figure 27. Board Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4277MDTEP	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	OPA4277EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA4277-EP :

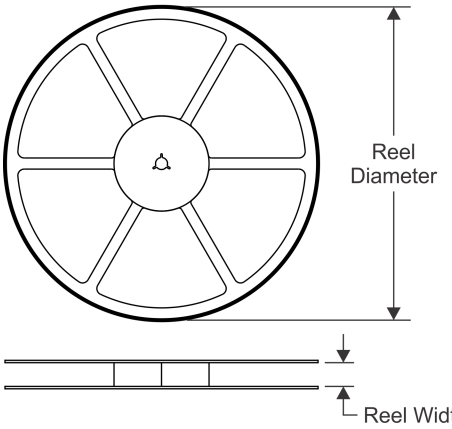
- Catalog : OPA4277
- Space : OPA4277-SP

NOTE: Qualified Version Definitions:

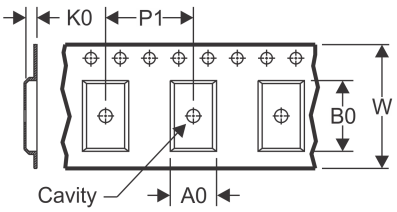
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

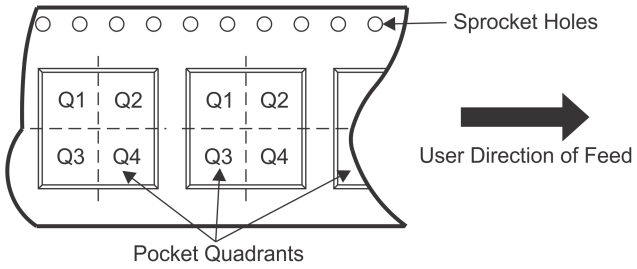


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

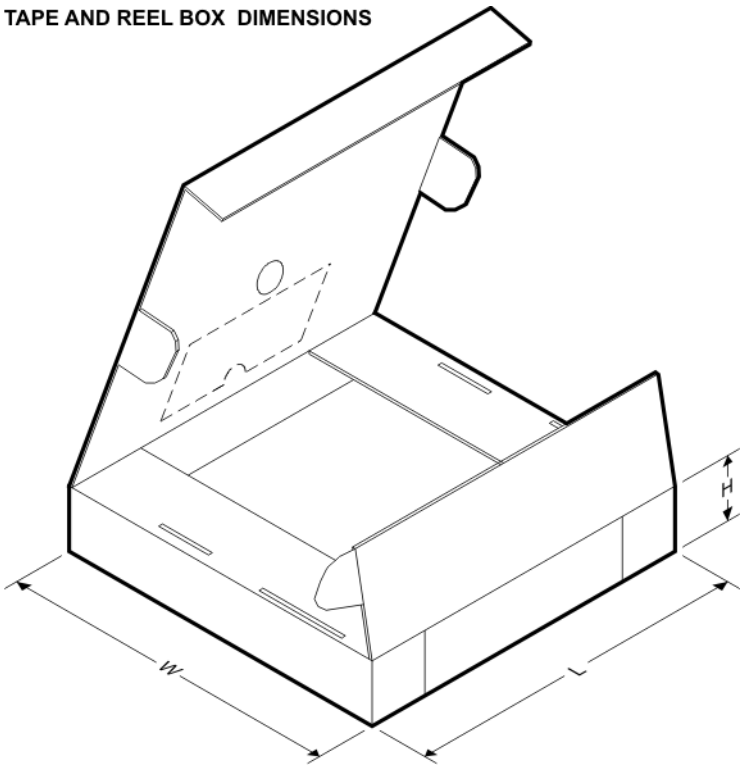
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

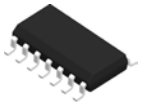
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4277MDTEP	SOIC	D	14	250	180.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4277MDTEP	SOIC	D	14	250	210.0	185.0	35.0

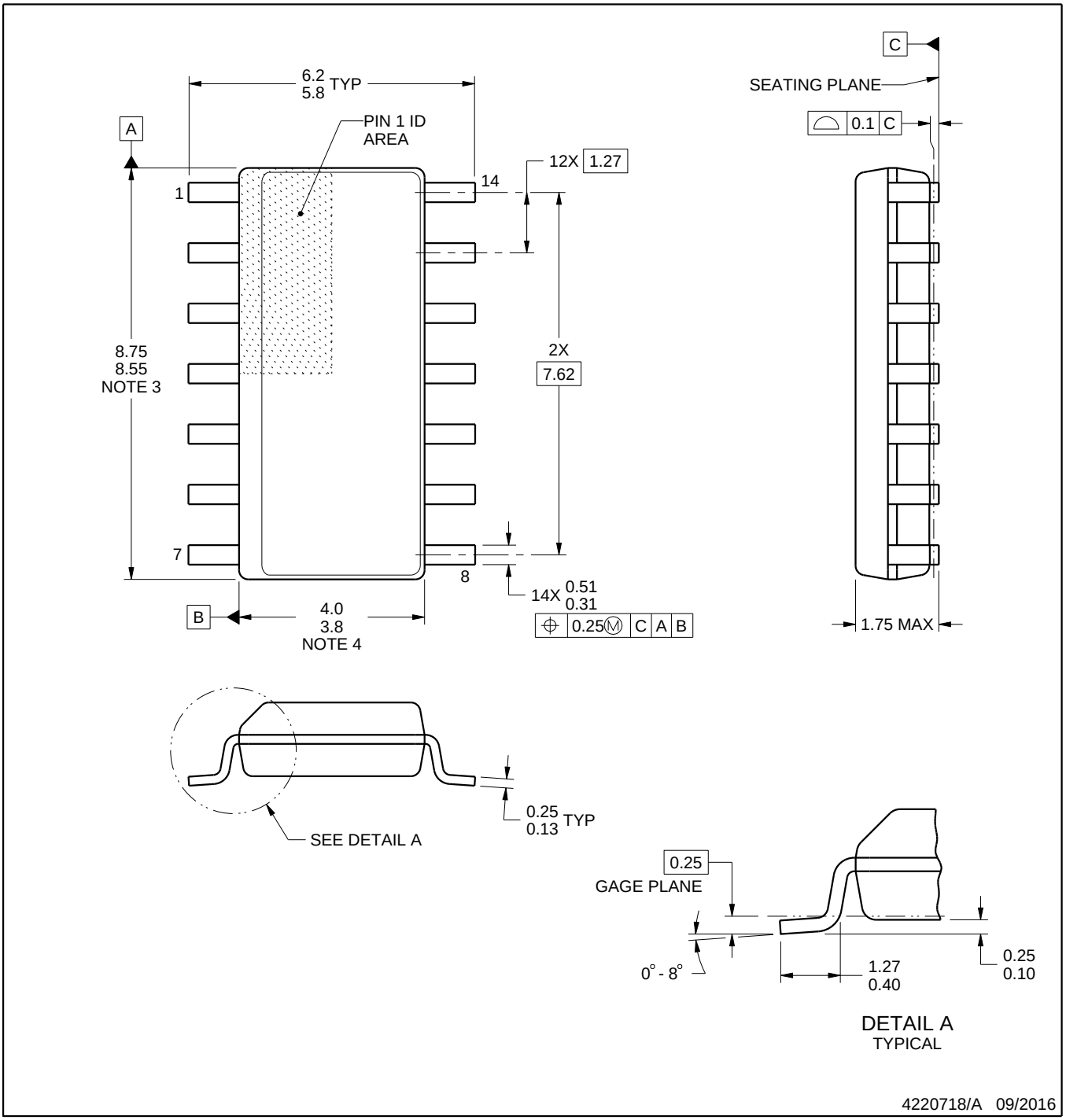


PACKAGE OUTLINE

D0014A

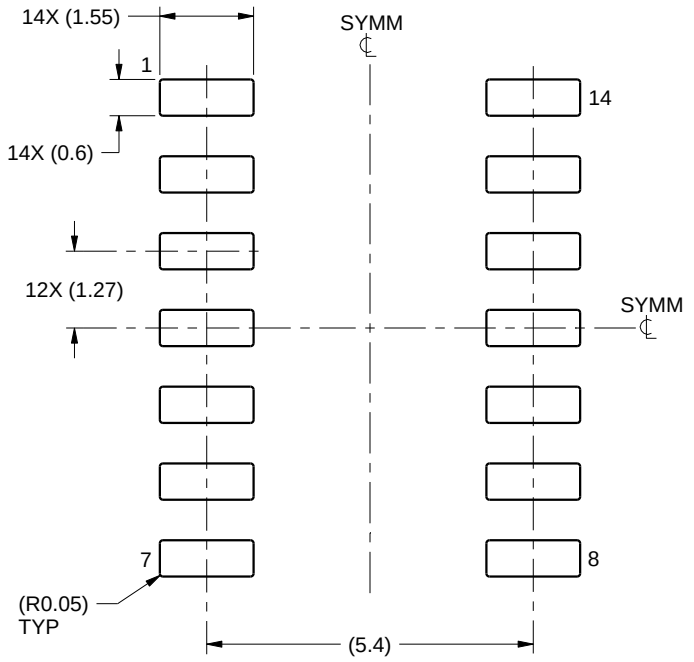
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

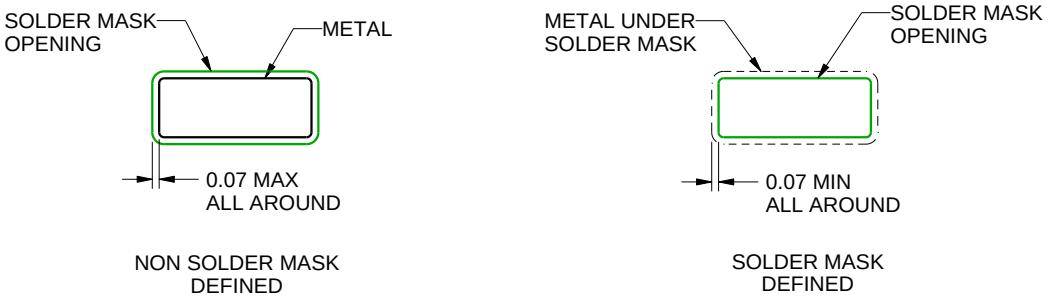


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

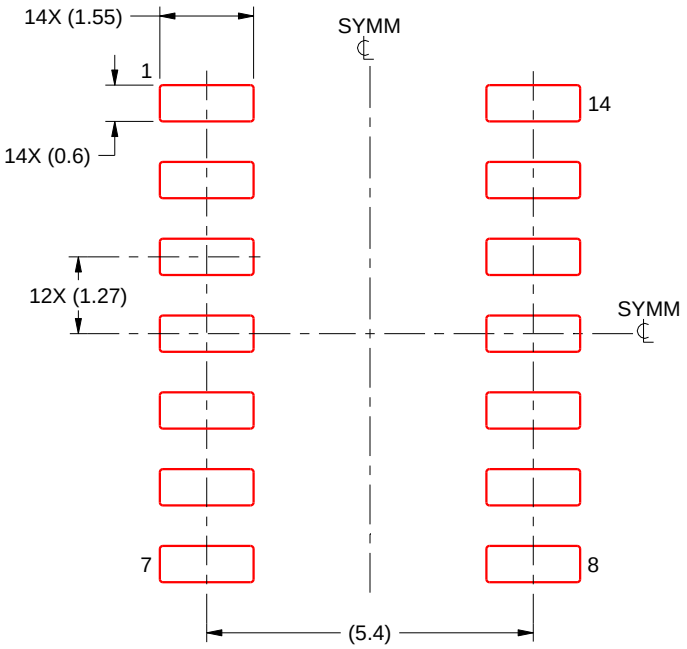
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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