

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

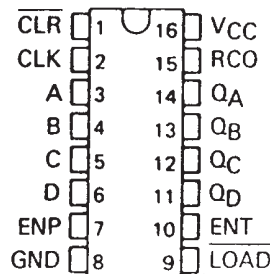
SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74' . . . N PACKAGE
SERIES 74LS', 74S' . . . D OR N PACKAGE

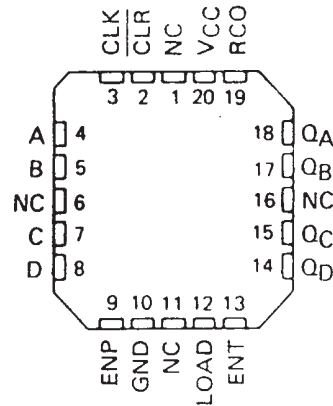
(TOP VIEW)



NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

TYPE	TYPICAL PROPAGATION	TYPICAL	TYPICAL
	TIME, CLOCK TO Q OUTPUT	MAXIMUM CLOCK FREQUENCY	POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1988, Texas Instruments Incorporated

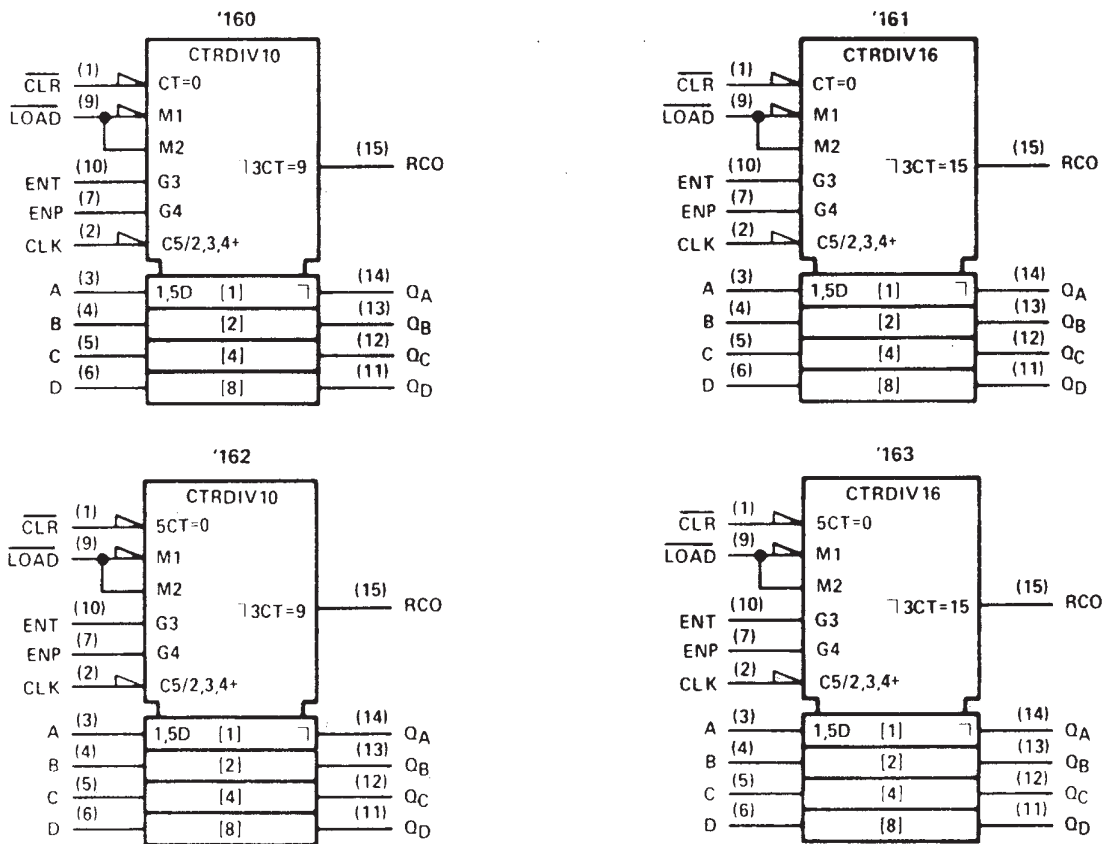
SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols[†]



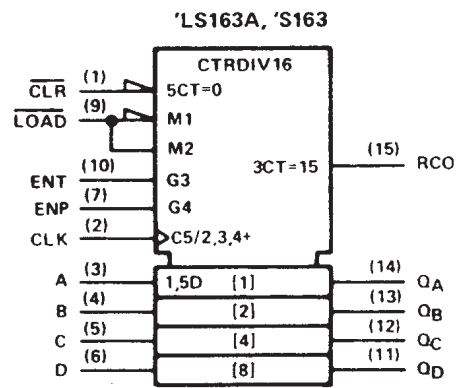
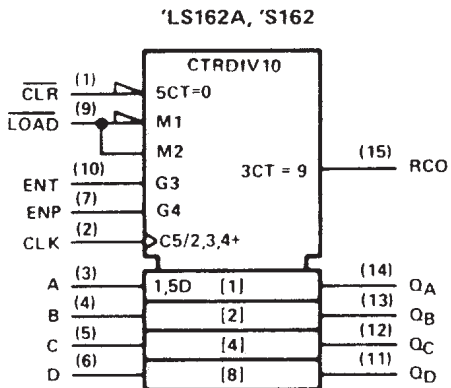
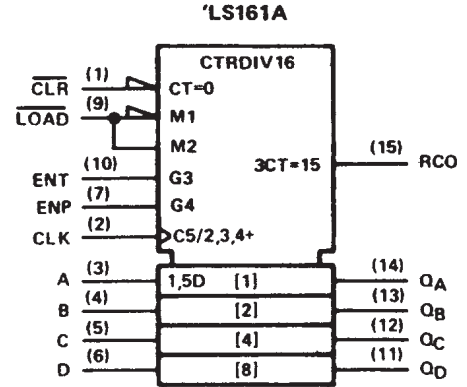
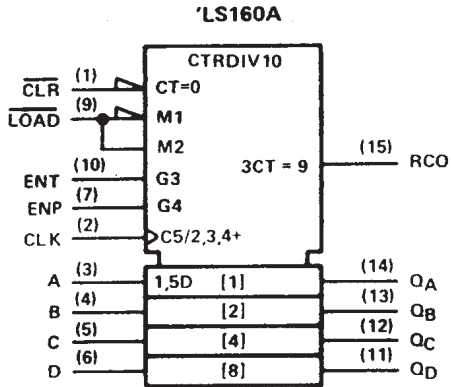
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic symbols (continued)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

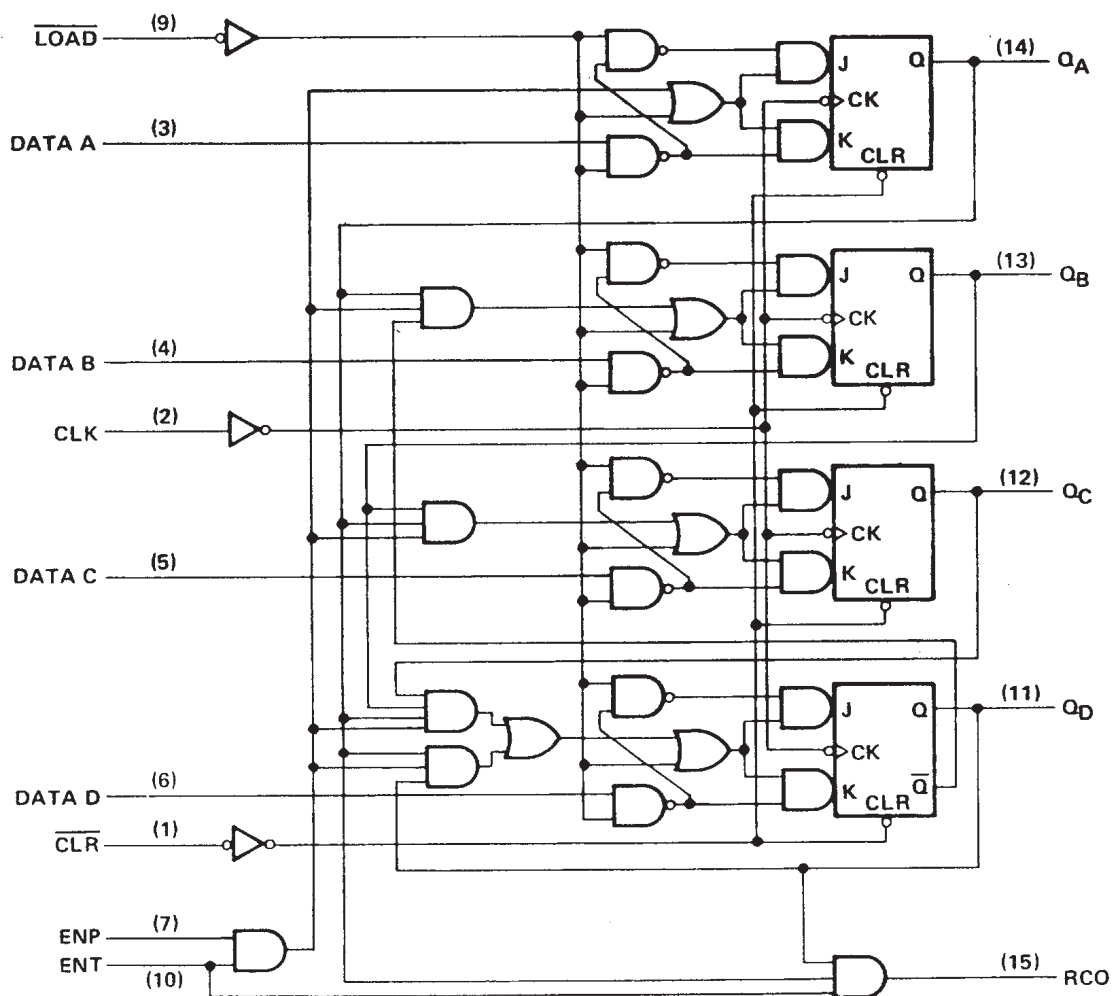
SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic diagram (positive logic)

SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



Pin numbers shown are for D, J, N, and W packages

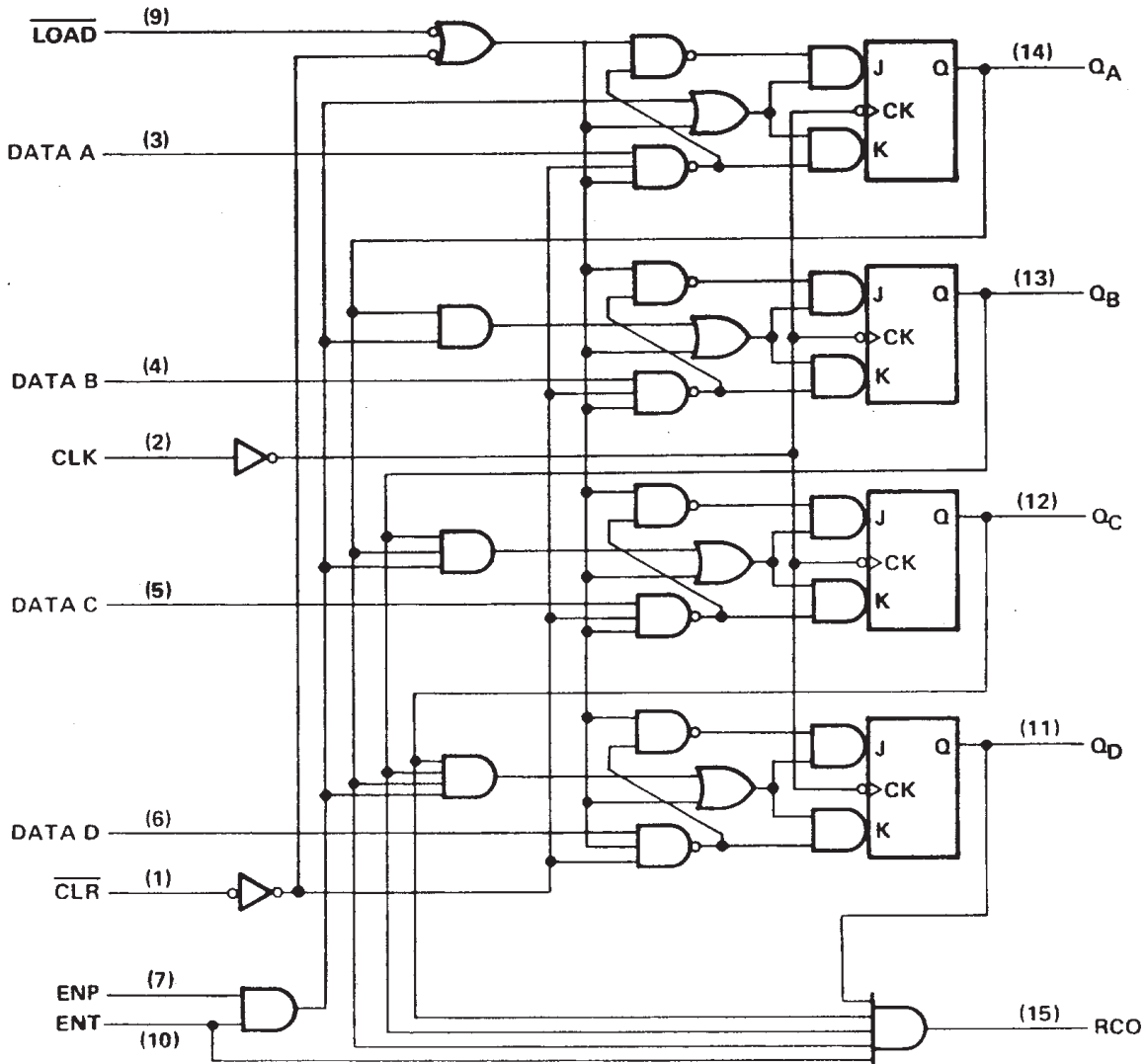


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)

SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



Pin numbers shown are for D, J, N, and W packages.

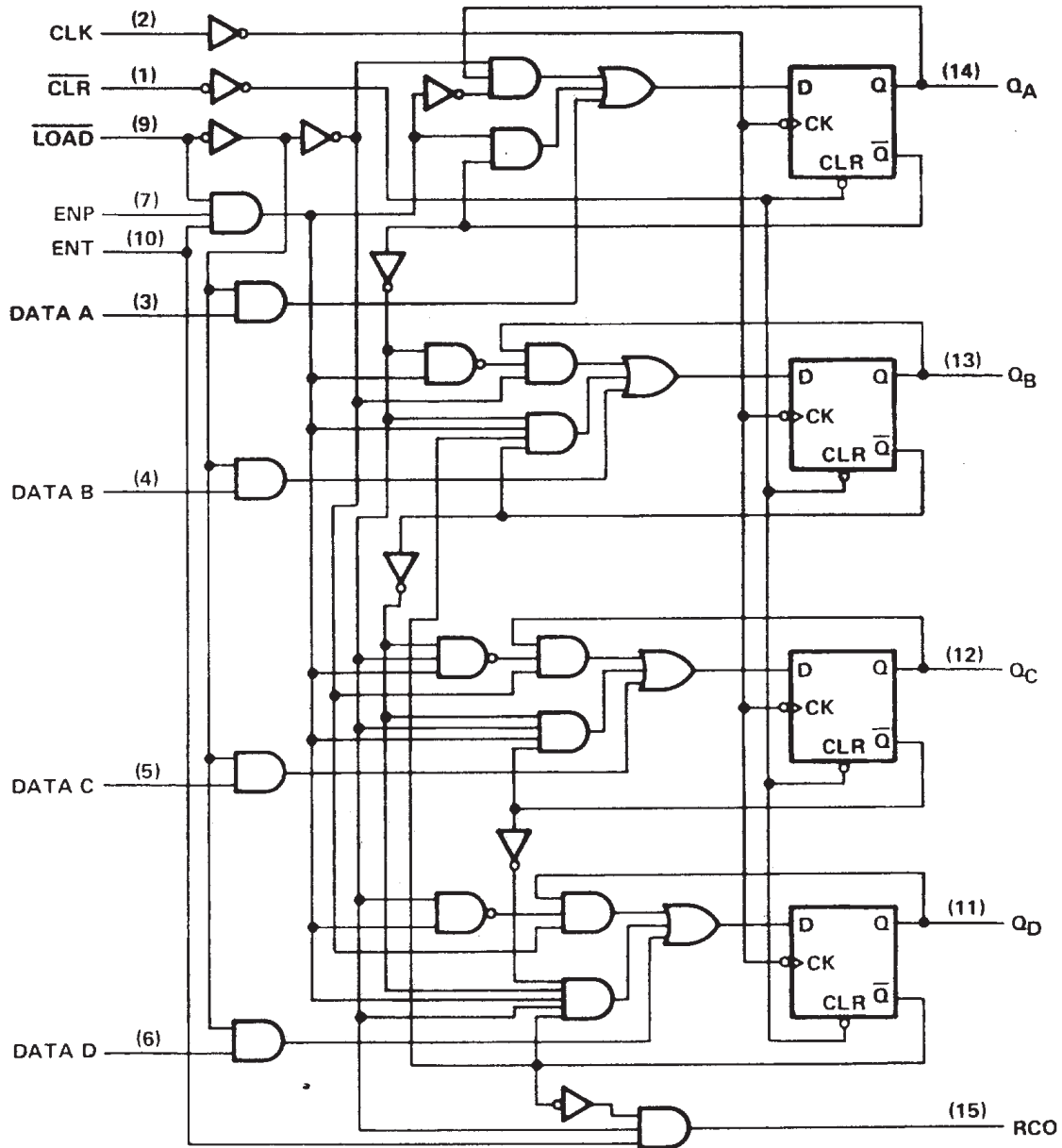
SN54LS160A, SN54LS162A, SN74LS160A, SN74LS162A SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic diagram (positive logic)

SN54LS160A, SN74LS160A SYNCHRONOUS DECADE COUNTERS

SN54LS162A, SN74LS162A synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163A, SN74LS163A binary counters at right.



Pin numbers shown are for D, J, N, and W packages.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

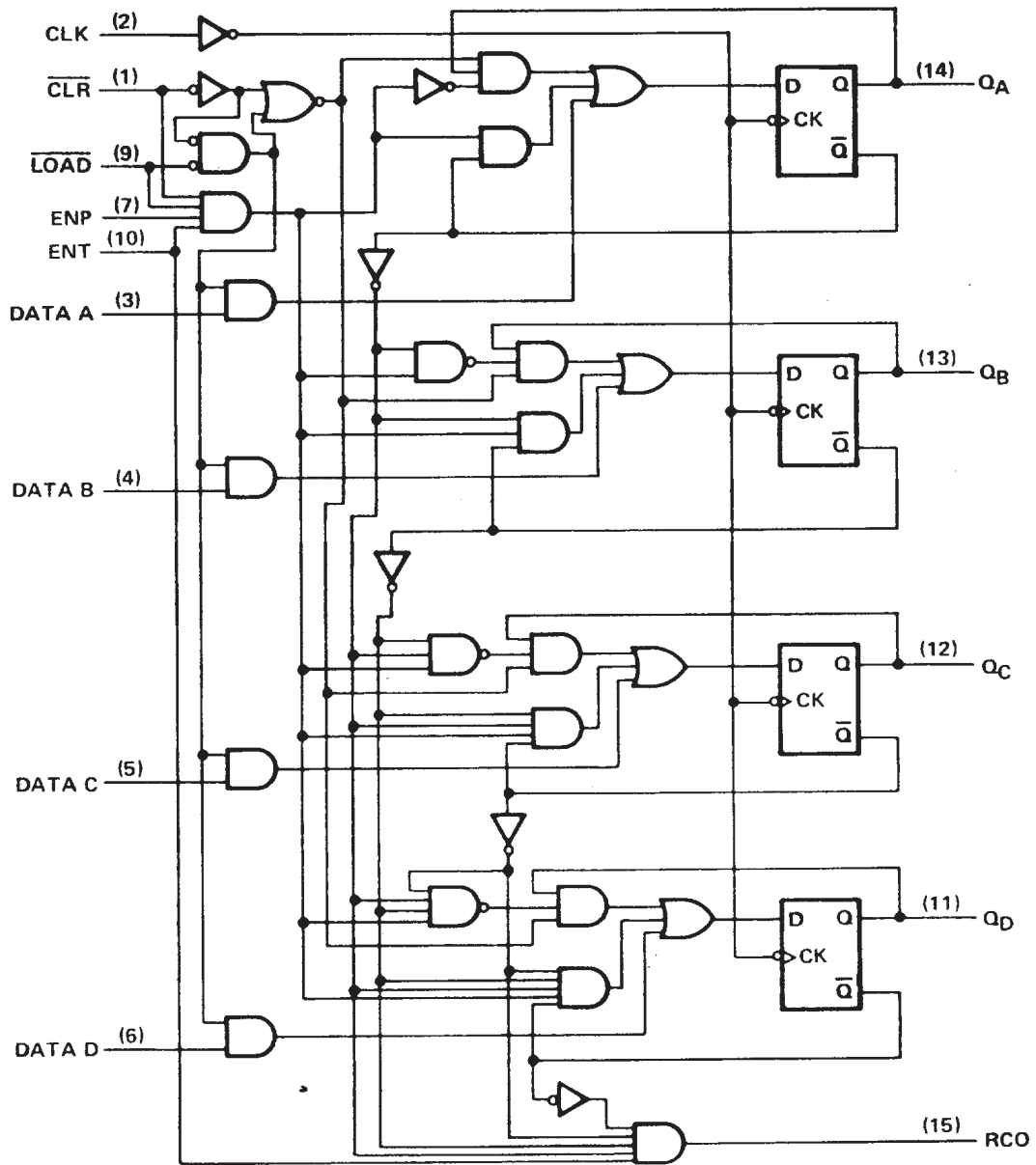
SN54LS161A, SN54LS163A, SN74LS161A, SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic diagram (positive logic)

SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



Pin numbers shown are for D, J, N, and W packages.

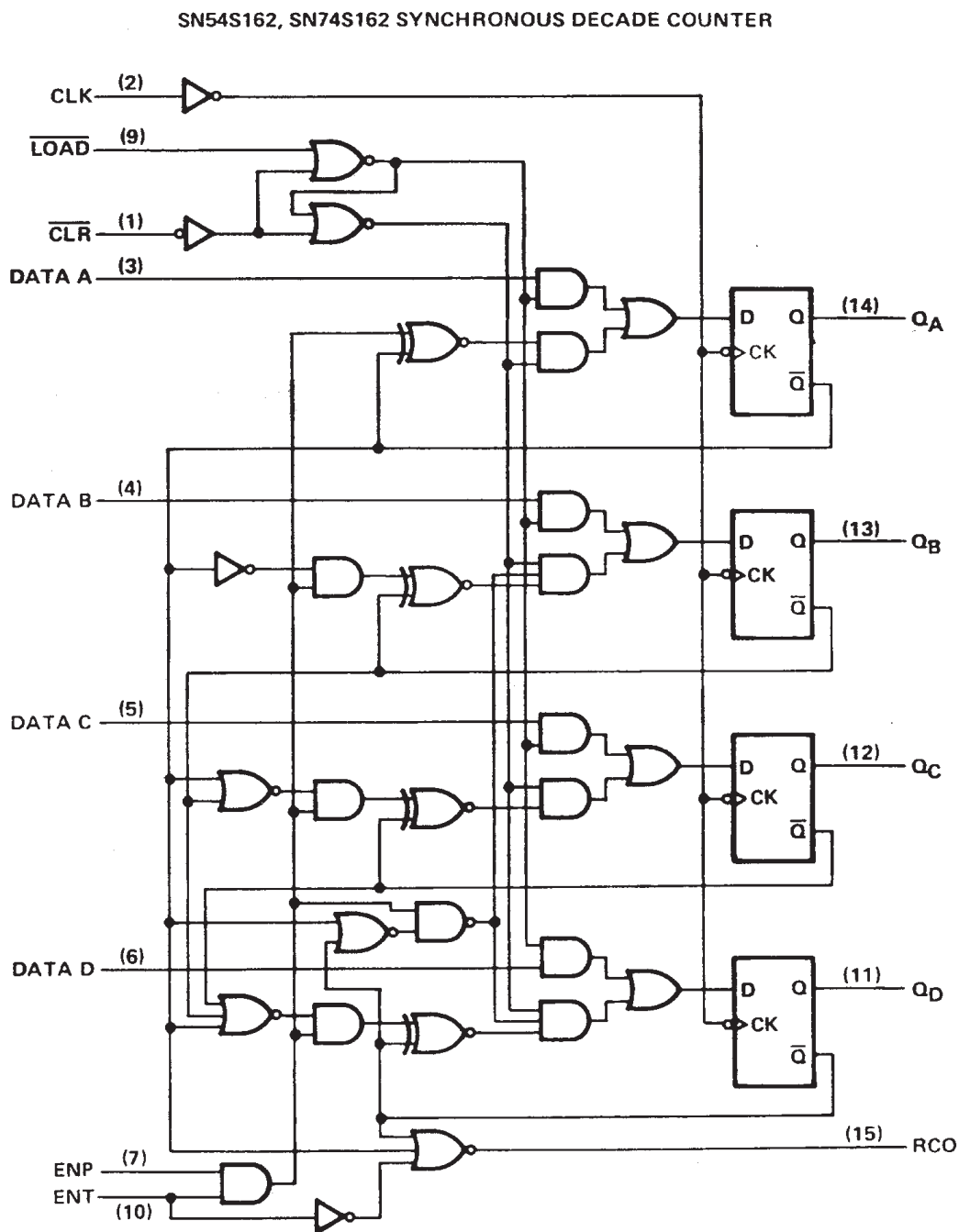


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54S162, SN74S162 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic diagram (positive logic)



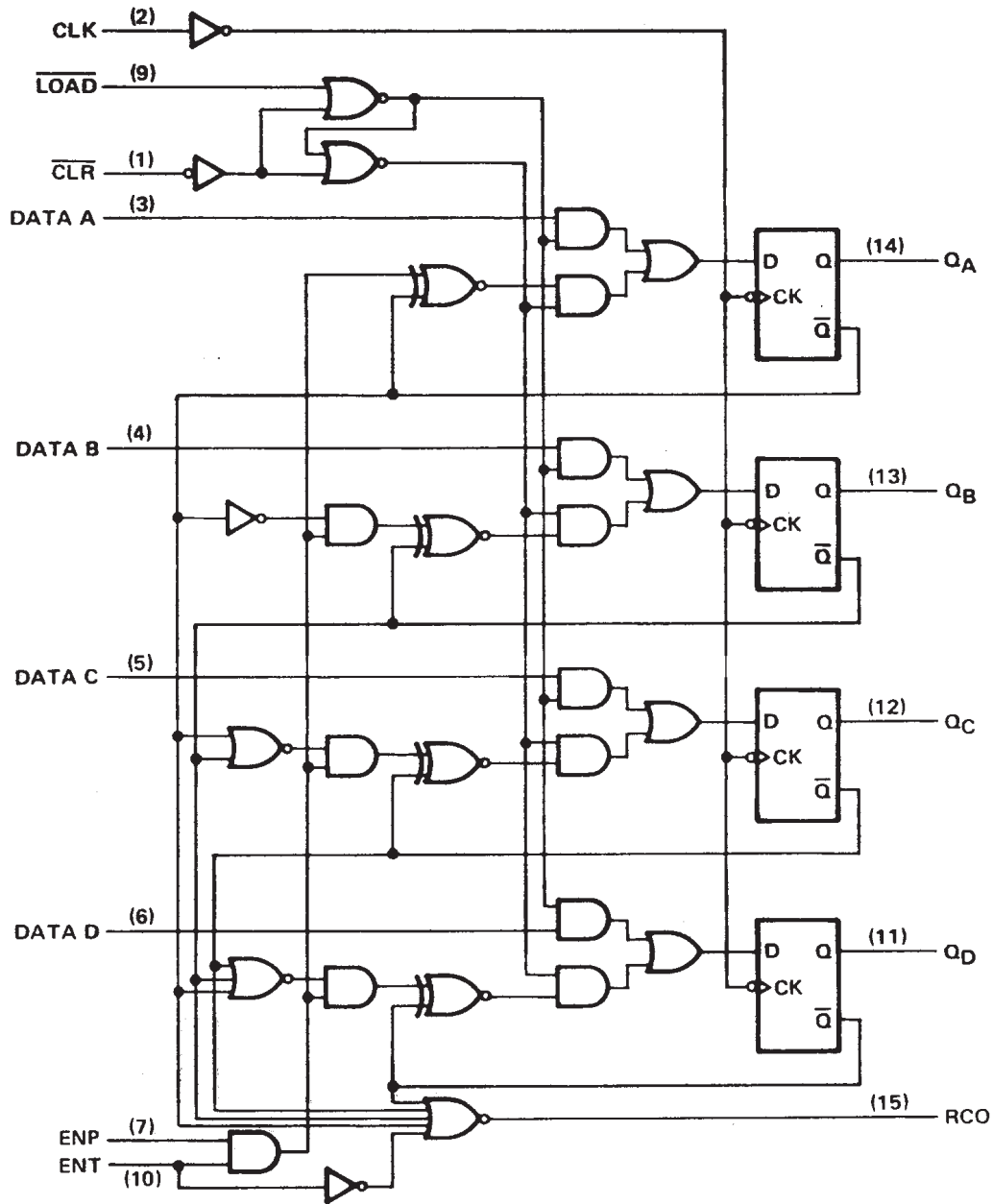
Pin numbers shown are for D, J, N, and W packages.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)

SN54S163, SN74S163 SYNCHRONOUS DECADE COUNTER



Pin numbers shown are for D, J, N, and W packages.

SN54160, SN54162, SN54LS160A, SN54LS162A, SN54S162,
 SN74160, SN74162, SN74LS160A, SN74LS162A, SN74S162
SYNCHRONOUS 4-BIT COUNTERS

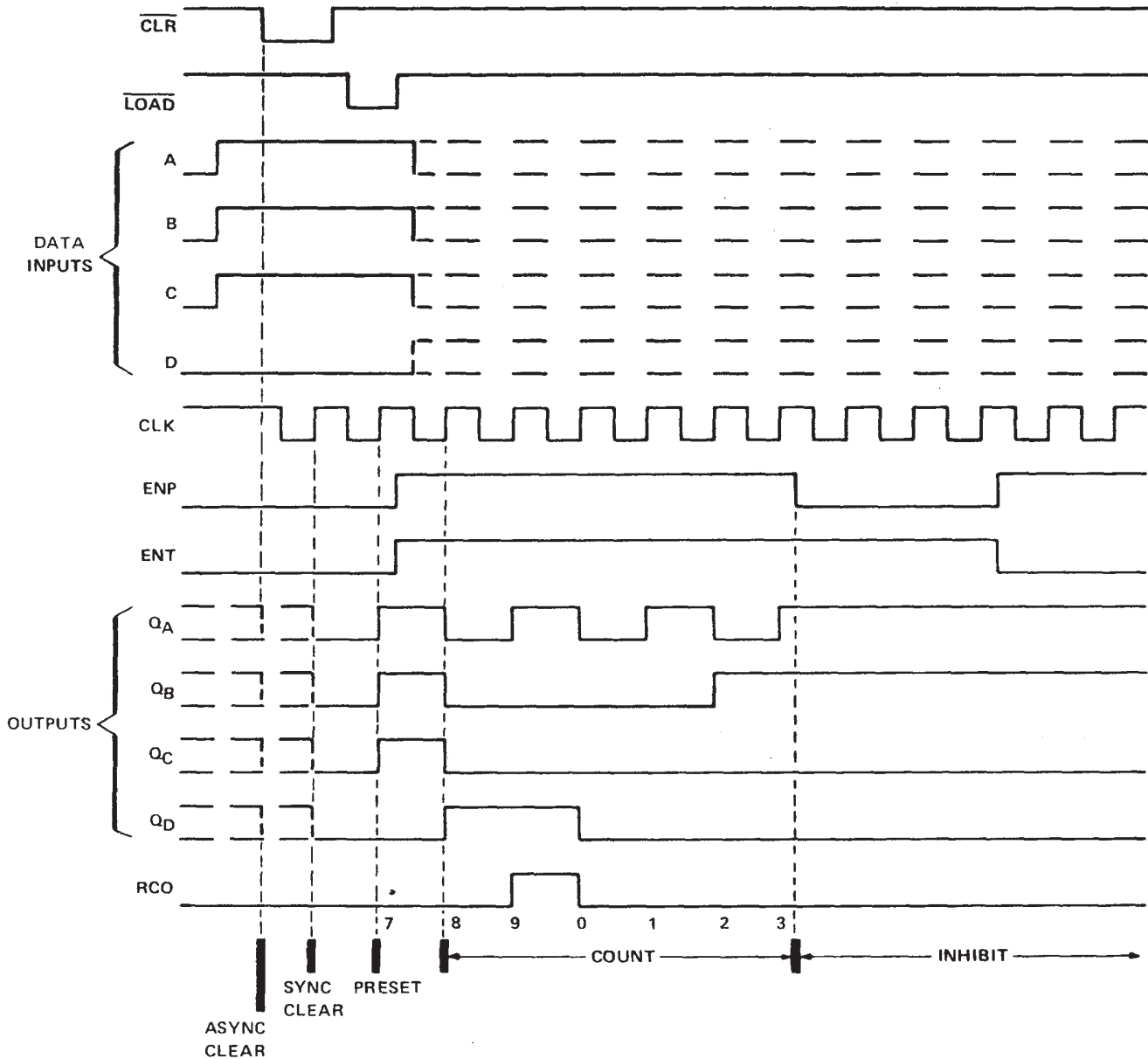
SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A, and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



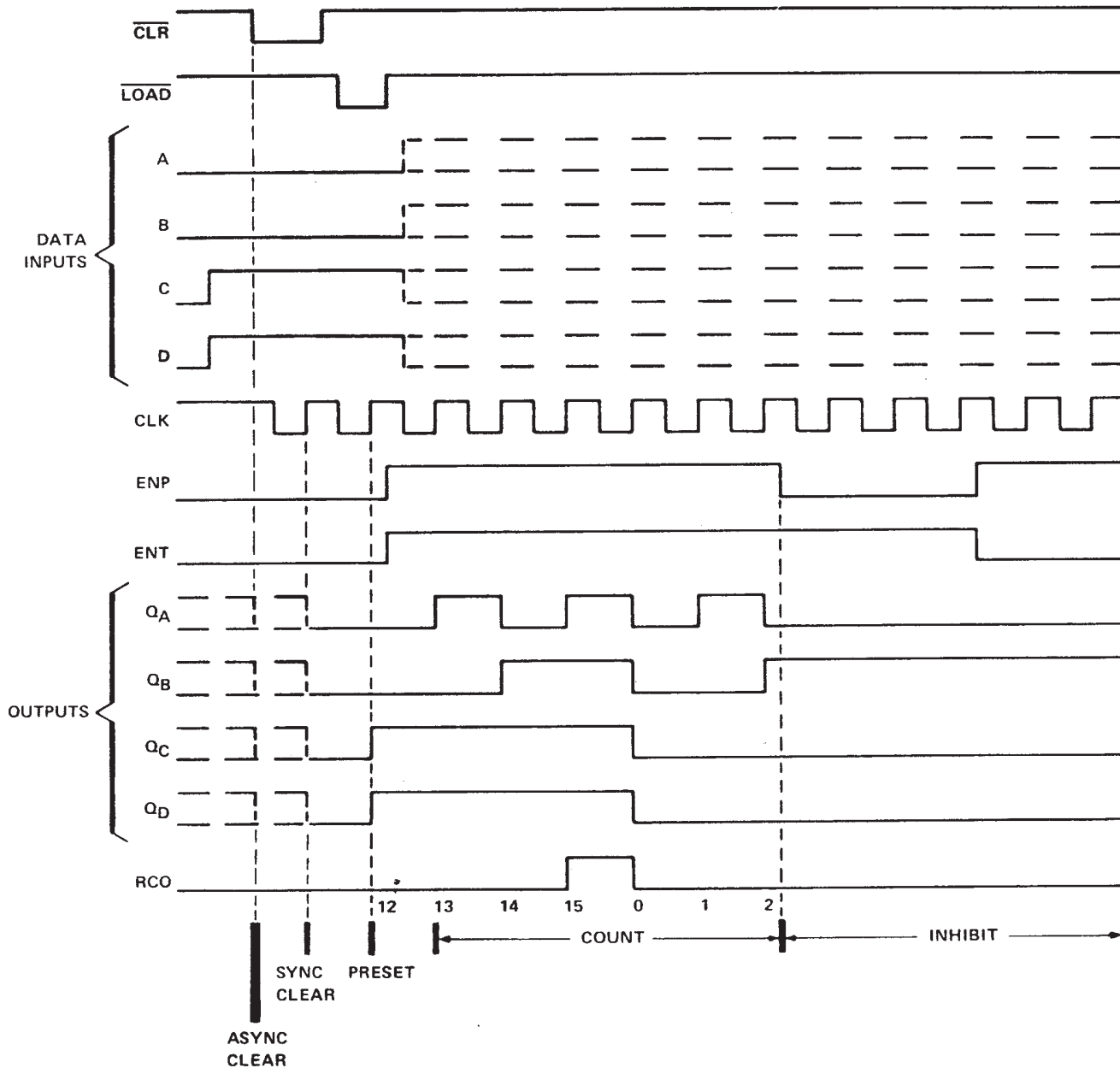
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

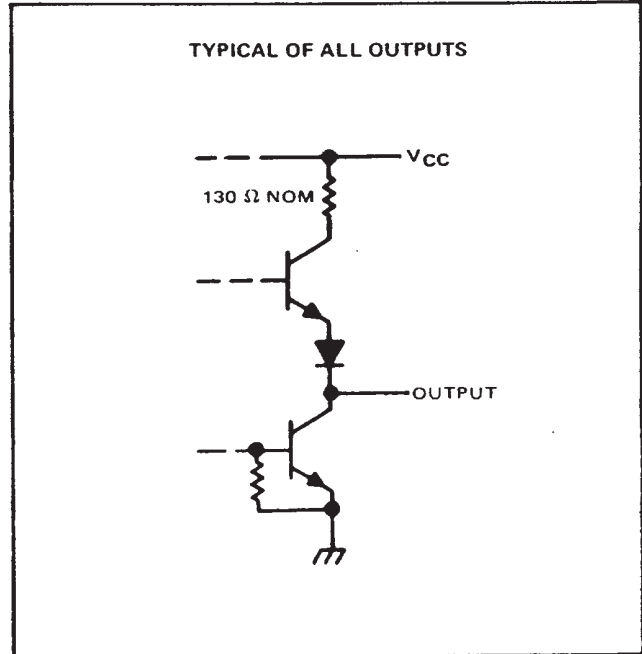
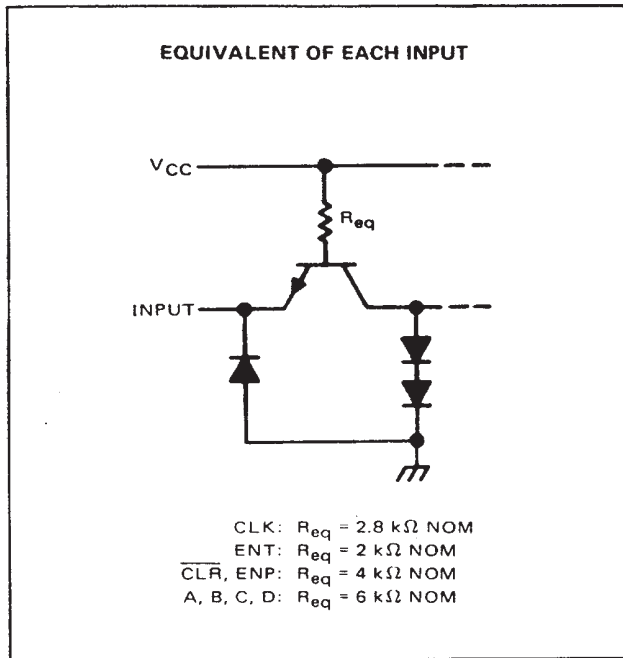
1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

	SN54160, SN54161			SN74160, SN74161			UNIT
	SN54162, SN54163			SN74162, SN74163			
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	25			25			ns
Width of clear pulse, $t_{w(clear)}$	20			20			ns
Setup time, t_{SU} (see Figures 1 and 2)	Data inputs A, B, C, D	20		20			ns
	ENP	20		20			
	LOAD	25		25			
	CLR †	20		20			
Hold time at any input, t_h	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

† This applies only for '162 and '163, which have synchronous clear inputs.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54160, SN54161		SN74160, SN74161		UNIT
			SN54162, SN54163	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage		0.8		0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-1.5		-1.5		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μA	2.4	3.4	2.4	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4	0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1		1		mA
I _{IH}	High-level input current	CLK or ENT	80		80		μA
		Other inputs	40		40		
I _{IL}	Low-level input current	CLK or ENT	-3.2		-3.2		mA
		Other inputs	-1.6		-1.6		
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-20	-57	-18	-57	mA
I _{CCH}	Supply current, all outputs high	V _{CC} = MAX, See Note 3	59	85	59	94	mA
I _{CCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4	63	91	63	101	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 400 Ω, See Figures 1 and 2 and Note 5	25	32		MHz
t _{PLH}	CLK	RCO			23	35	ns
t _{PHL}		Q			23	35	
t _{PLH}	CLK (LOAD input high)	Any			13	20	ns
t _{PHL}		Q			15	23	
t _{PLH}	CLK (LOAD input low)	Any			17	25	ns
t _{PHL}		Q			19	29	
t _{PLH}	ENT	RCO			11	16	ns
t _{PHL}		Q			11	16	
t _{PHL}	CLR	Any Q		26	38	ns	

¶ f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

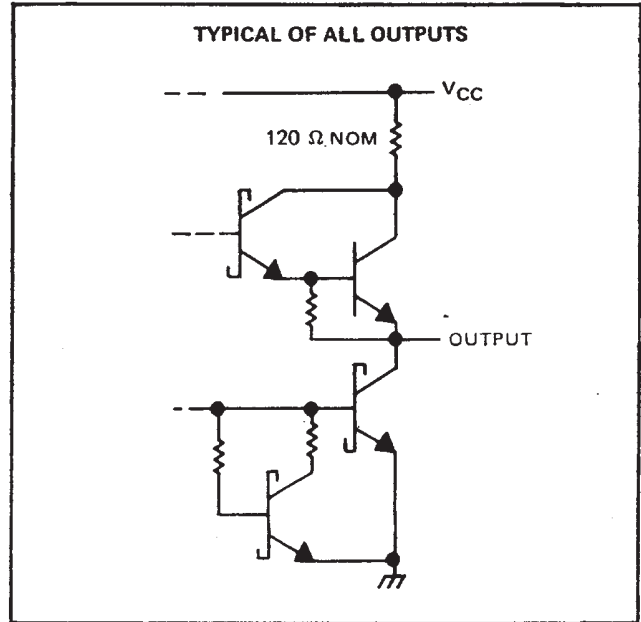
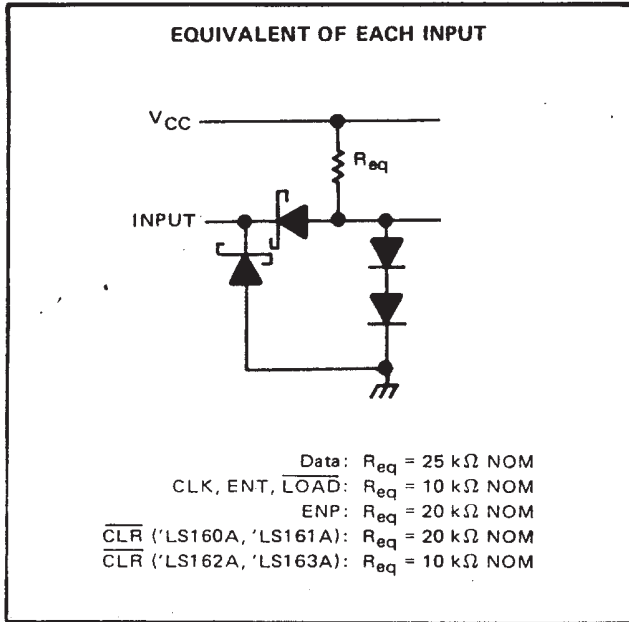
NOTE 5: Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.



SN54LS160 THRU SN54LS163A, SN74LS160 THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-400			-400	μA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
$t_{w(\text{clock})}$	Width of clock pulse	25			25			ns
$t_{w(\text{clear})}$	Width of clear pulse	20			20			ns
t_{su}	Setup time, (see Figures 1 and 2)	Data inputs A, B, C, D	20		20			ns
		ENP or ENT	20		20			
		$\overline{\text{LOAD}}$	20		20			
		$\overline{\text{LOAD}}$ inactive state	20		20			
		$\overline{\text{CLR}}^\dagger$	20		20			
t_h	Hold time at any input	3			3			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

[†] This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LS160 THRU SN54LS163A, SN74LS160 THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max} , I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max} , I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 8 mA					0.35	0.5	
I _I	Input current at maximum input voltage	Data or ENP						0.1	mA
		LOAD, CLK, or ENT	V _{CC} = MAX, V _I = 7 V					0.2	
		CLR ('LS160A, 'LS161A)						0.1	
		CLR ('LS162A, 'LS163A)						0.2	
I _{IH}	High-level input current	Data or ENP		V _{CC} = MAX, V _I = 2.7 V					20
		LOAD, CLK, or ENT						40	
		CLR ('LS160A, 'LS161A)						20	
		CLR ('LS162A, 'LS163A)						40	
I _{IL}	Low-level input current	Data or ENP	V _{CC} = MAX, V _I = 0.4 V					-0.4	mA
		LOAD, CLK, or ENT						-0.8	
		CLR ('LS160A, 'LS161A)						-0.4	
		CLR ('LS162A, 'LS163A)						-0.8	
I _{OS}	Short-circuit output current §	V _{CC} = MAX	-20	-100		-20	-100		mA
I _{CCH}	Supply current, all outputs high	V _{CC} = MAX, See Note 3		18	31		18	31	mA
I _{CCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4		19	32		19	32	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 2 kΩ, See figures 1 and 2 and Note 8	25	32		MHz
t _{PLH}	CLK	RCO			20	35	ns
t _{PHL}		Any Q			18	35	
t _{PLH}	CLK (LOAD input high)	Q			13	24	ns
t _{PHL}		Any Q			18	27	
t _{PLH}	CLK (LOAD input low)	Q			13	24	ns
t _{PHL}		Any Q			18	27	
t _{PLH}	ENT	RCO			9	14	ns
t _{PHL}		Any Q			9	14	
t _{PHL}	CLR	Any Q			20	28	ns

¶ f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

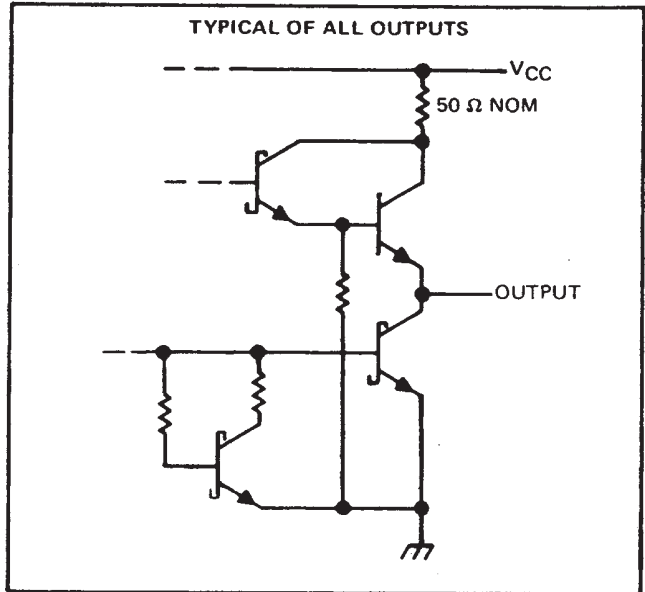
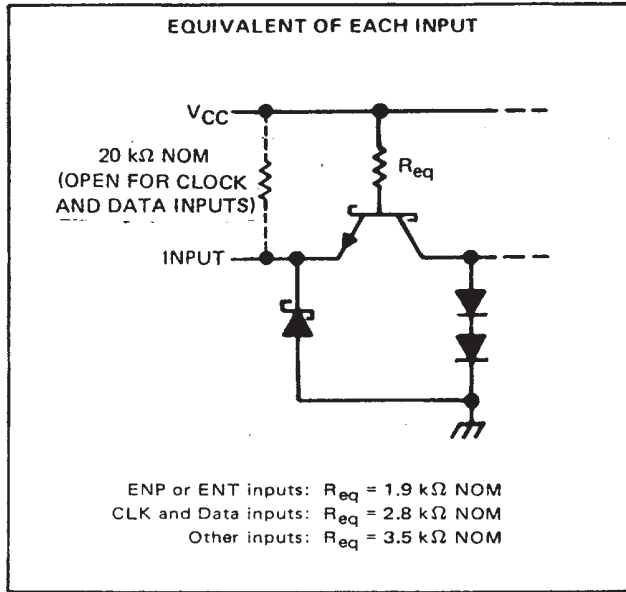
NOTE 8: Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.



SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10)	-55°C to 125°C
SN74S162, SN74S163	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54S162, SN54S163			SN74S162, SN74S163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			1	mA
Low-level output current, I_{OL}			20			20	mA
Clock frequency, f_{clock}	0		40	0		40	MHz
Width of clock pulse, $t_w(\text{clock})$ (high or low)	10			10			ns
Width of clear pulse, $t_w(\text{clear})$	10			10			ns
Setup time, t_{su} (see Figure 4)	Data inputs, A, B, C, D	4		4			ns
	ENP or ENT	12		12			
	LOAD	14		14			
	CLR	14		14			
	CLR inactive-state	12		12			
Release time, $t_{release}$ (see Figure 4)	ENP or ENT		4			4	ns
	Data inputs A, B, C, D	3		3			ns
Hold time, t_h (see Figure 4)	LOAD	0		0			
	CLR	0		0			
Operating free-air temperature, T_A (see Note 10)	55		125	0		70	C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
 2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
 10. An SN54S162 or SN54S163 in the W package operating at free air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S162 SN54S163		SN74S162 SN74S163		UNIT
		MIN	TYP‡	MAX	MIN	
V _{IH} High-level input voltage		2			2	V
V _{IL} Low-level input voltage				0.8		0.8 V
V _{ICP} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2		-1.2 V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4 V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA		0.5		0.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1		1	mA
I _{IH} High-level input current	CLK and data inputs		50		50	μA
	Other inputs		-10	-200	-10	
I _{IL} Low-level input current	ENT		-4		-4	mA
	Other inputs		2		2	
I _{OS} Short-circuit output current §	V _{CC} = MAX	-40	-100	-40	-100	mA
I _{CC} Supply current	V _{CC} = MAX		95	160	95	160 mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 280 Ω, See Figures 1, 3, and 4	40	70		MHz
t _{PLH}	CLK	RCO			14	25	ns
t _{PHL}					17	25	
t _{PLH}	CLK	Any Q			8	15	ns
t _{PHL}					10	15	
t _{PLH}	ENT	RCO			10	15	ns
t _{PHL}				10	15		

¶ f_{max} ≡ maximum clock frequency

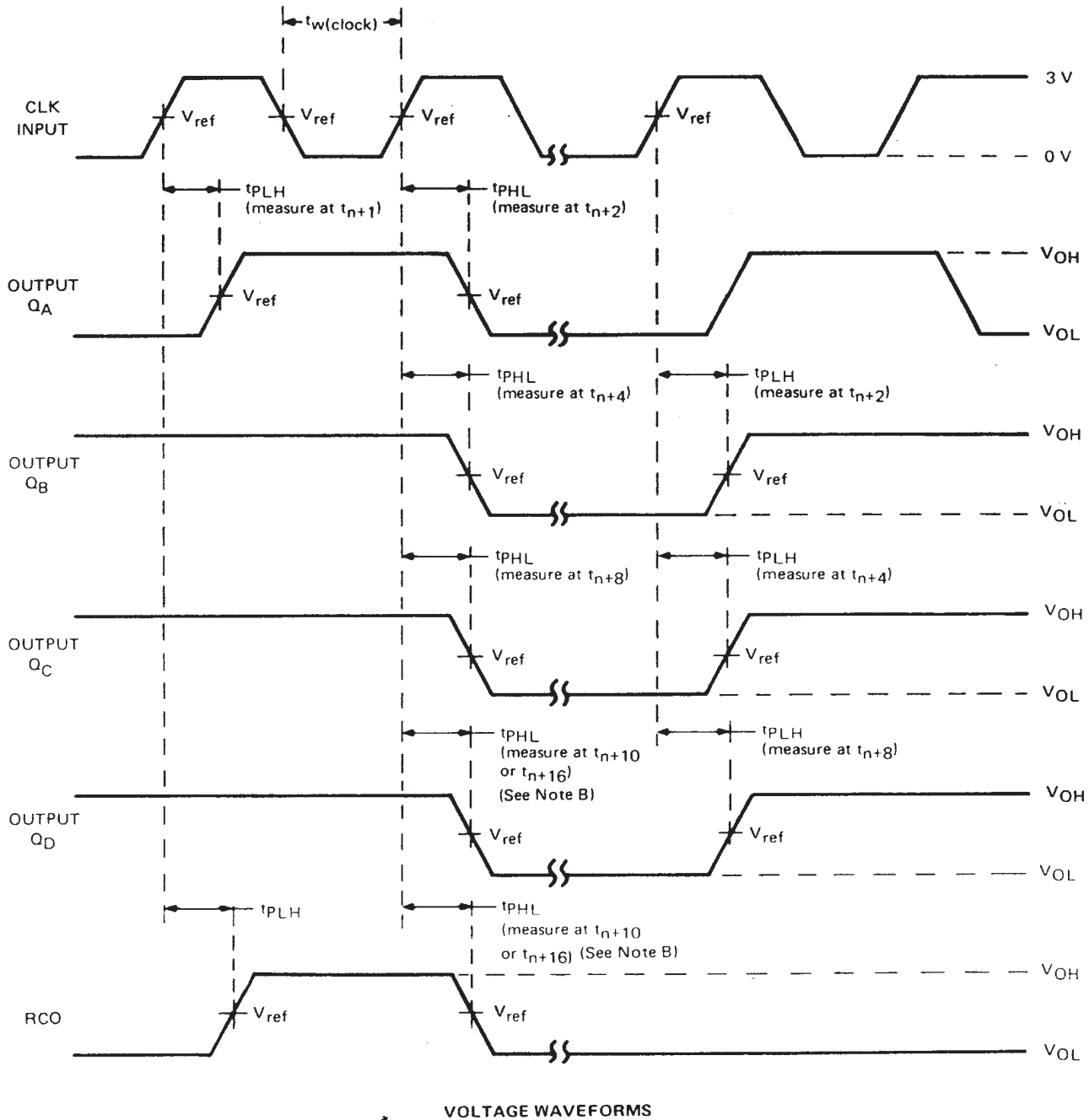
t_{PLH} ≡ propagation delay time, low to high level output

t_{PHL} ≡ propagation delay time, high to low level output

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

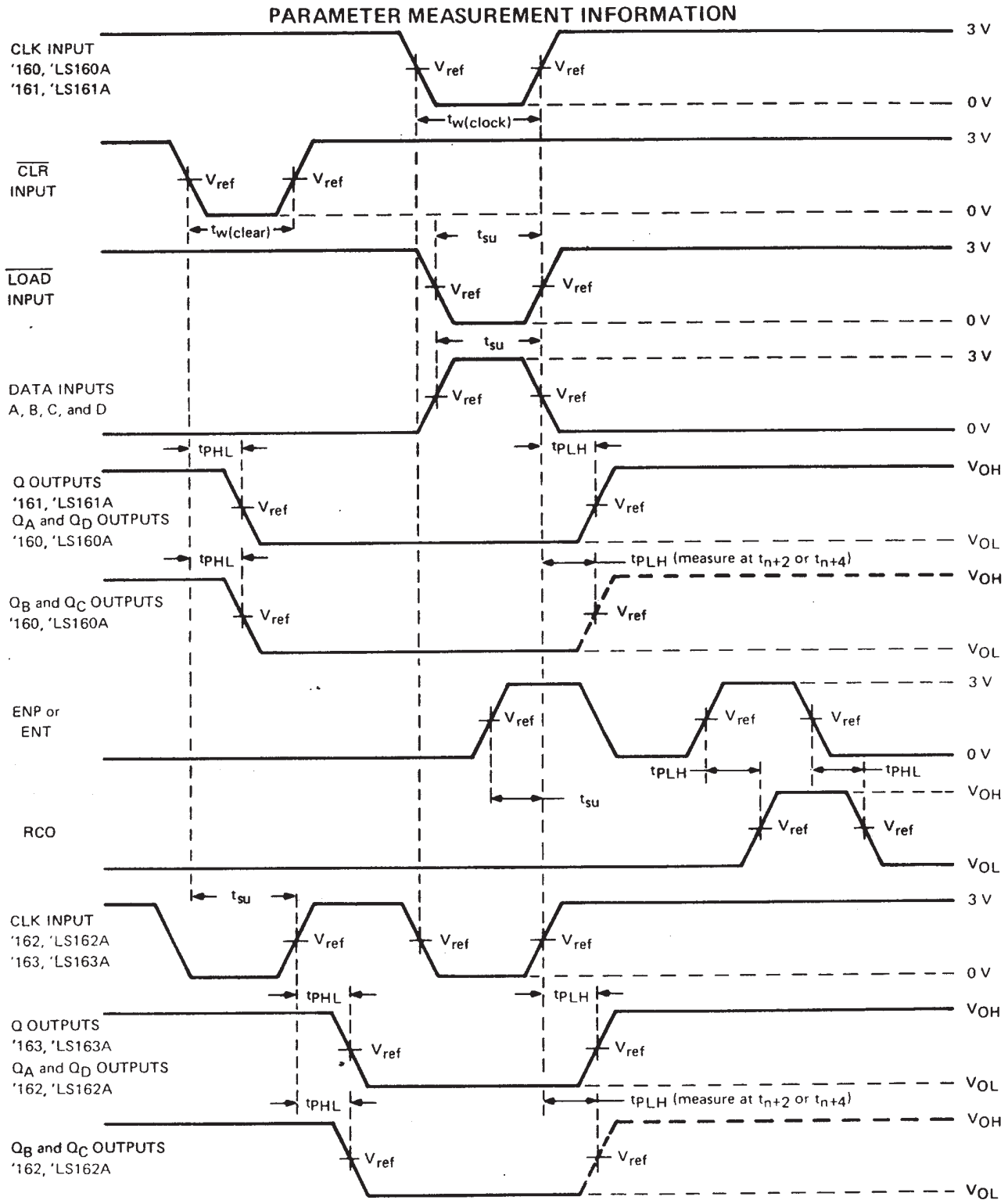
- NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{\text{out}} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max} .
- B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.
- C. For '160 thru '163, 'S162, and 'S163, $V_{\text{ref}} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{\text{ref}} = 1.3$ V.

FIGURE 1—SWITCHING TIMES



SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SYNCHRONOUS 4-BIT COUNTERS

SDLS060 - OCTOBER 1976 - REVISED MARCH 1988



VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. Enable P and enable T setup times are measured at t_{n+0} .
- C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.1$ V.

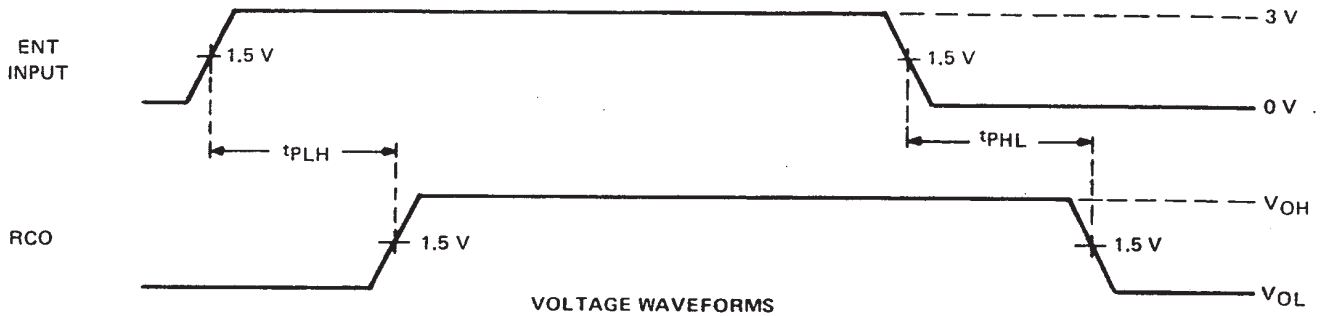
FIGURE 2—SWITCHING TIMES



SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

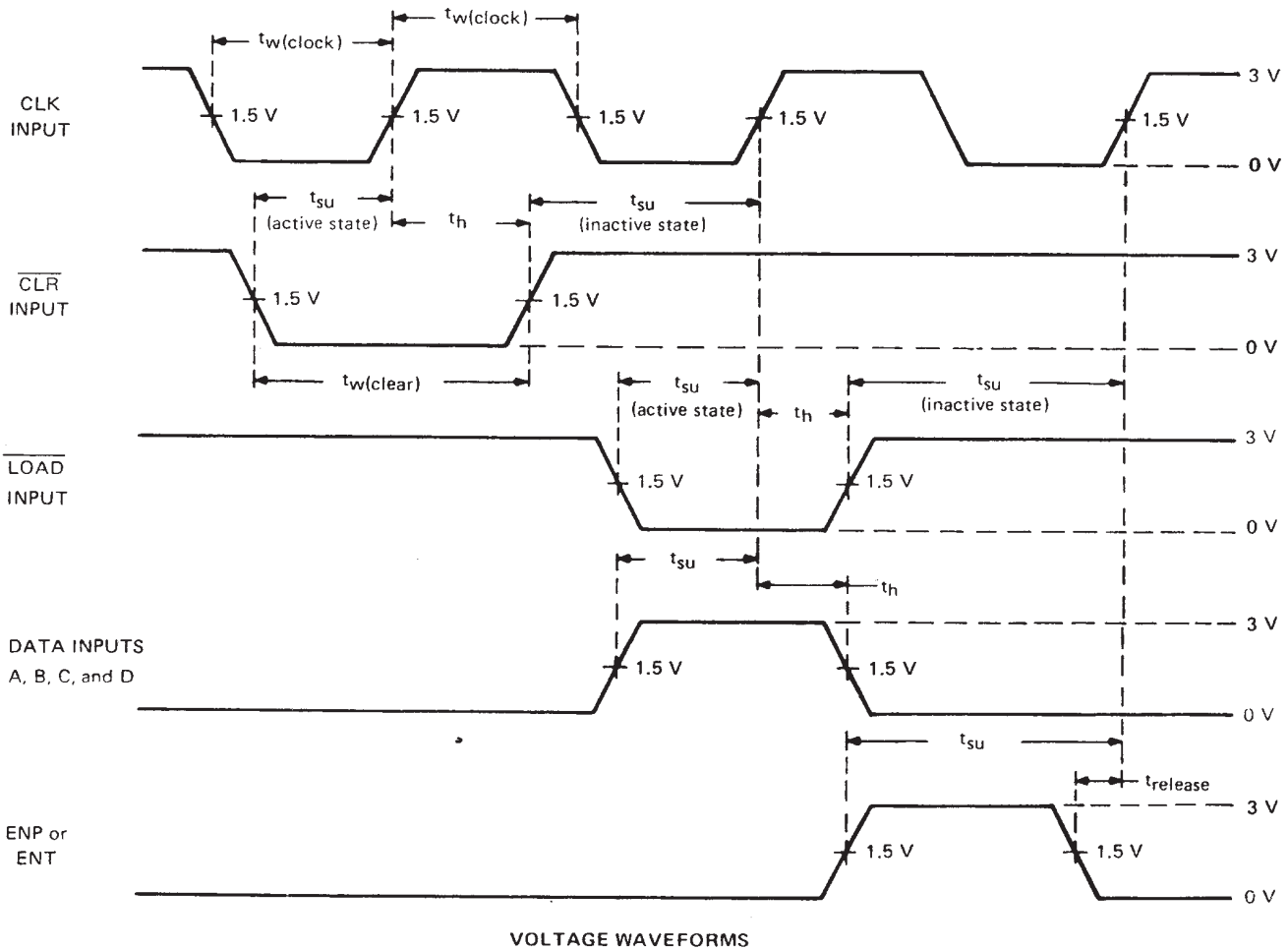
SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \approx 2.5$ ns, $t_f \approx 2.5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50 \Omega$.
B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3—PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



- NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r \approx 2.5$ ns, $t_f \approx 2.5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50 \Omega$.

FIGURE 4—PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

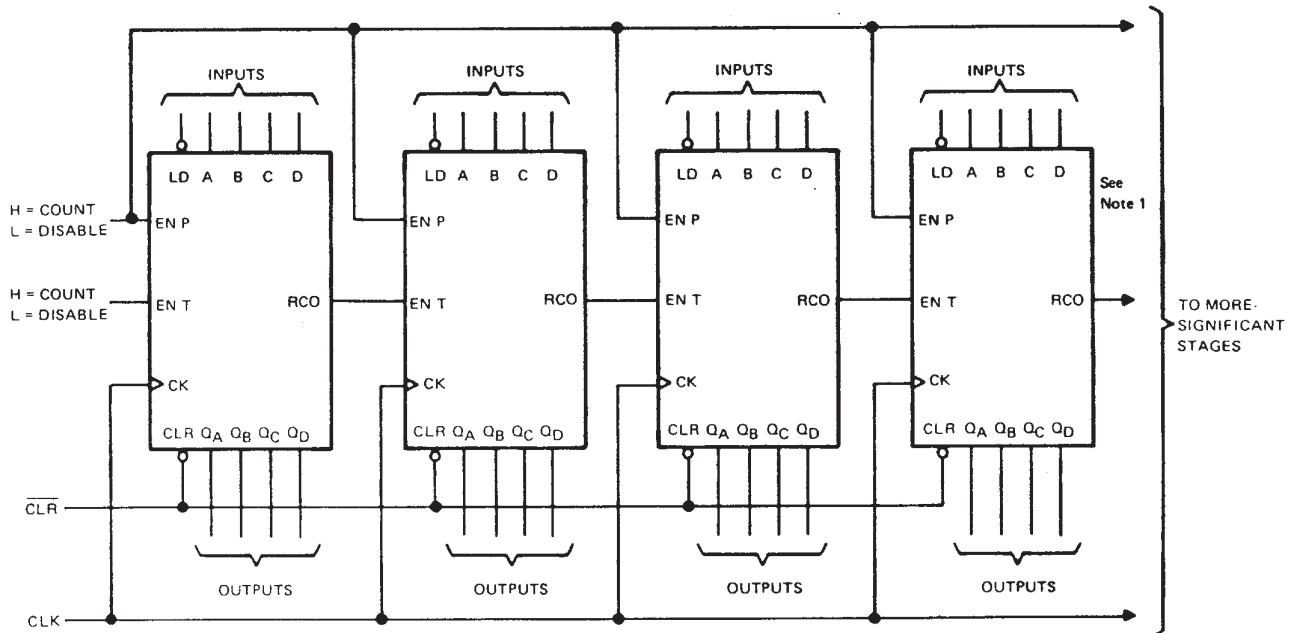
SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162,
 SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
 SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

TYPICAL APPLICATION DATA

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A, or 'S163 will count in binary. When additional stages are added the f_{MAX} decreases in Figure 1, but remains unchanged in Figure 2.

N-BIT SYNCHRONOUS COUNTERS



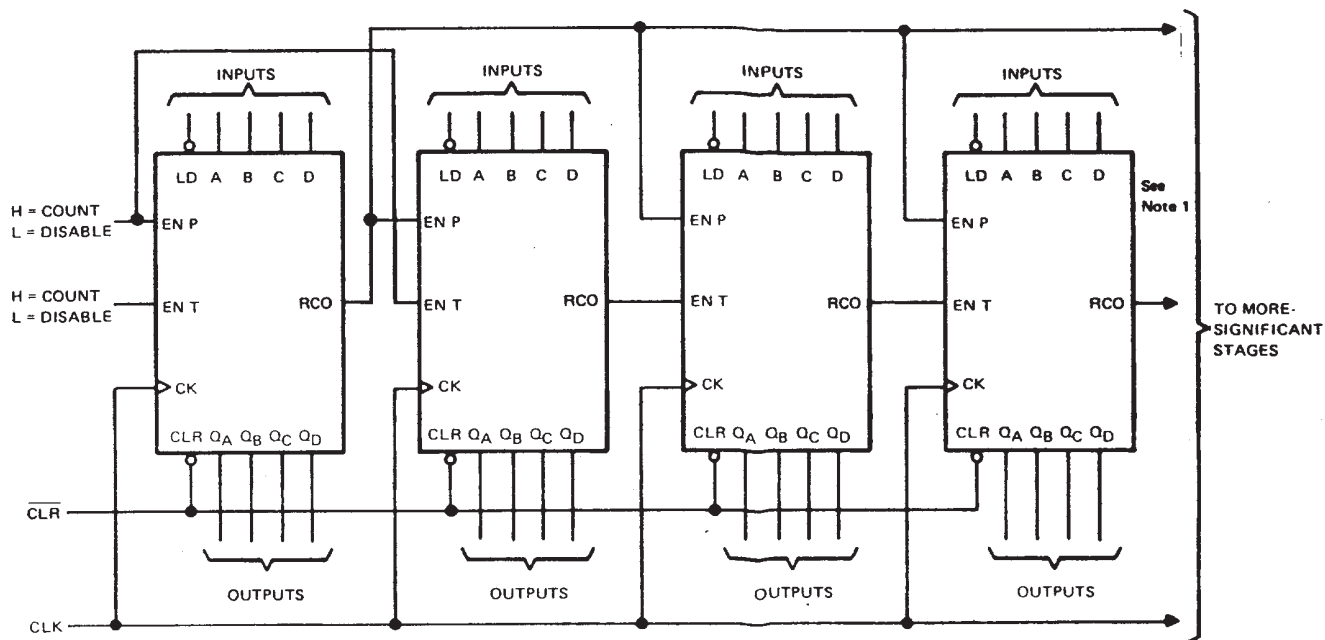
$$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH}) (N-2) + (\text{ENT } t_{SU})$$

FIGURE 1

**SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS**

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

TYPICAL APPLICATION DATA



$$f_{MAX} = 1 / (\text{CLK to RCO } t_{PLH}) + (ENP \ t_{su})$$

FIGURE 2



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

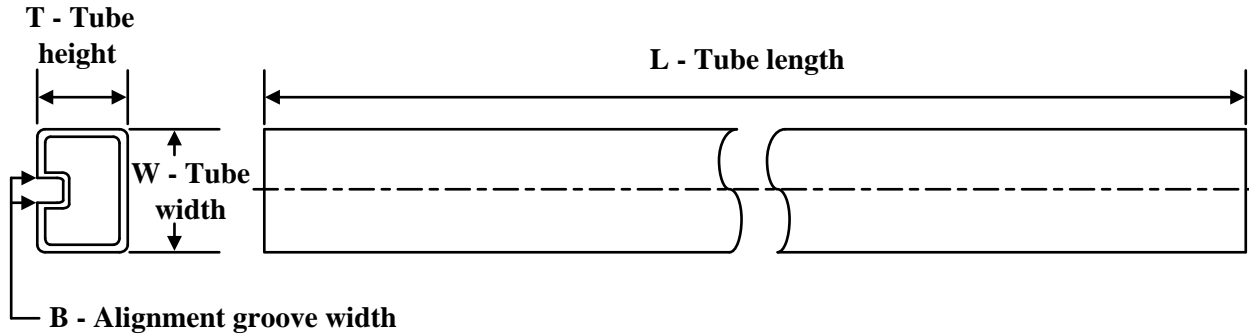
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS161ANSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS163ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS163ANSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS161ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS161ANSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74LS163ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS163ANSR	SOP	NS	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9754801QFA	W	CFP	16	25	506.98	26.16	6220	NA
76008012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7600801FA	W	CFP	16	25	506.98	26.16	6220	NA
76034012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7603401FA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31504B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31504BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31512B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31512BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31504B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31504BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31512B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31512BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74S163N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S163N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54163W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS161AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS161AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS163AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS163AW	W	CFP	16	25	506.98	26.16	6220	NA

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated