

## SNx4HC174 Hex D-Type Flip-Flops with Clear

### 1 Features

- Wide operating voltage range of 2 V to 6 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 80- $\mu$ A max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA output drive at 5 V
- Low input current of 1  $\mu$ A max
- Contain six flip-flops with single-rail

### 2 Applications

- Buffer/storage registers
- Shift registers
- Pattern generators

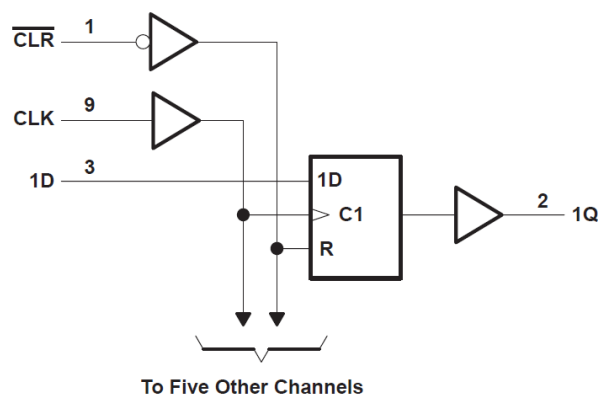
### 3 Description

The SNx4HC174 contains six positive-edge-triggered D-type flip-flops with shared clock (CLK) and clear ( $\overline{CLR}$ ) inputs.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74HC174D	SOIC (16)	9.90 mm × 3.90 mm
SN74HC174DB	SSOP (16)	6.20 mm × 5.30 mm
SN74HC174N	PDIP (16)	19.31 mm × 6.35 mm
SN74HC174NS	SO (16)	6.20 mm × 5.30 mm
SN74HC174PW	TSSOP (16)	5.00 mm × 4.40 mm
SN54HC174J	CDIP (16)	24.38 mm × 6.92 mm
SNJ54HC174FK	LCCC (20)	8.89 mm × 8.45 mm
SNJ54HC174W	CFP (16)	10.16 mm × 6.73 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



To Five Other Channels

**Functional Block Diagram**



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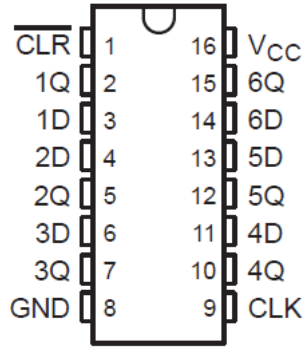
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## 4 Revision History

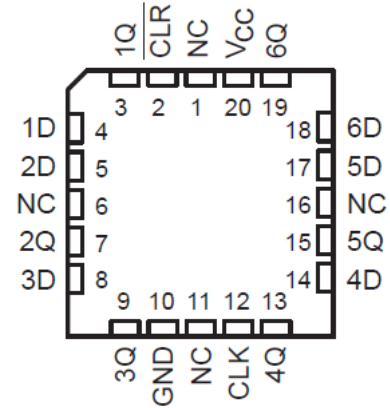
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (September 2003) to Revision E (February 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

## 5 Pin Configuration and Functions



**J, W, D, DB, N, NS, or PW Package**  
**16-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, TSSOP**  
**Top View**



NC – No internal connection

**FK Package**  
**20-Pin LCCC**  
**Top View**

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.2](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 Recommended Operating Conditions<sup>(1)</sup>

		SN54HC174			SN74HC174			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5			V
		V <sub>CC</sub> = 4.5 V	3.15		3.15			
		V <sub>CC</sub> = 6 V	4.2		4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5		V
		V <sub>CC</sub> = 4.5 V		1.35		1.35		
		V <sub>CC</sub> = 6 V		1.8		1.8		
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V		1000		1000		ns
		V <sub>CC</sub> = 4.5 V		500		500		
		V <sub>CC</sub> = 6 V		400		400		
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.3 Thermal Information

THERMAL METRIC		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	73	82	67	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			SN54HC174		SN74HC174		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -20 μA	2	1.9	1.998		1.9		1.9	V	
		4.5	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	I <sub>OH</sub> = -4 mA	4.5	3.98	4.3		3.7		3.84		
	I <sub>OH</sub> = -5.2 mA	6	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	2		0.002	0.1		0.1		0.1	
		4.5		0.001	0.1		0.1		0.1	
		6		0.001	0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	4.5		0.17	0.26		0.4		0.33	
	I <sub>OL</sub> = 5.2 mA	6		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6			8		160		80	μA
C <sub>i</sub>		2 to 6		3	10		10		10	pF

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 6.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		SN54HC174		SN74HC174		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2		6		4.2		5	MHz
		4.5		31		21		25	
		6		36		25		29	
t <sub>w</sub>	Pulse duration	CLR low	2	80		120		100	ns
			4.5	16		24		20	
			6	14		20		17	
		CLK high or low	2	80		120		100	
			4.5	16		24		20	
			6	14		20		17	
t <sub>su</sub>	Setup time before CLK↑	Data	2	100		150		125	ns
			4.5	20		30		25	
			6	17		25		21	
		CLR inactive	2	100		150		125	
			4.5	20		30		25	
			6	17		25		21	
t <sub>h</sub>	Hold time, data after CLK↑	2	0		0		0	ns	
		4.5	0		0		0		
		6	0		0		0		

## 6.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Section 7](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			2	6	9		4.2		5	MHz	
			4.5	31	44		21		25		
			6	36	50		25		29		
$t_{pd}$	$\overline{\text{CLR}}$	Any	2		58	160		240		200	ns
			4.5		17	32		48		40	
			6		14	27		41		34	
	CLK	Any	2		58	160		240		200	
			4.5		17	32		48		40	
			6		14	27		41		34	
$t_t$		Any	2		38	75		110		90	ns
			4.5		8	15		22		19	
			6		6	13		19		16	

## 6.7 Operating Characteristics

$T_a = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per flip-flop	No load	27	pF

## 7 Parameter Measurement Information

$t_{pd}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$

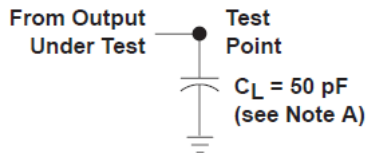


Figure 7-1. Load Circuit

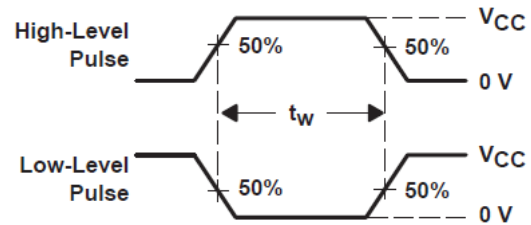


Figure 7-2. Voltage Waveforms Pulse Durations

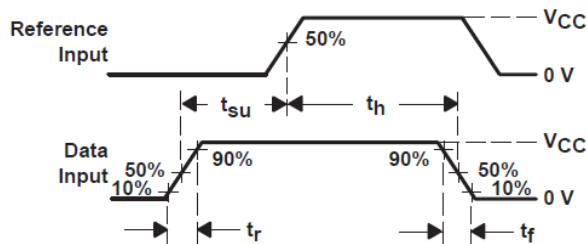


Figure 7-3. Voltage Waveforms Setup and Hold and Input Rise and Fall Times

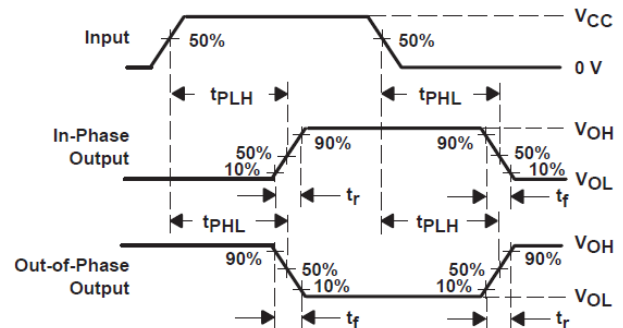


Figure 7-4. Voltage Waveforms Propagation Delay and Output Transition Times

- A.  $C_L$  includes probe and jig capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%
- D. The outputs are measured one at a time with one input transition per measurement.

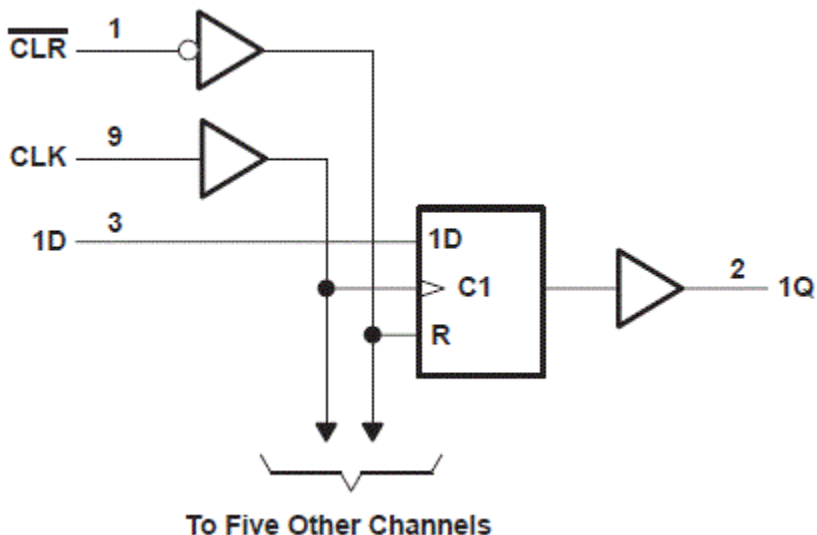
## 8 Detailed Description

### 8.1 Overview

These positive-edge-triggered D-type flip-flops have a direct clear ( $\overline{\text{CLR}}$ ) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

### 8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

### 8.3 Device Functional Modes

**Table 8-1. Function Table  
(each flip-flop)**

INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$



## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 10 Layout

### 10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84073012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84073012A SNJ54HC 174FK	<a href="#">Samples</a>
8407301EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407301EA SNJ54HC174J	<a href="#">Samples</a>
8407301FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407301FA SNJ54HC174W	<a href="#">Samples</a>
JM38510/65307BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65307BEA	<a href="#">Samples</a>
M38510/65307BEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65307BEA	<a href="#">Samples</a>
SN54HC174J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC174J	<a href="#">Samples</a>
SN74HC174D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	HC174	
SN74HC174DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC174	<a href="#">Samples</a>
SN74HC174DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC174	<a href="#">Samples</a>
SN74HC174DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC174	<a href="#">Samples</a>
SN74HC174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC174N	<a href="#">Samples</a>
SN74HC174NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC174N	<a href="#">Samples</a>
SN74HC174NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC174	<a href="#">Samples</a>
SN74HC174PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HC174	
SN74HC174PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC174	<a href="#">Samples</a>
SN74HC174PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC174	<a href="#">Samples</a>
SNJ54HC174FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84073012A SNJ54HC 174FK	<a href="#">Samples</a>
SNJ54HC174J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407301EA SNJ54HC174J	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC174W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407301FA SNJ54HC174W	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC174, SN74HC174 :**

- Catalog : [SN74HC174](#)
- Military : [SN54HC174](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

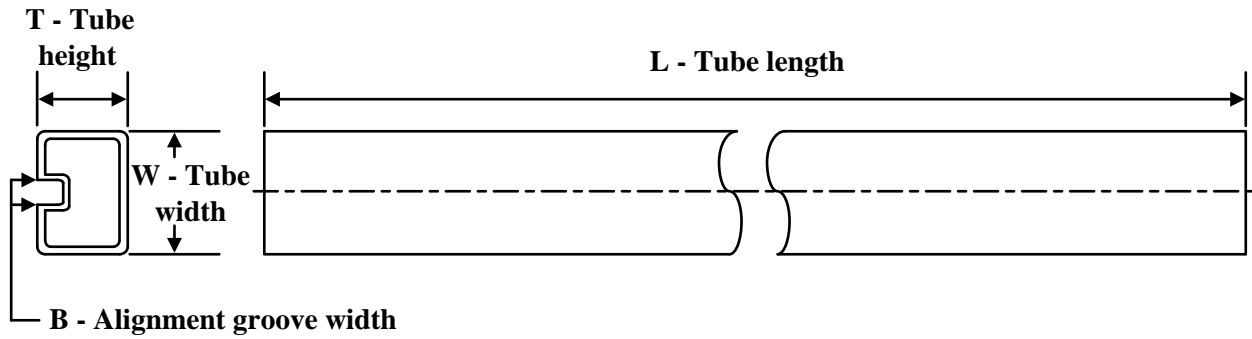

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC174DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC174DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC174DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC174NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC174PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC174PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC174DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC174DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC174DRG4	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC174NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74HC174PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC174PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84073012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8407301FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC174N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC174N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC174NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC174NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC174FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC174W	W	CFP	16	25	506.98	26.16	6220	NA





# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

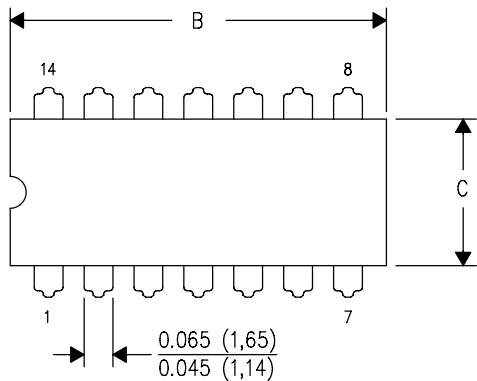
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



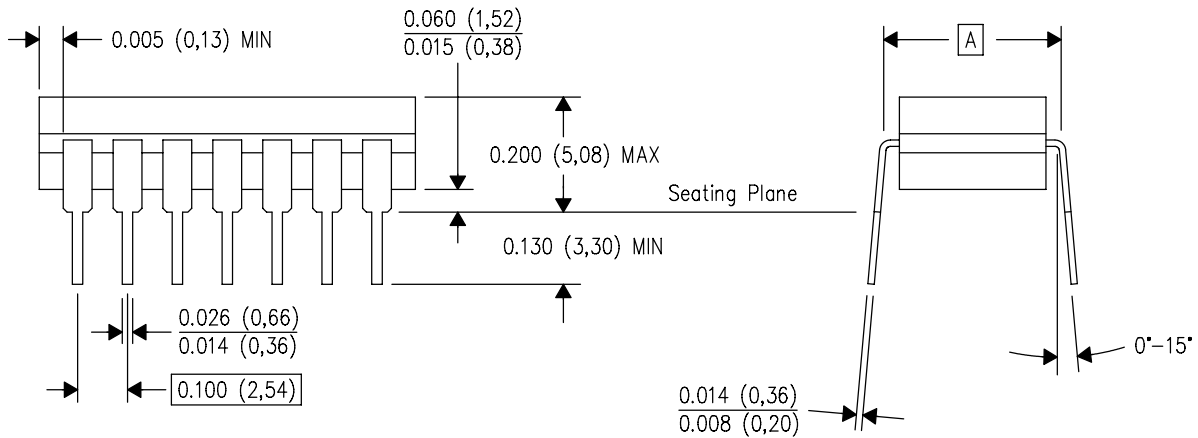
4229370VA\

J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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