- **Members of the Texas Instruments Widebus™ Family**

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 5 V, T_A = 25°C**

- **High-Impedance State During Power Up and Power Down**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

description/ordering information

These 20-bit transparent D-type latches feature noninverting 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT162841 devices can be used as two 10-bit latches or one 20-bit latch. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

SN54ABT162841 . . . WD PACKAGE
SN74ABT162841 . . . DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{\text{OE}}$	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
V_{CC}	7	50	V_{CC}
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
2$\overline{\text{OE}}$	28	29	2LE

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74ABT162841DL	ABT162841
		Tape and reel	SN74ABT162841DLR	
	TSSOP – DGG	Tape and reel	SN74ABT162841DGGR	ABT162841
−55°C to 125°C	CFP – WD	Tube	SNJ54ABT162841WD	SNJ54ABT162841WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

description/ordering information (continued)

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$ does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.
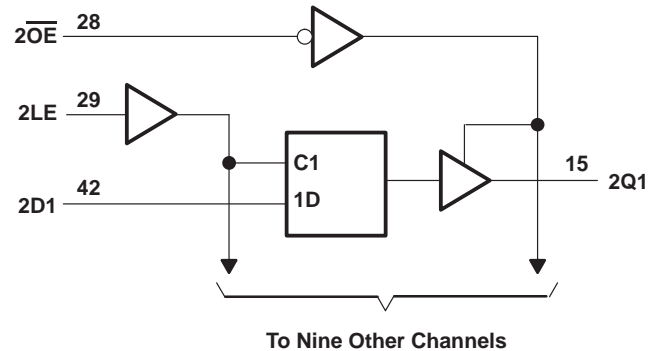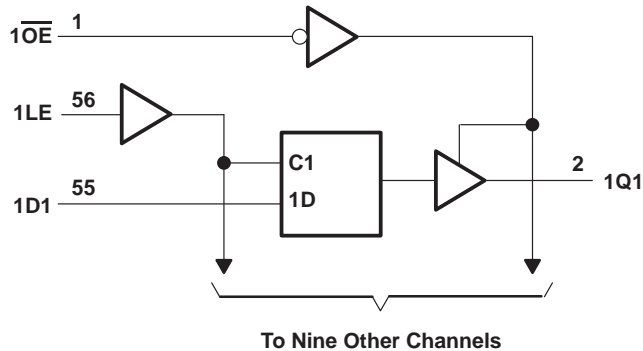
FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

To Nine Other Channels   **To Nine Other Channels**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V

Voltage range applied to any output in the high or power-off state, V_O .... −0.5 V to 5.5 V

Current into any output in the low state, I_O .... 30 mA

Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 64°C/W

DL package .... 56°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54ABT162841		SN74ABT162841		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−3		−12	mA
I_{OL}	Low-level output current			8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162841		SN74ABT162841		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −1 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4			2.4		2.4		
			I_{OH} = −12 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 8 mA		0.4			0.8		0.65	V
			I_{OL} = 12 mA		0.8*					0.8	
V_{hys}					100						mV
I_I		V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND			±1			±1		±1	μA
I_{OZPU}		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X			±50			±50		±50	μA
I_{OZPD}		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X			±50			±50		±50	μA
I_{OZH}		V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, $\overline{OE}$ ≥ 2 V			10			10		10	μA
I_{OZL}		V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, $\overline{OE}$ ≥ 2 V			−10			−10		−10	μA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V		±100					±100	μA
I_{CEX}	Outputs high	V_{CC} = 5.5 V,	V_O = 5.5 V		50			50		50	μA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.5 V	−25	−75	−100	−25	−100	−25	−100	mA
I_{CC}	Outputs high	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND			0.5			0.5		0.5	mA
	Outputs low				89			89		89	
	Outputs disabled				0.5			0.5		0.5	
ΔI_{CC}§		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5			1.5		1.5	mA
C_i		V_I = 2.5 V or 0.5 V			3.5						pF
C_o		V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V_{CC} = 5 V, T_A = 25°C		SN54ABT162841		SN74ABT162841		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	4		4		4		ns
t_{su}	Setup time, data before LE↓	0.8		0.8		0.8		ns
t_h	Hold time, data after LE↓	1.8		1.8		1.8		ns

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C$_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$ = 5 V, T$_A$ = 25°C			SN54ABT162841		SN74ABT162841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{PLH}$	D	Q	2.1	3.5	4.5	2.1	5.7	2.1	5.2	ns
t$_{PHL}$			3	4.3	5.3	3	6.2	3	6	
t$_{PLH}$	LE	Q	2.1	3.5	4.5	2.1	5.6	2.1	5.4	ns
t$_{PHL}$			2.8	4.1	5.1	2.8	6.1	2.8	5.8	
t$_{PZH}$	$\overline{OE}$	Q	2	3.6	4.7	2	5.8	2	5.7	ns
t$_{PZL}$			3	4.6	5.7	3	6.7	3	6.5	
t$_{PHZ}$	$\overline{OE}$	Q	2.6	4.3	5.7	2.6	6.6	2.6	6.5	ns
t$_{PLZ}$			2.2	3.6	5.8	2.2	8.4	2.2	7.1	

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION
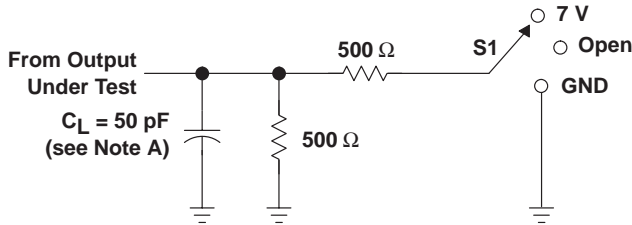
LOAD CIRCUIT

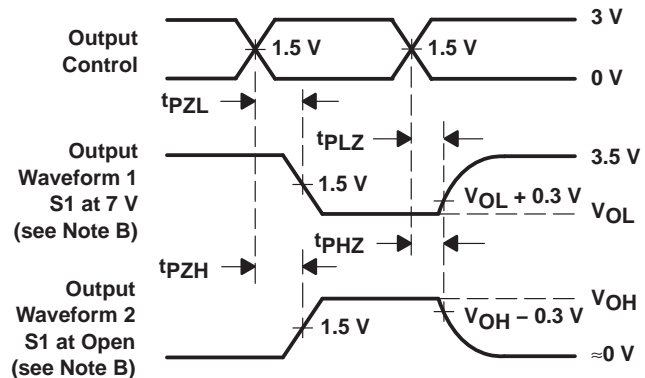| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
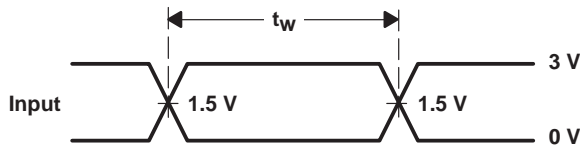
VOLTAGE WAVEFORMS
PULSE DURATION
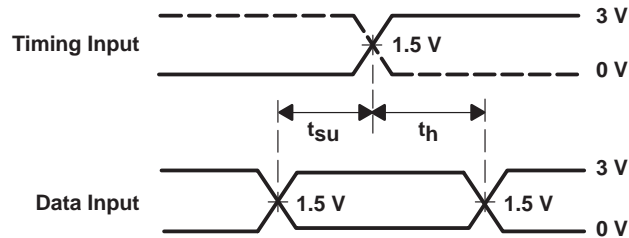
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
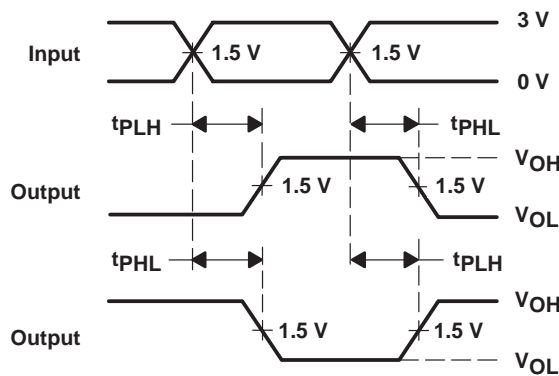
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT162841DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162841	Samples
SN74ABT162841DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162841	Samples
SN74ABT162841DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162841	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162841DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT162841DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162841DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ABT162841DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT162841DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56) PLASTIC SMALL−OUTLINE PACKAGE

4040048−4/F 05/13

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO−118

PowerPAD is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
www.ti.com

8.3
7.9 TYP

PIN 1 ID
AREA

A

1

54X 0.5

56

2X
13.5

14.1
13.9
NOTE 3

28

29

B

6.2
6.0

56X 0.27
0.17

⊕ 0.08Ⓜ C AⓈ BⓈ

C

SEATING PLANE

◠ 0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM

56

SYMM

28

29

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222167/A   07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A   07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.