

## SNx4AC86 Quadruple 2-Input Exclusive-OR Gates

### 1 Features

- 2V to 6V  $V_{CC}$  operation
- Inputs accept voltages to 6V
- Max  $t_{pd}$  of 9ns at 5V

### 2 Description

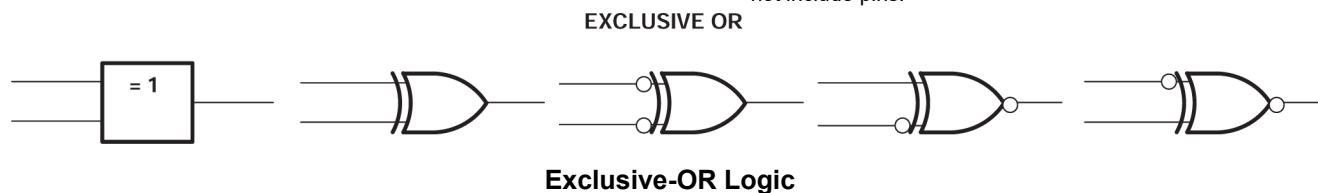
The 'AC86 devices are quadruple 2-input exclusive-OR gates. The devices perform the Boolean function  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SNx4AC86	DB (SSOP, 14)	6.2mm x 7.8mm	6.2mm x 5.3mm
	D (SOIC, 14)	8.65mm x 6mm	8.65mm x 3.9mm
	N (PDIP, 14)	19.3mm x 9.4mm	19.3mm x 6.35mm
	NS (SO, 14)	10.2mm x 7.8mm	10.3mm x 5.3mm
	PW (TSSOP, 14)	5mm x 6.4mm	5mm x 4.4mm

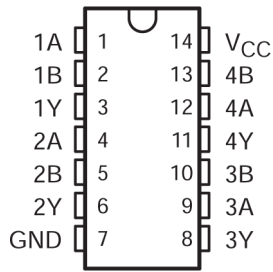
- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



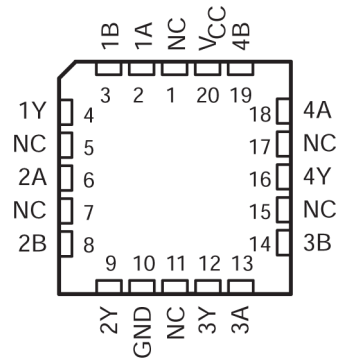
## Table of Contents

<b>1 Features</b> .....	1	6.2 Device Functional Modes.....	7
<b>2 Description</b> .....	1	<b>7 Application and Implementation</b> .....	8
<b>3 Pin Configuration and Functions</b> .....	3	7.1 Power Supply Recommendations.....	8
<b>4 Specifications</b> .....	4	7.2 Layout.....	8
4.1 Absolute Maximum Ratings.....	4	<b>8 Device and Documentation Support</b> .....	9
4.2 Recommended Operating Conditions.....	4	8.1 Documentation Support.....	9
4.3 Thermal Information.....	4	8.2 Receiving Notification of Documentation Updates.....	9
4.4 Electrical Characteristics.....	5	8.3 Support Resources.....	9
4.5 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$ .....	5	8.4 Trademarks.....	9
4.6 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$ .....	5	8.5 Electrostatic Discharge Caution.....	9
4.7 Operating Characteristics.....	5	8.6 Glossary.....	9
<b>5 Parameter Measurement Information</b> .....	6	<b>9 Revision History</b> .....	9
<b>6 Detailed Description</b> .....	7	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	9
6.1 Functional Block Diagram.....	7		

### 3 Pin Configuration and Functions



**Figure 3-1. SN54AC86 J or W Package; SN74AC86 D, DB, N, NS, or PW Package (Top View)**



NC – No internal connection

**Figure 3-2. SN54AC86 FK Package (Top View)**

**Table 3-1. Pin Functions**

NAME	PIN		I/O	DESCRIPTION
	D, N, NS, PW, J, or W	FK		
1A	1	2	Input	Channel 1, Input A
1B	2	3	Input	Channel 1, Input B
1Y	3	4	Output	Channel 1, Output Y
2A	4	6	Input	Channel 2, Input A
2B	5	8	Input	Channel 2, Input B
2Y	6	9	Output	Channel 2, Output Y
GND	7	10	—	Ground
3Y	8	12	Output	Channel 3, Output Y
3A	9	13	Input	Channel 3, Input A
3B	10	14	Input	Channel 3, Input B
4Y	11	16	Output	Channel 4, Output Y
4A	12	18	Input	Channel 4, Input A
4B	13	19	Input	Channel 4, Input B
V <sub>CC</sub>	14	20	—	Positive Supply
NC		1, 5, 7, 11, 15, 17	—	Not internally connected

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$ <sup>(2)</sup>	Input voltage range	-0.5	$V_{CC} + 0.5$	V
$V_O$ <sup>(2)</sup>	Output voltage range	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		$\pm 20$ mA
$I_{OK}$	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		$\pm 20$ mA
$I_O$	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		$\pm 50$ mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AC86		SN74AC86		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3 \text{ V}$	2.1	2.1		V
		$V_{CC} = 4.5 \text{ V}$	1.15	1.15		
		$V_{CC} = 5.5 \text{ V}$	1.85	1.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 \text{ V}$		0.9	0.9	V
		$V_{CC} = 4.5 \text{ V}$		1.35	1.35	
		$V_{CC} = 5.5 \text{ V}$		1.65	1.65	
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3 \text{ V}$		-12	-12	mA
		$V_{CC} = 4.5 \text{ V}$		-24	-24	
		$V_{CC} = 5.5 \text{ V}$		-24	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 3 \text{ V}$		12	12	mA
		$V_{CC} = 4.5 \text{ V}$		24	24	
		$V_{CC} = 5.5 \text{ V}$		24	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SNx4AC86					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.9	96	80	76	145.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC86		SN74AC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50μA	3V	2.9			2.9	2.9		V	
		4.5V	4.4			4.4	4.4			
		5.5V	5.4			5.4	5.4			
	I <sub>OH</sub> = -12mA	3V	2.56			2.4	2.46			
		4.5V	3.86			3.7	3.76			
	I <sub>OH</sub> = -24mA	5.5V	4.86			4.7	4.76			
		5.5V	I <sub>OH</sub> = -50mA <sup>(1)</sup>			3.85				
5.5V	I <sub>OH</sub> = -75mA <sup>(1)</sup>					3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50μA	3V	0.002		0.1	0.1		V		
		4.5V	0.001		0.1	0.1				
		5.5V	0.001		0.1	0.1				
	I <sub>OL</sub> = 12mA	3V			0.36	0.5			0.44	
		4.5V			0.36	0.5			0.44	
	I <sub>OL</sub> = 24mA	5.5V			0.36	0.5			0.44	
		5.5V	I <sub>OL</sub> = 50mA <sup>(1)</sup>				1.65			
5.5V	I <sub>OL</sub> = 75mA <sup>(1)</sup>						1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5V	±0.1			±1		±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5V	2			40		20		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V	2.6							pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

## 4.5 Switching Characteristics, V<sub>CC</sub> = 3.3V ± 0.3V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3V ± 0.3V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54AC86		SN74AC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	2	6.5	11.5	1	14	1.5	12.5	ns
t <sub>PHL</sub>			2	6	11.5	1	14	1.5	12.5	

## 4.6 Switching Characteristics, V<sub>CC</sub> = 5V ± 0.5V

over recommended operating free-air temperature range, V<sub>CC</sub> = 5V ± 0.5V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

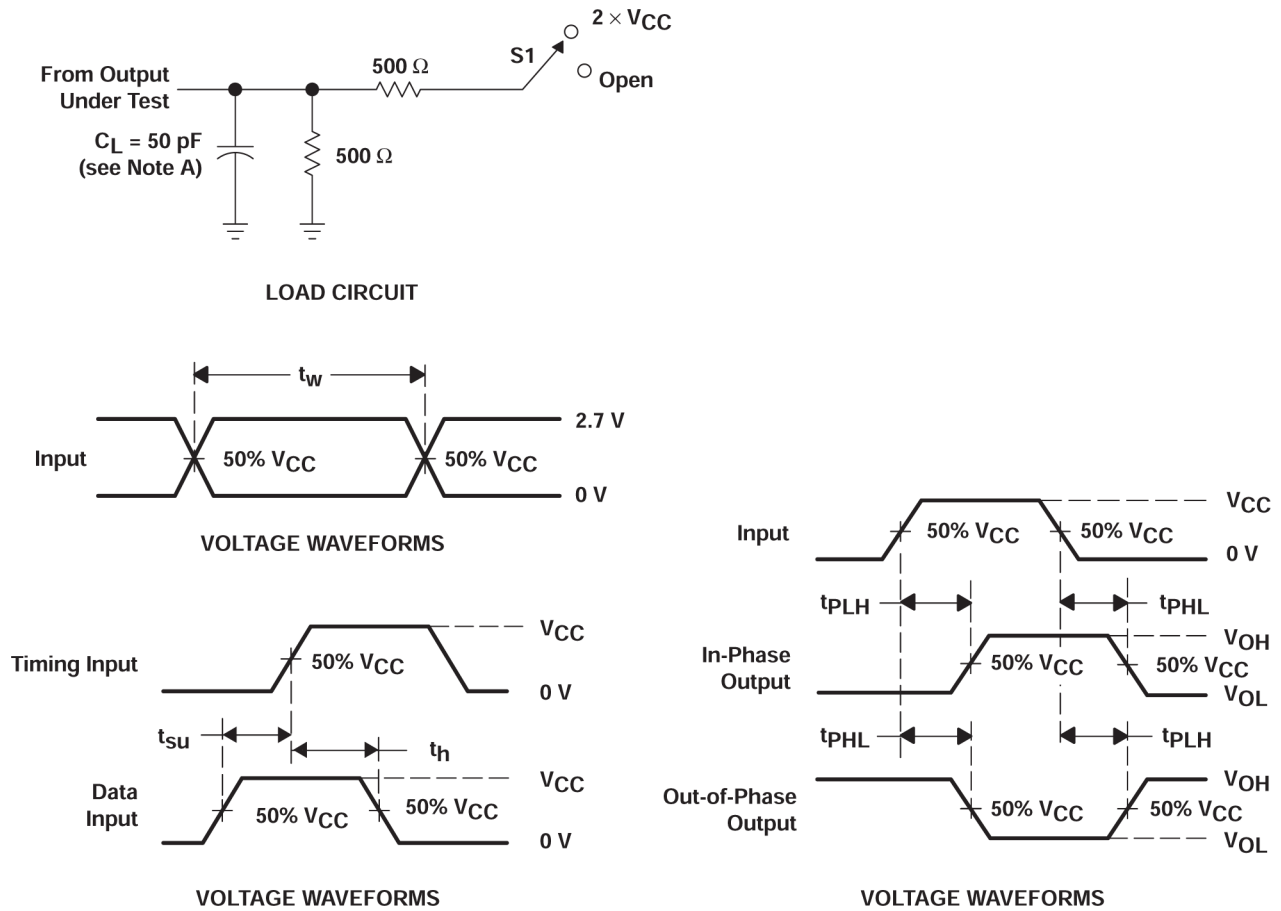
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54AC86		SN74AC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	1.5	4.5	8.5	1	10	1	9	ns
t <sub>PHL</sub>			1.5	4.5	8.5	1	10	1	9.5	

## 4.7 Operating Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance C <sub>L</sub> = 50 pF, f = 1 MHz	25	pF

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. The outputs are measured one at a time with one input transition per measurement.

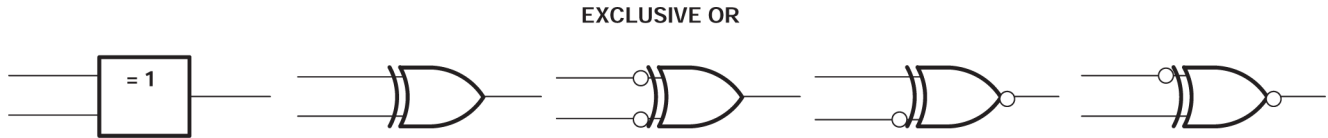
**Figure 5-1. Load Circuit and Voltage Waveforms**

TEST	S1
$t_{PLH}/t_{PHL}$	Open

## 6 Detailed Description

### 6.1 Functional Block Diagram

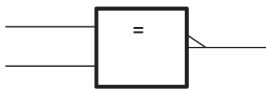
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



**Figure 6-1. Exclusive-OR Logic**

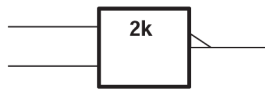
These five equivalent exclusive-OR symbols are valid for an 'AC86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



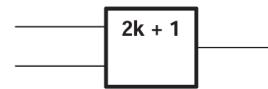
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

**EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

### 6.2 Device Functional Modes

**Table 6-1. Function Table (Each Gate)**

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Example Layout for the SN74AC86](#).

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

#### 7.2.2 Layout Example

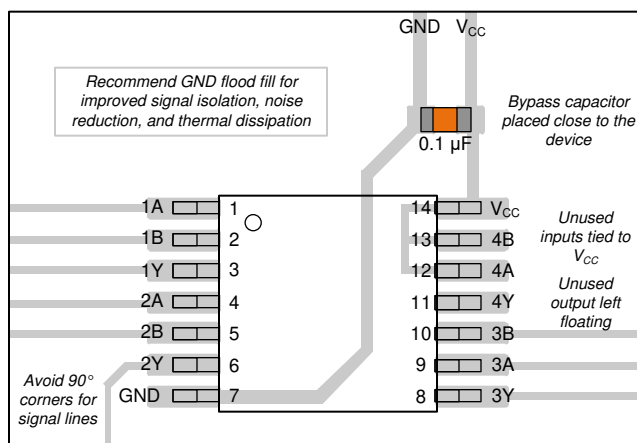


Figure 7-1. Example layout for the SN74AC86



## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AC86	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74AC86	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2003) to Revision D (July 2024)	Page
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Updated RθJA values: D = 86 to 119.9, PW = 113 to 145.7, all values in °C/W.....	4

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89550012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-89550012A SNJ54AC 86FK	<a href="#">Samples</a>
5962-8955001CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8955001CA SNJ54AC86J	<a href="#">Samples</a>
5962-8955001DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8955001DA SNJ54AC86W	<a href="#">Samples</a>
SN74AC86D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AC86	
SN74AC86DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC86	<a href="#">Samples</a>
SN74AC86DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC86	<a href="#">Samples</a>
SN74AC86N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC86N	<a href="#">Samples</a>
SN74AC86NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC86	<a href="#">Samples</a>
SN74AC86PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	AC86	
SN74AC86PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC86	<a href="#">Samples</a>
SNJ54AC86FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-89550012A SNJ54AC 86FK	<a href="#">Samples</a>
SNJ54AC86J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8955001CA SNJ54AC86J	<a href="#">Samples</a>
SNJ54AC86W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8955001DA SNJ54AC86W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AC86, SN74AC86 :**

● Catalog : [SN74AC86](#)

● Military : [SN54AC86](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AC86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC86NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC86DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AC86DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AC86NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AC86PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-89550012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8955001DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AC86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC86N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AC86FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC86W	W	CFP	14	25	506.98	26.16	6220	NA

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

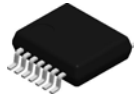
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14



# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

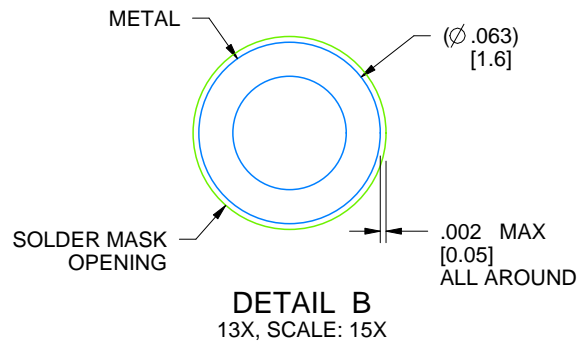
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



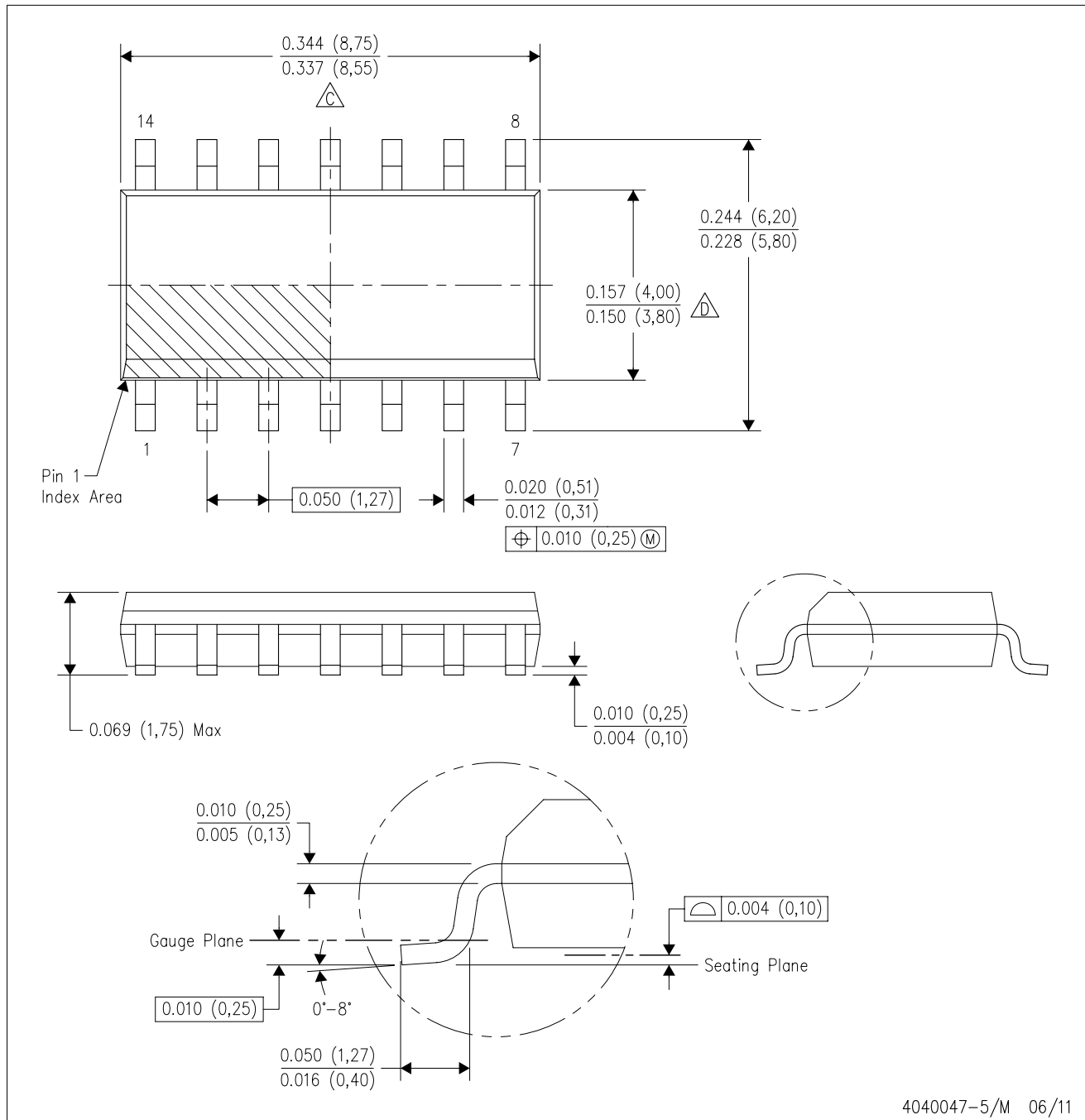
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



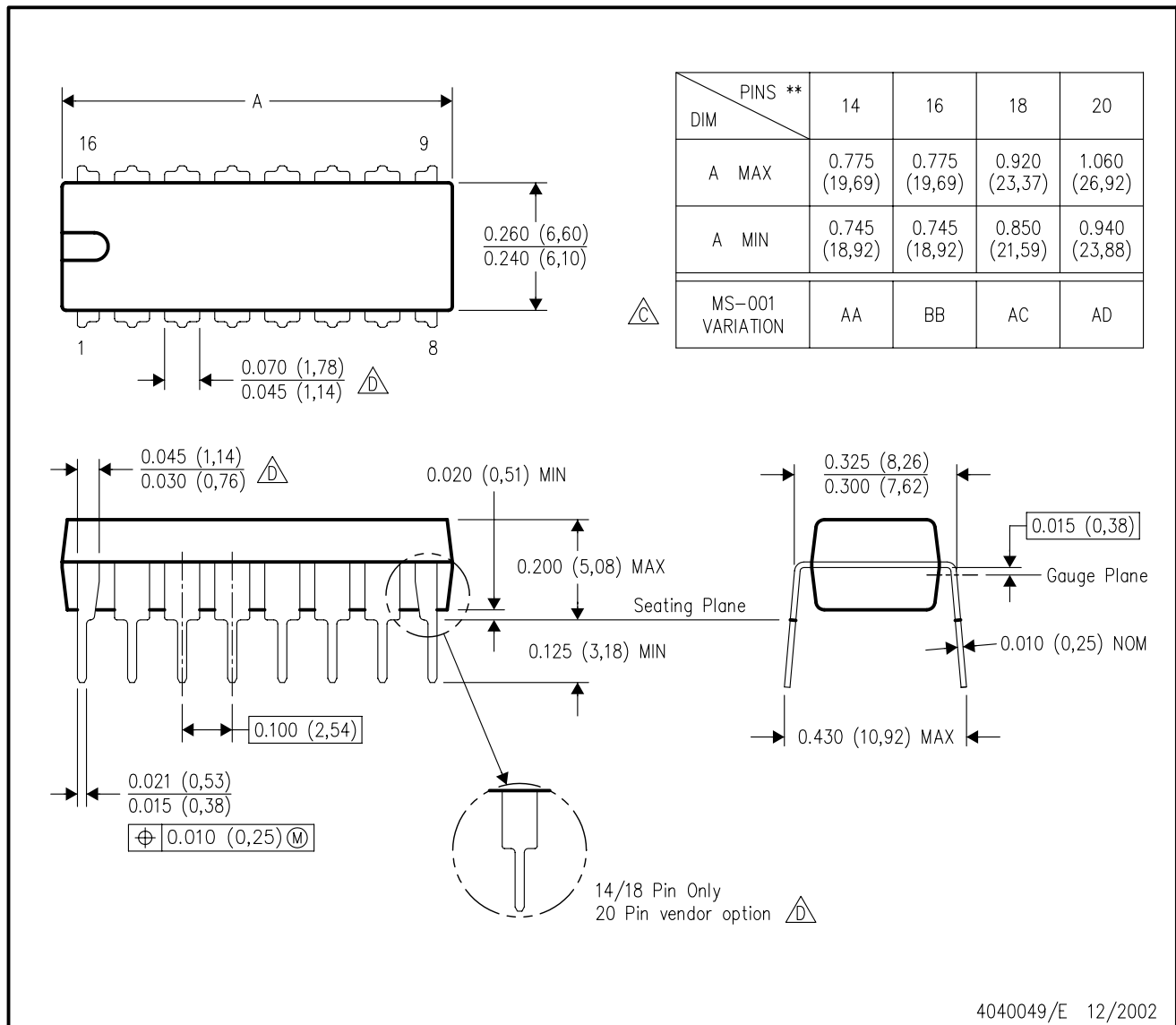
4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated