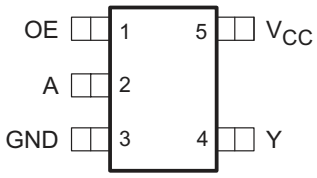
SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

Check for Samples: SN74AHC1G126-EP

FEATURES

- **Operating Range of 2 V to 5.5 V**
- **Max t_{pd} of 6 ns at 5 V**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±8-mA Output Drive at 5 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DCK PACKAGE
(TOP VIEW)



SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

The SN74AHC1G126 is a single bus buffer gate and line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION(1)

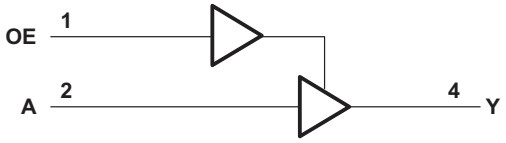
T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	SOT (SC-70) – DCK	Reel of 250	74AHC1G126MDCKTEP	SLI	V62/14605-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating junction temperature range (unless otherwise noted)

V_{CC}	Supply voltage range		−0.5 V to 7 V
V_I	Input voltage range(2)		−0.5 V to 7 V
V_O	Output voltage range(2)		−0.5 V to V_{CC} + 0.5 V
I_{IK}	Input clamp current	V_I < 0	-20 mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}	±20 mA
I_O	Continuous output current	V_O = 0 to V_{CC}	±25 mA
	Continuous current through V_{CC} or GND		±50 mA
T_J	Junction temperature range		−55°C to 150°C
T_{stg}	Storage temperature range		−65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL INFORMATION

THERMAL METRIC(1)		SN74AHC1G126-EP	UNITS
		DCK	
		5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	282.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	91.1	
θ_{JB}	Junction-to-board thermal resistance(4)	60.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	59.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		-50	µA
		V_{CC} = 3.3 V ±0.3 V		-4	mA
		V_{CC} = 5 V ±0.5 V		-8	
I_{OL}	Low-level output current	V_{CC} = 2 V		-50	µA
		V_{CC} = 3.3 V ±0.3 V		4	mA
		V_{CC} = 5 V ±0.5 V		8	
Δt/Δv	Input transition rise/fall time	V_{CC} = 3.3 V ±0.3 V		100	ns/V
		V_{CC} = 5 V ±0.5 V		20	
T_J	Operating junction temperature range		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = −50 µA	2 V	1.9		V
		3 V	2.9		
		4.5 V	4.4		
	I_{OH} = −4 mA	3 V	2.48		
	I_{OH} = −8 mA	4.5	3.8		
V_{OL}	I_{OH} = 50 µA	2 V		0.1	V
		3 V		0.1	
		4.5 V		0.1	
	I_{OH} = 4 mA	3 V		0.44	
	I_{OH} = 8 mA	4.5		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V		±2.5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V		10	µA
C_i	V_I = V_{CC} or GND	5 V		10	pF

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT
t_{PLH}	A	Y	C_L = 50 pF	1	13	ns
t_{PHL}				1	13	ns
t_{PZH}	OE	Y	C_L = 50 pF	1	13	ns
t_{PZL}				1	13	ns
t_{PHZ}	OE	Y	C_L = 50 pF	1	15	ns
t_{PLZ}				1	15	ns

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted)

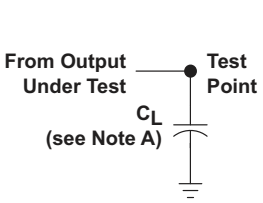
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	MAX	UNIT
t_{PLH}	A	Y	C_L = 50 pF	1	8.5	ns
t_{PHL}				1	8.5	ns
t_{PZH}	OE	Y	C_L = 50 pF	1	8	ns
t_{PZL}				1	8	ns
t_{PHZ}	OE	Y	C_L = 50 pF	1	10	ns
t_{PLZ}				1	10	ns

OPERATING CHARACTERISTICS

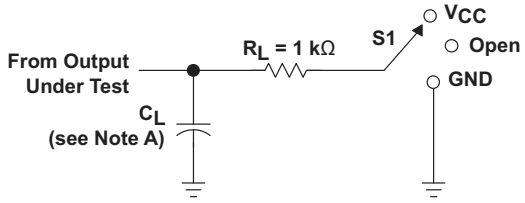
V_{CC} = 5 V, T_J = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

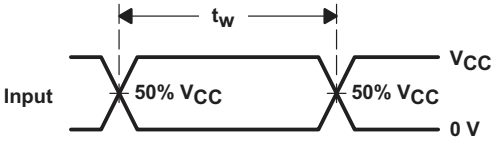


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

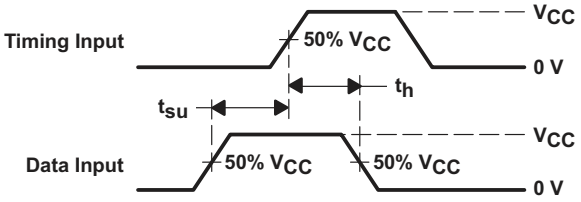


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

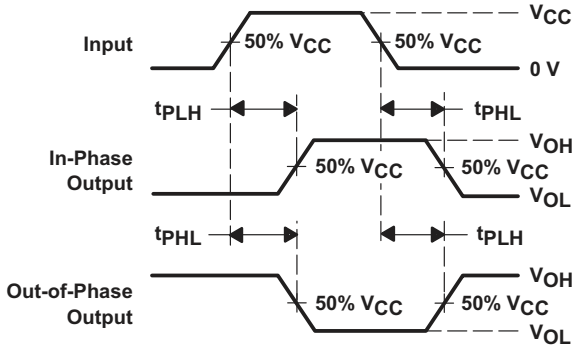
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



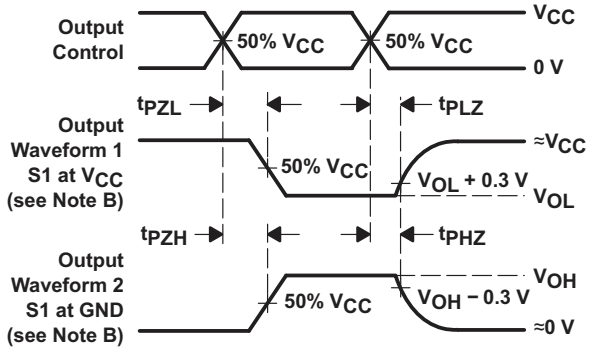
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

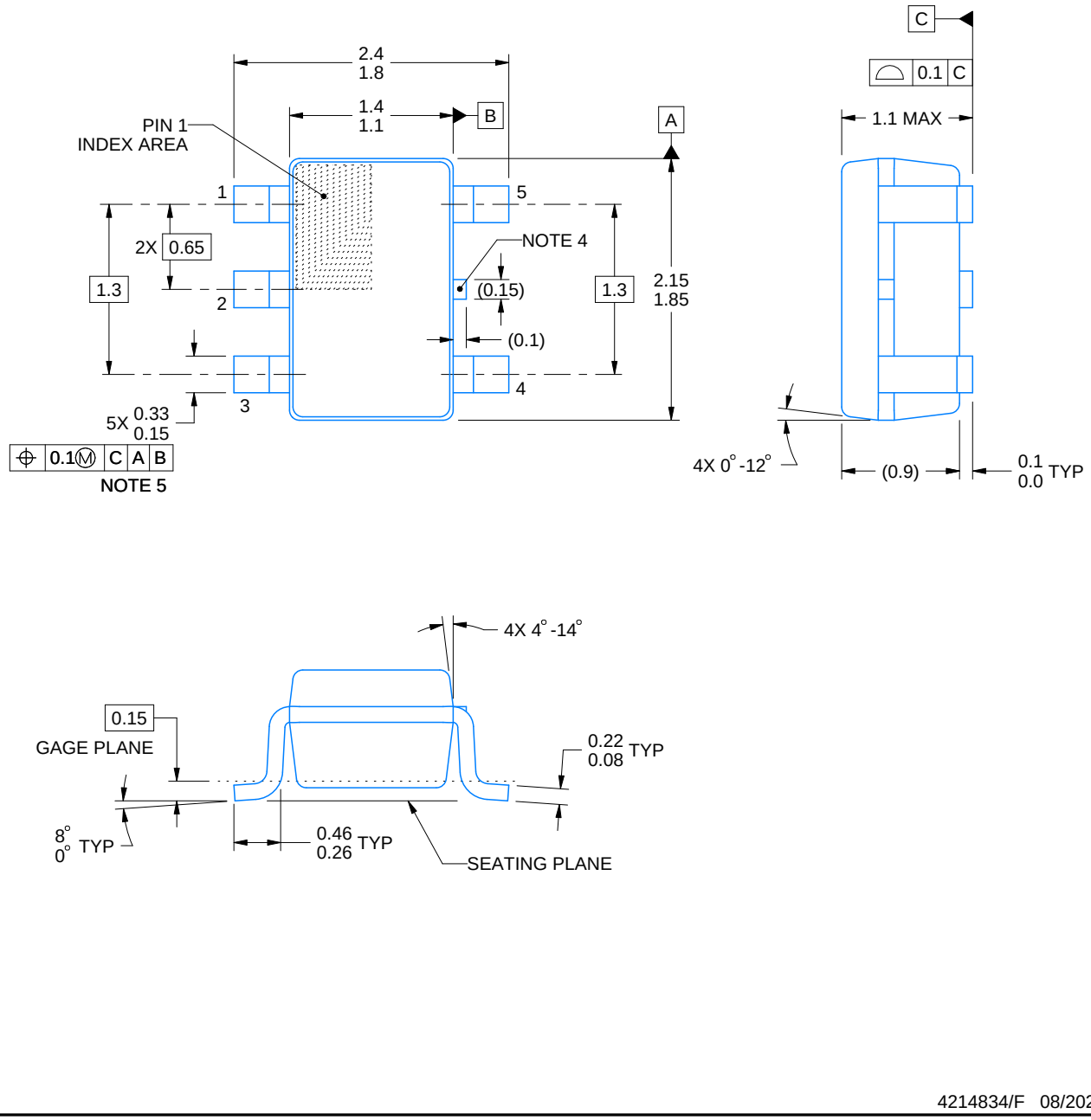
Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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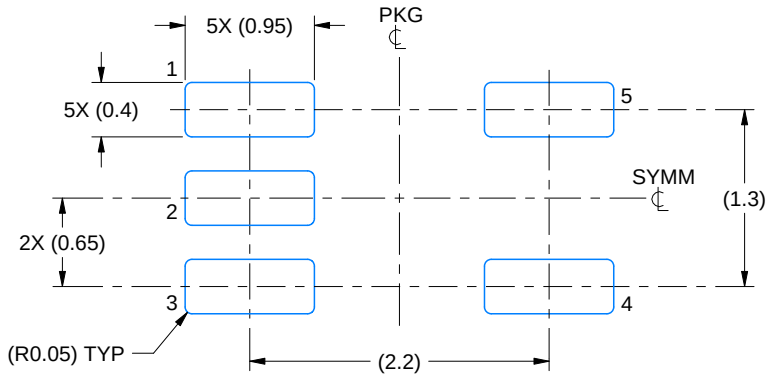
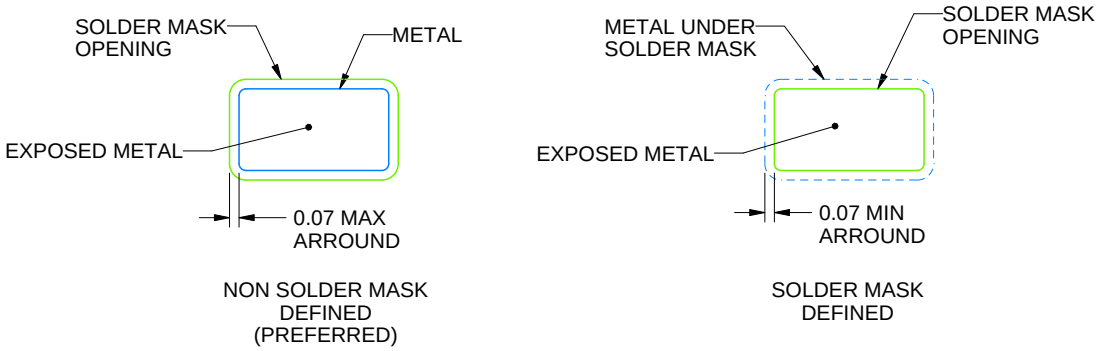
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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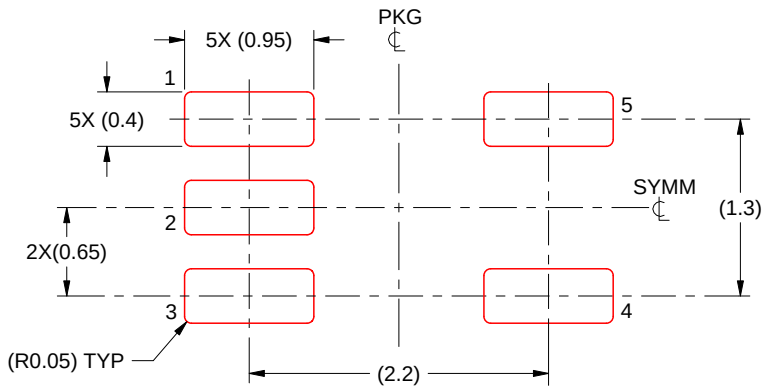
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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