# SN74AHC1G14 Single Schmitt-Trigger Inverter Gate

## 1 Features

- Operating range 2 V to 5.5 V
- Maximum $t_{pd}$ of 10 ns at 5 V
- Low power consumption, 10-µA max $I_{CC}$
- ±8-mA output drive at 5 V
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Barcode Scanners
- Cable Solutions
- E-Books
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Sever Motherboard and PSU
- Software Defined Radios (SDR)
- TV: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboards, Mice, and LAN Cards

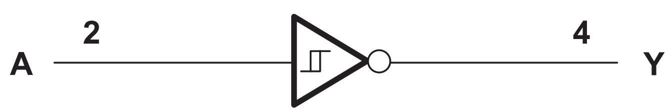
## 3 Description

The SN74AHC1G14 device is a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

**Package Information**

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] | BODY SIZE[3] |
|---|---|---|---|
| SN74AHC1G14 | DBV (SOT-23, 5) | 2.8 mm × 2.8 mm | 2.9 mm x 1.6 mm |
| | DCK (SC-70, 5) | 2 mm x 2.1 mm | 2 mm × 1.25 mm |
| | DRL (SOT-553, 5) | 1.6 mm x 1.6 mm | 1.6 mm × 1.2 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length x width) is a nominal value and does not include pins.




**Logic Diagram (Positive Side)**

## Table of Contents

**1 Features**........1
**2 Applications**........1
**3 Description**........1
**4 Pin Configuration and Functions**........3
**5 Specifications**........4
5.1 Absolute Maximum Ratings........4
5.2 ESD Ratings........4
5.3 Recommended Operating Conditions........4
5.4 Thermal Information........5
5.5 Electrical Characteristics........5
5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V........6
5.7 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V........6
5.8 Operating Characteristics........6
5.9 Typical Characteristics........6
**6 Parameter Measurement Information**........7
**7 Detailed Description**........8
7.1 Overview........8
7.2 Functional Block Diagram........8
7.3 Feature Description........8
7.4 Device Functional Modes........8
**8 Application and Implementation**........9
8.1 Application Information........9
8.2 Typical Application........9
8.3 Power Supply Recommendations........10
8.4 Layout........10
**9 Device and Documentation Support**........12
9.1 Documentation Support (Analog)........12
9.2 Support Resources........12
9.3 Trademarks........12
9.4 Electrostatic Discharge Caution........12
9.5 Glossary........12
**10 Revision History**........12
**11 Mechanical, Packaging, and Orderable Information**........12

# 4 Pin Configuration and Functions

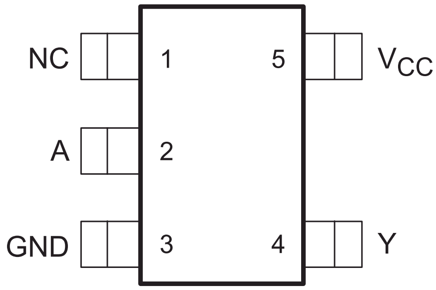



**Figure 4-1. DBV Package 5-Pin SOT-23 Top View**

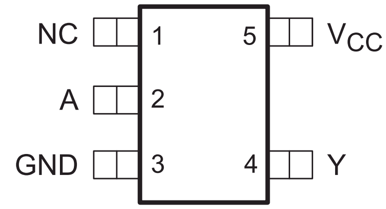



**Figure 4-2. DCK Package 5-Pin SC70 Top View**

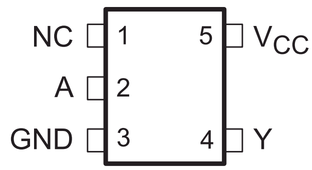



**Figure 4-3. DRL Package 5-Pin SOT Top View**

**Table 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | NC | — | No connect |
| 2 | A | I | Data Input |
| 3 | GND | — | Ground |
| 4 | Y | O | Data Output |
| 5 | VCC | — | Power |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage[(2)] | | –0.5 | 7 | V |
| $V_O$ | Output voltage[(2)] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_j$ | Maximum junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)] | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

### 5.4 Thermal Information

| THERMAL METRIC[1] | | SN74AHC1G14 DBV (SOT-23) 5 PINS | SN74AHC1G14 DCK (SC70) 5 PINS | SN74AHC1G14 DRL (SOT) 5 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278 | 289.2 | 271.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 180.5 | 205.8 | 116.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 184.4 | 176.2 | 89.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 115.4 | 117.6 | 17.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 183.4 | 175.1 | 89.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bot) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

### 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C MIN | $T_A$ = 25°C TYP | $T_A$ = 25°C MAX | $T_A$ = –40°C to 85°C MIN | TYP | MAX | RECOMMENDED $T_A$ = –40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going input threshold voltage | | 3 V | 1.2 | | 2.2 | 1.2 | | 2.2 | 1.2 | | 2.2 | V |
| | | | 4.5 V | 1.75 | | 3.15 | 1.75 | | 3.15 | 1.75 | | 3.15 | |
| | | | 5.5 V | 2.15 | | 3.85 | 2.15 | | 2.85 | 2.15 | | 3.85 | |
| $V_{T-}$ | Negative-going input threshold voltage | | 3 V | 0.9 | | 1.9 | 0.9 | | 1.9 | 0.9 | | 1.9 | V |
| | | | 4.5 V | 1.35 | | 2.75 | 1.35 | | 2.75 | 1.35 | | 2.75 | |
| | | | 5.5 V | 1.65 | | 3.35 | 1.65 | | 3.35 | 1.65 | | 3.35 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ – $V_{T-}$) | | 3 V | 0.3 | | 1.2 | 0.3 | | 1.2 | 0.25 | | 1.2 | V |
| | | | 4.5 V | 0.4 | | 1.4 | 0.4 | | 1.4 | 0.35 | | 1.4 | |
| | | | 5.5 V | 0.5 | | 1.6 | 0.5 | | 1.6 | 0.45 | | 1.6 | |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 µA | 2 V | 1.9 | 2 | | 1.9 | | | 1.9 | | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | | 2.9 | | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | | 4.4 | | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | | 2.4 | | | |
| | | $I_{OL}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | | 3.7 | | | |
| $V_{OL}$ | Low level output voltage | $I_{OH}$ = 50 µA | 2 V | | | 0.1 | | | 0.1 | | | 0.1 | V |
| | | | 3 V | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | $I_{OH}$ = 4 mA | 3 V | | | 0.36 | | | 0.44 | | | 0.55 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | | 0.44 | | | 0.55 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | | ±1 | | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | | 10 | | | 10 | µA |
| $C_i$ | Input Capacitance | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | 10 | | | 10 | pF |

## 5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A$ = 25°C | | $T_A$ = –40°C to 85°C | | RECOMMENDED $T_A$ = –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | 8.3 | 12.8 | 1 | 15 | 1 | 16 | ns |
| $t_{PHL}$ | | | | 8.3 | 12.8 | 1 | 15 | 1 | 16 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | 10.8 | 16.3 | 1 | 18.5 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | 10.8 | 16.3 | 1 | 18.5 | 1 | 19.5 | ns |

## 5.7 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

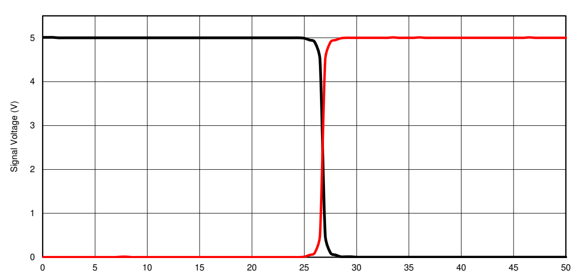
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A$ = 25°C | | $T_A$ = –40°C to 85°C | | RECOMMENDED $T_A$ = –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | 5.5 | 8.6 | 1 | 10 | 1 | 11 | ns |
| $t_{PHL}$ | | | | 5.5 | 8.6 | 1 | 10 | 1 | 11 | ns |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | 7 | 10.6 | 1 | 12 | 1 | 11 | ns |
| $t_{PHL}$ | | | | 7 | 10.6 | 1 | 12 | 1 | 11 | ns |

## 5.8 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 9 | pF |

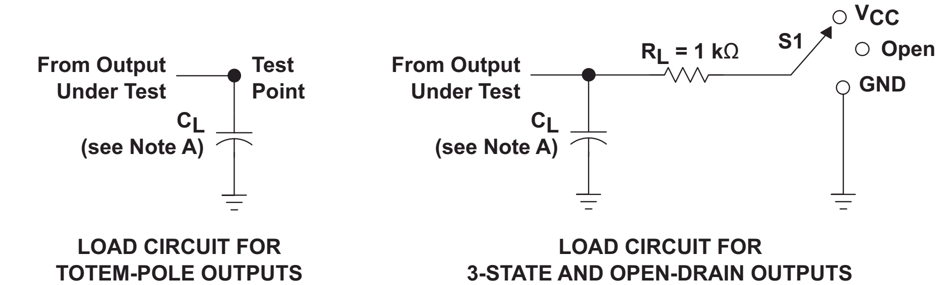
## 5.9 Typical Characteristics



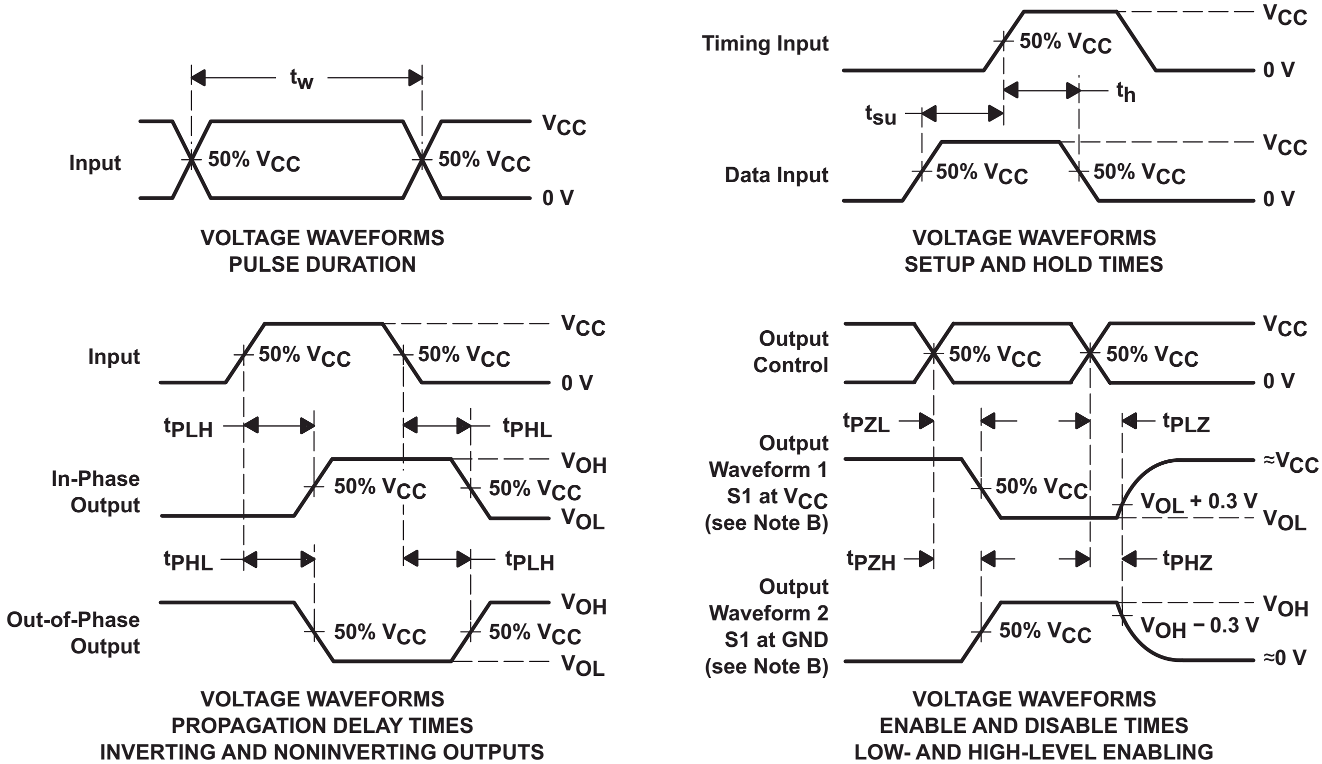

$T_A$ = 25°C, $V_A$ = 5 V

**Figure 5-1. Response Time vs Output Voltage**

## 6 Parameter Measurement Information




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |




A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The SN74AHC1G14 device is a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- ($V_{T+}$) and negative-going ($V_{T-}$) signals.

## 7.2 Functional Block Diagram

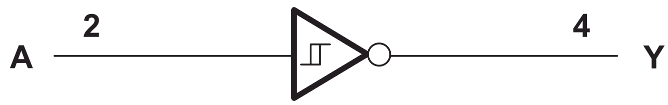



**Figure 7-1. Logic Diagram (Positive Side)**

## 7.3 Feature Description

The SN74AHC1G14 device has a wide operating $V_{CC}$ range of 2 V to 5.5 V, which allows it to be used in a broad range of systems. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low-power consumption makes this device a good choice for portable and battery power-sensitive applications.

## 7.4 Device Functional Modes

Table 7-1 lists the functional modes for SN74AHC1G14.

**Table 7-1. Function Table**

| INPUT(1) A | OUTPUT(2) Y |
|---|---|
| H | L |
| L | H |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

Physically interactive interface elements like push buttons or rotary knobs offer simple and easy ways to interact with an electronic system. Many of these physical interface elements often have issues with bouncing, or where the physical conductive contact can connect and disconnect multiple times during a button push or release. This bouncing can cause one or more faulty transient signals to be passed during this transitional period. These faulty signals can be observed in many common applications, for example, a television remote with bouncing error can adjust the TV channel multiple times despite the button being pushed only once. To mitigate these faulty signals, we can use a Schmitt-trigger, or a device with hysteresis, to remove these faulty signals. Hysteresis allows a device to *remember* its history, and in this case, the SN74AHC1G14 uses this memory to debounce the signal of the physical element, or filter the faulty transient signals and pass only the valid signal each time the element is used. In this example, we show a push-button signal passed through an SN74AHC1G14 that is debounced and inverted to the microprocessor for push detection.

## 8.2 Typical Application

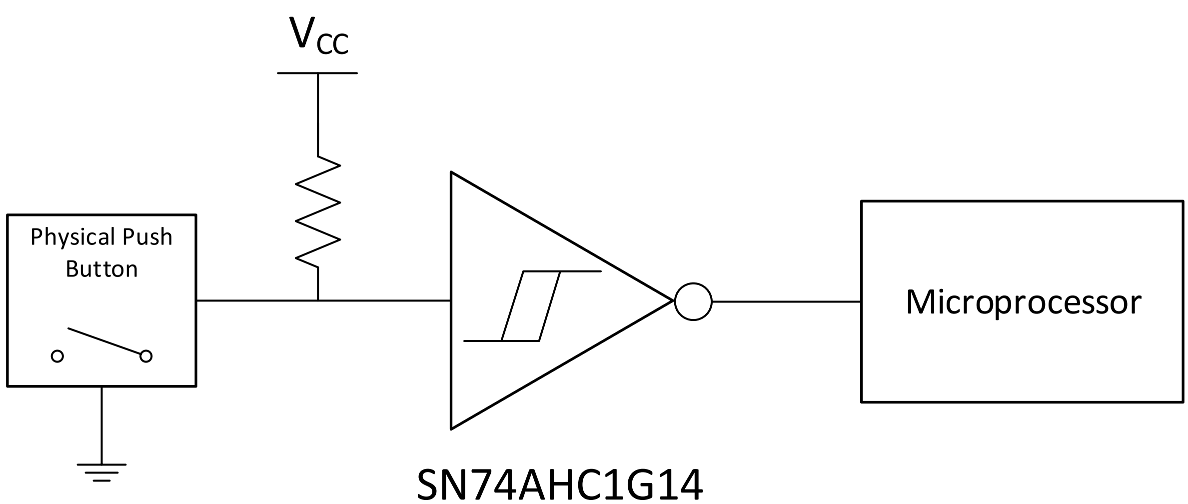



**Figure 8-1. Switch Debouncer**

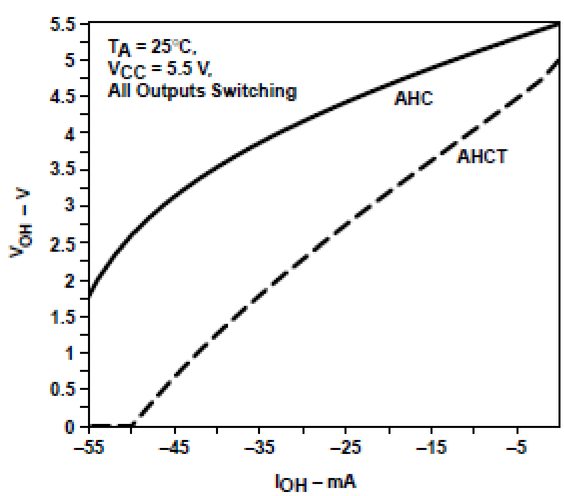
### 8.2.1 Design Requirements

The SN74AHC1G14 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The SN74AHC1G14 allows for performing logical Boolean functions with hysteresis using digital signals. All input signals must remain as close as possible to either 0 V or VCC for optimal operation.

### 8.2.2 Detailed Design Procedure

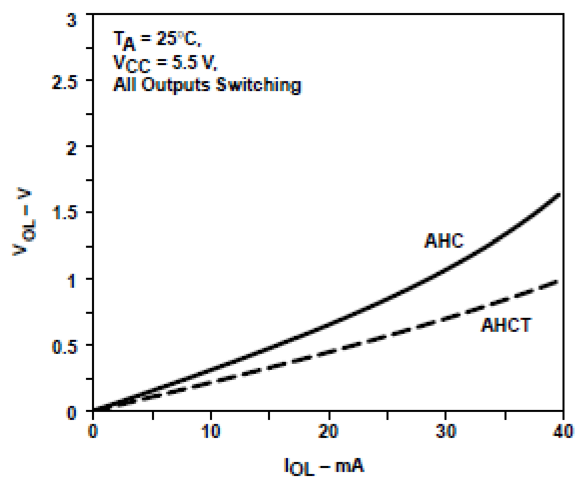
1. Recommended input conditions:
   - For rise time and fall time specifications, see Δt/Δv in the *Section 5.3* table.
   - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Section 5.3* table.
   - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid $V_{CC}$.
2. Recommended output conditions:
   - Load currents must not exceed ±50 mA.
3. Frequency selection criterion:
   - The effects of frequency upon the power consumption of the device can be studied in *CMOS Power Consumption and CPD Calculation*, SCAA035.
   - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the *Section 8.4.1* section.

### 8.2.3 Application Curves




$V_{CC}$ = 5.5 V

**Figure 8-2. AHC Family $V_{OH}$ vs $I_{OH}$**




$V_{CC}$ = 5.5 V

**Figure 8-3. AHC Family $V_{OL}$ vs $I_{OL}$**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Section 5.3* table.

Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If multiple pins are labeled $V_{CC}$, then a 0.01-μF or 0.022-μF capacitor is recommended for each $V_{CC}$ because the $V_{CC}$ pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example $V_{CC}$ and $V_{DD}$, a 0.1-μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight;

therefore some traces must turn corners. Figure 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

#### *8.4.1.1 Layout Example*

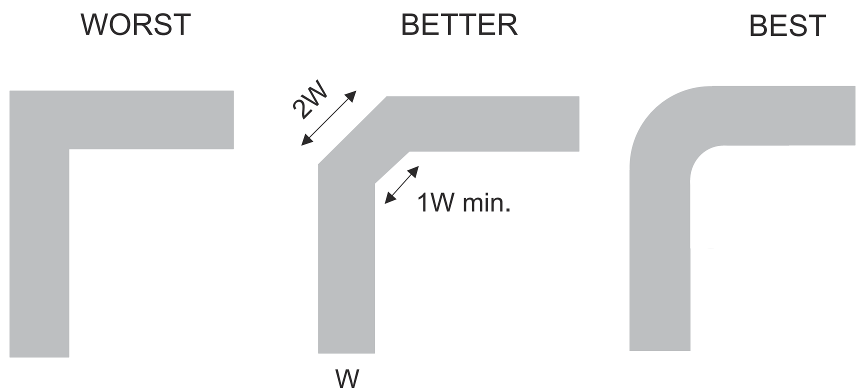



**Figure 8-4. Trace Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support (Analog)

### 9.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *CMOS Power Consumption and CPD Calculation*, SCAA035
- *Selecting the Right Texas Instruments Signal Switch*, SZZA030

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision R (October 2023) to Revision S (February 2024)** — **Page**

- Updated thermal values for DBV package from RθJA = 225.7 to 278, RθJC(top) = 160.3 to 180.5, RθJB = 59.4 to 184.4, ΨJT = 41.0 to 115.4, ΨJB = 58.7 to 183.4, RθJC(bot) = N/A, all values in °C/W ...................... 5

**Changes from Revision Q (February 2014) to Revision R (October 2023)** — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Updated thermal values for DCK package: RθJA = 287.6 to 289.2, all values in °C/W ..................................5
- Added thermal values for DCK package: RθJC(top) = 205.8, RθJB = 176.2, ΨJT = 117.6, ΨJB = 175.1, RθJC(bot) = N/A, all values in °C/W ..........................................................................................................5

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC1G14DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | (38SH, 3C2F, A143, A14G, A14J, A 14L, A14S) | Samples |
| SN74AHC1G14DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (3C1F, A14G) | Samples |
| SN74AHC1G14DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (3C1F, A14G) | Samples |
| SN74AHC1G14DBVT | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI | -40 to 125 | (A143, A14G, A14J, A14S) | |
| SN74AHC1G14DCK3 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Non-Green | SNBI | Level-1-260C-UNLIM | -40 to 125 | AFY | Samples |
| SN74AHC1G14DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | (1R9, AF3, AFG, AF J, AFL, AFS) | Samples |
| SN74AHC1G14DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | Call TI | Call TI | -40 to 125 | AF3 | Samples |
| SN74AHC1G14DCKT | OBSOLETE | SC70 | DCK | 5 | | TBD | Call TI | Call TI | -40 to 125 | (AF3, AFG, AFJ, AF S) | |
| SN74AHC1G14DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AF3 | Samples |
| SN74AHC1G14DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AF3 | Samples |
| SN74AHC1G14DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AFS | Samples |
| SN74AHC1G14DRLRG4 | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AFS | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHC1G14 :**

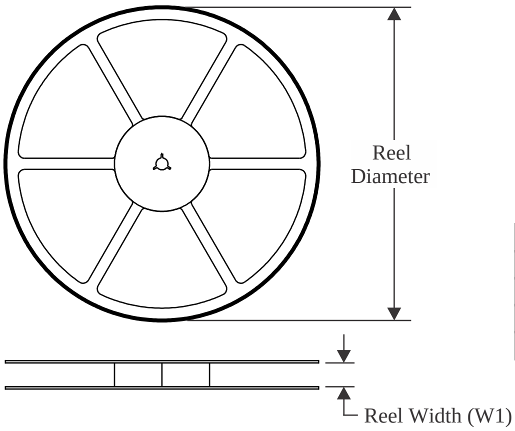
- Automotive : SN74AHC1G14-Q1

NOTE: Qualified Version Definitions:

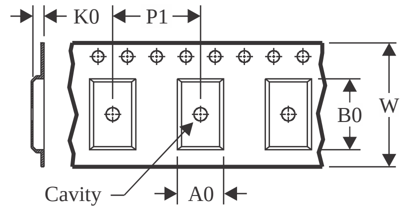
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

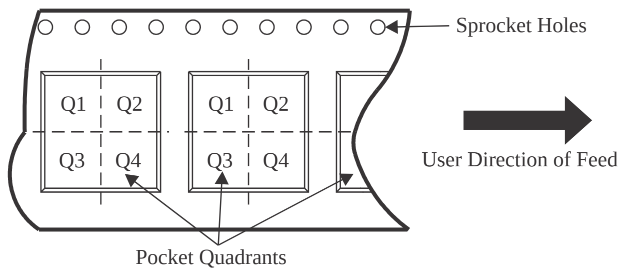



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

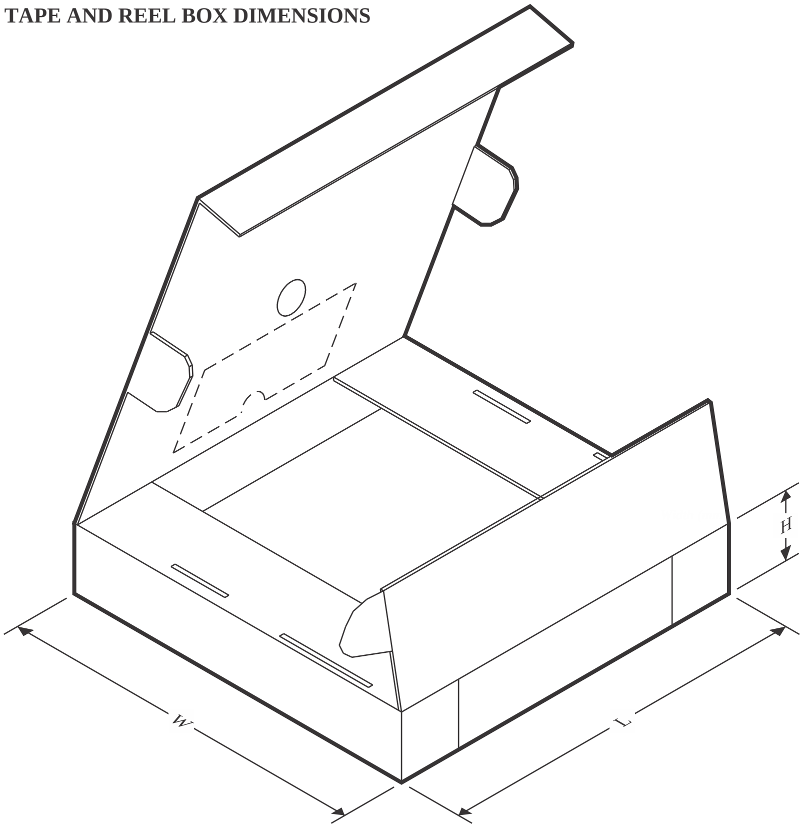
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

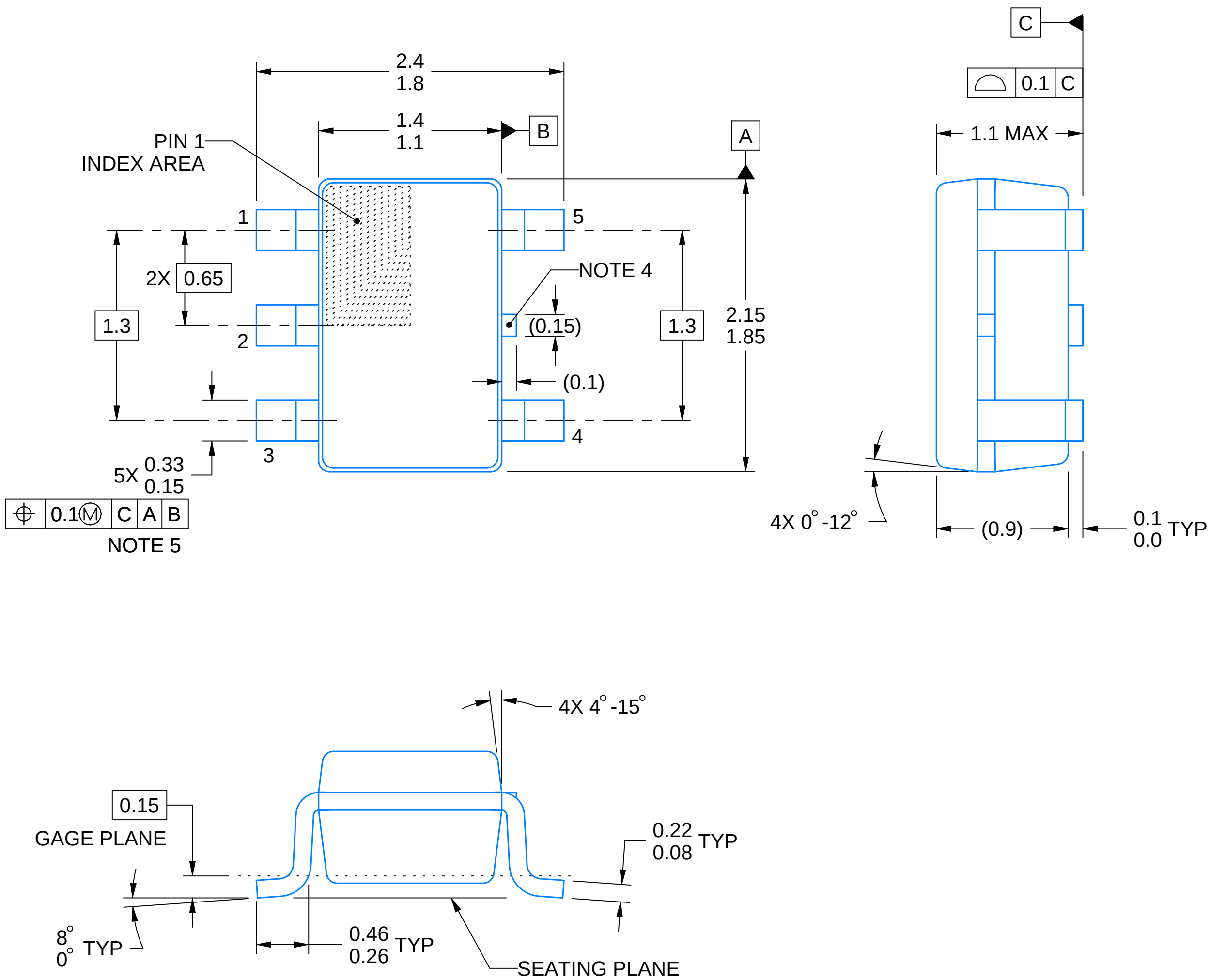
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC1G14DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHC1G14DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G14DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G14DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G14DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

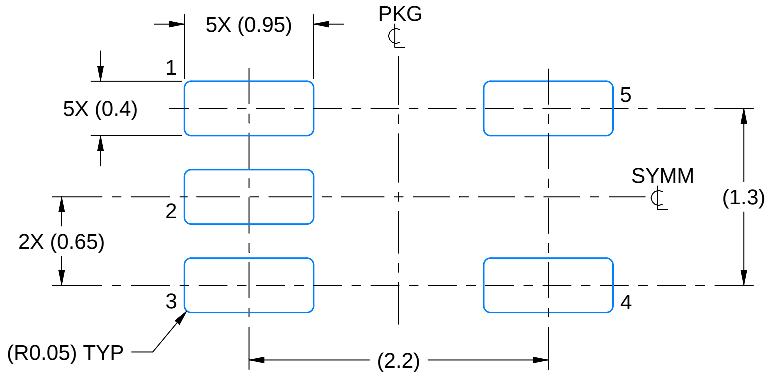
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC1G14DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G14DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G14DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G14DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G14DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |



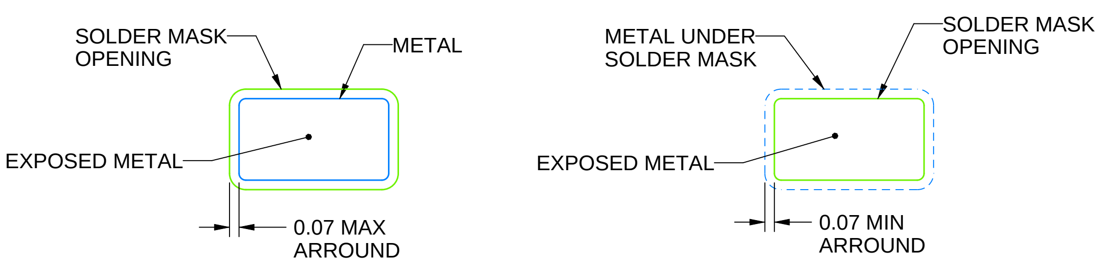

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X




NON SOLDER MASK DEFINED (PREFERRED)

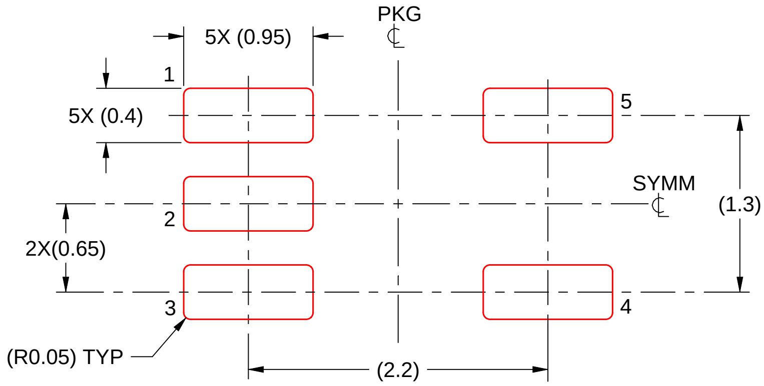
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

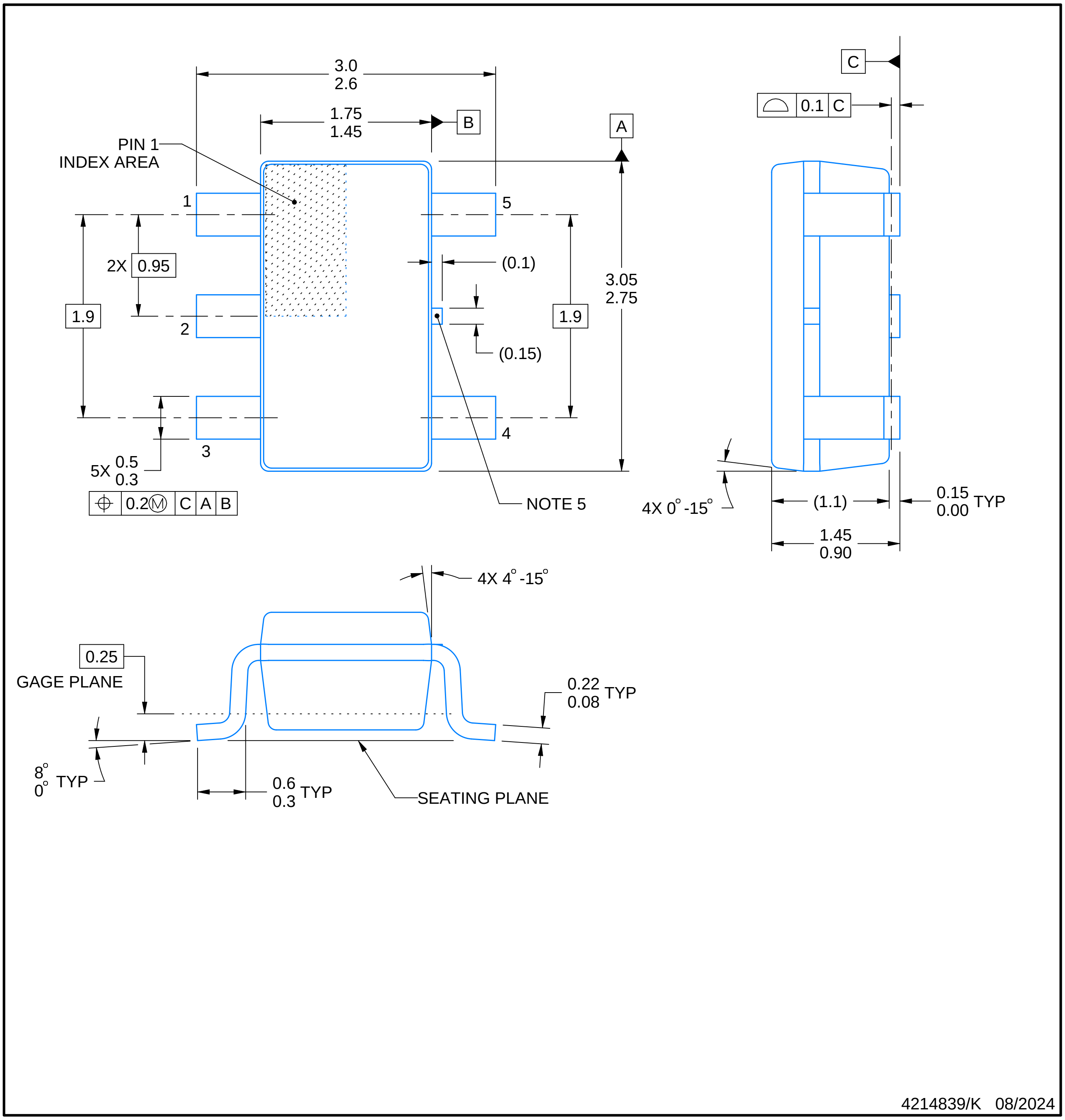



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

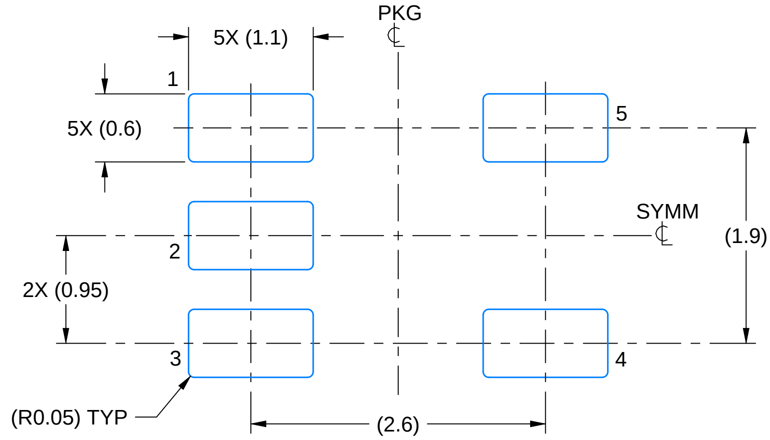
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

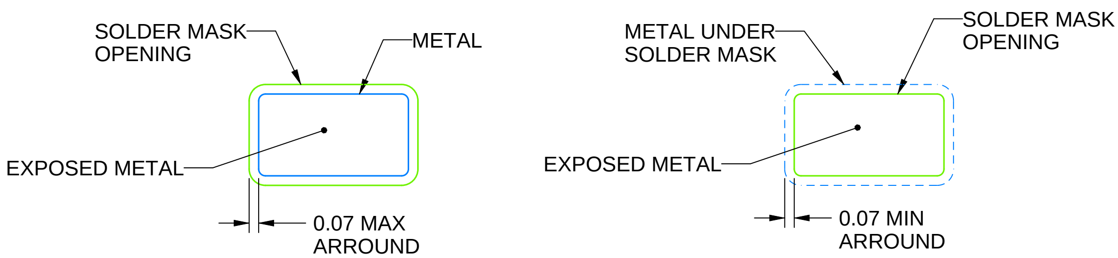



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




NON SOLDER MASK DEFINED (PREFERRED)

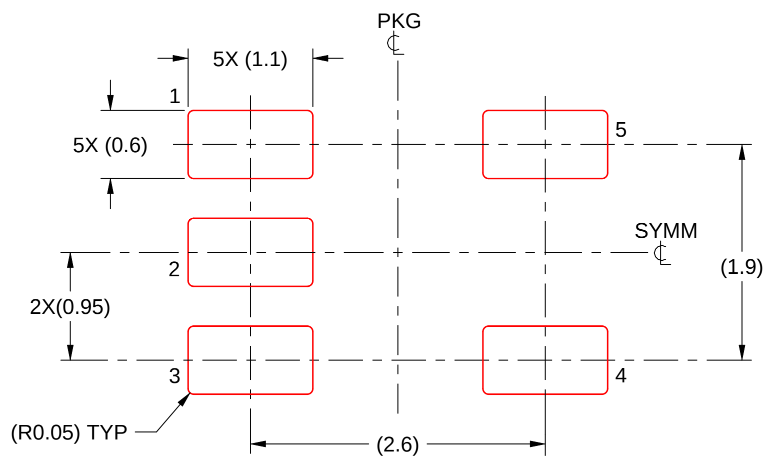
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

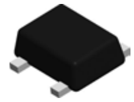



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

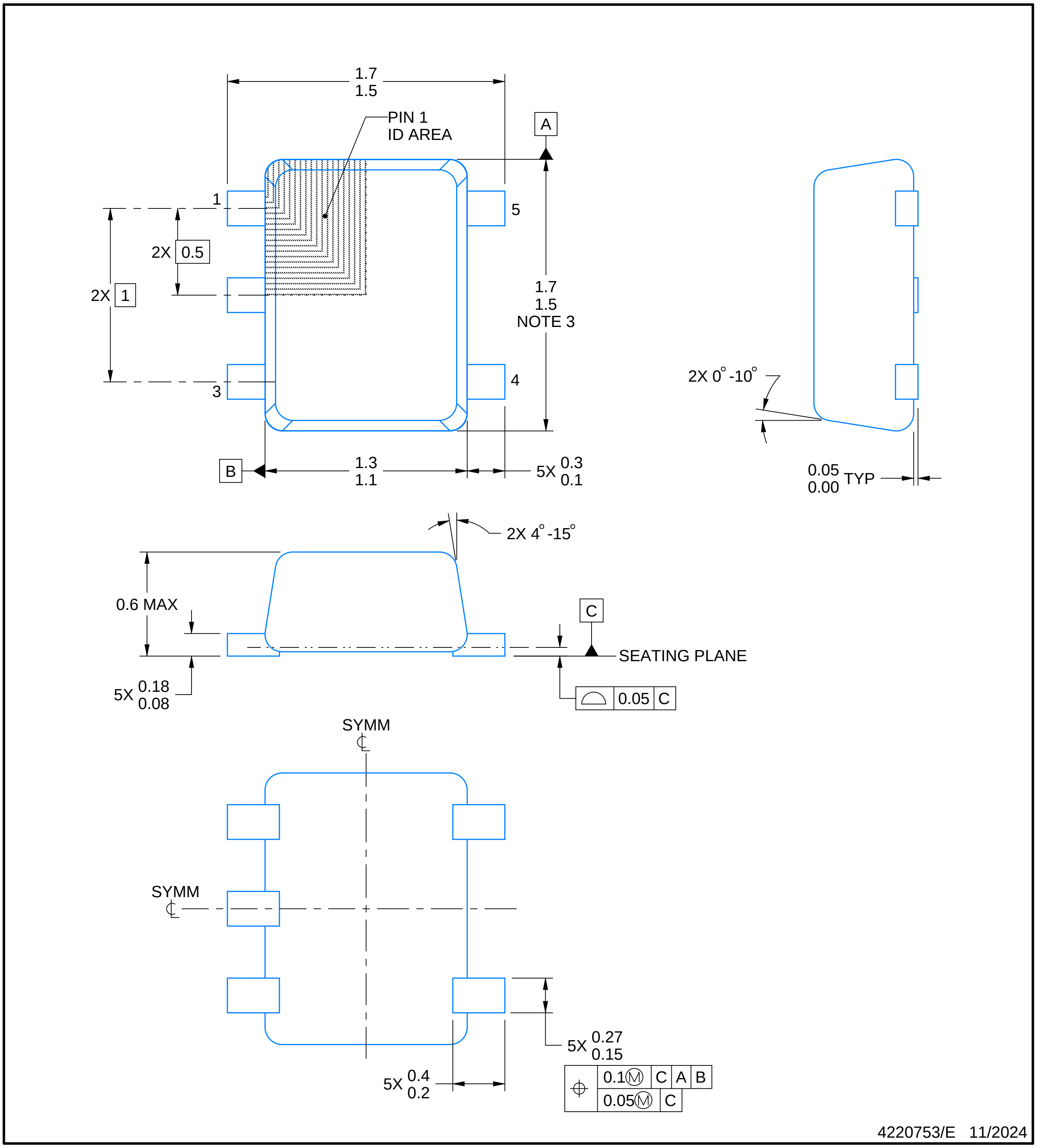
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

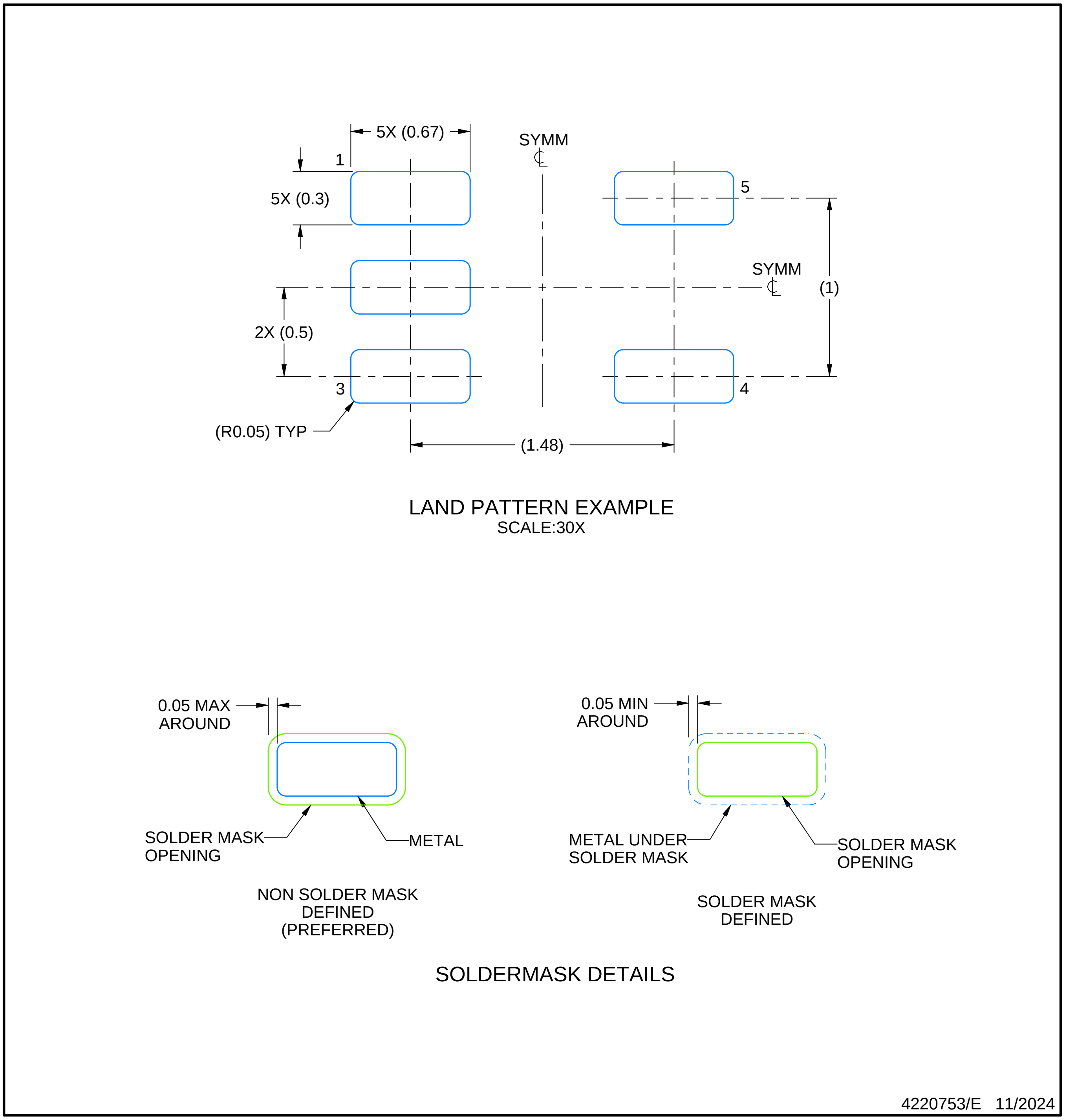
## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



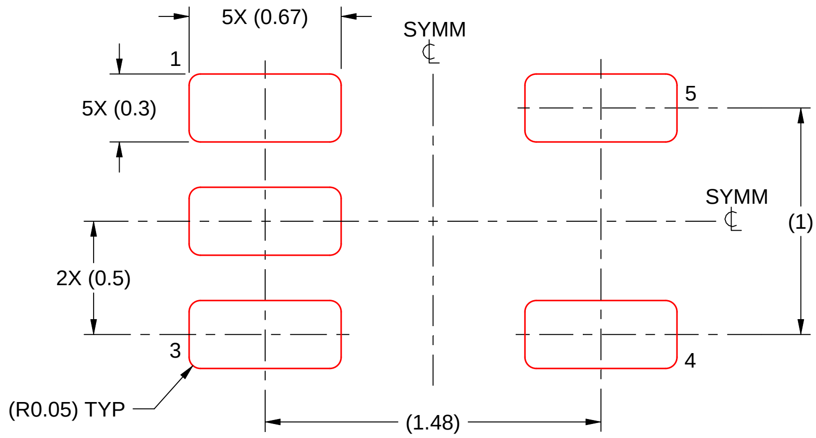

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.