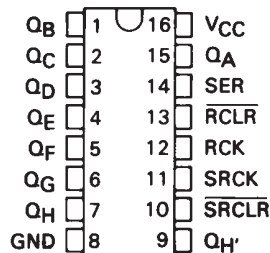


SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

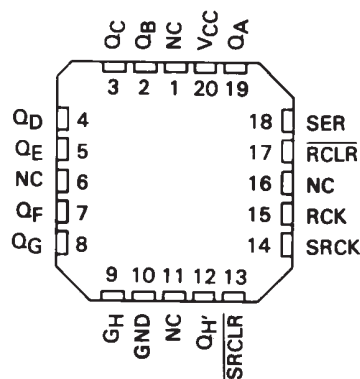
SDLS005 – D2747, JUNE 1983 – REVISED MARCH 1988

- **8-Bit Serial-In, Parallel-Out Shift Registers with Storage**
- **Choice of Output Configurations:**
'LS594 ... Buffered
'LS599 ... Open-Collector
- **Guaranteed Shift Frequency:**
DC to 20 MHz
- **Independent Direct-Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Both Shift and Storage Registers**

SN54LS594, SN54LS599 . . . J OR W PACKAGE
SN74LS594, SN74LS599 . . . N PACKAGE
(TOP VIEW)



SN54LS594, SN54LS599 . . . FK PACKAGE
(TOP VIEW)



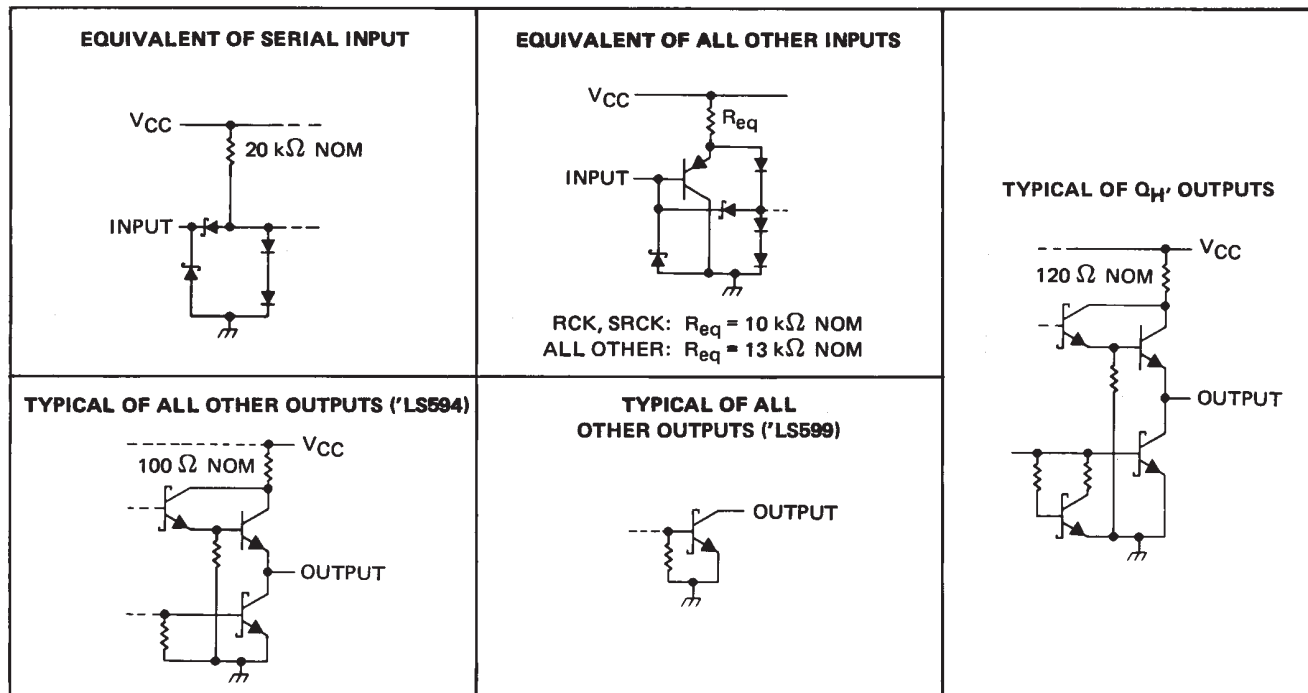
description

These devices each contain an 8-bit D-type storage register. The storage register has buffered ('LS594) or open-collector ('LS599) outputs. Separate clocks and direct-overriding clears are provided on both the shift and storage registers. A shift output (Q_H') is provided for cascading purposes.

Both the shift register and the storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one clock pulse ahead of the storage register.

NC — No internal connection

schematics of inputs and outputs



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

SDLS005 – D2747, JUNE 1983 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS'		SN74LS'		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5		V		
V _{OH}	'LS594 Q Q _H '	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA		2.4 3.2		V	
			I _{OH} = -2.6 mA		2.4 3.1			
			I _{OH} = -1 mA		2.4 3.2			
I _{OH}	'LS599 Q	V _{CC} = MIN, V _{OH} = 5.5 V	V _{IH} = 2 V, V _{IL} = MAX,	0.1		0.1	mA	
V _{OL}	Q Q _H '	V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V,	I _{OL} = 12 mA		0.25 0.4		V
				I _{OL} = 24 mA		0.35 0.5		
				I _{OL} = 8 mA		0.25 0.4		
				I _{OL} = 16 mA		0.35 0.5		
I _I		V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20		20	μA
I _{IL}	SER	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA
	All others				-0.2		-0.2	
I _{OS} §	'LS594 Q	V _{CC} = MAX, V _O = 0			-30 -130		-30 -130	mA
	Q _H '				-20 -100		-20 -100	
I _{CCH}	'LS594	V _{CC} = MAX, All possible inputs grounded,			34 50		34 50	mA
	'LS599				30 45		30 45	
I _{CCL}	'LS594	All outputs open			42 65		42 65	mA
	'LS599				38 55		38 55	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS594			'LS599			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	SRCK↑	Q _H '	R _L = 1 kΩ, C _L = 30 pF	12 18			12 18			ns
t _{PHL}				15 23			17 25			
t _{PLH}	RCK↑	Q _A thru Q _H	R _L = 667 Ω, C _L = 45 pF	12 18			28 42			ns
t _{PHL}				20 30			24 35			
t _{PHL}	SRCLR↓	Q _H '	R _L = 1 kΩ, C _L = 30 pF	22 33			24 35			ns
t _{PHL}	RCLR↓	Q _A thru Q _H	R _L = 667 Ω, C _L = 45 pF	38 57			40 60			ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

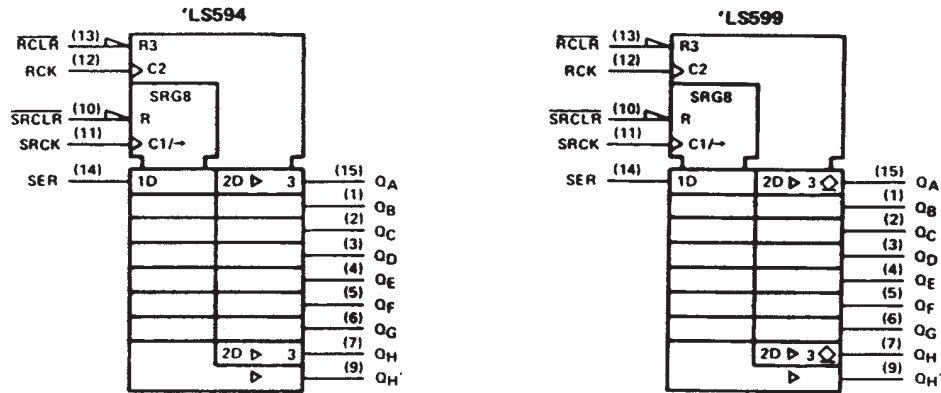


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SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

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logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS594, SN54LS599	-55°C to 125°C
SN74LS594, SN74LS599	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current	Q_A thru Q_H , 'LS599 only						mA
		Q_H'			-1		-1	
I_{OL}	Low-level output current	Q_A thru Q_H , 'LS594 only						mA
		Q_H'			-1		-2.6	
I_{OL}	Low-level output current	Q			8		16	mA
					12		24	
f_{SRCK}	Shift clock frequency	0		20	0		20	MHz
f_{RCK}	Register clock frequency	0		25	0		25	MHz
$t_w(SRCK)$	Duration of shift clock pulse	25			25			ns
$t_w(RCK)$	Duration of register clock pulse	20			20			ns
$t_w(SRCLR)$	Duration of shift clear pulse, low level	20			20			ns
$t_w(RCLR)$	Duration of register clear pulse, low level	35			35			ns
t_{su}	Setup time	SRCLR inactive before SRCK↑		20		20		ns
		SER before SRCK↑		20		20		
		SRCK↑ before RCK↑ (see Note 2)		40		40		
		SRCLR low before RCK↑		40		40		
		RCLR high before RCK↑		20		20		
t_h	Hold time	SER after SRCK↑		0		0		ns
T_A	Operating free-air temperature		-55	125		0	70	$^{\circ}\text{C}$

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.

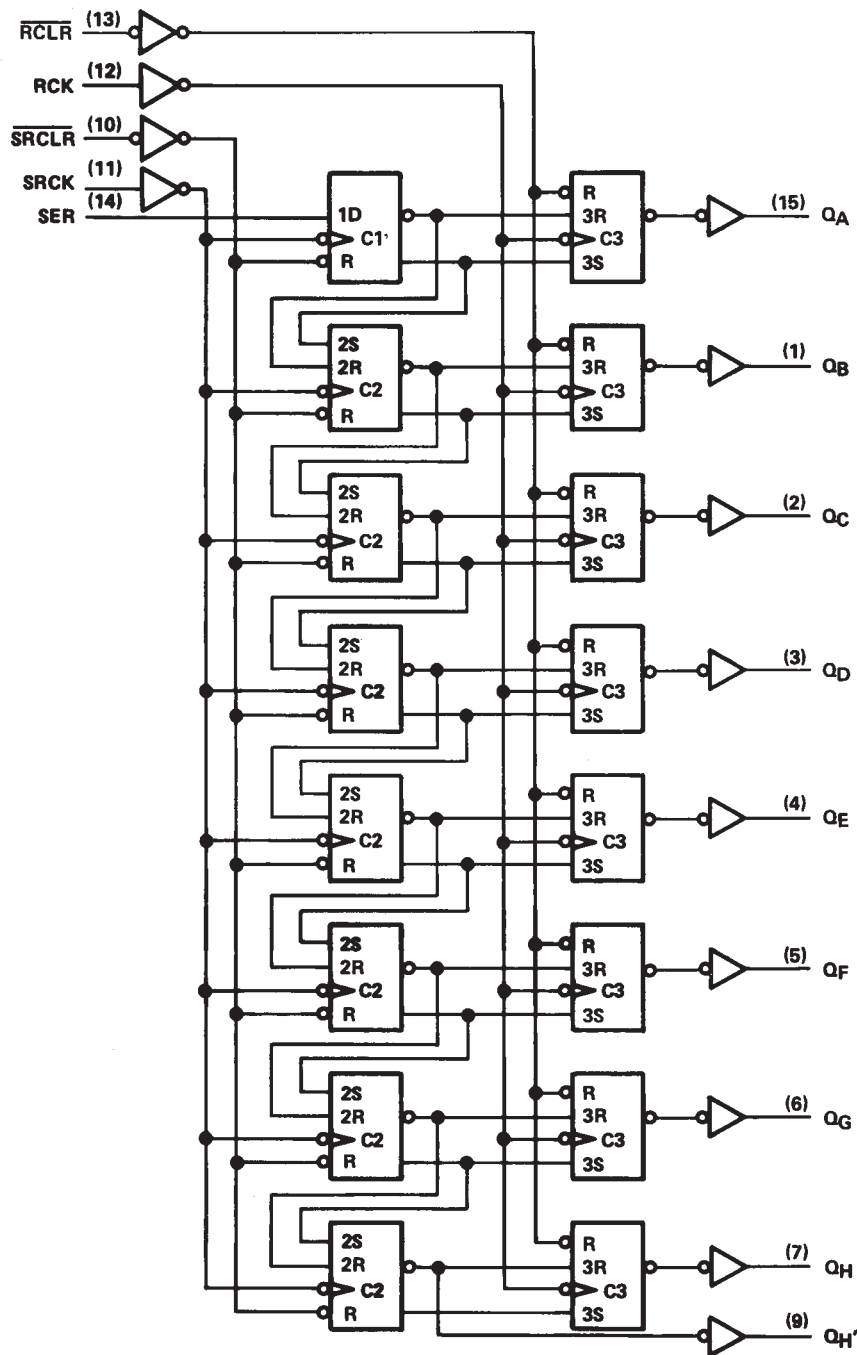


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SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

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logic diagram (positive logic)



Pin numbers shown are for J, N, and W packages.



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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS594NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS594NSR	SO	NS	16	2000	346.0	346.0	33.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS594N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS594N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS594N	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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