SN54LVTH16501, SN74LVTH16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- **Members of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVTH16501 . . . WD PACKAGE
SN74LVTH16501 . . . DGG OR DL PACKAGE
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
$\overline{OEBA}$	27	30	CLKBA
LEBA	28	29	GND
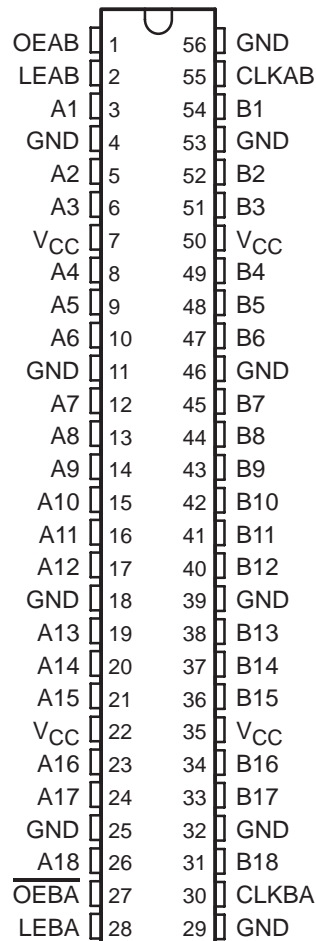
description/ordering information

The 'LVTH16501 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74LVTH16501DL	LVTH16501
		Tape and reel	SN74LVTH16501DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH16501DGGR	LVTH16501
−55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16501WD	SNJ54LVTH16501WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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1

description/ordering information (continued)

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE[†]

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0[‡]
H	L	L	X	B_0[§]

[†] A-to-B data flow is shown; B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
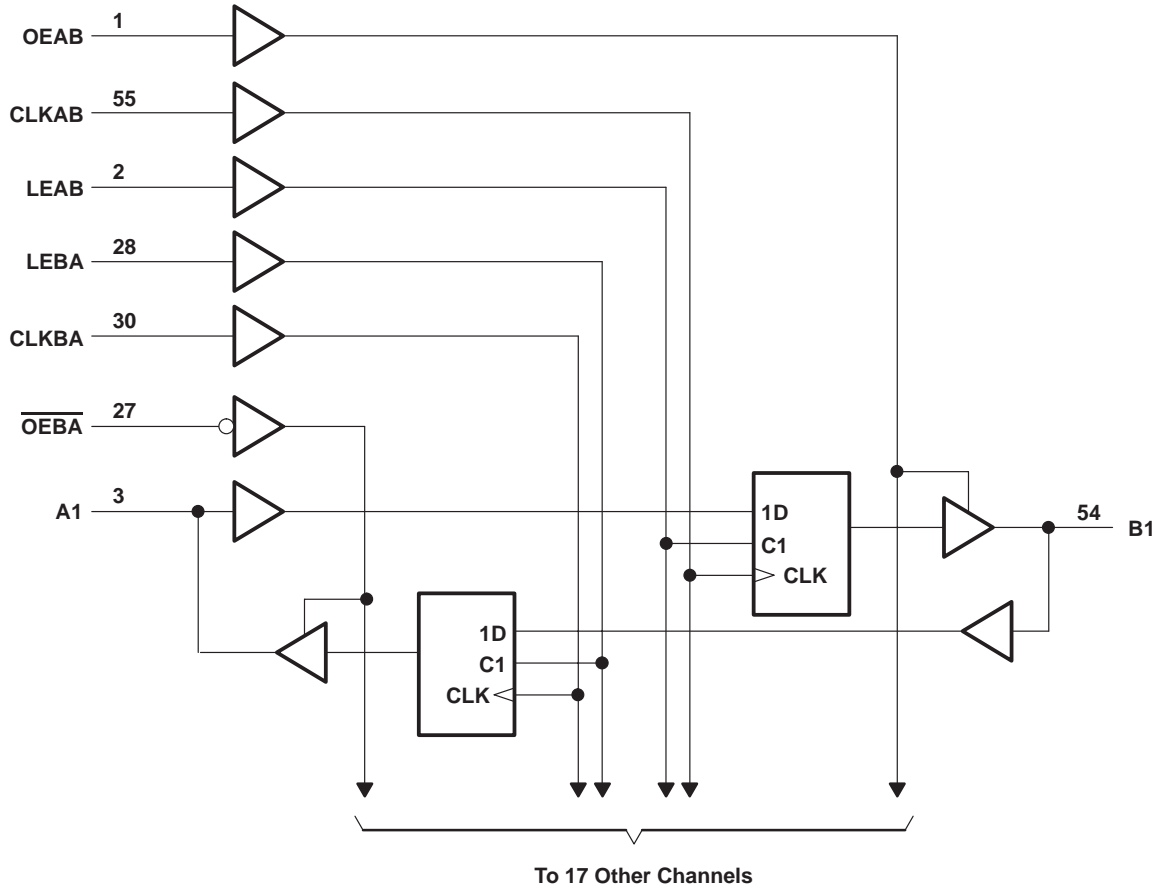
[§] Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)

To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the high-impedance
  or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O: SN54LVTH16501 . . . . 96 mA
                                                     SN74LVTH16501 . . . . 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16501 . . . . 48 mA
                                                       SN74LVTH16501 . . . . 64 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . 64°C/W
                                                 DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
        3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH16501		SN74LVTH16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16501			SN74LVTH16501			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B ports‡	V_{CC} = 3.6 V	V_I = 5.5 V			120			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	A or B ports	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V§,	V_I = 0 to 3.6 V						±500	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$/OE = don't care				±100*			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$/OE = don't care				±100*			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}¶		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0				4			4	pF
C_{io}		V_O = 3 V or 0				10			10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Unused pins at V_{CC} or GND
§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS INSTRUMENTS

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH16501				SN74LVTH16501				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before CLKAB↑	2.5		2.8		2.1		2.4		ns
		B before CLKBA↑	2.5		2.8		2.1		2.4		
		A or B before LE↓ — CLK high	3.4		2.8		2.4		1.6		
		A or B before LE↓ — CLK low	2.2		1.3		1.4		0.5		
t_h	Hold time	A or B after CLK↑	2.2		1.5		1		0		ns
		A or B after LE↓	2.1		1.9		1.7		1.7		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16501				SN74LVTH16501					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	B or A	A or B	1.2	4.3		4.7	1.3	2.7	3.7		4	ns
t_{PHL}			1.2	4.3		4.6	1.3	2.4	3.7		4	
t_{PLH}	LEBA or LEAB	A or B	1.4	6.2		6.6	1.5	3.4	5.1		5.7	ns
t_{PHL}			1.4	5.9		6.5	1.5	3.5	5.1		5.7	
t_{PLH}	CLKBA or CLKAB	A or B	1.2	6		6.7	1.3	3.5	5.1		5.7	ns
t_{PHL}			1.2	5.9		6.6	1.3	3.4	5.1		5.7	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.5		5.9	1.3	3.4	4.8		5.5	ns
t_{PZL}			1.2	5.5		5.9	1.3	3.4	4.8		5.5	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	1.6	6.3		6.7	1.7	4.2	5.8		6.3	ns
t_{PLZ}			1.6	6.1		6.6	1.7	3.8	5.8		6.3	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION

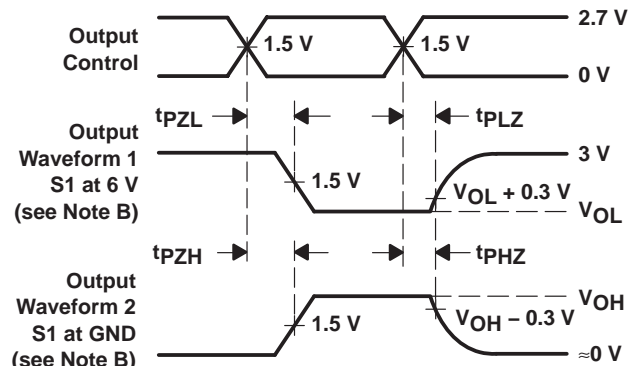| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
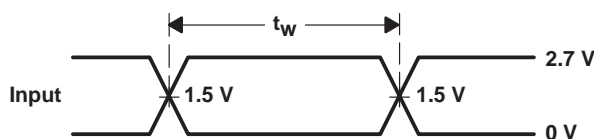
VOLTAGE WAVEFORMS
PULSE DURATION
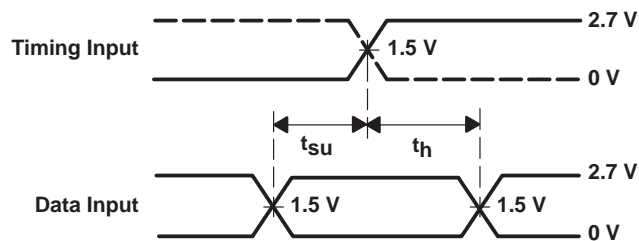
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
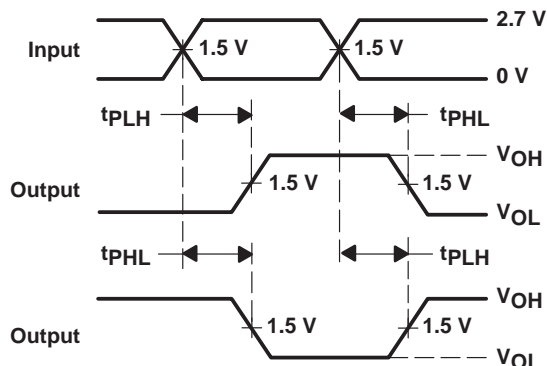
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVTH16501DGGRE4	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16501	Samples
SN74LVTH16501DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16501	Samples
SN74LVTH16501DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16501	Samples
SN74LVTH16501DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16501DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVTH16501DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16501DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74LVTH16501DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
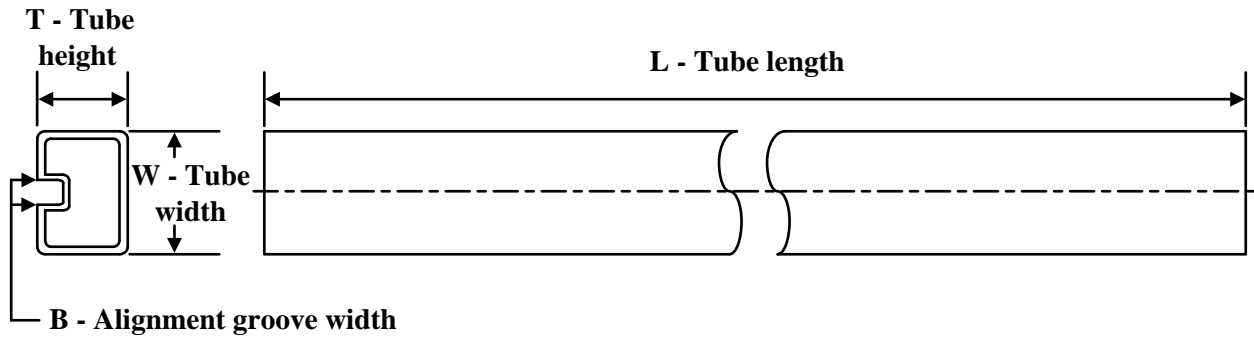
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTH16501DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

4040048−4/F 05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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8.3
7.9 TYP

A

PIN 1 ID
AREA

54X 0.5

56

14.1
13.9
NOTE 3

2X
13.5

1

28

29

B

6.2
6.0

56X 0.27
0.17

⊕ 0.08Ⓜ C AⓈ BⓈ

C

SEATING PLANE

▱ 0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM

56

28

29

SYMM

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222167/A   07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DGG0056A

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05) TYP

SYMM

SYMM

56

28

29

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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