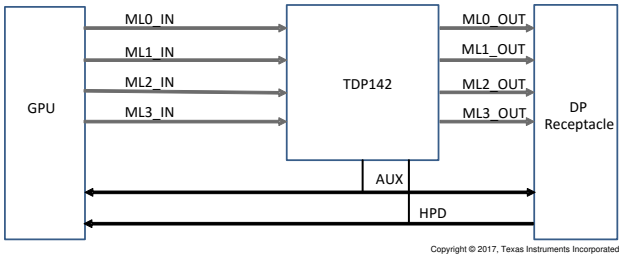
TDP142-Q1 DisplayPort™ 8.1Gbps Linear Redriver

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature: –40°C to 105°C, T_A
- DisplayPort™ 1.4 up to 8.1Gbps (HBR3)
- Ultra-low-power architecture
- Linear redriver with up to 12dB at 4.05GHz equalization
- Transparent to DisplayPort™ link training
- Configuration through GPIO or I^2C
- Hot-Plug capable
- Support DisplayPort™ dual-mode standard version 1.1 (AC-coupled HDMI)
- Available in a 7mm × 5mm, 0.5mm pitch VQFN package

2 Applications

- Rear seat entertainment
- Automotive head unit
- Automotive infotainment and cluster
- Active cables



Simplified Schematic

3 Description

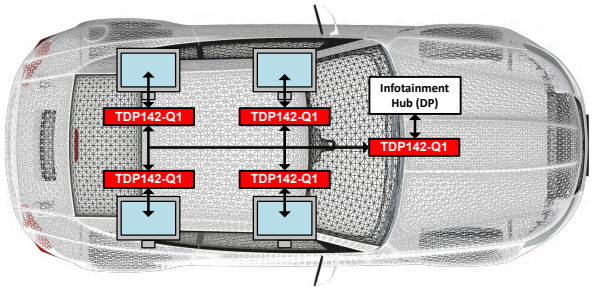
The TDP142-Q1 is a DisplayPort™ (DP) linear redriver that is able to snoop AUX and HPD signals. The device complies with the VESA® DisplayPort™ standard Version 1.4, and supports a 1-lane to 4-lane Main Link interface signaling up to HBR3 (8.1Gbps per lane). Additionally, this device is position independent. The TDP142-Q1 can be placed inside source, cable or sink effectively providing a "negative loss" component to the overall link budget.

The TDP142-Q1 provides several levels of receive linear equalization to compensate for cable and board trace loss due to inter symbol interference (ISI). The TDP142-Q1 operates on a single 3.3V supply and comes in an automotive grade 2 temperature range.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TDP142-Q1	RGF (VQFN, 40)	7mm × 5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Use Case

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4 Pin Configuration and Functions

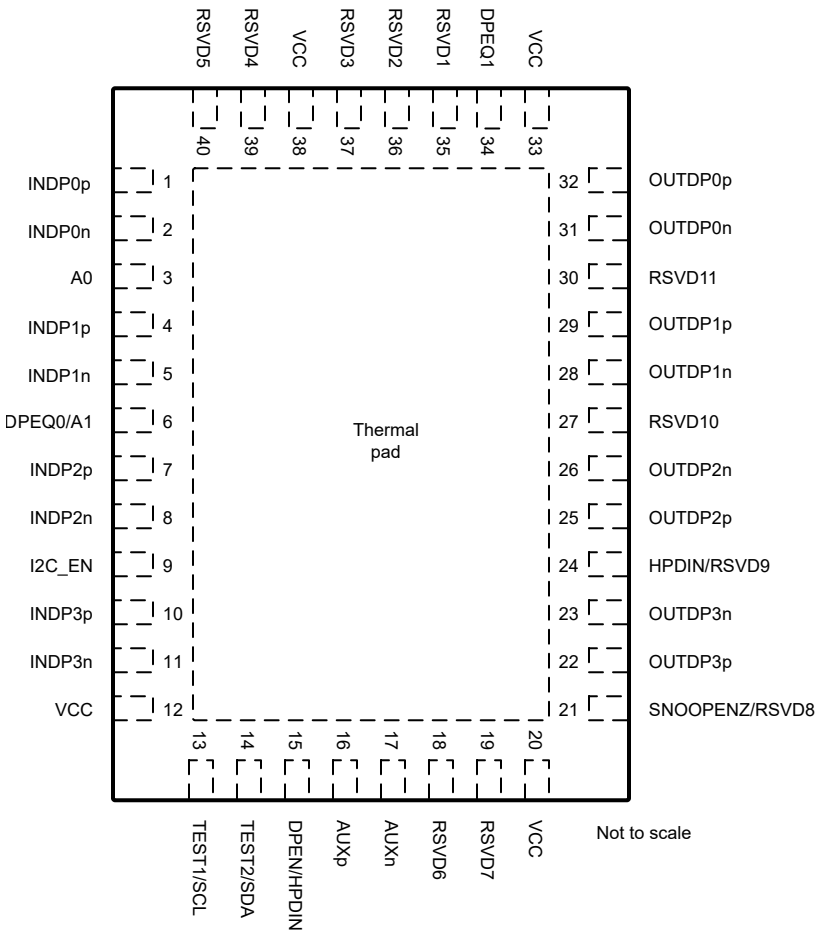

Figure 4-1. RGF Package 40-Pin (VQFN) Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INDP0p	1	I	DP Differential positive input for DisplayPort Lane 0.
INDP0n	2	I	DP Differential negative input for DisplayPort Lane 0.
A0	3	4 Level I	When I2C_EN = 0, leave the pin unconnected. When I2C_EN is not '0', this pin also sets the TDP142-Q1 I^2C address. See Table 6-4. If I2C_EN = "F", then this pin must be set to "F" or "0".
INDP1p	4	Diff I	DP Differential positive input for DisplayPort Lane 1.
INDP1n	5	Diff I	DP Differential negative input for DisplayPort Lane 1.
DPEQ0/A1	6	4 Level I	DisplayPort Receiver EQ control. This along with DPEQ1 selects the DisplayPort receiver equalization gain. Refer to Table 6-2 for equalization settings. When I2C_EN is not '0', this pin also sets the TDP142-Q1 I^2C address. See Table 6-4.
INDP2p	7	Diff I	DP Differential positive input for DisplayPort Lane 2.
INDP2n	8	Diff I	DP Differential negative input for DisplayPort Lane 2.

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Table 4-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
I2C_EN	9	4 Level I	I²C Programming Mode or GPIO Programming Select. I²C is only disabled when this pin is '0". 0 = GPIO mode (I²C disabled). R = TI Test Mode (I²C enabled at 3.3V). F = I²C enabled at 1.8V when RSVD11 = "0" and RSVD10 = "0". Otherwise, GPIO mode (I²C disabled) 1 = I²C enabled at 3.3 V.
INDP3p	10	Diff I	DP Differential positive input for DisplayPort Lane 3.
INDP3n	11	Diff I	DP Differential negative input for DisplayPort Lane 3.
VCC	12, 20, 33, 38	P	3.3V Power Supply.
TEST1/SCL	13	2 Level I	When I2C_EN='0', pull down with 10k or directly connect to ground. Otherwise this pin is I²C clock. When used for I²C clock, pull up this pin to the VCC I²C supply of the I²C controller.
TEST2/SDA	14	2 Level I	When I2C_EN='0' , pull down with 10k or directly connect to ground. Otherwise this pin is I²C data. When used for I²C data, pull up this pin to the VCC I²C supply of the I²C controller.
DPEN/HPDIN	15	2 Level I (Failsafe) (PD)	DP Enable Pin. When I2C_EN = '0', this pin enables or disables the DisplayPort functionality. Otherwise, when I2C_EN is not "0", DisplayPort functionality is enabled and disabled through I²C registers. L = DisplayPort Disabled. (Pull down with 10k resistor) H = DisplayPort Enabled. (Pull up with 10k resistor) When I2C_EN is not "0" this pin is an input for Hot Plug Detect (HPD) received from DisplayPort sink. When this HPDIN is low for greater than 2ms, all DisplayPort lanes are disabled.
AUXp	16	I/O, CMOS	This pin along with AUXN is used by the TDP142-Q1 for AUX snooping. See the *Application and Implementation* section for more detail.
AUXn	17	I/O, CMOS	This pin along with AUXP is used by the TDP142-Q1 for AUX snooping. See the *Application and Implementation* section for more detail.
RSVD6	18	I/O, CMOS	Reserved.(1)
RSVD7	19	I/O, CMOS	Reserved.(1)
SNOOPENZ/RSVD8	21(2)	I/O (PD)	When I2C_EN ! = 0, this pin is reserved. When I2C_EN = 0 , this pin is SNOOPENZ (L = AUX snoop enabled and H = AUX snoop disabled with all lanes active).
OUTDP3p	22	Diff O	DP Differential positive output for DisplayPort Lane 3.
OUTDP3n	23	Diff O	DP Differential negative output for DisplayPort Lane 3.
HPDIN/RSVD9	24(2)	I/O (PD)	When I2C_EN ! = 0, this pin is reserved. When I2C_EN = 0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is low for greater than 2ms, all DisplayPort lanes are disabled.
OUTDP2p	25	Diff O	DP Differential positive output for DisplayPort Lane 2.
OUTDP2n	26	Diff O	DP Differential negative output for DisplayPort Lane 2.
RSVD10	27	I	Reserved. Connect to GND when 1.8V I²C is used, otherwise leave pin floating.
OUTDP1n	28	Diff O	DP Differential negative output for DisplayPort Lane 1.
OUTDP1p	29	Diff O	DP Differential positive output for DisplayPort Lane 1.
RSVD11	30	I	Reserved. Connect to GND when 1.8V I²C is used, otherwise leave pin floating.
OUTDP0n	31	Diff O	DP Differential negative output for DisplayPort Lane 0.
OUTDP0p	32	Diff O	DP Differential positive output for DisplayPort Lane 0.
DPEQ1	34	4 Level I	DisplayPort Receiver EQ control. This along with DPEQ0 selects the DisplayPort receiver equalization gain. Refer to Table 6-2 for equalization settings.
RSVD1	35	I	Reserved.(1)
RSVD2	36	O	Reserved.(1)
RSVD3	37	O	Reserved.(1)
RSVD4	39	I	Reserved.(1)
RSVD5	40	I	Reserved.(1)

(1) Leave unconnected on PCB.
(2) Not a fail-safe I/O. Actively driving pin high while VCC is removed results in leakage voltage on VCC pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{CC}	–0.3	4	V
Voltage range at any input or output pin	Differential voltage between positive and negative inputs	–2.5	2.5	V
	Voltage at differential inputs	–0.5	4	V
	CMOS Inputs	–0.5	4	V
Maximum junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), all pins	±2000	V
		Charged-device model (CDM), per AEQ Q100-011, all pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	3.0	3.3	3.6	V
	Main supply ramp requirement	0.1		50	ms
$V_{(I2C)}$	Supply that external resistors are pulled up to on SDA and SCL	1.7		3.6	V
$V_{(PSN)}$	Supply noise on V_{CC} pins (less than 4MHz)			100	mV
T_A	Operating free-air temperature	–40		105	°C
T_{PCB}	PCB temperature (1mm away from the device)	–40		112	°C

5.4 Thermal Information

THERMAL METRIC(1)		Device RGF (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE--4DP)}$	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1Gbps; PRBS7 pattern; DPEN = H; LINR_L3;		500		mW
$P_{CC(HPDLOW--4DP)}$	Power 4 Lane DP Only when HPDIN = L	DPEN = H; HPDIN = L;		0.475		mW

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(DISABLED-I2C)}$	Device disabled power in I^2C Mode	I2C_EN != 0; HPDIN = L; CTLSEL = 0x0;		0.122		mW
$P_{CC(DISABLED)}$	Device disabled power	DPEN = L; I2C_EN = 0; HPDIN = L;		0.110		mW

5.6 Control I/O DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-level Inputs						
I_{IH}	High level input current	V_{CC} = 3.6V; V_{IN} = 3.6V	20		60	µA
I_{IL}	Low level input current	V_{CC} = 3.6V; V_{IN} = 0V	–100		-40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3V		0.55		V
4-Level V_{TH}	Threshold R/ Float	V_{CC} = 3.3V		1.65		V
4-Level V_{TH}	Threshold Float / 1	V_{CC} = 3.3V		2.7		V
R_{PU}	Internal pullup resistance			48		kΩ
R_{PD}	Internal pulldown resistance			98		kΩ
2-State CMOS Input						
V_{IH}	High-level input voltage	V_{CC} = 3.0V	2		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 3.6V	0		0.8	V
R_{PD}	Internal pulldown resistance for HPDIN, CADSNK		400	500	600	kΩ
R_{PD}	Internal pulldown resistance for DPEN		400	500	600	kΩ
I_{IH_DPEN}	High-level input current for DPEN	V_{IN} = 3.6V	–11		11	µA
I_{IL_DPEN}	Low-level input current for DPEN	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
$I_{IH\_HPD\_CAD}$	High-level input current for HPDIN, CADSNK	V_{IN} = 3.6V	–11		11	µA
$I_{IL\_HPD\_CAD}$	Low-level input current for HPDIN, CADSNK	V_{IN} = GND, V_{CC} = 3.6V	–1		1	µA
I^2C Control Pins (SCL, SDA)						
V_{IH_3p3V}	High-level input voltage when configured for 3.3V I^2C level	I2C_EN = 1	2.0		3.6	V
V_{IL_3p3V}	Low-level input voltage when configured for 3.3V I^2C level	I2C_EN = 1	0		0.8	V
V_{IH_1p8V}	High-level input voltage when configured for 1.8V I^2C level	I2C_EN = F	1.2			V
V_{IL_1p8V}	Low-level input voltage when configured for 1.8V I^2C level	I2C_EN = F	0		0.6	V
V_{OL}	Low-level output voltage	I2C_EN = 0; I_{OL} = 6mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN = 0; V_{OL} = 0.4V	20			mA
$I_{I(I2C)}$	Input current	0.1 × $V_{(I2C)}$ < Input voltage < 3.3V	–1		1	µA
$C_{I(I2C)}$	Input capacitance				10	pF
$C_{(I2C\_FM+\_BUS)}$	I^2C bus capacitance for FM+ (1MHz)				150	pF
$C_{(I2C\_FM\_BUS)}$	I^2C bus capacitance for FM (400kHz)				150	pF
$R_{(EXT\_I2C\_FM+)}$	External resistors on both SDA and SCL when operating at FM+ (1MHz)	$C_{(I2C\_FM+\_BUS)}$ = 150pF	620	820	910	Ω
$R_{(EXT\_I2C\_FM)}$	External resistors on both SDA and SCL when operating at FM (400kHz)	$C_{(I2C\_FM\_BUS)}$ = 150pF	620	1500	2200	Ω

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5.7 DP Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC Characteristics						
$CP_{LF-LINRL0}$	Low-frequency –1dB compression point at LINR_L0 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		600		mVppd
$CP_{HF-LINRL0}$	High-frequency –1dB compression point at LINR_L0 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		550		mVppd
$CP_{LF-LINRL1}$	Low-frequency –1dB compression point at LINR_L1 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		700		mVppd
$CP_{HF-LINRL1}$	High-frequency –1dB compression point at LINR_L1 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		650		mVppd
$CP_{LF-LINRL2}$	Low-frequency –1dB compression point at LINR_L2 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		800		mVppd
$CP_{HF-LINRL2}$	High-frequency –1dB compression point at LINR_L2 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		750		mVppd
$CP_{LF-LINRL3}$	Low-frequency –1dB compression point at LINR_L3 setting.	At 100MHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		900		mVppd
$CP_{HF-LINRL3}$	High-frequency –1dB compression point at LINR_L3 setting.	At 5GHz, 200mVpp < V_{ID} < 1200mVpp, EQ = 0		830		mVppd
t_{TX_DJ}	TX output deterministic residual jitter	VID = 0.8Vppd; Optimal EQ setting; 12in prechannel (SDD21 = –8.2dB at 5GHz); 1.6in post channel (SDD21 = –1.8dB at 5GHz); PRBS7; DP at 8.1Gbps		0.04		UI
DisplayPort Receiver						
$V_{ID(PP)}$	Peak-to-peak input differential dynamic voltage range			1400		V
V_{IC}	Input common-mode voltage		0	1.75	2	V
$V_{RX\_CM-INST}$	Maximum instantaneous RX DC common-mode voltage change under following operating states: OFF to ON, Disabled to 4DP low power, 4DP active to Disabled. (1)	Measured single-ended at non-redriver side of AC-coupling capacitor with 200kΩ load.	–1200		1000	mV
$V_{RX\_CM-INST}$	Maximum instantaneous RX DC common-mode voltage change under following operating states: Disabled to 4DP active (D0), D0 to D3, D3 to D0.	Measured single-ended at non-redriver side of AC-coupling capacitor with 50Ω load.	–500		1000	mV
d_R	Data rate				8.1	Gbps
$R_{(ti)}$	Input termination resistance		75	90	110	Ω
$C_{(AC)}$	External required AC-coupling capacitor		75		265	nF
E_{Q_DP0}	DP0 Receiver equalization at 100MHz	DP0EQ_SEL = 0;		–0.2		dB
E_{Q_DP15}	DP0 Receiver equalization at 100MHz	DP0EQ_SEL = 15;		2.3		dB
E_{Q_DP0}	DP0 Receiver equalization at 4.05GHz	DP0EQ_SEL = 0;		0.6		dB
E_{Q_DP15}	DP0 Receiver equalization at 4.05GHz	DP0EQ_SEL = 15;		14.5		dB
DisplayPort Transmitter						
$V_{TX-CM-INST}$	Maximum instantaneous TX DC common-mode voltage change for following operating states: Disabled to 4DP active (D0), D0 to D3, D3 to D0.	Measured at non-redriver side of AC-coupling capacitor with 50Ω load.	–500		1000	mV
$V_{TX-CM-INST}$	Maximum instantaneous TX DC common-mode voltage change under following operating states: Disabled to 4DP low power, 4DP active to Disabled	Measured at non-redriver side of AC-coupling capacitor with 200kΩ load.	–1000		1000	mV
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)		0.6		1	V
$R_{TX(DIFF)}$	Differential impedance of the driver		80	90	120	Ω

(1) Instantaneous common mode excursions observed by GPU (DPTX) can be minimized by disabling redriver prior to disabling DPTX termination.

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5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HPDIN						
$t_{HPDIN\_DEBOUNCE}$	DPEN and HPDIN debounce time when transitioning from H to L.		2		10	ms
I²C						
f_{SCL}	I²C clock frequency				1	MHz
t_{BUF}	Bus-free time between START and STOP conditions	Refer to Figure 6-1	0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	Refer to Figure 6-1	0.26			µs
t_{LOW}	Low period of the I²C clock	Refer to Figure 6-1	0.5			µs
t_{HIGH}	High period of the I²C clock	Refer to Figure 6-1	0.26			µs
t_{SUSTA}	Setup time for a repeated START condition	Refer to Figure 6-1	0.26			µs
t_{HDDAT}	Data hold time	Refer to Figure 6-1	0.008			µs
t_{SUDAT}	Data setup time	Refer to Figure 6-1	50			ns
t_R	Rise time of both SDA and SCL signals	Refer to Figure 6-1			120	ns
t_F	Fall time of both SDA and SCL signals	Refer to Figure 6-1	1.2		120	ns
t_{SUSTO}	Setup time for STOP condition	Refer to Figure 6-1	0.26			µs
C_b	Capacitive load for each bus line				150	pF

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5.9 Typical Characteristics

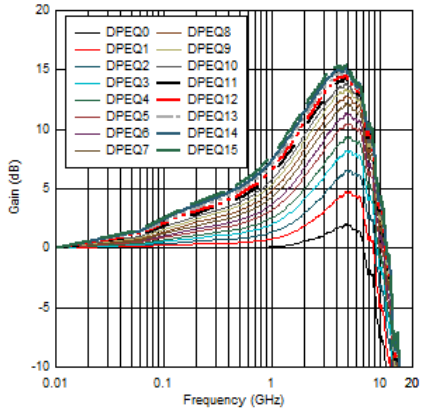

Figure 5-1. DisplayPort EQ Settings Curves

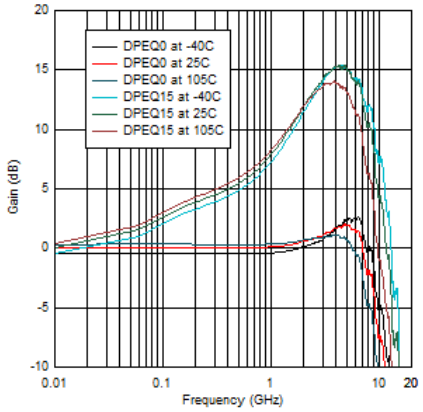

Figure 5-2. DisplayPort EQ Settings Curves Across Temperature

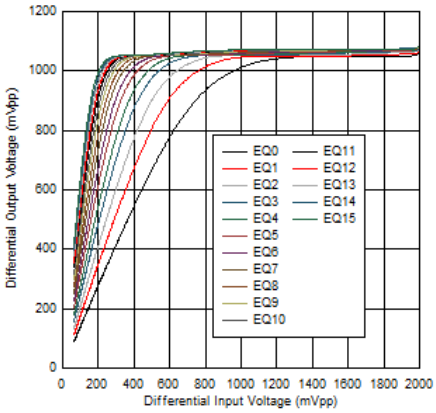

Figure 5-3. DisplayPort Linearity Curves at 4.05GHz

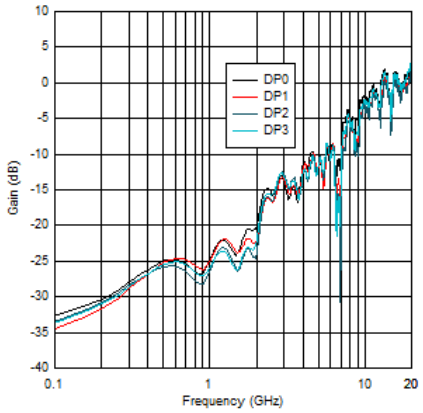

Figure 5-4. DisplayPort Input Return Loss Performance

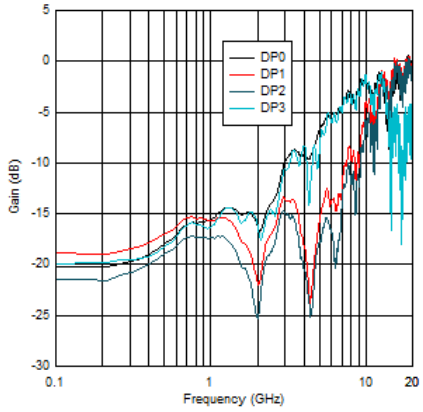

Figure 5-5. DisplayPort Output Return Loss Performance

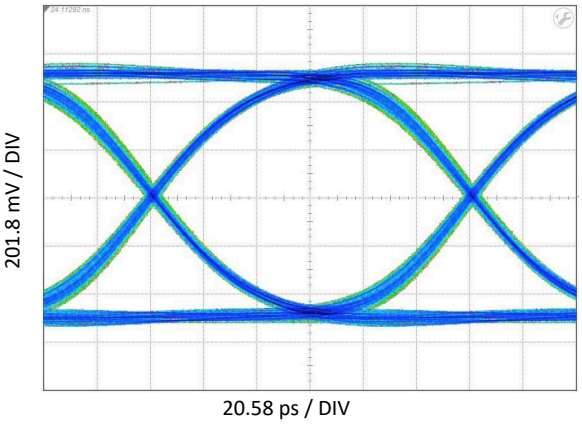

Figure 5-6. DisplayPort HBR3 Eye-Pattern Performance with 12in Input PCB Trace at 8.1Gbps

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5.9 Typical Characteristics (continued)

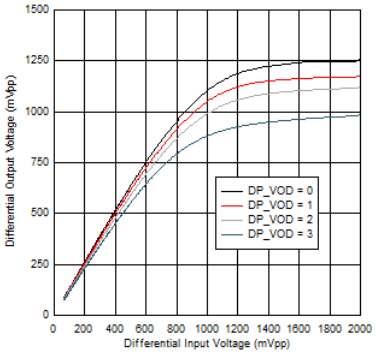

Figure 5-7. DP VOD Linearity Settings at 100MHz

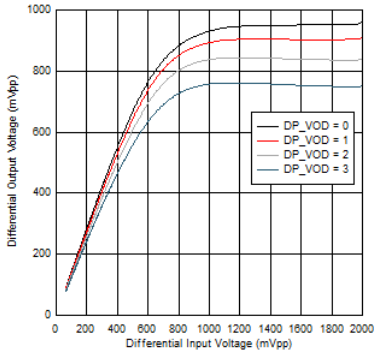

Figure 5-8. DP VOD Linearity Settings at 5GHz

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Parameter Measurement Information

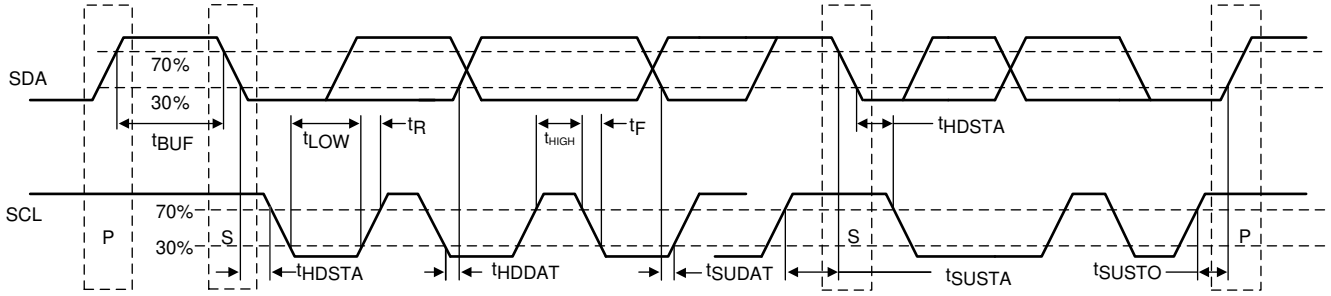

Figure 6-1. I²C Timing Diagram Definitions

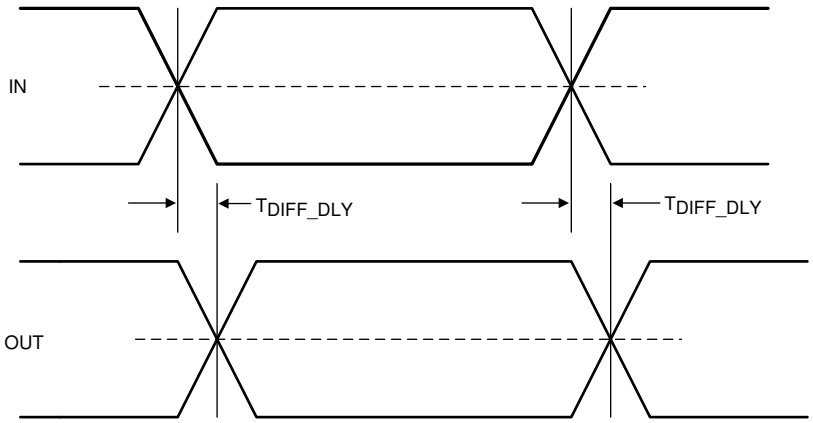

Figure 6-2. Propagation Delay

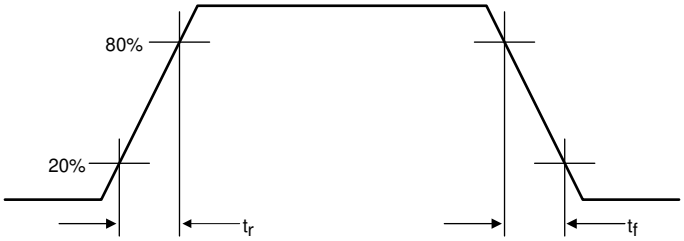

Figure 6-3. Output Rise and Fall Times

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6 Detailed Description

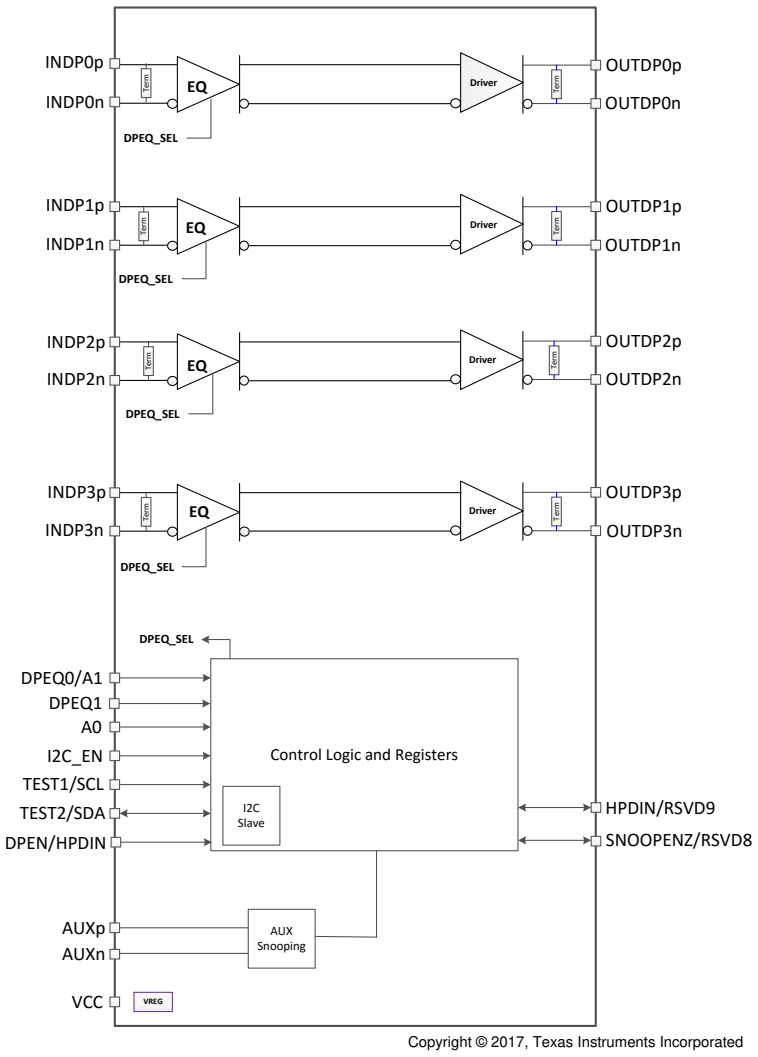
6.1 Overview

The TDP142-Q1 is a DisplayPort linear redriver that supports up to 8.1Gbps for each lane. Additionally, the transparency of the device to the DP link training makes the TDP142-Q1 a position independent device designed for source/sink or cable applications.

The TDP142-Q1 helps the system to pass compliance of both transmitter and receiver for DisplayPort version 1.4 HBR3. The redriver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. Set the equalization based on the amount of insertion loss before the TDP142-Q1 receivers. The equalization control can be controlled by DPEQ[1:0] pins or I^2C registers.

The device ultra-low-power architecture operates at a 3.3V power supply and achieves enhanced performance. Also, the TDP142-Q1 comes in a commercial temperature range and industrial temperature range.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 DisplayPort

The TDP142-Q1 supports up to four DisplayPort lanes at data rates up to 8.1Gbps (HBR3). The TDP142-Q1 monitors the native AUX traffic as the device traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TDP142-Q1 manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TDP142-Q1 snoops native AUX writes to the DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE) of the DisplayPort sink. The TDP142-Q1 disables or enables lanes based on the value written to LANE_COUNT_SET. The TDP142-Q1 disables all lanes when SET_POWER_STATE is in the D3. Otherwise active lanes are based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. When AUX snoop is disabled, the TDP142-Q1 DisplayPort lanes are controlled through various configuration registers. When TDP142-Q1 is enabled for GPIO mode (I2C_EN = "0"), the SNOOPENZ pin can be used to disable AUX snooping. When SNOOPENZ pin is high, the AUX snooping functionality is disabled and all four DisplayPort lanes are active.

6.3.2 Configuration Jumper Levels

The TDP142-Q1 EVM has 4-level inputs pins (I2C_EN, A0, and DPEQ[1:0]) that are used to control the equalization gain and place the TDP142-Q1 into different modes of operation. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings. There are internal pullup and pulldown resistors that can combine with the external resistor connection to achieve the desired voltage level

Table 6-1. 4-Level Configuration Jumper Settings

LEVEL	SETTINGS
Low	Tie 1kΩ 5% to GND.
R	Tie 20kΩ 5% to GND.
F	Float (leave pin open)
High	Tie 1kΩ 5% to V_{CC}.

Note

All 4-level inputs are latched on rising edge of internal reset. After t_{cfg_hd}, the internal pullup and pulldown resistors are isolated in order to save power.

6.3.3 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TDP142-Q1. The receiver overcomes these losses by attenuating the low-frequency components of the signals with respect to the high-frequency components. Select the proper gain setting to match the channel insertion loss before the input of the TDP142-Q1 receivers. Two 4-level inputs pins enable up to 16 possible equalization settings. The TDP142-Q1 also provides the flexibility of adjusting settings through I^2C registers.

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6.4 Device Functional Modes

6.4.1 Device Configuration in GPIO Mode

The TDP142-Q1 is in GPIO configuration when I2C_EN = “0”. The DPEN pin controls whether DisplayPort is enabled and SNOOPENZ pin controls whether AUX snoop mode is enabled.

6.4.2 Device Configuration in I^2C Mode

The TDP142-Q1 is in I^2C mode when I2C_EN is not equal to “0”. The same configurations defined in GPIO mode are also available in I^2C mode. The TDP142-Q1 DisplayPort configuration is programmed based on the *Programming* section.

6.4.3 Linear EQ Configuration

The receiver equalization gain value can be controlled either through I^2C registers or through GPIOs. Table 6-2 details the gain value for each available combination when TDP142-Q1 is in GPIO mode. The I^2C mode can do the same option or even individual lane EQ setting by updating registers DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, and DP3EQ_SEL.

Table 6-2. TDP142-Q1 Receiver Equalization Control

REGISTER(S): DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, OR DP3EQ_SEL EQUALIZATION SETTING #	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN AT 2.7/4.05/5GHz MINUS GAIN AT 100MHz (dB)
0	0	0	0.4/0.8/0.83
1	0	R	2.0/3.1/3.4
2	0	F	3.0/4.6/5.0
3	0	1	4.2/6.0/6.5
4	R	0	5.0/7.0/7.5
5	R	R	6.0/8.0/8.4
6	R	F	6.5/8.7/9.1
7	R	1	7.2/9.4/9.8
8	F	0	7.8/10.0/10.3
9	F	R	8.3/10.4/10.7
10	F	F	8.7/10.7/10.9
11	F	1	9.1/11.1/11.2
12	1	0	9.4/11.3/11.3
13	1	R	9.7/11.5/11.5
14	1	F	10.0/11.7/11.6
15	1	1	10.2/11.8/11.7

ADVANCE INFORMATION

6.4.4 Operation Timing – Power Up

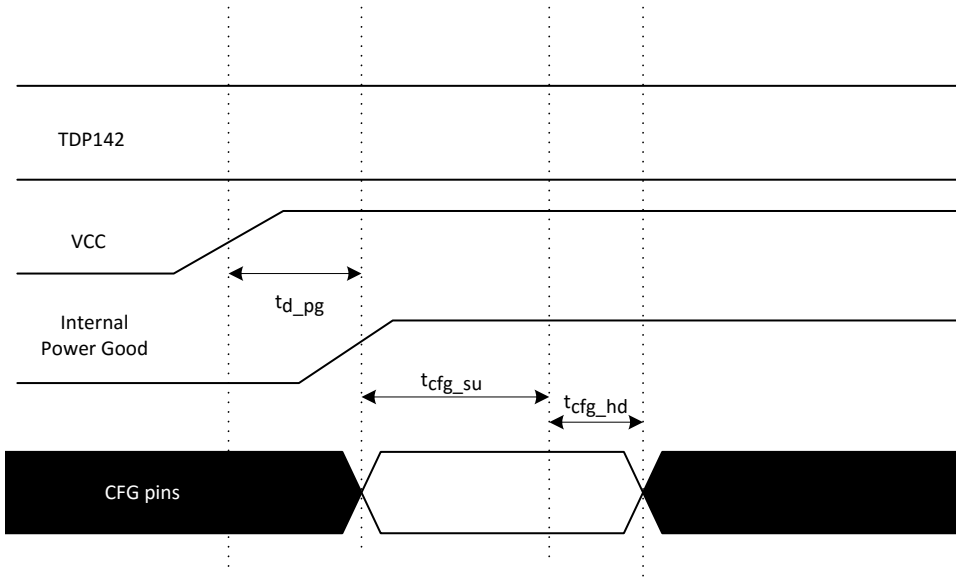

Figure 6-1. Power-Up Timing

Table 6-3. Power-Up Timing (1) (2)

PARAMETER		MIN	MAX	UNIT
t_{d_pg}	V_{CC} (minimum) to Internal Power Good asserted high		500	µs
t_{cfg_su}	CFG(1) pins setup(2)	50		µs
t_{cfg_hd}	CFG(1) pins hold	10		µs
t_{VCC_RAMP}	VCC supply ramp requirement		100	ms

(1) Following pins comprise CFG pins: I2C_EN, DPEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at min.

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6.5 Programming

For further programmability, the TDP142-Q1 can be controlled using I^{2}C. When I2C_EN !=0, the SCL and SDA pins are used for I^{2}C clock and I^{2}C data, respectively.

Table 6-4. TDP142-Q1 I^{2}C Target Address

DPEQ0/A1 PIN LEVEL	A0 PIN LEVEL	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

Use the following procedure to write to TDP142-Q1 I^{2}C registers:

1. The controller initiates a write operation by generating a start condition (S), followed by the TDP142-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP142-Q1 acknowledges the address cycle.
3. The controller presents the sub-address (I^{2}C register within TDP142-Q1) to be written, consisting of one byte of data, MSB-first.
4. The TDP142-Q1 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I^{2}C register.
6. The TDP142-Q1 acknowledges the byte transfer.
7. The controller can continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TDP142-Q1.
8. The controller terminates the write operation by generating a stop condition (P).

Use the following procedure to read the TDP142-Q1 I^{2}C registers:

1. The controller initiates a read operation by generating a start condition (S), followed by the TDP142-Q1 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TDP142-Q1 acknowledges the address cycle.
3. The TDP142-Q1 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I^{2}C register occurred prior to the read, then the TDP142-Q1 starts at the sub-address specified in the write.
4. The TDP142-Q1 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I^{2}C controller acknowledges reception of each data byte transfer.
5. If an ACK is received, the TDP142-Q1 transmits the next byte of data.
6. The controller terminates the read operation by generating a stop condition (P).

Use the following procedure for setting a starting sub-address for I^2C reads:

1. The controller initiates a write operation by generating a start condition (S), followed by the TDP142-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP142-Q1 acknowledges the address cycle.
3. The controller presents the sub-address (I^2C register within TDP142-Q1) to be written, consisting of one byte of data, MSB-first.
4. The TDP142-Q1 acknowledges the sub-address cycle.
5. The controller terminates the write operation by generating a stop condition (P).

Note

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I^2C controller terminates the read operation. If a I^2C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

Table 6-5. Register Legend

ACCESS TAG	NAME	MEANING
R	Read	The field can be read by software
W	Write	The field can be written by software
S	Set	The field can be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field can be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable

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7 Register Maps

7.1 TDP142-Q1 Registers

Table 7-1 lists the TDP142-Q1 registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. TDP142-Q1 Registers

Offset	Acronym	Register Name	Section
0xA	General_1	General Register	Go
0x10	DP01EQ_SEL	DisplayPort Lane 0 and 1 EQ Control	Go
0x11	DP23EQ_SEL	DisplayPort Lane 2 and 3 EQ Control	Go
0x12	DisplayPort_1	AUX Snoop Status	Go
0x13	DisplayPort_2	DP Lane Enable/Disable Control	Go
0x32	VOD_CTRL	VOD Linearity	Go

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. TDP142-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WS	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 General_1 Register (Offset = 0xA) [reset = 0x1]

General_1 is shown in Table 7-3.

Return to the Summary Table.

This register is used to select between disabled and DisplayPort modes. Software can set the EQ_OVERRIDE bit to use the EQ registers instead of pins.

Table 7-3. General_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	SWAP_HPDIN	R/W	0x0	Controls which pin HPDIN is derived from. 0x0 = HPDIN is in default location 0x1 = HPDIN location is swapped (PIN 23 to PIN 32, or PIN 32 to PIN 23).

Table 7-3. General_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EQ_OVERRIDE	R/W	0x0	Setting this field allows software to use EQ settings from registers instead of value sampled from pins. 0x0 = EQ settings based on sampled state of EQ pins. 0x1 = EQ settings based on programmed value of each of the EQ registers.
3	HPDIN_OVERRIDE	R/W	0x0	Overrides HPDIN pin state. 0x0 = HPD_IN based on HPD_IN pin. 0x1 = HPD_IN high.
2	RESERVED	R/W	0x0	RESERVED
1-0	CTLSEL	R/W	0x1	Upon power-on, software must write 0x2 to enable DisplayPort functionality. If DisplayPort funcitonality is not required, then software must write 0x0 to disable DisplayPort 0x0 = Disabled. DP disabled and lowest power state 0x1 = DP disabled but not lowest power state. 0x2 = DisplayPort enabled. 0x3 = Reserved

7.1.2 DP01EQ_SEL Register (Offset = 0x10) [reset = 0x0]

DP01EQ_SEL is shown in Table 7-4.

Return to the Summary Table.

This register controls the receiver equalization setting for the DisplayPort receivers 0 and 1.

Table 7-4. DP01EQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DP1EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 1 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 1 based on value written to this field.
3-0	DP0EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 0 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 0 based on value written to this field.

7.1.3 DP23EQ_SEL Register (Offset = 0x11) [reset = 0x0]

DP23EQ_SEL is shown in Table 7-5.

Return to the Summary Table.

This register controls the receiver equalization setting for the DisplayPort receivers 2 and 3.

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Table 7-5. DP23EQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DP3EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 3 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 3 based on value written to this field.
3-0	DP2EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 2 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 2 based on value written to this field.

7.1.4 DisplayPort_1 Register (Offset = 0x12) [reset = 0x0]

DisplayPort_1 is shown in Table 7-6.

Return to the Summary Table.

This register provides status of AUX snooping when AUX Snooping is enabled.

Table 7-6. DisplayPort_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-5	SET_POWER_STATE	RH	0x0	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 0b, the enable/disable of DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1b, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0h by hardware when CTLSEL1 changes from a 1b to a 0b.
4-0	LANE_COUNT_SET	RH	0x0	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 0b, DP lanes enabled specified by the snoop value. Unused DP lanes is disabled to save power. When AUX_SNOOP_DISABLE = 1b, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0h by hardware when CTLSEL1 changes from a 1b to a 0b.

7.1.5 DisplayPort_2 Register (Offset = 0x13) [reset = 0x0]

DisplayPort_2 is shown in Table 7-7.

Return to the Summary Table.

This register provides controls for enabling and disabling AUX snooping and individual DP lanes.

Table 7-7. DisplayPort_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0x0	Controls whether DP lanes are enabled based on AUX snooped value or registers. 0x0 = AUX snoop enabled. 0x1 = AUX snoop disabled. DP lanes are controlled by registers.
6	RESERVED	R	0x0	Reserved

Table 7-7. DisplayPort_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	RESERVED	R/W	0x0	Reserved
3	DP3_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 0b, changes to this field have no effect on lane 3 functionality. 0x0 = DP Lane 3 enabled. 0x1 = DP Lane 3 disabled.
2	DP2_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 0b, changes to this field have no effect on lane 2 functionality. 0x0 = DP Lane 2 enabled. 0x1 = DP Lane 2 disabled.
1	DP1_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 0b, changes to this field have no effect on lane 1 functionality. 0x0 = DP Lane 1 enabled. 0x1 = DP Lane 1 disabled.
0	DP0_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 0b, changes to this field have no effect on lane 0 functionality. 0x0 = DP Lane 0 enabled. 0x1 = DP Lane 0 disabled.

7.1.6 VOD_CTRL Register (Offset = 0x32) [reset = 0x40]

VOD_CTRL is shown in Table 7-8.

Return to the Summary Table.

This register controls the transmitters output linearity range.

Table 7-8. VOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0x1	Reserved
5-4	DP_VOD	R/W	0x0	VOD linearity control for DP paths. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)
3-0	Reserved	R/W	0x0	Reserved

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TDP142-Q1 is a linear redriver designed specifically to compensate the inter-symbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cable. The device can be used in source, sink, and cable applications, where the device is transparent to the link training. For illustrating purposes, this section shows the implementations of source application and sink application. Figure 8-1 and Figure 8-2 are the high level block diagram for DisplayPort source side application and DisplayPort sink side application respectively, where the TDP142-Q1 is snooping both channels of AUX signal and HPD signal.

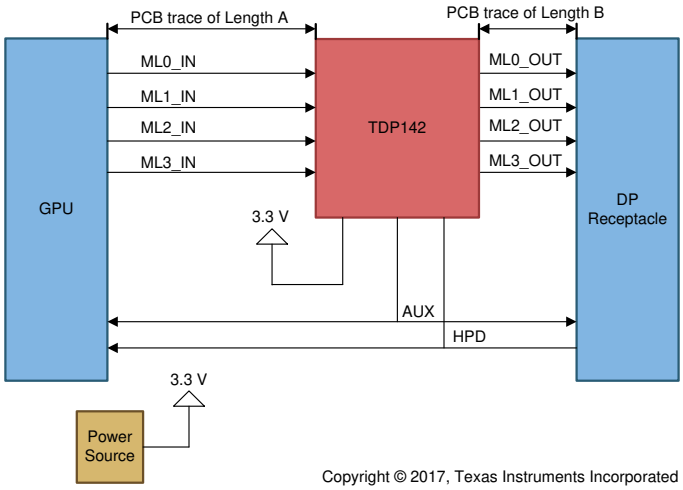

Figure 8-1. Source Application for TDP142-Q1

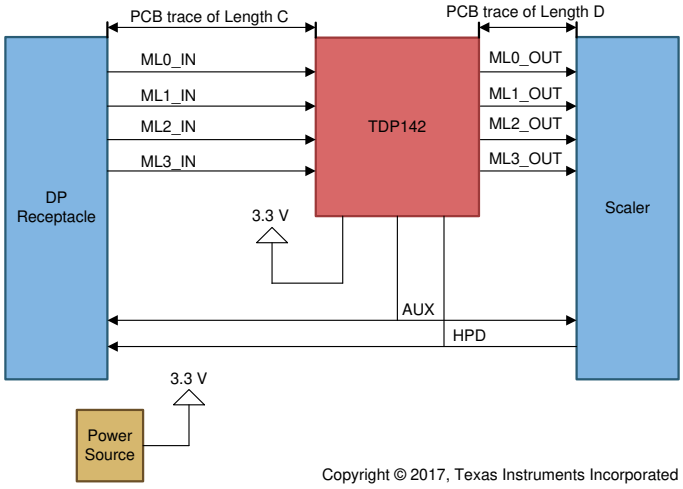

Figure 8-2. Sink Application for TDP142-Q1

8.1.1 ESD Protection

It may be necessary to incorporate an ESD component to protect the TDP142-Q1 from electrostatic discharge (ESD). TI recommends following the ESD protection recommendations listed in Table 8-1. A clamp voltage greater than value specified in Table 8-1 may require a R_{ESD} on each differential pin. Place the ESD component near the USB connector.

Table 8-1. ESD Diodes Recommended Characteristics

Parameter	Recommendation
Breakdown voltage	≥ 3.5V for DP input pins ≥ 1.5V for non-DP input pins
I/O line capacitance	Data rates ≤ 5Gbps: ≤ 0.50pF
	Data rates > 5Gbps: ≤ 0.35pF
Delta capacitance between any P and N I/O pins	≤ 0.07pF
Clamping voltage at 8A I_{PP} IO to GND(1)	≤ 4.5V
Typical dynamic resistance	≤ 30mΩ

(1) According to IEC 61000-4-5 (8/20µs current waveform)

Table 8-2. Recommended ESD Protection Component

Manufacturer	Part Number	R_{ESD} to support IEC 61000-4-2 Contact ±8kV
Nexperia	PUSB3FR4	1Ω
Nexperia	PESD2V8Y1BSF	1Ω
Texas Instruments	TPD1E04U04DPLR	2Ω
Texas Instruments	TPD4E02B04DQAR	2Ω

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8.2 Typical Application

8.2.1 Source Application Implementation

Figure 8-3 shows the schematic for the Source side application. The TDP142-Q1 is placed between the DisplayPort Graphics Processor Unit (GPU) and the DisplayPort receptacle. The TDP142-Q1 monitors AUX traffic for power management purposes when SNOOPENZ is low.

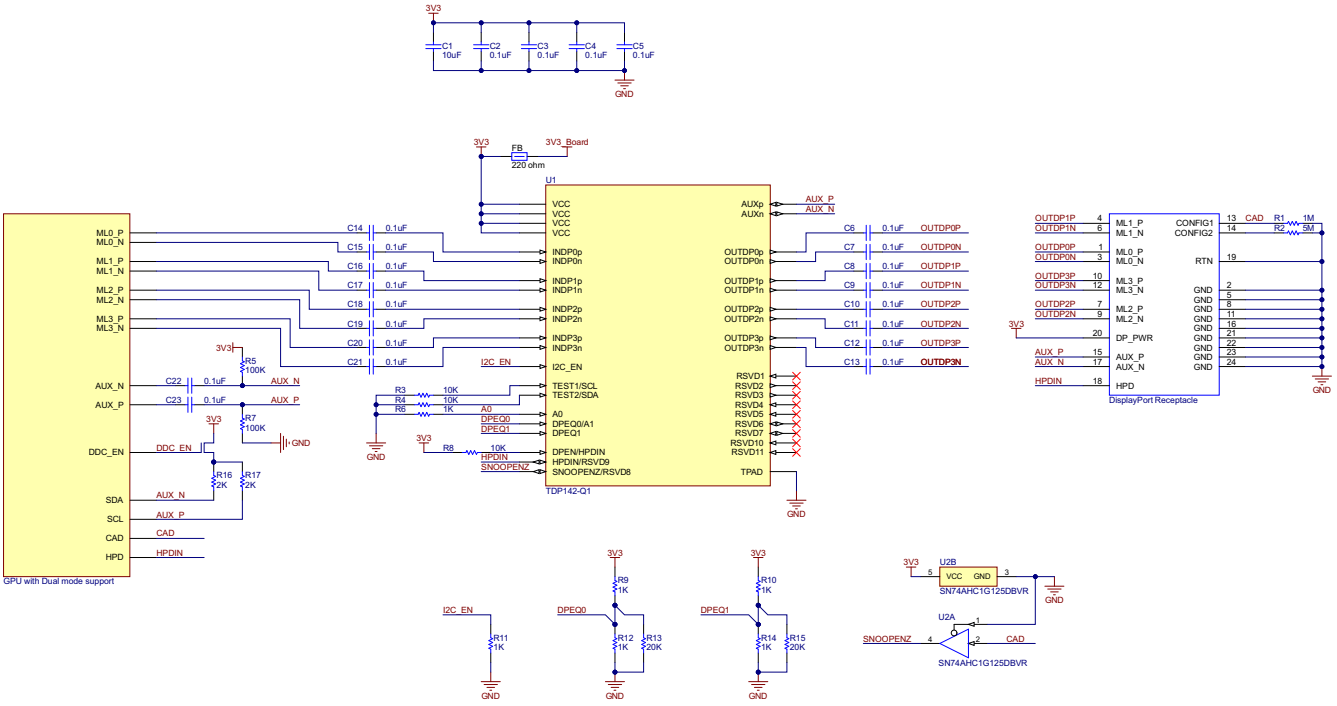

Figure 8-3. Block Diagram of DisplayPort Source Application

8.2.1.1 Design Requirement

The TDP142-Q1 can be designed into many types of applications. All applications have certain requirements for the system to work properly. For example, source application uses different hardware configuration on the HPD channel and AUX channel from a sink application. The device can be configured by using I^2C. However, the GPIO configuration is provided as I^2C is not available in all cases. Additionally, because sources may have different naming conventions, confirm the link between source and receptacle is correctly mapped through the TDP142-Q1.

Table 8-3. Design Parameters

PARAMETER	VALUE
Maximum Operating data rate (RBR, HBR, HBR2, or HBR3)	HBR3 (8.1Gbps)
Supply voltage	3.3V
Trace length/width of A	12 inch /6 mil width
Trace length/width of B	2 inch/ 6 mil width
Main link AC-decoupling capacitor (75nF to 265nF)	Recommend 100nF
Control mode (I^2C or GPIO)	GPIO (I2C_EN = 0)
Dual Mode DisplayPort Support (Yes/No)	Yes. SNOOPENZ must be connected to CONFIG1 thru a buffer.

8.2.1.2 Detail Design Procedure

Designing in the TDP142-Q1 requires the following:

- Determine the loss profile on the DisplayPort input (A) and output (B) channels. See Figure 8-5 for 6mil trace insertion loss.
- Based upon the loss profile, determine the optimal configuration for the TDP142-Q1, to pass electrical compliance. DPEQ[1:0] must be set to appropriate value. For this case, 12 inches of FR4 trace approximately equates to 8dB loss at 4.05GHz. Therefore, tie DPEQ1 20kΩ to ground and DPEQ0 1kΩ to ground.
- See Figure 8-3 for information on the source application that uses AC-coupling capacitors, control pin resistors, and the recommended decouple capacitors from VCC pins to ground.
  - AUX: Make sure the AUXP has a 100kΩ pulldown resistor and the AUXN has a 100kΩ pullup resistor. These 100kΩ resistors must be on the TDP142-Q1 side of the 100nF capacitors.
  - HPDIN is used to enable or disable DisplayPort functionality for power saving. Route the HPD signal to either pin 23 or pin 32 based on the GPIO/I^{2}C mode.

Table 8-4. HPD GPIO/I^{2}C Selection

MODE	HPD
GPIO (I2C_EN = 0)	Pin 32
I^{2}C (I2C_EN != 0)	Pin 23

  - For the application supporting Dual mode DisplayPort: SNOOPENZ pin must be connected to the CONFIG1 on DisplayPort Receptacle through a buffer like the SN74AHC125. The buffer is needed because the internal pulldown on SNOOPENZ pin is too strong to register a valid VIH when a Dual mode adapter is plugged into the DisplayPort receptacle.
- Configure the TDP142-Q1 using the GPIO terminals or the I^{2}C interface:
  - GPIO – Using the terminals DPEQ0 and DPEQ1.
  - I^{2}C – Refer to the *I2C Register Maps* and the *Programming* section for a detail configuration procedures.
- The thermal pad must be connected to ground.

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8.2.2 Sink Application Implementation

Figure 8-4 is the schematic for the sink application. The left side of the TDP142-Q1 is connected to DisplayPort receptacle, and the right side of the TDP142-Q1 is connected to Scaler or DisplayPort sink.

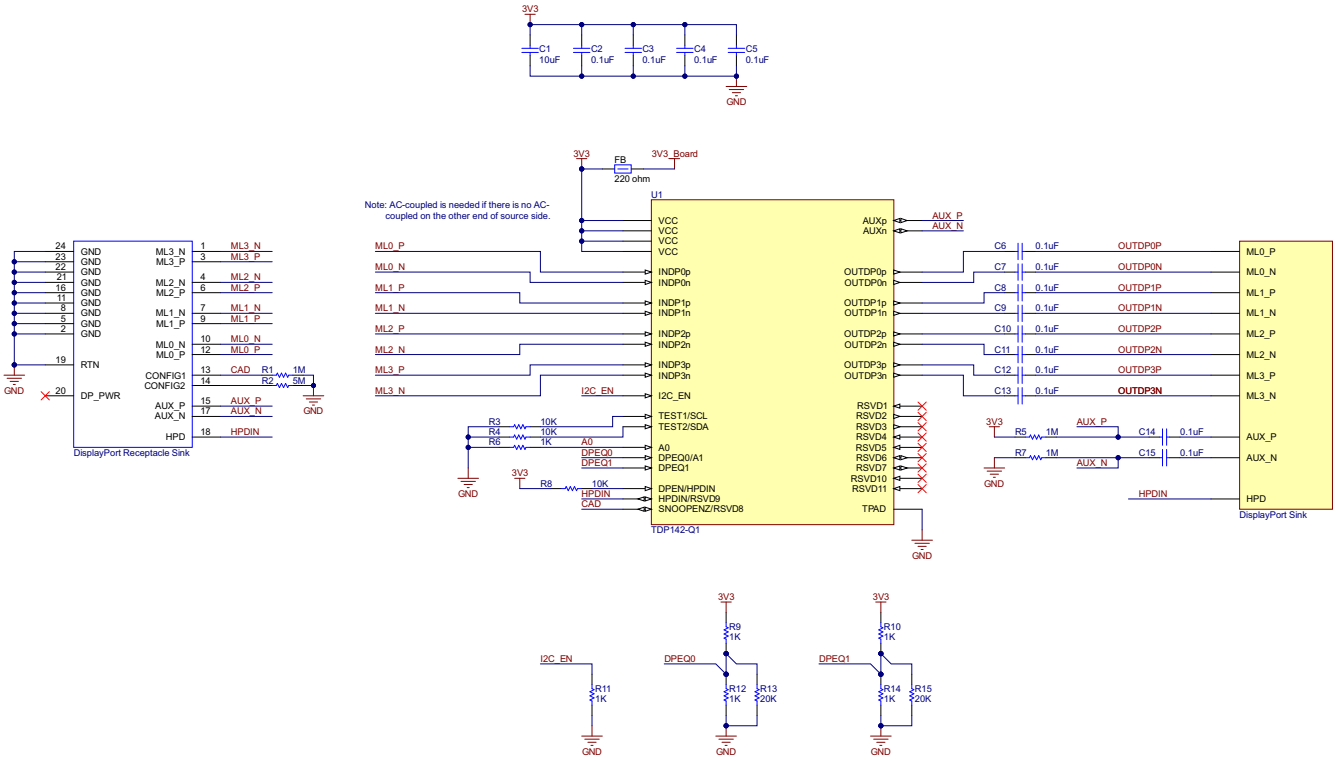

Figure 8-4. Block diagram of DisplayPort Sink Application

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-5.

Table 8-5. Design Parameters

PARAMETER	VALUE
Maximum Operating data rate (RBR, HBR, HBR2, or HBR3)	HBR3 (8.1Gbps)
Supply voltage	3.3V
Trace length/width of C	12 inch/ 6 mil
Trace length/width of D	2 inch/ 6 mil
Main link AC-decoupling capacitor (75nF to 265nF)	Recommend 100nF
Control mode (I^2C or GPIO)	GPIO (I2C_EN = 0)

8.2.2.2 Detailed Design Procedure

The design procedure for sink application is listed as follows:

- Determine the loss profile on the DP input (C) and output (D) channels and cables. See Figure 8-5 for 6mil trace insertion loss.
- Based on the loss profile, determine the optimal configuration for the TDP142, to pass electrical compliance.
- See Figure 8-4 for information on the source application that uses AC coupling capacitors, control pin resistors, and the recommended decouple capacitors from VCC pins to ground.
  - AUX: Make sure the AUXP has a 1MΩ pullup resistor and the AUXN has a 1MΩ pulldown resistor. The 1MΩ resistors must be on the TDP142-Q1 side of the 100nF capacitors.
  - HPDIN: Route the HPD signal to either pin 23 or pin 32 based on the GPIO/I2C mode. With this setup, the TDP142-Q1 is able to conserve power when a source is not connected.

Table 8-6. HPD GPIO/I2C Selection

MODE	HPD
GPIO (I2C_EN = 0)	Pin 32
I2C (I2C_EN != 0)	Pin 23

- Configure the TDP142-Q1 using the GPIO terminals or the I^2C interface:
  - GPIO – Using the terminals DPEQ0 and DPEQ1.
  - TI recommends to start a higher equalization value like 13dB and 15dB first and adjust the value if necessary.
  - I^2C – Refer to the *I2C Register Maps* and the *Programming* section for a detail configuration procedures.
- The thermal pad must be connected to ground.

8.2.3 Application Curve

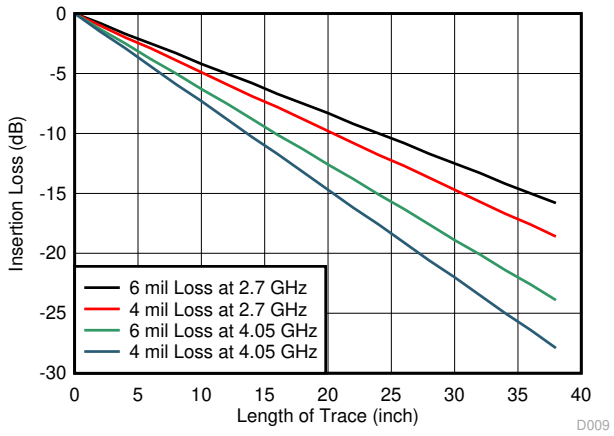

Figure 8-5. Insertion Loss of FR4 PCB Traces

8.3 Power Supply Recommendations

The TDP142-Q1 is designed to operate with a 3.3V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If the application has a higher voltage system power supply, use a voltage regulator to step down to 3.3V. Use decoupling capacitors to reduce noise and improve power supply integrity. Use a 0.1µF capacitor on each power pin.

ADVANCE INFORMATION

8.4 Layout

8.4.1 Layout Guidelines

1. Route the INDP[3:0]P/N and OUTDP[3:0]P/N pairs swith controlled 100Ω differential impedance (±10%).
2. Keep away from other high speed signals.
3. Keep intra-pair routing within 5 mils.
4. Keep inter-pair skew within 2 UI according to the *DisaplyPort Design Guide*
5. Make sure length matching is near the location of mismatch.
6. Separate each pair by at least 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, make sure the number of left and right bends are as equal as possible and that the angle of the bend is ≥ 135 degrees. This setup minimizes any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
8. Route all differential pairs on the same of layer.
9. Keep the number of VIAS to a minimum. TI recommends to keep the VIAS count to 2 or less.
10. Refer to Figure 8-7, the layout might face signal crossing on OUTDP2 and OUTDP3 due to mismatched order between the output pins of the device and the connector. One solution is to do a polarity swap on the input of the device when GPU is a BGA package to help minimize the number of VIAS being used.
11. Keep traces on layers adjacent to ground plane.
12. Do NOT route differential pairs over any plane split.
13. Adding test points can cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, place the test points in series and symmetrically. Do not place test points in a manner that causes a stub on the differential pair.

8.4.2 Layout Example

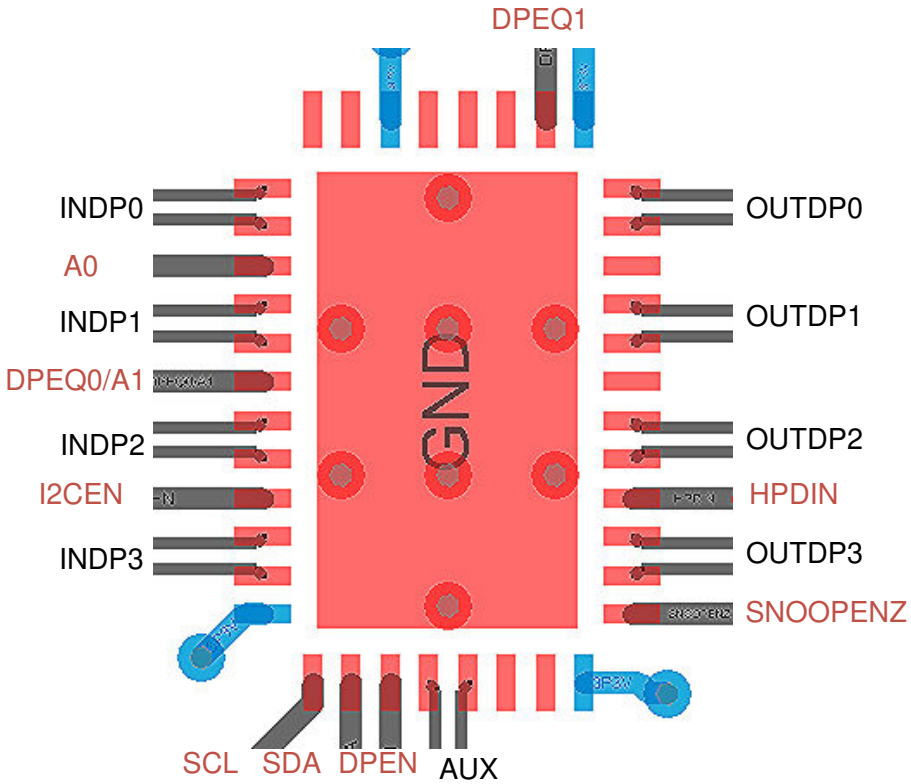

Figure 8-6. Layout Example

The following figures demonstrate the solution of mismatched order between the output of the device and the DisplayPort connector for the source using BGA package. Figure 8-7 shows the crossing section between TDP142-Q1 and connector. Usually, vias are applied to avoid the cross, but using a via can attenuate the signal integrity. Therefore, the polarity swap can be implemented at the input of TDP142-Q1. Figure 8-8 shows there is no more crossing section between the TDP142-Q1 and connector, which can minimize the number of vias being used. Note that the solution is only useful for the source using BGA package.

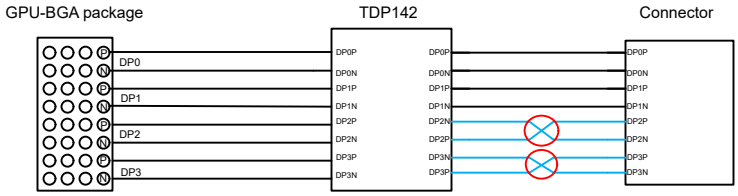

Figure 8-7. Layout Example: Signal Crossing on the Output

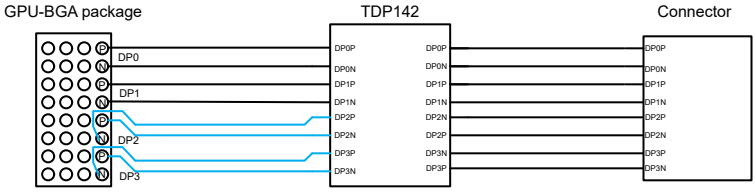

Figure 8-8. Layout Example: INDP2 and INDP3 Polarity Swap

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

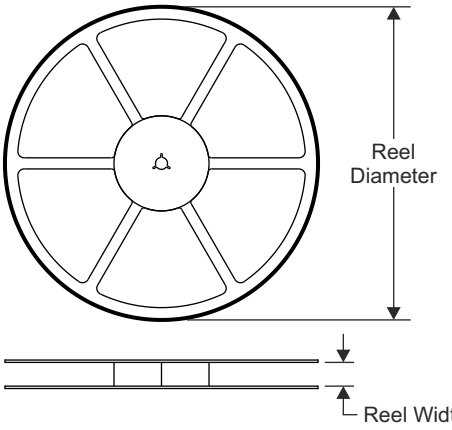
DATE	REVISION	NOTES
November 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

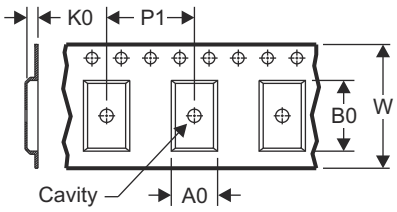
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

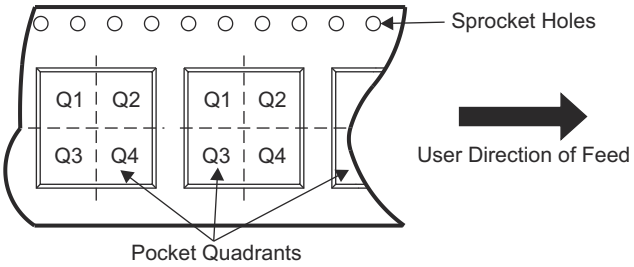


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

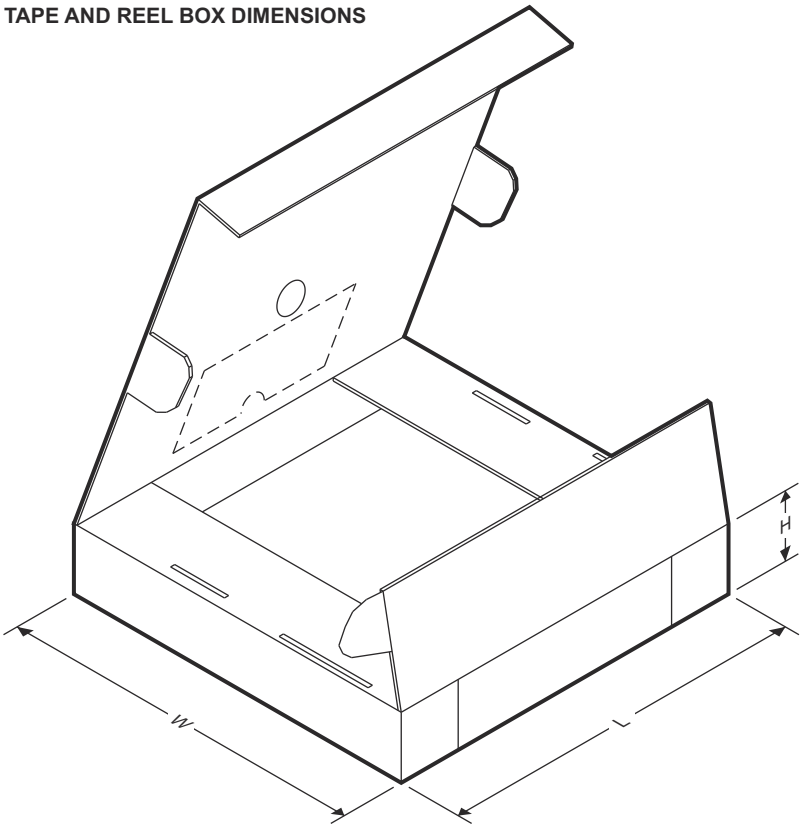


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTDP142RGFQ1	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



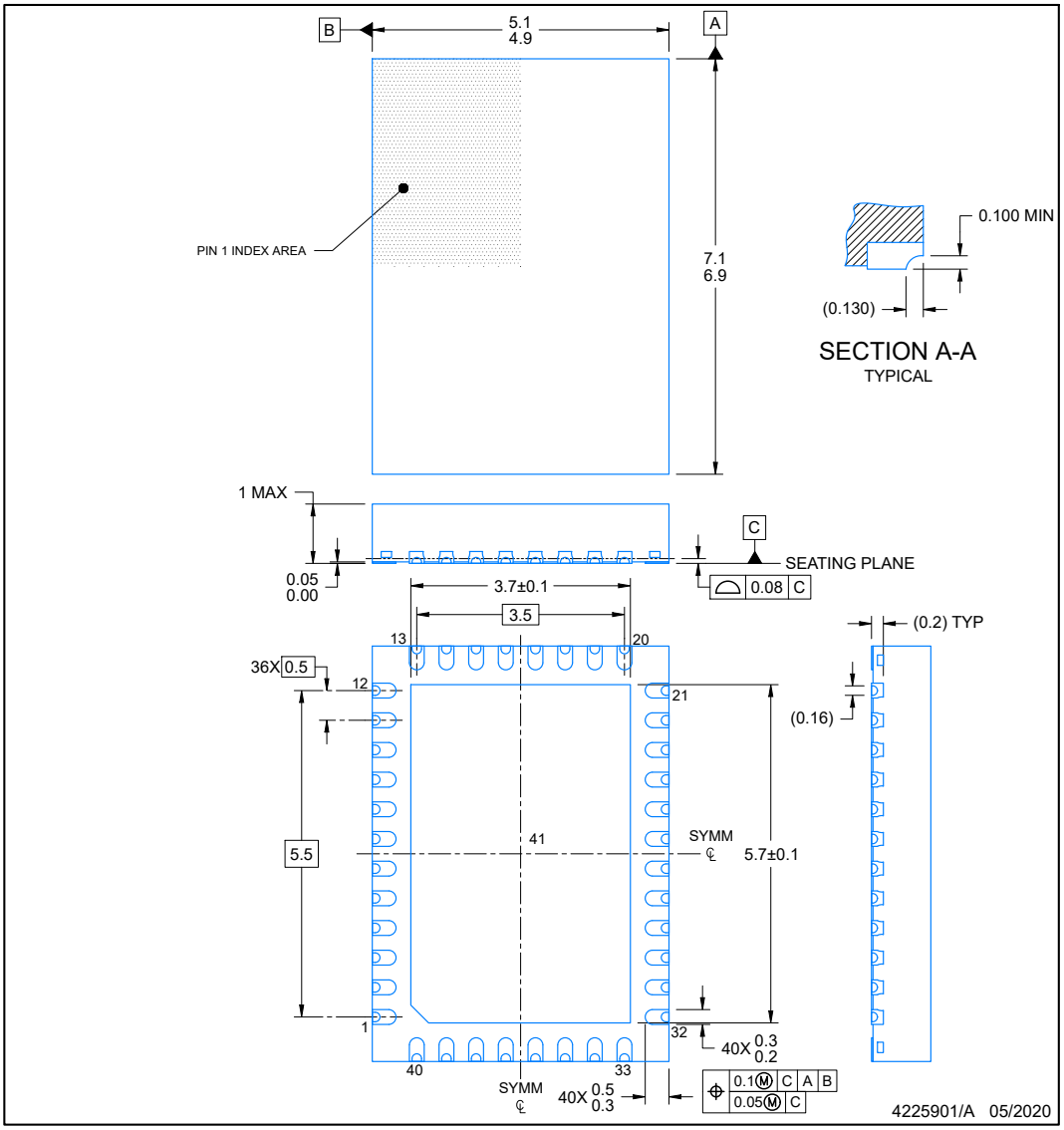
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTDP142RGFQ1	VQFN	RGF	40	3000	367.0	367.0	35.0

11.2 Mechanical Data

PACKAGE OUTLINE

RGF0040F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

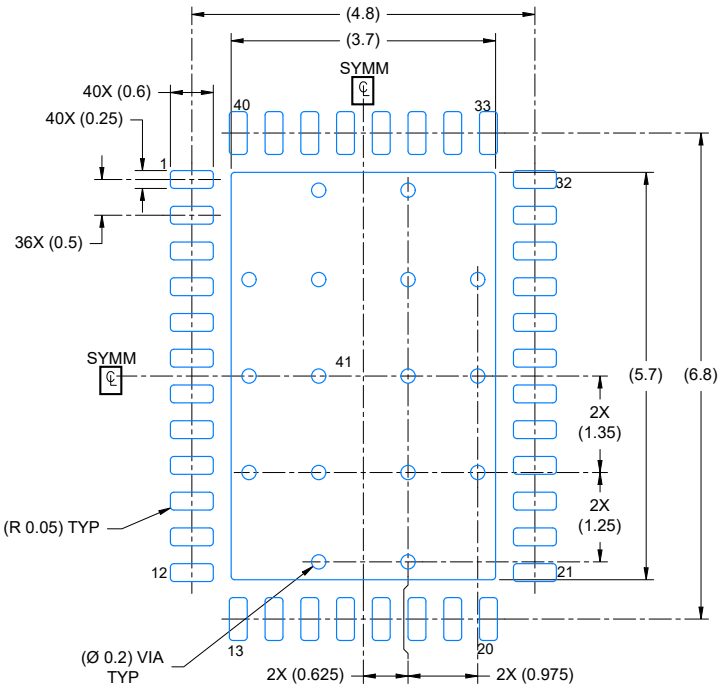
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

ADVANCE INFORMATION

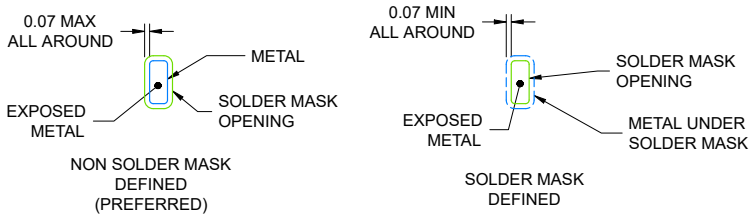
EXAMPLE BOARD LAYOUT

RGF0040F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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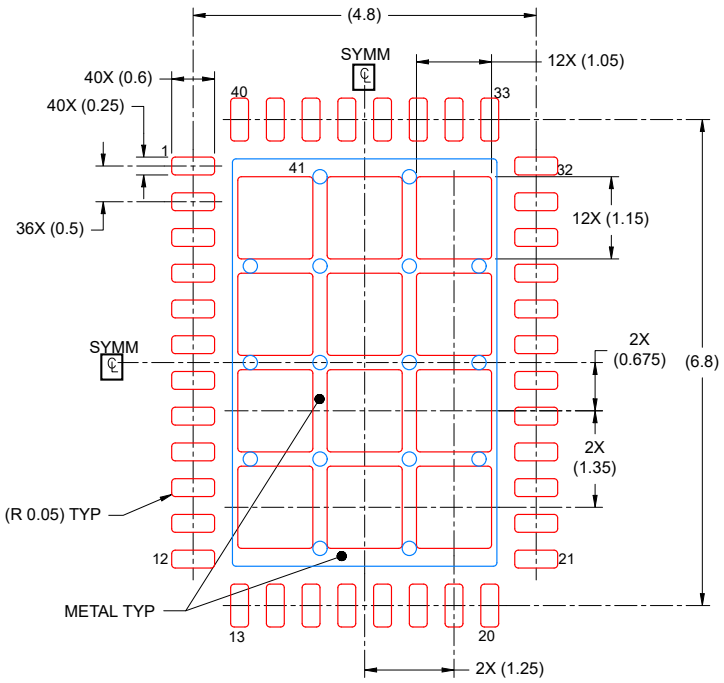
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGF0040F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

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