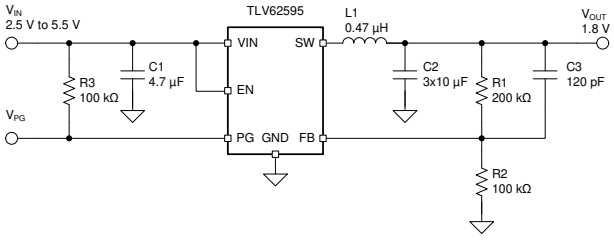
TLV62595, 2.5-V to 5.5-V Input, 4-A Step-Down Converter with 1% Output Accuracy in 1.5-mm × 1.5-mm QFN Package

1 Features

- Up to 97% efficiency
- Low $R_{DS(ON)}$ power switches 26 mΩ / 25 mΩ
- 2.5-V to 5.5-V input voltage range
- Adjustable output voltage from 0.6 V to 4 V
- 1% feedback voltage accuracy (full temperature range)
- DCS-control topology
- Power save mode for light load efficiency
- 100% duty cycle for lowest dropout
- 10-µA operating quiescent current
- 2.2-MHz typical switching frequency
- Short circuit protection (HICCUP)
- Active output discharge
- Power good output
- Thermal shutdown protection
- Create a custom design using the TLV62595 with the WEBENCH® Power Designer

2 Applications

- Solid state drive
- Portable electronics
- IP network camera
- Industrial PC
- Multifunction printers



Typical Application Schematic

3 Description

The TLV62595 is a high-frequency synchronous step-down converter optimized for compact solution size and high efficiency. The device integrates switches capable of delivering an output current up to 4 A. At medium to heavy loads, the converter operates in pulse width modulation (PWM) mode with typical 2.2-MHz switching frequency. At light load, the device automatically enters Power Save Mode (PSM) to maintain high efficiency over the entire load current range with a quiescent current as low as 10 µA.

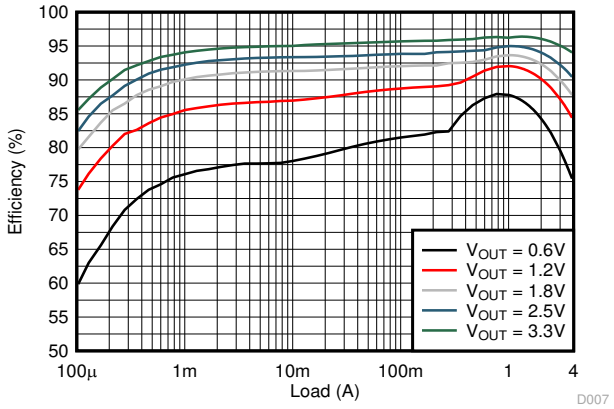
Based on the DCS Control topology, the device provides a fast transient response. The internal reference regulates the output voltage down to 0.6 V with a high feedback voltage accuracy of 1% over the junction temperature range of –40°C to 125°C. The entire solution requires a small 470-nH inductor, a single 4.7-µF input capacitor and three 10-µF or single 47-µF output capacitor.

The device is available in a 6-pin 1.5-mm × 1.5-mm QFN package, offering a high power density solution.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TLV62595	DMQ (VSON-HR, 6)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency at V_{IN} = 5 V

Table of Contents

4 Revision History

Changes from Revision * (December 2020) to Revision A (January 2023)	Page
• Updated ESD Ratings	6
• Removed duplicate table in *Output Filter Design* section	11

5 Pin Configuration and Functions

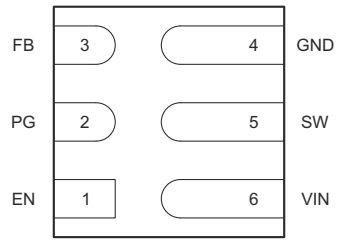


Figure 5-1. 6-Pin VSON-HR DMQ Package (Bottom View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
PG	2	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
FB	3	I	Feedback pin. For the fixed output voltage versions, this pin must be connected to the output.
GND	4		Ground pin
SW	5	PWR	Switch pin of the power stage
VIN	6	PWR	Input voltage pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, FB, EN, PG	– 0.3	6	V
Pin voltage(2)	SW (DC)	– 0.3	V_{IN} + 0.3	V
Pin voltage(2)	SW (DC, in current limit)	– 1	V_{IN} + 0.3	
Pin voltage(2)	SW (AC, less than 10ns)(3)	– 2.5	10	V
Temperature	Operating Junction, T_J	–40	150	°C
Temperature	Storage, T_{STG}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ABSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		4.0	V
I_{OUT}	Output curent range	0		4	A
V_{PG}	Pull-up resistor voltage			5.5	V
I_{SINK_PG}	Sink current at PG pin			1	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV62595	TLV62595EVM-794	UNIT
		DMQ (JEDEC)	DMQ (EVM)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.5	71.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.9	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	3.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	33.1	38.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = 25 °C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		10		µA
I_{SD}	Shutdown current	EN = Low, T_J = -40 ℃ to 85 ℃		0.05		µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level threshold voltage	V_{IN} = 2.5 V to 5.5 V	1.0			V
V_{IL}	Low-level threshold voltage	V_{IN} = 2.5 V to 5.5 V			0.4	V
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		1.75		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		96		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		92		%
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		105		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		110		%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		µA
$t_{PG,DLY}$	Power good deglitch delay	PG rising edge		100		µs
		PG falling edge		20		
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode, 2.5 V ≤ V_{IN} ≤ 5.5 V, T_J = -40°C to 125°C	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current for adjustable output voltage	V_{FB} = 0.6 V		0.01		µA
I_{DIS}	Output discharge current	V_{SW} = 0.4V; EN = LOW		400		mA
	Load regulation	I_{OUT} = 0.5 A to 3 A, V_{OUT} = 1.8 V		0.1		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			25		mΩ
I_{LIM}	High-side FET switch current limit, DC		4.8	5.6		A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.2		MHz

6.6 Typical Characteristics

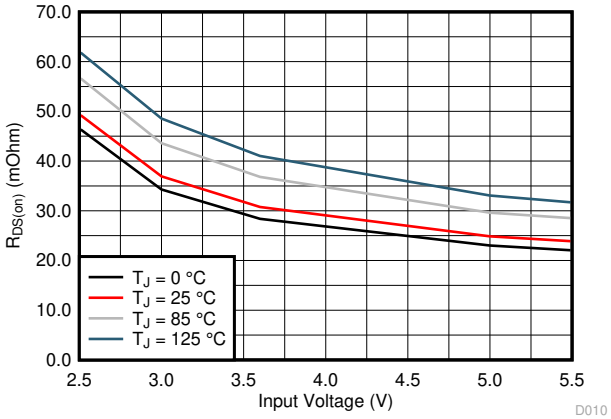


Figure 6-1. High-Side FET On-Resistance

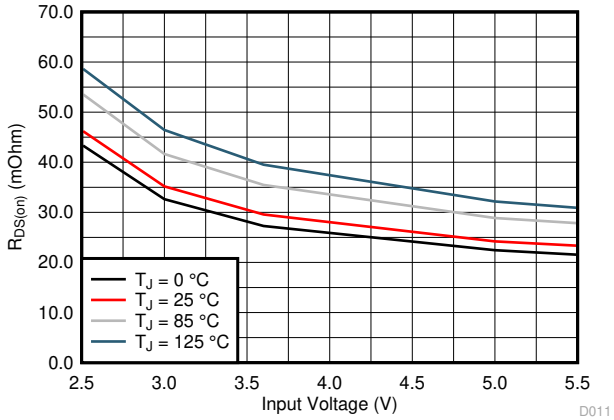


Figure 6-2. Low-Side FET On-Resistance

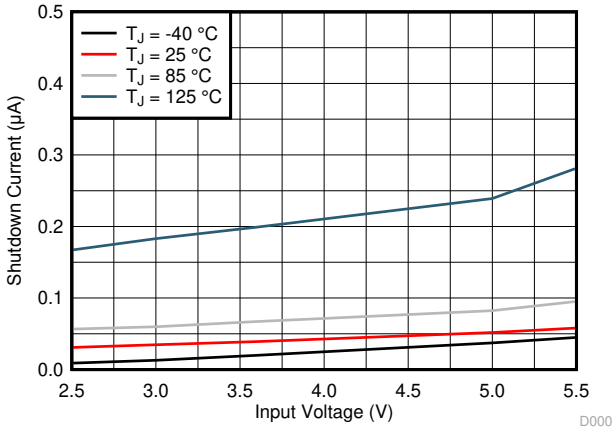


Figure 6-3. Shutdown Current

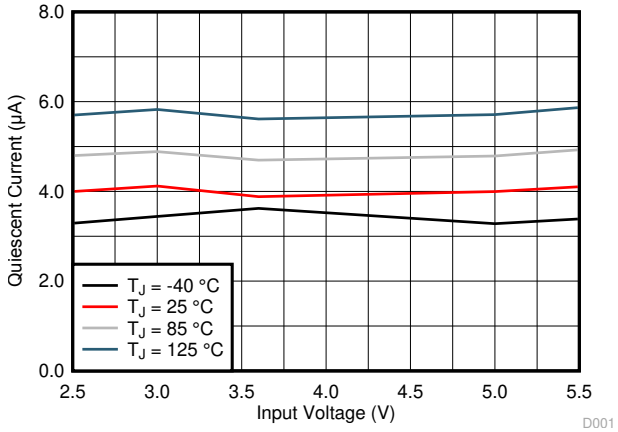


Figure 6-4. Quiescent Current

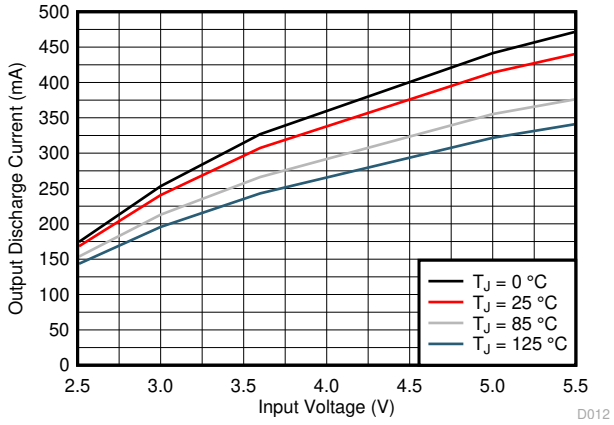


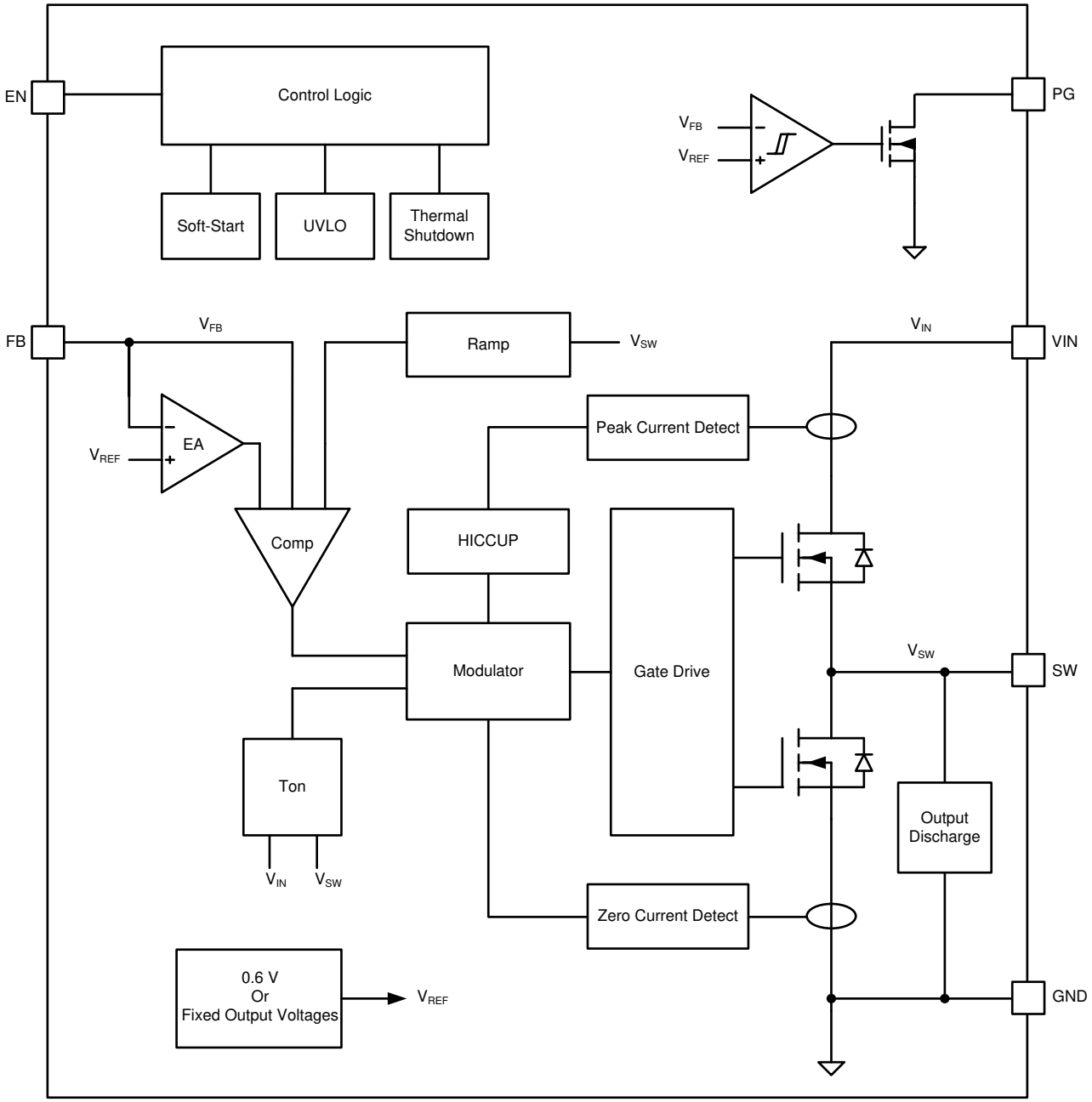
Figure 6-5. Output Discharge Current

7 Detailed Description

7.1 Overview

The TLV62595 are synchronous step-down converters based on the DCS-Control topology with an adaptive constant on-time control and a stabilized switching frequency. The devices operate in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. The nominal switching frequency is about 2.2 MHz with a small and controlled variation over the input voltage range. As the load current decreases, the converter enters PSM, reducing the switching frequency to keep efficiency high over the entire load current range. Since combining both PWM and PSM within a single building block, the transition between modes is seamless and without effect on the output voltage. The devices offer both excellent dc voltage and fast load transient regulation, combined with a very low output voltage ripple.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM). The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 450ns \tag{1}$$

7.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates now with a fixed on-time and the switching frequency further decreases proportionally to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \tag{2}$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM. The device maintains output regulation in PWM mode.

7.3.3 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles, because even at very low duty cycles, the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between VIN and VOUT is determined by the voltage drop across the high-side FET and the dc resistance of the inductor. The minimum VIN that is needed to maintain a specific VOUT value is estimated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \tag{3}$$

where

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.4 Soft Start

About 250 µs after EN goes high, the internal soft-start circuitry controls the output voltage during start-up. This avoids excessive inrush current and ensures a controlled output voltage ramp. It also prevents unwanted voltage drops from high-impedance power sources or batteries. The TLV62595 can start into a pre-biased output.

7.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from drawing excessive current in case of externally-caused overcurrent or short circuit condition. Due to an internal propagation delay (typically 60 ns), the actual ac peak current can exceed the static current limit during that time.

If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles (about 13 µs), the device turns off the high-side MOSFET for about 100 µs which allows

the inductor current to decrease through the low-side MOSFET body diode and then restart again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

7.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to about 2.2 V with a hysteresis of typically 160 mV.

7.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typical), the device goes in thermal shutdown with a hysteresis of typically 20°C. After the TJ has decreased enough, the device resumes normal operation.

7.4 Device Functional Modes

7.4.1 Enable, Disable and Output Discharge

The device starts operation, when Enable (EN) is set High. The input threshold levels are typically 0.9 V for rising and 0.7 V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled low with a shutdown current of typically 50 nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry, are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

7.4.2 Power Good

The TLV62595 has a built-in power good (PG) function. The PG pin goes high impedance, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is low (see Table 7-1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge has a 100-µs blanking time and the PG falling edge has a deglitch delay of 20 µs.

Table 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, V_{FB} ≥ 0.576 V	√	
	EN = High, V_{FB} ≤ 0.552 V		√
	EN = High, V_{FB} ≤ 0.63 V	√	
	EN = High, V_{FB} ≥ 0.66 V		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	0.7 V < V_{IN} < V_{UVLO}		√
Power Supply Removal	V_{IN} < 0.7 V	√	

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

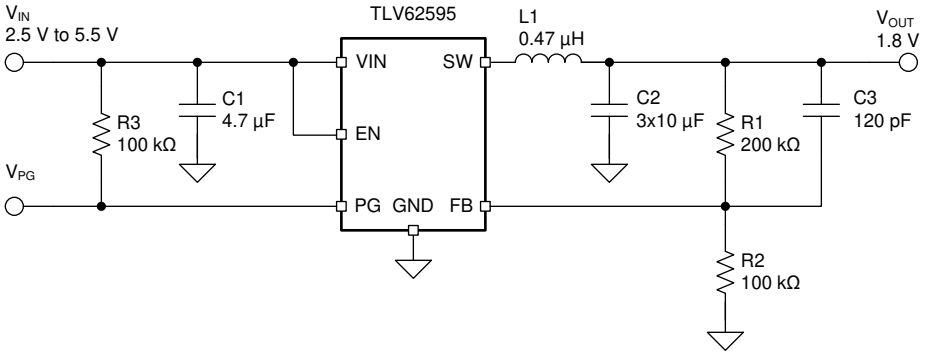


Figure 8-1. Typical Application of TLV62595

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, TLV62595	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 20 mV
Maximum output current, TLV62595	4 A

Table 8-2 lists the components used for the example.

Table 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475MA	Taiyo Yuden
C2	3 × 10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C3	120 pF, Ceramic capacitor, 50 V, size 0402	Std
L1	0.47 µH, Power Inductor, XFL4015-471MEB	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std

1. See the *Third-Party Products Disclaimer*.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62595 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to Equation 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (4)$$

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Equation 5 shows how to compute the value of the feedforward capacitor for a given R2 value. For the recommended 100 k value for R2, a 120-pF feedforward capacitor is used.

$$C3 = \frac{12\mu}{R2} \quad (5)$$

For the fixed output voltage versions, connect the FB pin to the output. R1, R2, and C3 are not needed. The fixed output voltage devices have an internal feedforward capacitor.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, Table 8-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations must be checked for each individual application.

Table 8-3. Matrix of Output Capacitor and Inductor Combinations, TLV62595

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	22	3 x 10	47	100
0.33				
0.47		+(1)	+	+
1.0				

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –35%.

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 6 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. Table 8-4 lists recommended inductors.

Table 8-4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS [L x W x H mm]	MAX. DC RESISTANCE [mΩ]	MFR PART NUMBER(1)
0.47	4.8	2.0 × 1.6 × 1.0	32	HTEN20161T-R47MDR, Cyntec
	4.6	2.0 × 1.2 × 1.0	25	HTEH20121T-R47MSR, Cyntec
	4.8	2.0 × 1.6 × 1.0	32	DFE201610E - R47M, MuRata
	4.8	2.0 × 1.6 × 1.0	32	DFE201210S - R47M, MuRata
	5.1	2.0 × 1.6 × 1.0	34	TFM201610ALM-R47MTAA, TDK
	5.2	2.0 × 1.6 × 1.0	25	TFM201610ALC-R47MTAA, TDK
	6.6	4.0 × 4.0 × 1.6	8.36	XFL4015-471ME, Coilcraft
	8.0	3.5 × 3.2 × 2.0	10.85	XEL3520-471ME, Coilcraft
	6.8	4.5 × 4 × 1.8	11.2	WE-LHMI-744373240047, Würth

(1) See *Third-party Products Disclaimer*.

8.2.2.5 Capacitor Selection

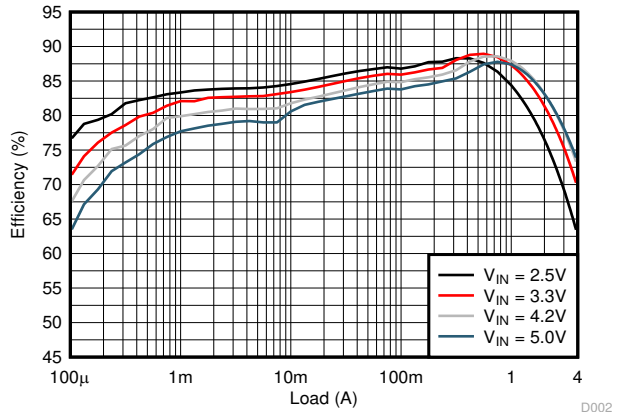
The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, a minimum effective input capacitance of 3 µF must be present, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. Considering the DC-bias derating the capacitance, the minimum effective output capacitance is 20 µF for TLV62595.

A feedforward capacitor is required for the adjustable version, as described in *Section 8.2.2.2*. This capacitor is not required for the fixed output voltage versions.

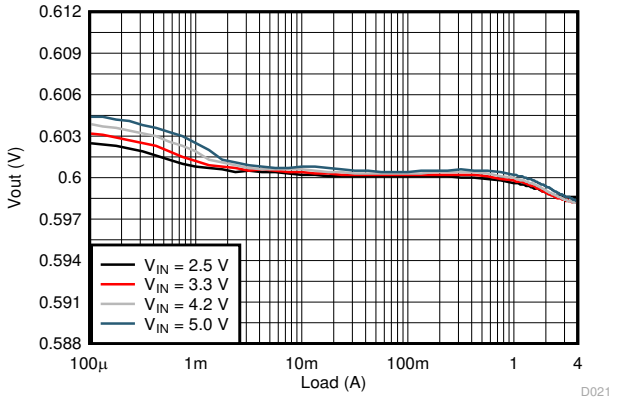
8.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25°C, BOM = Table 8-2, unless otherwise noted.



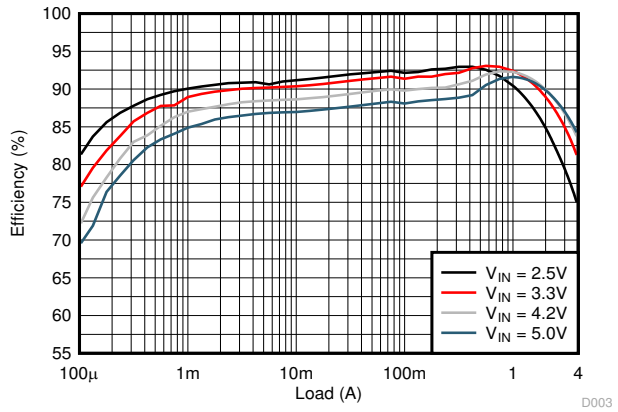
V_{OUT} = 0.6 V

Figure 8-2. Efficiency



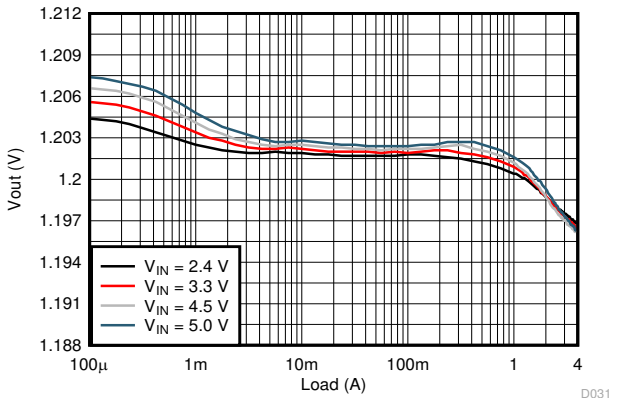
V_{OUT} = 0.6 V

Figure 8-3. Load Regulation



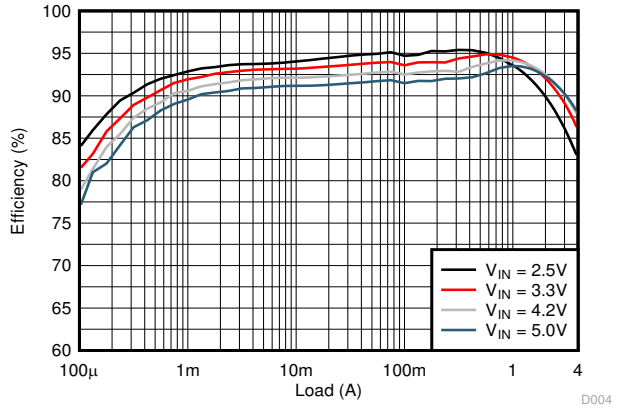
V_{OUT} = 1.2 V

Figure 8-4. Efficiency



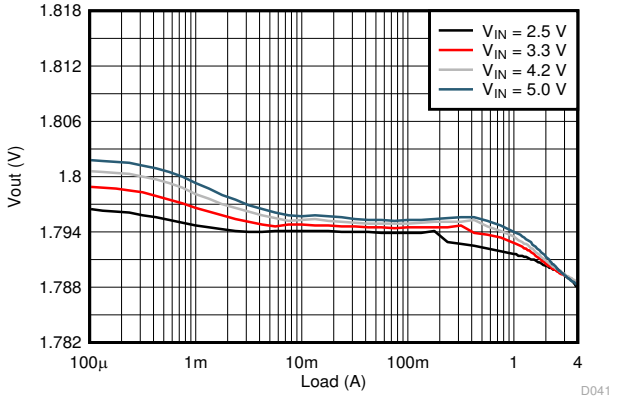
V_{OUT} = 1.2 V

Figure 8-5. Load Regulation



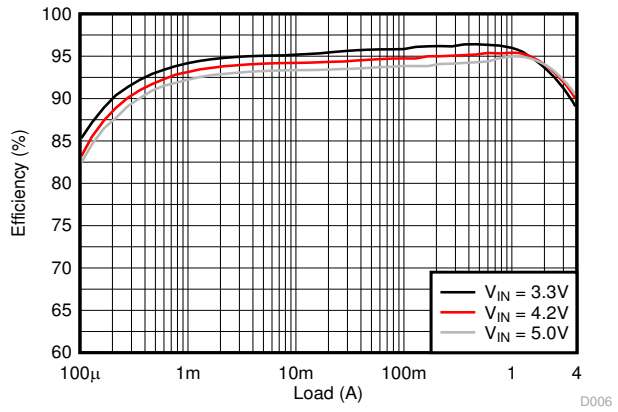
V_{OUT} = 1.8 V

Figure 8-6. Efficiency



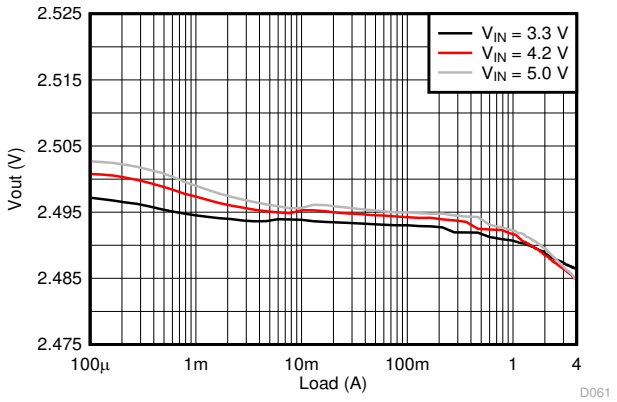
V_{OUT} = 1.8 V

Figure 8-7. Load Regulation



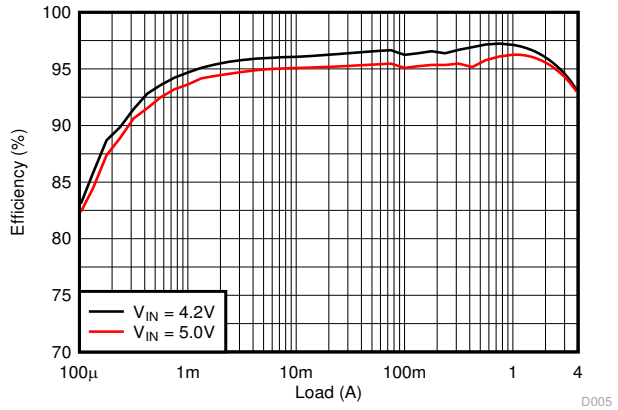
V_{OUT} = 2.5 V

Figure 8-8. Efficiency



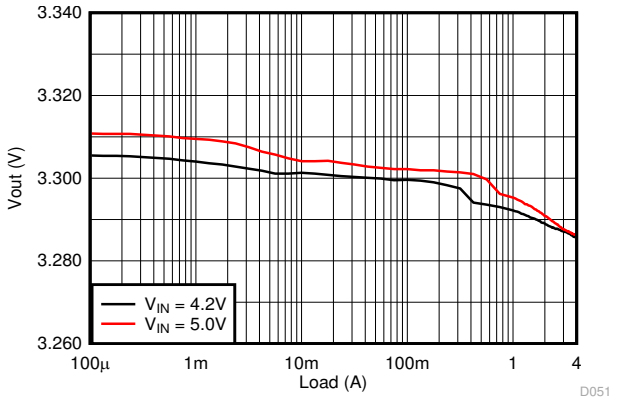
V_{OUT} = 2.5 V

Figure 8-9. Load Regulation



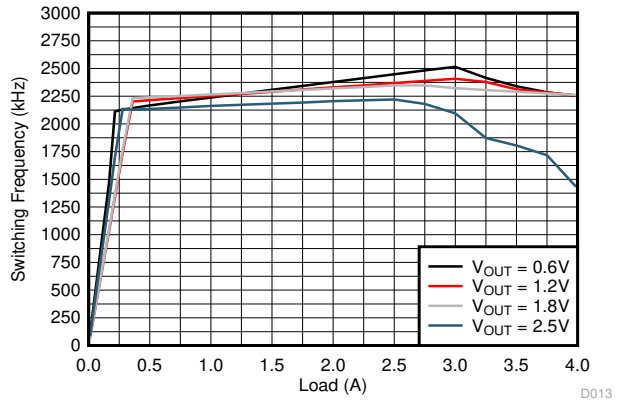
V_{OUT} = 3.3 V

Figure 8-10. Efficiency



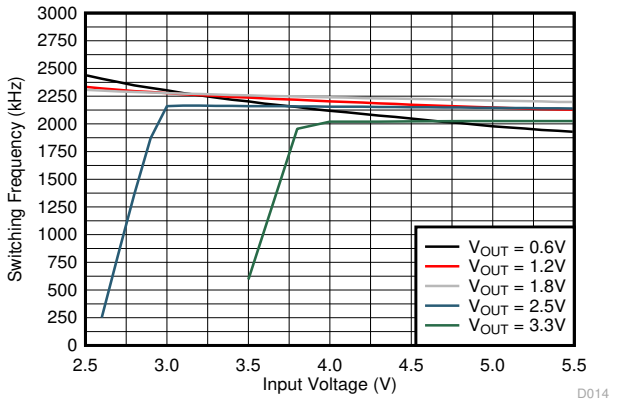
V_{OUT} = 3.3 V

Figure 8-11. Load Regulation



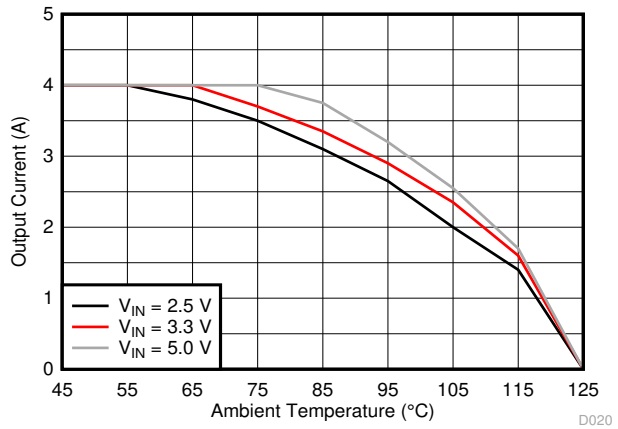
V_{IN} = 3.3 V

Figure 8-12. Switching Frequency



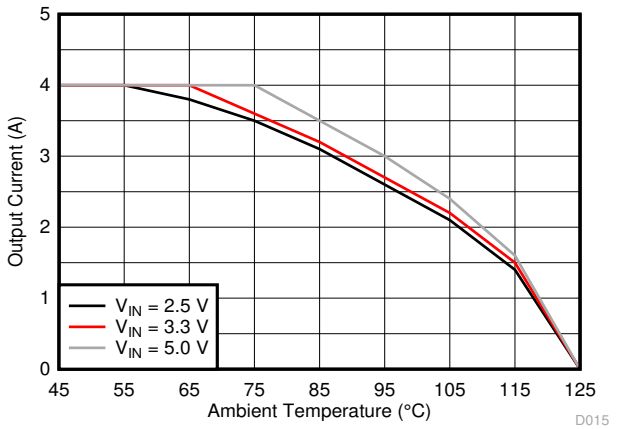
I_{OUT} = 1.0 A

Figure 8-13. Switching Frequency



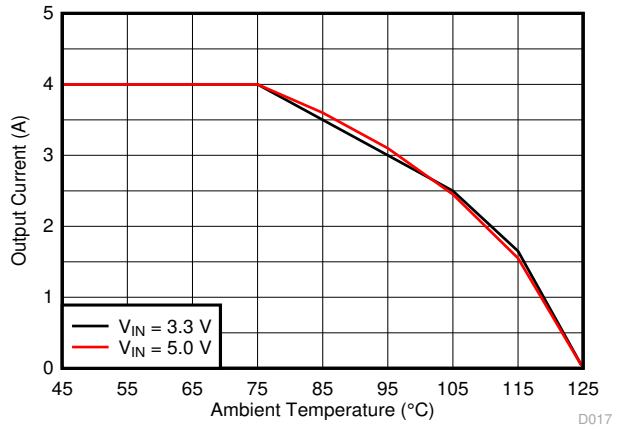
V_{OUT} = 1.2 V θ_{JA}= 71.4 °C/W

Figure 8-14. Thermal Derating



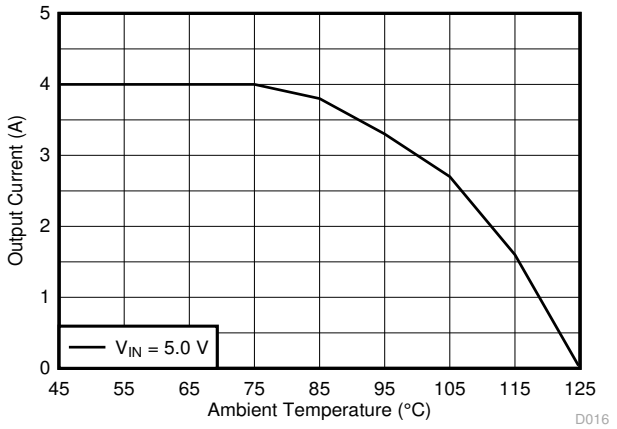
V_{OUT} = 1.8 V θ_{JA}= 71.4 °C/W

Figure 8-15. Thermal Derating



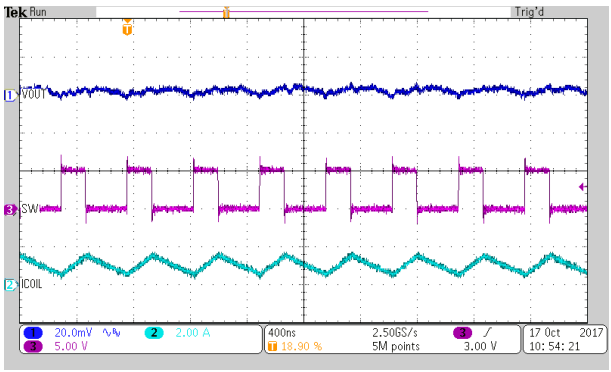
V_{OUT} = 2.5 V θ_{JA}= 71.4 °C/W

Figure 8-16. Thermal Derating



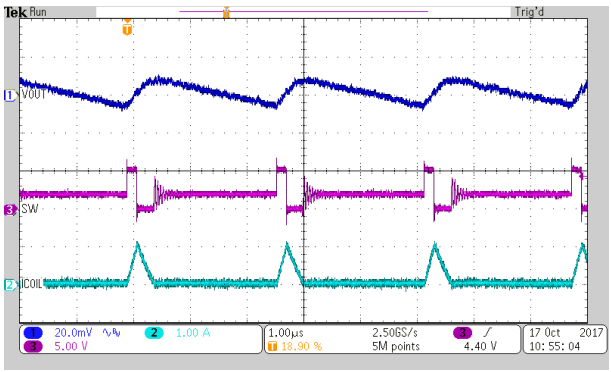
V_{OUT} = 3.3 V θ_{JA}= 71.4 °C/W

Figure 8-17. Thermal Derating



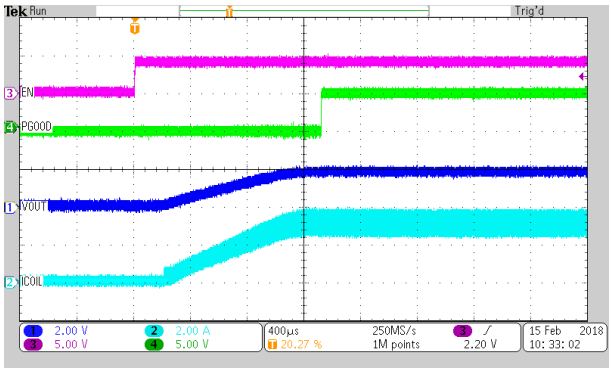
I_{OUT} = 1.0 A

Figure 8-18. PWM Operation



I_{OUT} = 0.1 A

Figure 8-19. PSM Operation



Load = 0.6 Ω

Figure 8-20. Start-up with Load

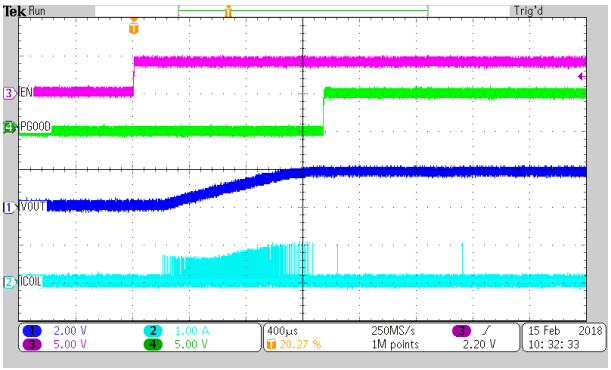
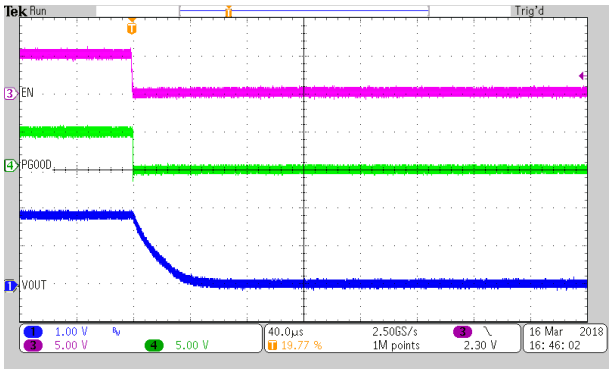


Figure 8-21. Startup with No Load



Load = 1.8 Ω

Figure 8-22. Disable, Active Output Discharge

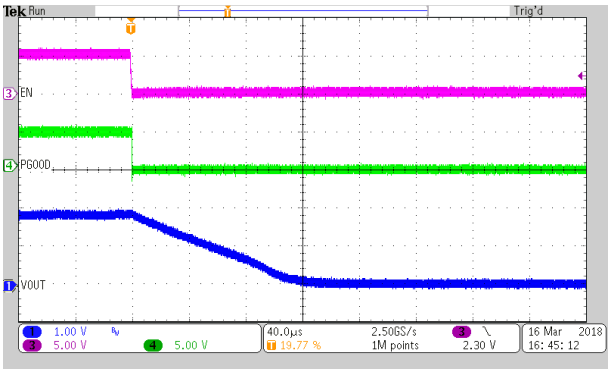
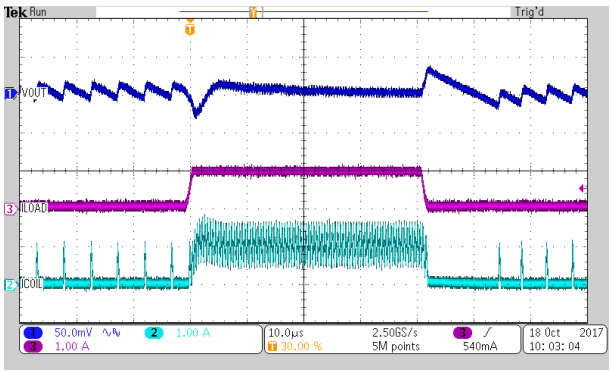
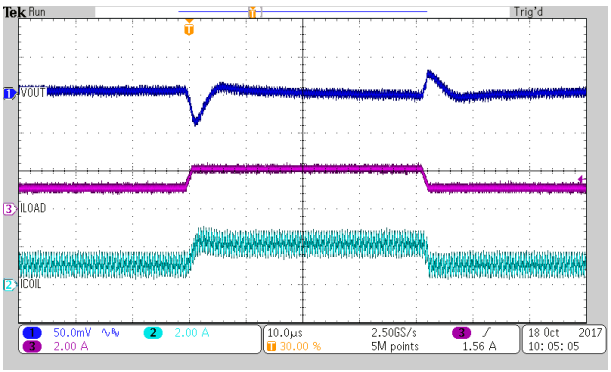


Figure 8-23. Disable, Active Output Discharge at No Load



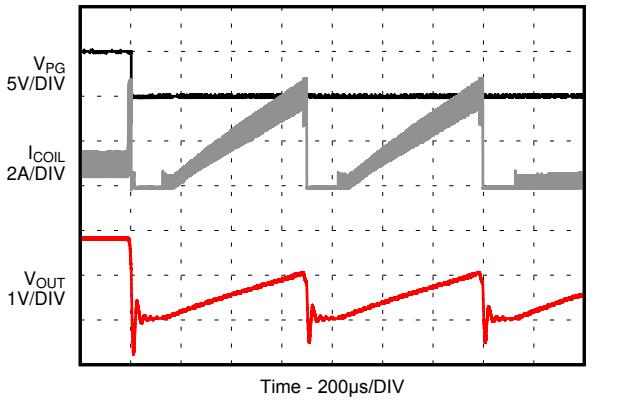
I_{OUT} = 0.05 A to 1A

Figure 8-24. Load Transient



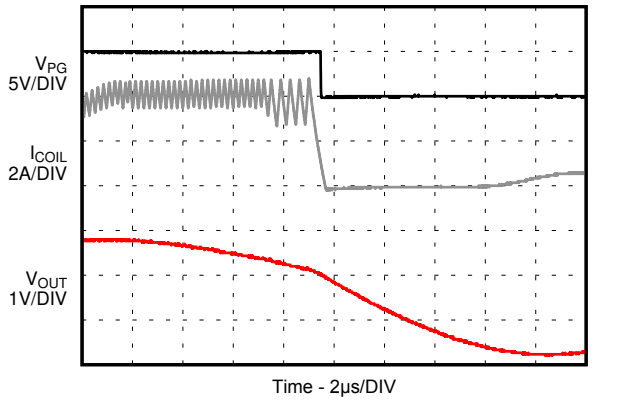
I_{OUT} = 1 A to 2 A

Figure 8-25. Load Transient



I_{OUT} = 1 A

Figure 8-26. HICCUP Short Circuit Protection



I_{OUT} = 1 A

Figure 8-27. HICCUP Short Circuit Protection (Zoom In)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See Figure 8-28 for the recommended PCB layout.

- The input/output capacitors and the inductor must be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care must be taken to avoid noise being induced. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to Figure 8-28 for an example of component placement, routing and thermal design.

8.4.2 Layout Example

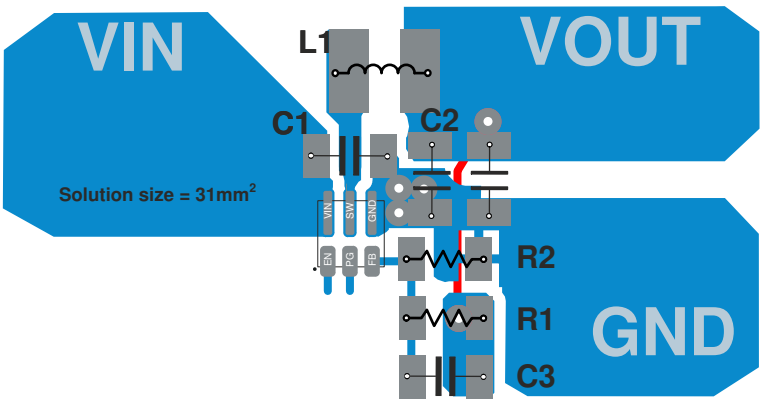


Figure 8-28. PCB Layout Recommendation

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

Thermal Information provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the *Thermal Characteristics application notes*, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62595 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62595DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

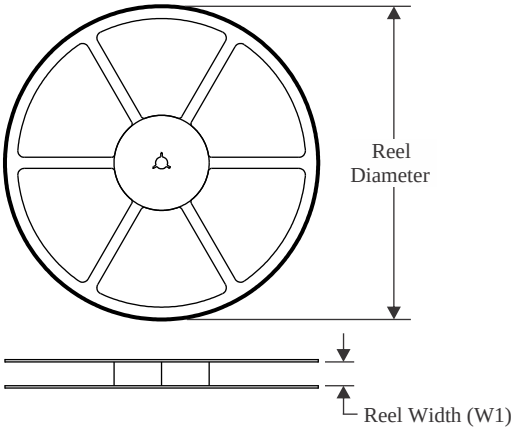
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

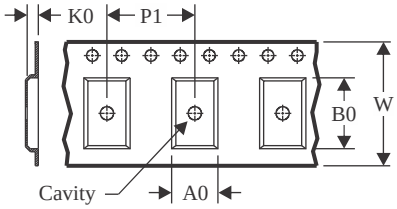
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

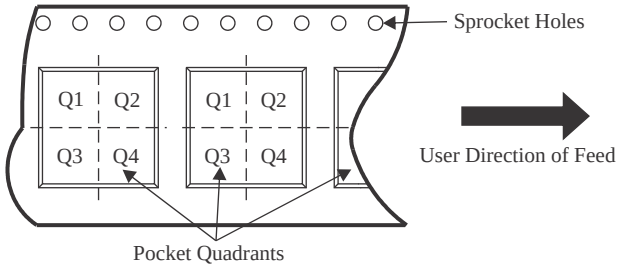


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

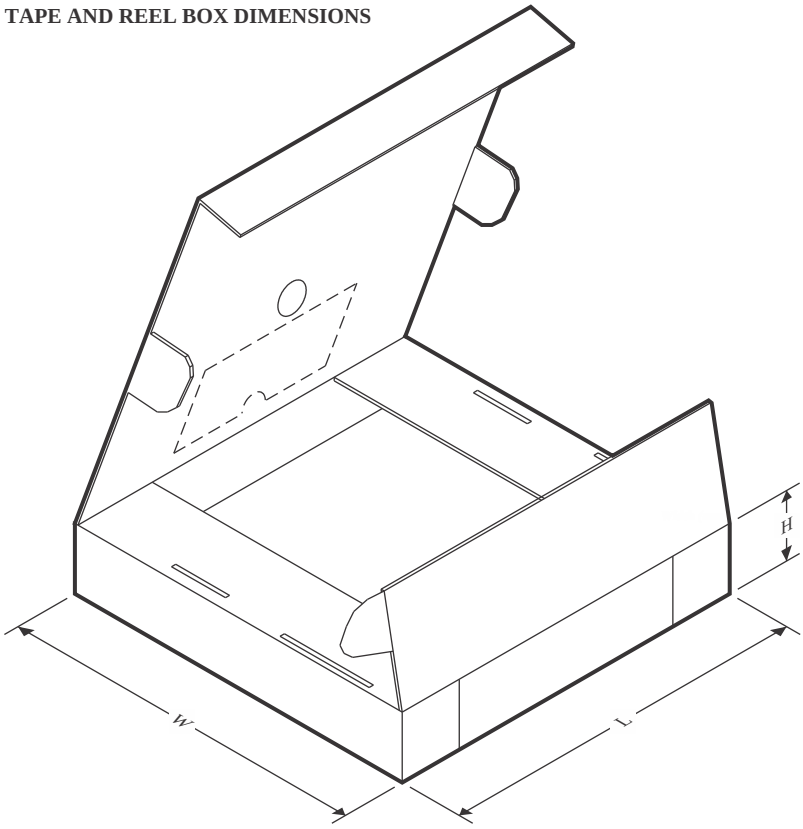
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62595DMQR	VSON-HR	DMQ	6	3000	180.0	8.4	1.7	1.7	1.14	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

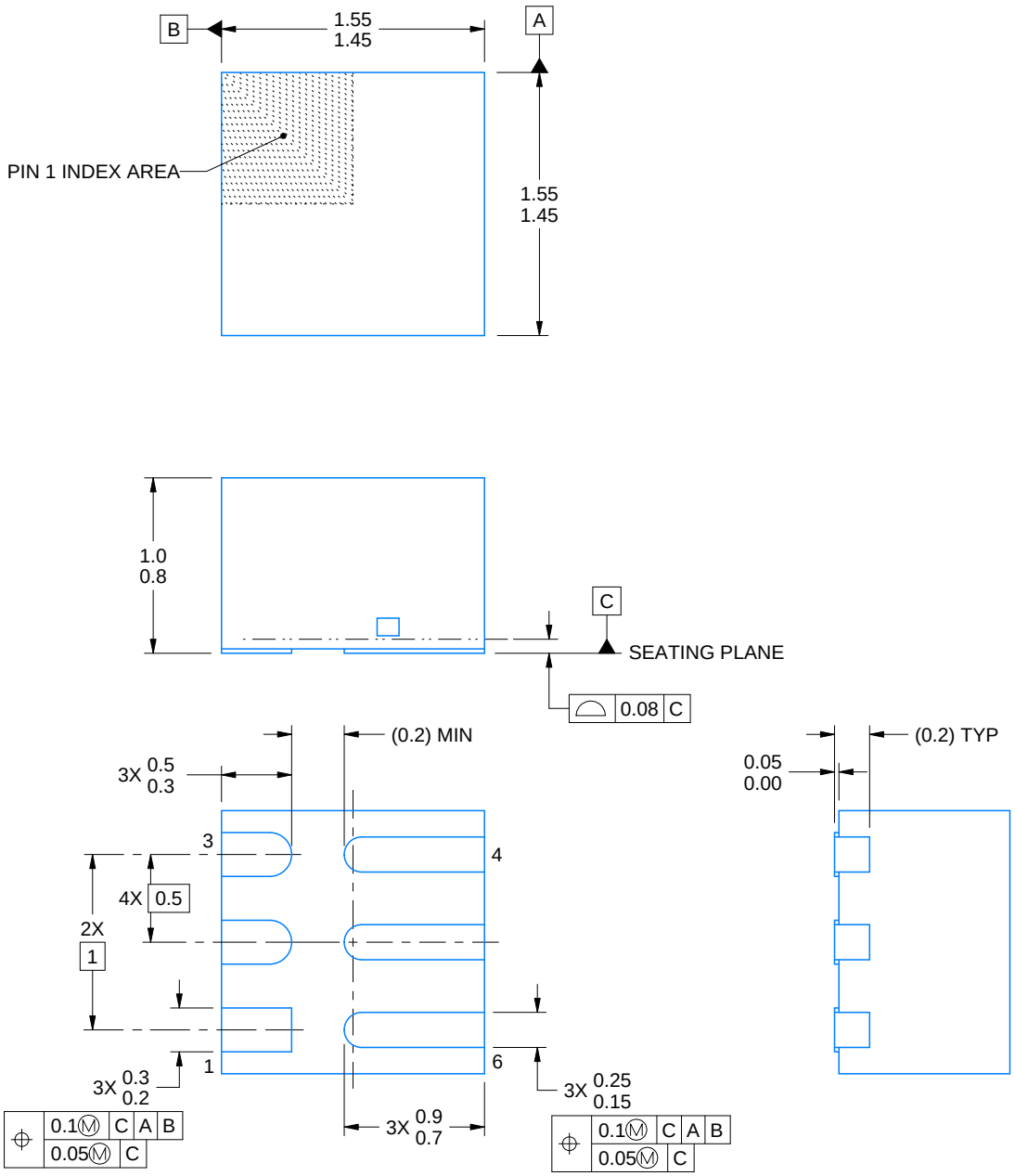
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62595DMQR	VSON-HR	DMQ	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DMQ0006A

VSON - 1 mm max height

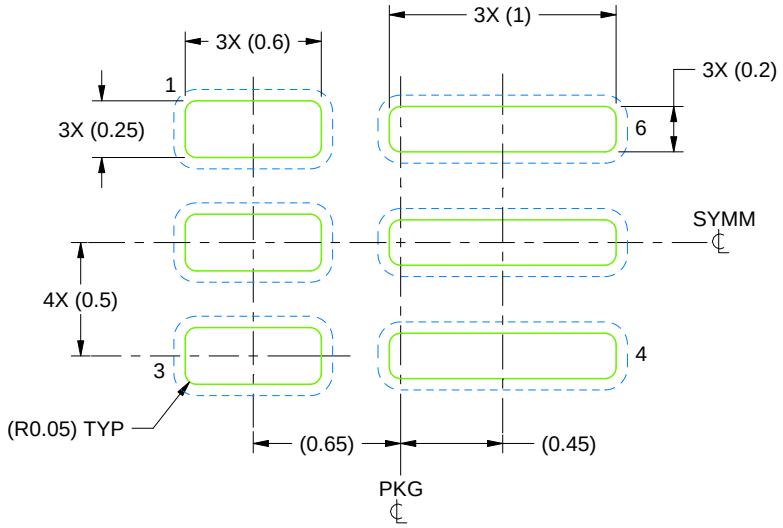
PLASTIC SMALL OUTLINE - NO LEAD



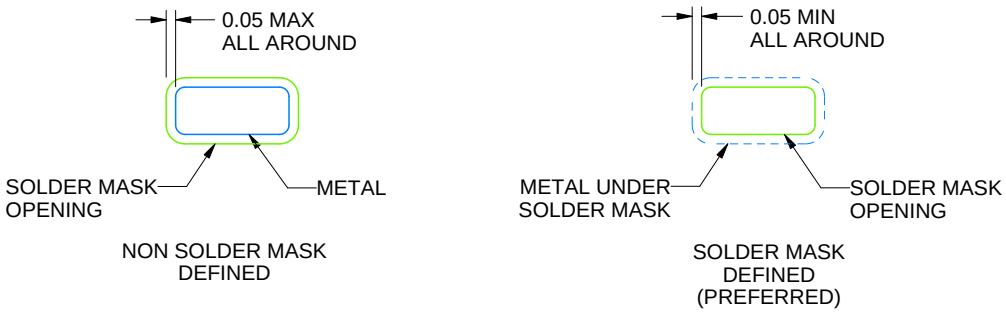
4222645/E 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

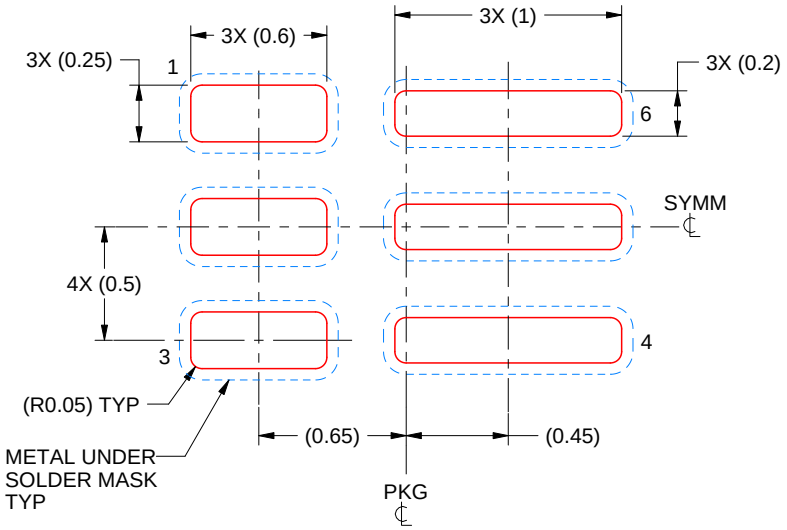


SOLDER MASK DETAILS

4222645/E 09/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:30X

4222645/E 09/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265