TPS26750 USB Type-C® and USB PD Controller With Integrated Power Switches Optimized for Power Applications

1 Features

- This device is certified by the USB-IF for PD3.1
  - PD3.1 silicon is required for certification of new USB PD designs
  - TPS26750 TID#: 11450
  - Article on PD2.0 vs. PD3.0
- Optimized for USB Type-C PD power applications
  - Integrated I2C control for TI battery chargers
    - Ex: In Development
  - Web-based GUI and pre-configured firmware
  - For a more extensive selection guide and getting started information, please refer to www.ti.com/usb-c and E2E guide
- Extended Power Range (EPR)
  - Supports EPR source and sink
  - EPR 28V, 36V, 48V, and AVS
- Programmable Power Supply(PPS)
  - Supports PPS source and sink
  - Standalone PPS source control TI battery chargers
  - Programmable interface for PPS sink
- Liquid Detection
  - Measures directly at the Type-C connector
  - Integrated error handling and protection
- Integrated fully managed power path & protection
  - Integrated 5V, 3A, and 36mΩ sourcing switch
  - Integrated undervoltage and overvoltage protection and current limiting for inrush current protection for the 5V and 3A source power path
  - 26V tolerant CC pins for robust protection when connected to non-compliant devices
- USB Type-C® Power Delivery (PD) controller
  - 10 configurable GPIOs
  - BC1.2 charging support
  - 3.3V LDO output for dead battery support
  - Power supply from 3.3V or VBUS source
  - 1 I2C primary port
  - 1 I2C secondary port

2 Applications

- Power tools, power banks, retail automation and payment
- Wireless speakers, headphones
- Other personal electronics and industrial applications

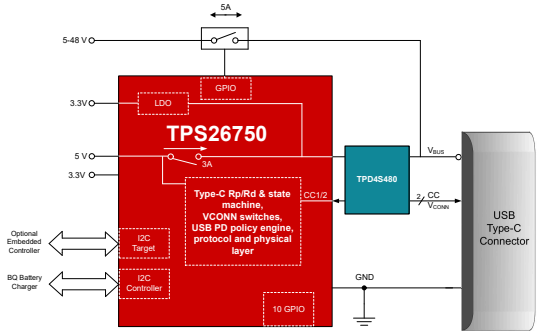
3 Description

The TPS26750 is a highly integrated stand-alone USB Type-C and Power Delivery (PD) controller optimized for applications supporting USB-C PD Power. The TPS26750 integrates fully managed power paths with robust protection for a complete USB-C PD solution. The TPS26750 also integrates control for external battery charger ICs for added ease of use and reduced time to market. The intuitive web based GUI asks the user a few simple questions on the applications needs using clear block diagrams and simple multiple-choice questions. As a result, the GUI will create the configuration image for the user's application, reducing much of the complexity associated with competitive USB PD solutions.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS26750	RSM (QFN, 32)	4mm × 4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

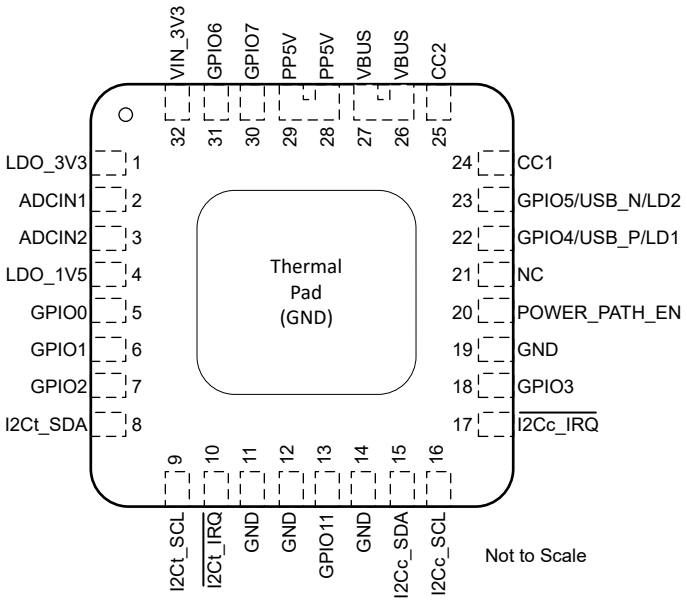


Figure 4-1. TPS26750 RSM Package, 32-Pin QFN (Top View)

Table 4-1. TPS26750 Pin Functions

PIN		TYPE	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
CC2	25	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (CCCy).
POWER_PATH_EN	20	O	Hi-Z	Power path enable for external load swith. Leave floating when unused. This is NOT a logic voltage level output.
GND	11, 12, 14	—	—	Ground. Connect to ground plane.
GPIO0	5	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO1	6	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO2	7	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO3	18	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO4/USB_P/LD1	22	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. This can be connected to D+ for BC1.2 support.
GPIO5/USB_N/LD2	23	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. This can be connected to D- for BC1.2 support.
GPIO6	31	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO7	30	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
$\overline{\text{I2Ct\_IRQ}}$	10	O	Hi-Z	I2C target interrupt. Active low. Connect to external voltage through a pull-up resistor. This can be re-configured to GPIO10. Tie to ground when unused.
I2Cc_SCL	16	O	Hi-Z	I^2C controller serial clock. Open-drain output. Tie to pullup voltage through a resistor when used or unused.
GPIO11	13	O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2Cc_SDA	15	I/O	Hi-Z	I^2C controller serial data. Open-drain input/output. Tie to pullup voltage through a resistor when used or unused.
$\overline{\text{I2Cc\_IRQ}}$	17	I	Hi-Z	I2C controller interrupt. Active low. Connect to external voltage through a pull-up resistor. Do NOT tie to GND when unused. This can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
PP5V	28, 29	I	—	5-V System Supply to VBUS, supply for CCy pins as VCONN.
VSYS	19	I	—	Tie to GND. Used as a reference for POWER_PATH_EN.
VBUS	26, 27	I/O		5-V to 20-V input. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.

5 Specifications

5.1 Absolute Maximum Ratings

5.1.1 TPS26750 - Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	PP5V	–0.3	6	V
	VIN_3V3	–0.3	4	
	ADCIN1, ADCIN2	–0.3	4	
	VBUS_IN, VBUS	–0.3	28	V
	CC1, CC2	–0.5	26	
	GPIOx	–0.3	6.0	
	I2Cc_SDA, I2Cc_SCL, $\overline{\text{I2Cc\_IRQ}}$, $\overline{\text{I2Ct\_IRQ}}$,I2Ct_SCL, I2Ct_SDA	–0.3	4	
Output voltage range	LDO_1V5	–0.3	2	V
	LDO_3V3	–0.3	4	
Source current	Source or sink current VBUS		internally limited	A
	Positive source current on CC1, CC2		1	
	Positive sink current on CC1, CC2 while VCONN switch is enabled		1	
	Positive sink current for I2Cc_SDA, I2Cc_SCL, I2Cc_IRQ, I2Ct_IRQ,I2Ct_SCL, I2Ct_SDA		internally limited	
	Positive source current for LDO_3V3, LDO_1V5		internally limited	
Source current	GPIOx		0.005	A
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

5.1.2 TPS26750 - Absolute Maximum Ratings

		MIN	MAX	UNIT
POWER_PATH_EN	V_{VSYS} = GND	–0.5	12	V

5.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3.1 TPS26750 - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	
		VBUS	4	22	
		VSYS	0	22	

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IO}	I/O voltage range	I2Cx_SDA, I2Cx_SCL, $\overline{\text{I2Cx\_IRQ}}$, ADCIN1, ADCIN2	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	sum of current from LDO_3V3 and GPIOx		5	mA
T_A	Ambient operating temperature	$I_{PP\_5V} \le 1.5$ A, $I_{PP\_CABLE} \le 315$ mA	–40	105	°C
		$I_{PP\_5V} \le 3$ A, $I_{PP\_CABLE} \le 315$ mA	–40	85	
T_J	Operating junction temperature		–40	125	°C

5.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3 V	5	10		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4 V	4.5		12	µF
C_{VBUS}	Capacitance on VBUS	25 V	1	4.7	10	µF
C_{PP5V}	Capacitance on PP5V	10 V	120			µF
C_{CCy}	Capacitance on CCy pins	6.3 V	200	400	480	pF

5.5 Thermal Information

5.5.1 TPS26750 - Thermal Information

THERMAL METRIC		TPS26750 QFN (RSM) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JC}$	Junction-to-board (bottom) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

5.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
V_{VBUS_UVLO}	VBUS UVLO threshold	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		
V_{VIN3V3_UVLO}	Voltage required on VIN_3V3 for power on	rising, V_{VBUS} = 0	2.56	2.66	2.76	V
		falling, V_{VBUS} = 0	2.44	2.54	2.64	
		hysteresis		0.12		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	Voltage on LDO_3V3	V_{VIN_3V3} = 0 V, 10 µA ≤ I_{LOAD} ≤ 18 mA, $_{VBUS}$ ≥ 3.9 V	3.0	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3} = 50 mA			1.4	Ω
V_{LDO_1V5}	Voltage on LDO_1V5	up to maximum internal loading condition	1.49	1.5	1.65	V

5.7 Power Consumption

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN\_3V3,ActSrc}$	Current into VIN_3V3	Active Source mode: V_{VBUS} = 5.0 V, V_{VIN_3V3} = 3.3 V		3		mA
$I_{VIN\_3V3,ActSnk}$	Current into VIN_3V3	Active Sink mode: 22 V ≥ V_{VBUS} ≥ 4.0 V, V_{VIN_3V3} = 3.3 V		3	6	mA
$I_{VIN\_3V3,IdlSrc}$	Current into VIN_3V3	Idle Source mode: V_{VBUS} = 5.0 V, V_{VIN_3V3} = 3.3 V		1.0		mA
$I_{VIN\_3V3,IdlSnk}$	Current into VIN_3V3	Idle Sink mode: 22 V ≥ V_{VBUS} ≥ 4.0 V, V_{VIN_3V3} = 3.3 V		1.0		mA
$P_{MstbySnk}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Sink Mode	CCm floating, V_{CCn} = 0.4 V, V_{PP5V} = 5 V, V_{VIN_3V3} = 3.3 V, V_{VBUS} = 5.0 V, POWER_PATH_EN disabled, and T_J = 25°C		4.1		mW
$P_{MstbySrc}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Source Mode	CCm floating, CCn tied to GND through 5.1 kΩ, V_{PP5V} = 5 V, V_{VIN_3V3} = 3.3 V, I_{VBUS} = 0, T_J = 25°C		4.5		mW
$I_{PP5V,Sleep}$	Current into PP5V	Sleep mode: V_{PA_VBUS} = 0 V, V_{VIN_3V3} = 3.3 V		2		µA
$I_{VIN\_3V3,Sleep}$	Current into VIN_3V3	Sleep mode: V_{VBUS} = 0 V, V_{VIN_3V3} = 3.3 V		56		µA

5.8 PP_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J = 25°C		36	38	mΩ
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A,T_J = 125°C		36	53	mΩ
I_{PP5V_REV}	VBUS to PP5V leakage current	V_{PP5V} = 0 V, V_{VBUS} = 5.5 V, PP_5V disabled, T_J ≤ 85°C, measure I_{PP5V}			5	µA
I_{PP5V_FWD}	PP5V to VBUS leakage current	V_{PP5V} = 5.5 V, V_{VBUS} = 0 V, PP_5V disabled, T_J ≤ 85°C, measure I_{VBUS}			15	µA
I_{LIM5V}	Current limit setting	Configure to setting 0	1.15		1.36	A
I_{LIM5V}	Current limit setting	Configure to setting 1	1.61		1.90	A
I_{LIM5V}	Current limit setting		2.3		2.70	A
I_{LIM5V}	Current limit setting	Configure to setting 3	3.04		3.58	A
I_{LIM5V}	Current limit setting	Configure to setting 4	3.22		3.78	A

5.8 PP_5V Power Switch Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS}	PP5V to VBUS current sense accuracy	3.64 A ≥ I_{VBUS} ≥ 1 A	3.05	3.5	3.75	A/V
$V_{PP\_5V\_RCP}$	RCP clears and PP_5V starts turning on when V_{VBUS} – V_{PP5V} < $V_{PP\_5V\_RCP}$. Measure V_{VBUS} – V_{PP5V}		10		20	mV
$t_{iOS\_PP\_5V}$	Response time to VBUS short circuit	VBUS to GND through 10 mΩ, C_{VBUS} = 0		1.15		µs
$t_{PP\_5V\_ovp}$	Response time to V_{VBUS} > $V_{OVP4RCP}$	Enable PP_5V, I_{RpDef} being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 20 V at 100 V/ms, C_{PP5V} = 2.5 µF, measure time from OVP detection until reverse current < 100 mA		4.5		µs
$t_{PP\_5V\_uvlo}$	Response time to V_{PP5V} < V_{PP5V_UVLO}, PP_VBUS is deemed off when V_{VBUS} < 0.8 V	R_L = 100 Ω, no external capacitance on VBUS		4		µs
$t_{PP\_5V\_rcp}$	Response time to V_{PP5V} < V_{VBUS} + $V_{PP\_5V\_RCP}$	V_{PP5V} = 5.5 V, I_{RpDef} being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4 V to 21.5 V at 10 V/µs, measure V_{PP5V}. C_{PP5V} = 104 µF, C_{VBUS}=10 µF, measure time from RCP detection until reverse current < 100 mA		0.7		µs
t_{ILIM}	Current clamping deglitch time			5.1		ms
t_{ON}	From enable signal to VBUS at 90% of final value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	2.3	3.3	4.3	ms
t_{OFF}	From disable signal to VBUS at 10% of final value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	0.30	0.45	0.6	ms
t_{RISE}	VBUS from 10% to 90% of final value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	1.2	1.7	2.2	ms
t_{FALL}	VBUS from 90% to 10% of initial value	R_L = 100 Ω, V_{PP5V} = 5 V, C_L = 0	0.06	0.1	0.14	ms

5.9 POWER_PATH_EN Characteristics - TPS26750

Operating under these conditions unless otherwise noted: , 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{POWER\_PATH\_EN}$	Sourcing current	V_{GATE_VSYS} = 0 V	8.5		11.5	µA
$V_{POWER\_PATH\_EN}$	Sourcing voltage (ON)	V_{VSYS} = 0 V,	6		12	V
$I_{POWER\_PATH\_EN}$	Sinking strength	V_{VSYS} = 0 V	13			µA

5.10 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PP5V_UVLO}	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DSCH}	VBUS discharge current	V_{VBUS} = 22 V, measure I_{VBUS}	4		15	mA

5.11 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pullup)						
$V_{OC\_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	V_{LDO_3V3} > 2.302 V, R_{CC} = 47 kΩ	1.85			V
V_{OC_5}	Attached CCy open circuit voltage while Rp enabled, no load	V_{PP5V} > 3.802 V, R_{CC} = 47 kΩ	2.95			V
I_{Rev}	Unattached reverse current on CCy	V_{CCy} = 5.5 V, V_{CCx} = 0 V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 3.8 V, measure current into CCy			10	µA
		V_{CCy} = 5.5 V, V_{CCx} = 0 V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 0, T_J ≤ 85°C, measure current into CCy			10	
I_{RpDef}	Current source - USB Default	0 < V_{CCy} < 1.0 V, measure I_{CCy}	64	80	96	µA
$I_{Rp1.5}$	Current source - 1.5 A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 1.5 V, measure I_{CCy}	166	180	194	µA
$I_{Rp3.0}$	Current source - 3.0 A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 2.45 V, measure I_{CCy}	304	330	356	µA
Type-C Sink (Rd pulldown)						
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	rising	0.2		0.24	V
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	falling	0.16		0.20	V
	Hysteresis			0.04		V
V_{SNK2}	Default/1.5-A detection threshold	falling	0.62		0.68	V
V_{SNK2}	Default/1.5-A detection threshold	rising	0.63	0.66	0.69	V
	Hysteresis			0.01		V
V_{SNK3}	1.5-A/3.0-A detection threshold when Rd applied to CCy	falling	1.17		1.25	V
V_{SNK3}	1.5-A/3.0-A detection threshold when Rd applied to CCy	rising	1.22		1.3	V
	Hysteresis			0.05		V
R_{SNK}	Rd pulldown resistance	0.25 V ≤ V_{CCy} ≤ 2.1 V, measure resistance on CCy	4.6		5.6	kΩ
R_{VCONN_DIS}	VCONN discharge resistance	0V ≤ V_{CCy} ≤ 5.5 V, measure resistance on CCy	4.0		6.12	kΩ
V_{CLAMP}	Dead battery Rd clamp	V_{VIN_3V3} = 0 V, 64 µA < I_{CCy} < 96 µA	0.25		1.32	V
		V_{VIN_3V3} = 0 V, 166 µA < I_{CCy} < 194 µA	0.65		1.32	
		V_{VIN_3V3} = 0 V, 304 µA < I_{CCy} < 356 µA	1.20		2.18	

5.11 CC Cable Detection Parameters (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{Open}	Resistance from CCy to GND when configured as open	V_{VBUS} = 0, V_{VIN_3V3} = 3.3 V, V_{CCy} = 5 V, measure resistance on CCy	500			kΩ
		V_{VBUS} = 5 V, V_{VIN_3V3} = 0, V_{CCy} = 5 V, measure resistance on CCy	500			kΩ

5.12 CC VCONN Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{PP5V} = 5 V, I_L = 250 mA, measure resistance from PP5V to CCy			1.2	Ω
I_{LIMVC}	Short circuit current limit	Setting 0, V_{PP5V} = 5 V, R_L=10 mΩ, measure I_{CCy}	350	410	470	mA
I_{LIMVC}	Short circuit current limit	Setting 1, V_{PP5V} = 5 V, R_L=10 mΩ, measure I_{CCy}	540	600	660	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, T_J ≤ 85°C, V_{CCy} = 5.5 V, V_{PP5V} = 0 V, V_{VBUS} = 5 V, LDO forced to draw from VBUS, measure I_{CCy}			10	µA
V_{VC_OVP}	Overvoltage protection threshold for PP_CABLE	V_{PP5V} rising	5.6	5.9	6.2	V
V_{VC_RCP}	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	V_{PP5V} ≥ 4.9 V, V_{CCy} = V_{PP5V}, V_{CCx} rising	60	200	340	mV
		V_{PP5V} ≥ 4.9 V, V_{CCy} ≤ 4 V, V_{CCx} rising	210	340	470	mV
t_{VCILIM}	Current clamp deglitch time			1.3		ms
$t_{PP\_CABLE\_FSD}$	Time to disable PP_CABLE after V_{PP5V} > V_{VC_OVP} or V_{CCx} - V_{PP5V} > V_{VC_RCP}	C_L = 0		0.5		µs
$t_{PP\_CABLE\_off}$	From disable signal to CCy at 10% of final value	I_L = 250 mA, V_{PP5V} = 5 V, C_L = 0	100	200	300	µs
$t_{iOS\_PP\_CABLE}$	Response time to short circuit	V_{PP5V} = 5 V, for short circuit R_L = 10 mΩ		2		µs

5.13 CC PHY Parameters

Operating under these conditions unless otherwise noted: and (3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{VBUS} ≥ 3.9 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on CCy	Standard External load	–75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using CCy	measured at 750 kHz	33	54	75	Ω
t_{Rise}	Rise time. 10 % to 90 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520 pF	300			ns
t_{Fall}	Fall time. 90 % to 10 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520 pF	300			ns

Operating under these conditions unless otherwise noted: and (3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{VBUS} ≥ 3.9 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PHY_OVP}	OVP detection threshold for USB PD PHY	0 ≤ V_{VIN_3V3} ≤ 3.6 V, 0 ≤ V_{PP5V} ≤ 5.5 V, V_{VBUS} ≥ 4 V. Initially V_{CC1} ≤ 5.5 V and V_{CC2} ≤ 5.5 V, then V_{CCx} rises	5.5		8.5	V
Receiver						
Z_{BMCRX}	Receiver input impedance on CCy	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z	1			MΩ
C_{CC}	Receiver capacitance on CCy (1)	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX\_SNK\_R}$	Rising threshold on CCy for receiver comparator	Sink mode (rising)	499	525	551	mV
$V_{RX\_SRC\_R}$	Rising threshold on CCy for receiver comparator	Source mode (rising)	784	825	866	mV
$V_{RX\_SNK\_F}$	Falling threshold on CCy for receiver comparator	Sink mode (falling)	230	250	270	mV
$V_{RX\_SRC\_F}$	Falling threshold on CCy for receiver comparator	Source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{CCy} externally.

5.14 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		Hysteresis		15		°C
T_{SD_PP5V}	Temperature controlled shutdown threshold. The power paths for each port sourcing from PP5V and PP_CABLE power paths have local sensors that disables them when the temperature is exceeded	Temperature rising	135	150	165	°C
		Hysteresis		10		°C

5.15 ADC Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6-V max scaling, voltage divider of 3		14		mV
		25.2-V max scaling, voltage divider of 21		98		mV
		4.07-A max scaling		16.5		mA
GAIN_ERR	Gain error	0.05 V ≤ V_{ADCINx} ≤ 3.6 V, V_{ADCINx} ≤ V_{LDO_3V3}	–2.7		2.7	%
		0.05 V ≤ V_{GPIOx} ≤ 3.6 V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7 V ≤ V_{LDO_3V3} ≤ 3.6 V	–2.4		2.4	
		0.6 V ≤ V_{VBUS} ≤ 22 V	–2.1		2.1	
		1 A ≤ I_{VBUS} ≤ 3 A	–2.1		2.1	
VOS_ERR	Offset error (1)	0.05 V ≤ V_{ADCINx} ≤ 3.6 V, V_{ADCINx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
		0.05 V ≤ V_{GPIOx} ≤ 3.6 V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7 V ≤ V_{LDO_3V3} ≤ 3.6 V	–4.5		4.5	
		0.6 V ≤ V_{VBUS} ≤ 22 V	–4.1		4.1	
		1 A ≤ I_{VBUS} ≤ 3 A	–4.5		4.5	mA

(1) The offset error is specified after the voltage divider.

5.16 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB_P, USB_N						
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3 V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3 V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3 V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45 V	–1		1	µA
GPIO_RPU	GPIOx internal pullup	Pullup enabled	50	100	150	kΩ
GPIO_RPD	GPIOx internal pulldown	Pulldown enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20	50	ns
GPIO0-7 (Outputs)						
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3 V, I_{GPIOx}= -2 mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3 V, I_{GPIOx} = 2 mA			0.4	V

5.16 Input/Output (I/O) Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCIN1, ADCIN2						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} ≤ V_{LDO_3V3}	–1		1	µA
t_{BOOT}	Time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

5.17 BC1.2 Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA CONTACT DETECT						
I_{DP_SRC}	DCD source current	V_{LDO_3V3} = 3.3 V	7	10	13	µA
R_{DM_DWN}	DCD pulldown resistance	V_{USB_N} = 3.6 V	14.25	20	24.8	kΩ
R_{DP_DWN}	DCD pulldown resistance	V_{USB_P} = 3.6 V	14.25	20	24.8	kΩ
V_{LGC_HI}	Threshold for no connection	V_{USB_P} ≥ V_{LGC_HI}, V_{LDO_3V3} = 3.3 V, R_{USB_P} = 300 kΩ	2		3.6	V
V_{LGC_LO}	Threshold for connection	V_{USB_N} ≤ V_{LGC_LO}, V_{LDO_3V3} = 3.3 V, R_{USB_P} = 24.8 kΩ	0		0.8	V
Advertisement and Detection						
V_{DX_ILIM}	VDX_SRC current limit		250		400	µA
I_{DX_SNK}	Sink Current	V_{USB_P} ≥ 250 mV	25	75	125	µA
I_{DX_SNK}	Sink Current	V_{USB_N} ≥ 250 mV	25	75	125	µA
R_{DCP_DAT}	Dedicated Charging Port Resistance	0.5 V ≤ V_{USB_P} ≤ 0.7 V, 25 µA ≤ I_{USB_N} ≤ 175 µA			200	Ω

5.18 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{I2Ct\_IRQ}}$						
OD_VOL_IRQ	Low level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, V_{I2Cx_IRQ} = 3.45 V	–1		1	µA
$\overline{\text{I2Cc\_IRQ}}$						
IRQ_VIH	High-Level input voltage	V_{LDO_3V3} = 3.3 V	1.3			V
IRQ_VIH_THRESH	High-Level input voltage threshold	V_{LDO_3V3} = 3.3 V	0.72		1.3	V
IRQ_VIL	low-level input voltage	V_{LDO_3V3} = 3.3 V			0.54	V
IRQ_VIL_THRESH	low-level input voltage threshold	V_{LDO_3V3} = 3.3 V	0.54		1.08	V
IRQ_HYS	input hysteresis voltage	V_{LDO_3V3} = 3.3 V	0.09			V
IRQ_DEG	input deglitch			20		ns
IRQ_ILKG	$\overline{\text{I2Cc\_IRQ}}$ leakage current	V_{I2Cc_IRQ} = 3.45 V	–1		1	µA
SDA and SCL Common Characteristics (Controller, Target)						
V_{IL}	Input low signal	V_{LDO_3V3} = 3.3 V			0.54	V
I_{OL}	Max output low current	V_{OL} = 0.4 V	15			mA
I_{OL}	Max output low current	V_{OL} = 0.6 V	20			mA
t_f	Fall time from 0.7 × V_{DD} to 0.3 × V_{DD}	V_{DD} = 1.8 V, 10 pF ≤ C_b ≤ 400 pF	12		80	ns
		V_{DD} = 3.3 V, 10 pF ≤ C_b ≤ 400 pF	12		150	ns
t_{SP}	I^2C pulse width suppressed				50	ns

5.18 I2C Requirements and Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Target)						
f_{SCLS}	Clock frequency for target	V_{DD} = 1.8 V or 3.3 V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8 V or 3.3 V, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8 V or 3.3 V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Target)						
f_{SCLS}	Clock frequency for target	V_{DD} = 1.8 V or 3.3 V	100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8 V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8 V or 3.3 V, ACK signal from SCL low to SDA (out) low			0.9	µs
f_{SCLS}	Clock frequency for Fast Mode Plus(1)	V_{DD} = 1.8 V or 3.3 V	400		800	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8 V or 3.3 V, SCL low to SDA output valid			0.55	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8 V or 3.3 V, ACK signal from SCL low to SDA (out) low			0.55	µs
t_{LOW}	Clock low time	V_{DD} = 3.3 V	1.3			µs
t_{HIGH}	Clock high time	V_{DD} = 3.3 V	0.6			µs

(1) Controller must control fSCLS to ensure tLOW > tVD; ACK.

5.19 Typical Characteristics

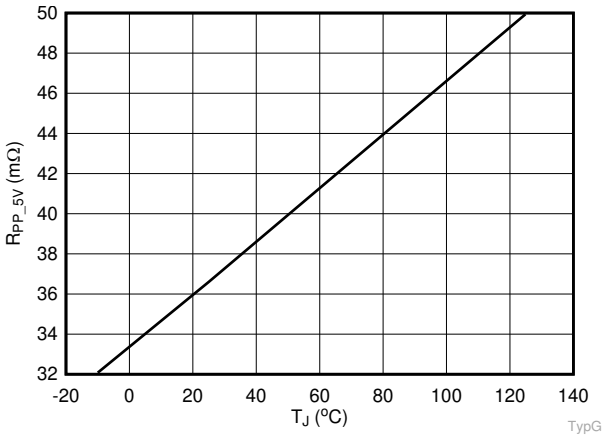


Figure 5-1. PP_5V Rdson vs. Temperature.

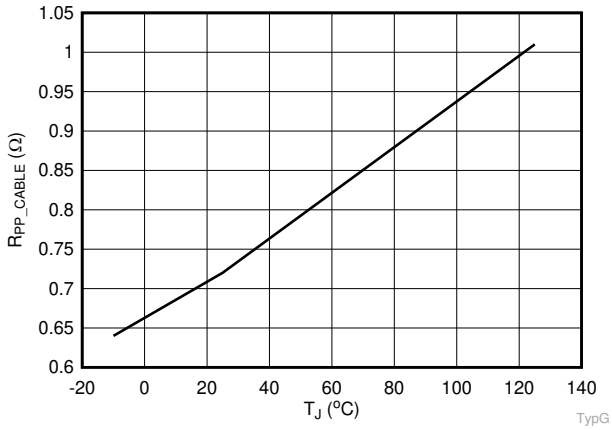


Figure 5-2. PP_CABLE Rdson vs. Temperature

6 Parameter Measurement Information

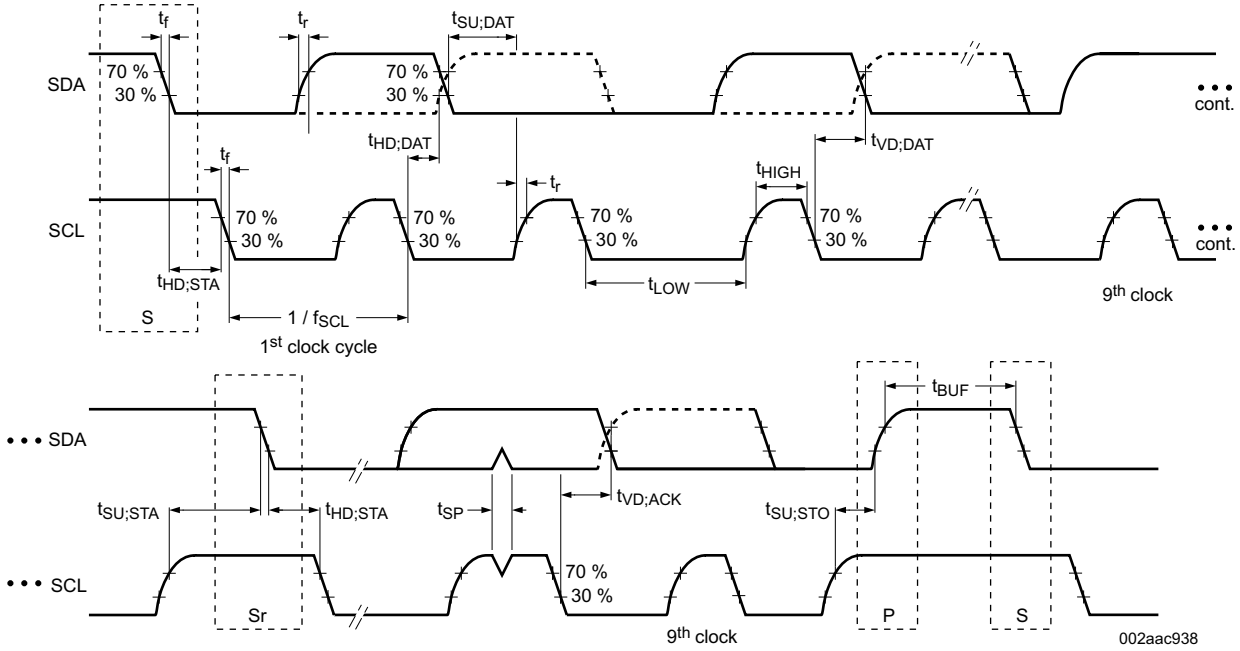


Figure 6-1. I²C Target Interface Timing

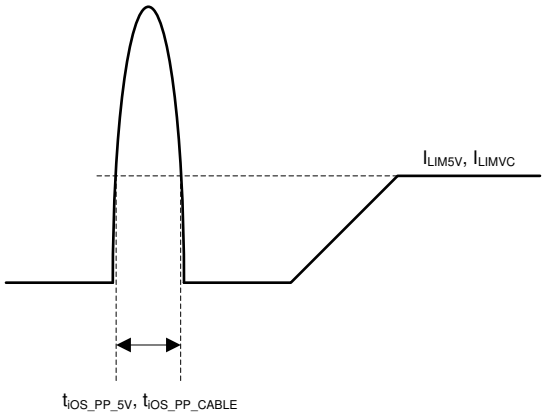


Figure 6-2. Short-circuit Response Time for Internal Power Paths PP_5V and PP_CABLE

7 Detailed Description

7.1 Overview

The TPS26750 is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacles. The TPS26750 communicates with the cable and another USB Type-C and PD device at the opposite end of the cable. The device also enables integrated port power switch for sourcing, and controls a high current port power switch for sinking.

The TPS26750 is divided into several main sections:

- USB-PD controller
- Cable plug and orientation detection circuitry
- Port power switches
- Power management circuitry
- Digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features, and more detailed circuitry, see *USB-PD Physical Layer*.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features, and more detailed circuitry, see *Cable Plug and Orientation Detection*.

The port power switches provide power to the VBUS pin and CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features, and more detailed circuitry, see *Power Paths*.

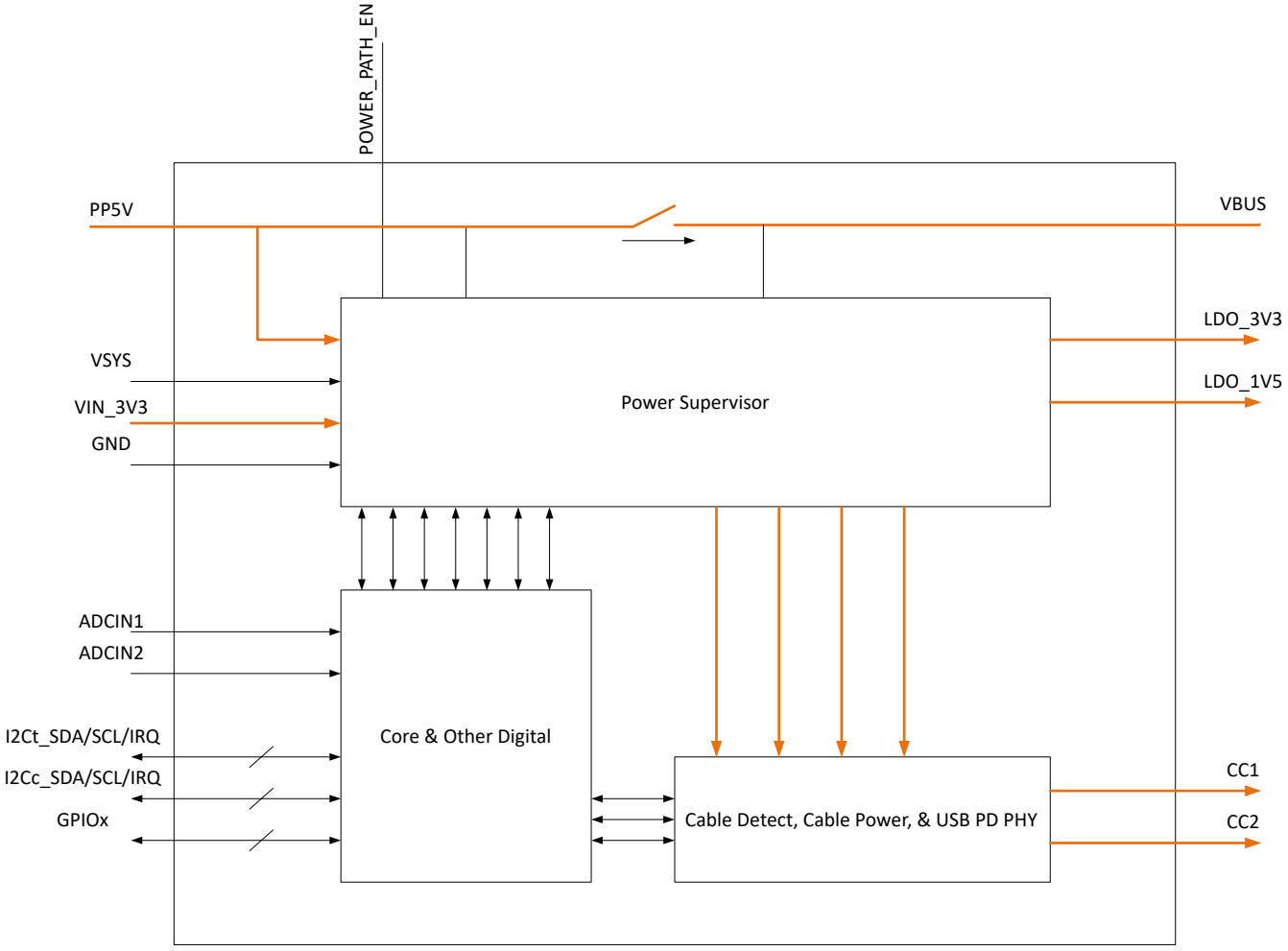
The power management circuitry receives and provides power to the TPS26750 internal circuitry and LDO_3V3 output. See *Power Management* for more information.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS26750 functionality. A portion of the digital core contains ROM memory, which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called boot code, is capable of initializing the TPS26750, loading of the device configuration information, and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features, and more detailed circuitry, see *Digital Core*.

The TPS26750 has one I^2C controller to write to and read from external target devices such as a battery charger or an optional external EEPROM memory (see *I2C Interface*).

The TPS26750 also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 USB-PD Physical Layer

Figure 7-1 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

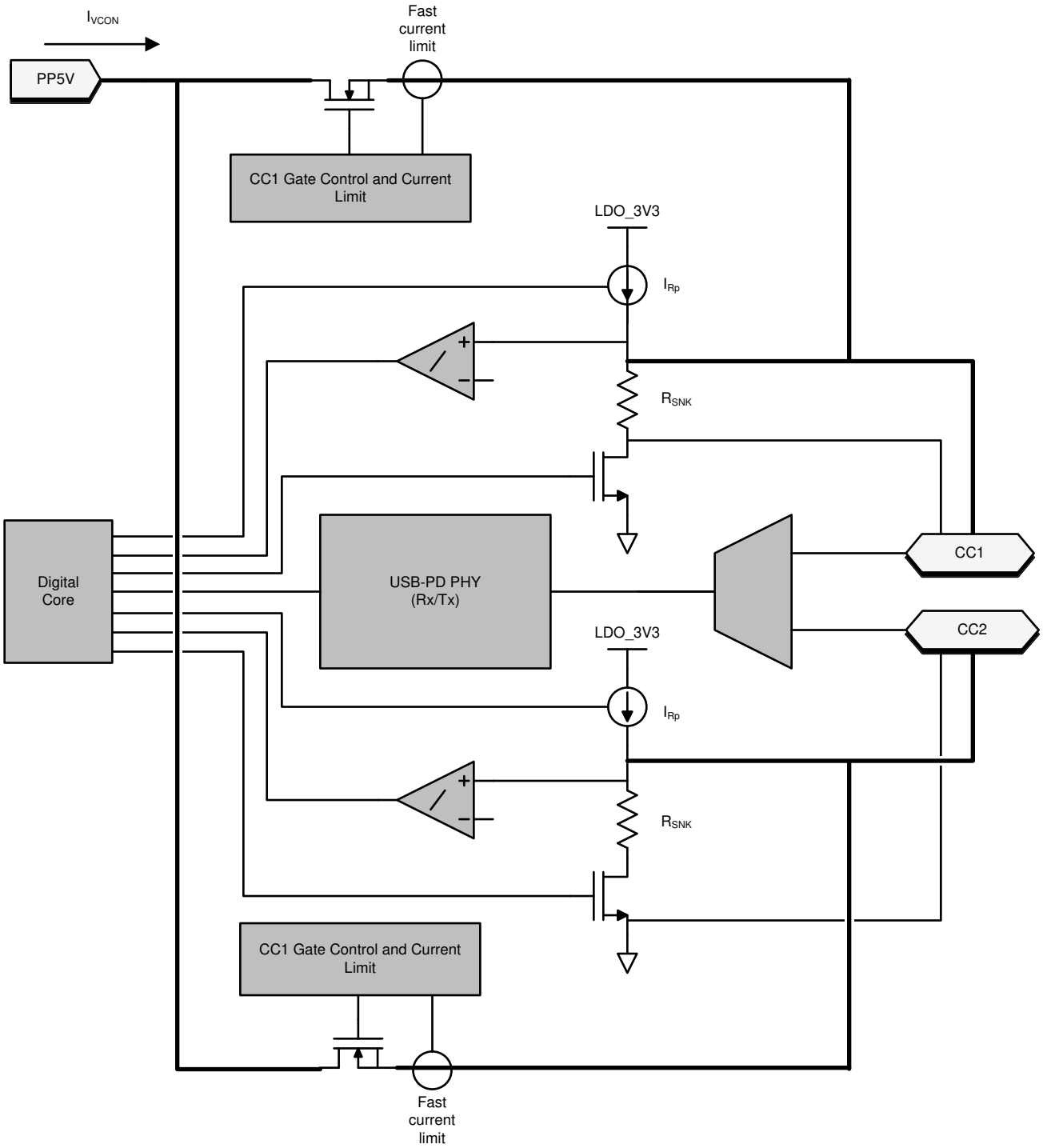


Figure 7-1. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

7.3.1.1 USB-PD Encoding and Signaling

Figure 7-2 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 7-3 illustrates the high-level block diagram of the baseband USB-PD receiver.

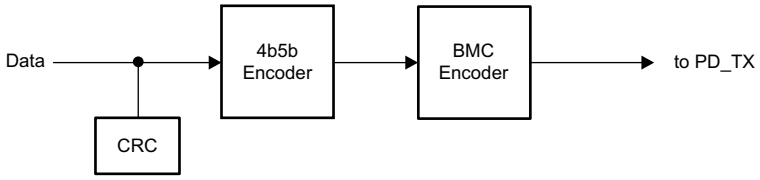


Figure 7-2. USB-PD Baseband Transmitter Block Diagram

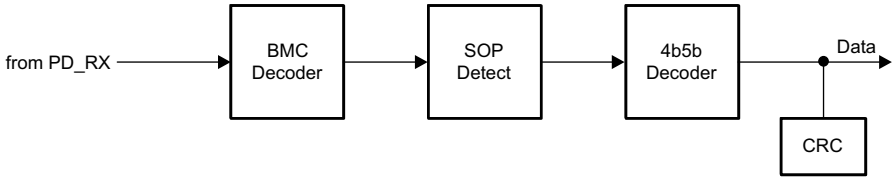


Figure 7-3. USB-PD Baseband Receiver Block Diagram

7.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS26750 is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 7-4 illustrates Biphase Mark Coding.

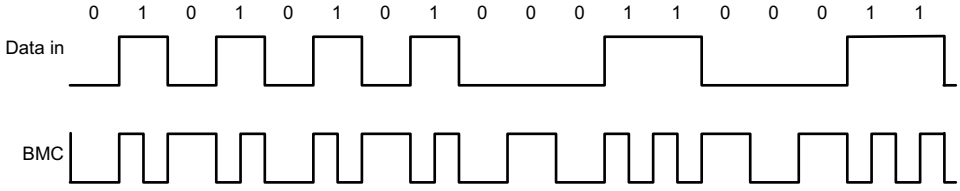


Figure 7-4. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

7.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Because a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

7.3.1.4 USB-PD BMC Transmitter

The TPS26750 transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CCy pin when it is not transmitting. While either CC1 or CC2 can be used for transmitting and receiving, during a given connection only, the one that mates with the CC pin of the plug is used, so there is no dynamic switching between CC1 and CC2. Figure 7-5 shows the USB-PD BMC TX and RX driver block diagram.

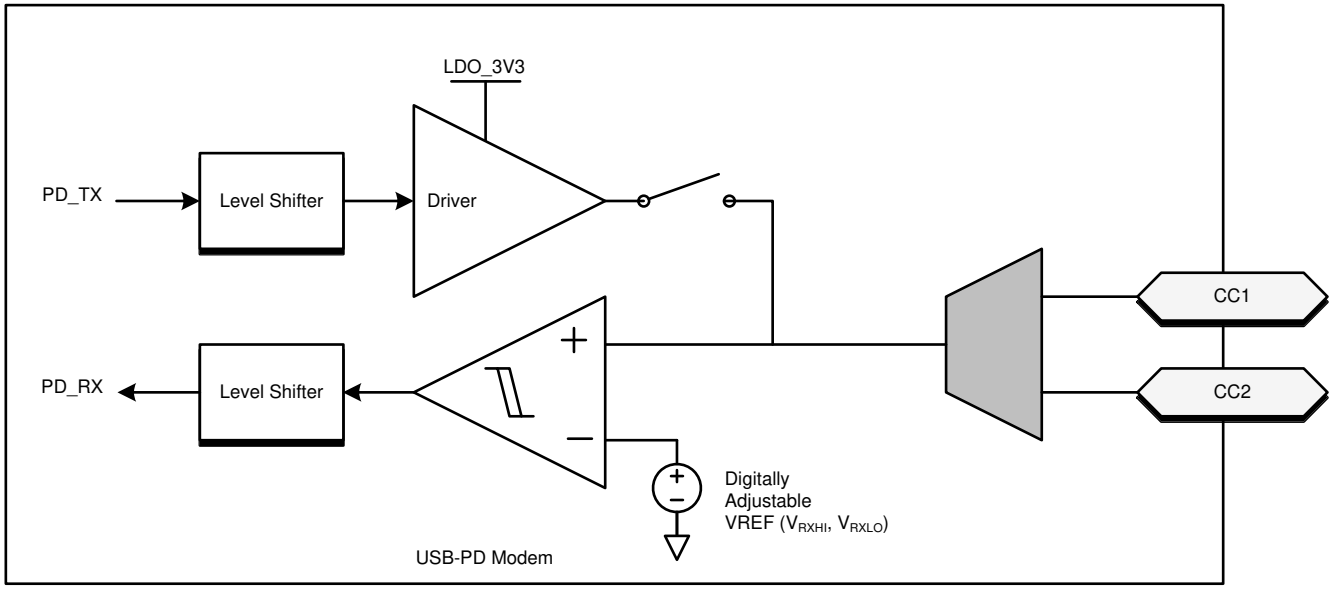


Figure 7-5. USB-PD BMC TX/Rx Block Diagram

Figure 7-6 shows the transmission of the BMC data on top of the DC bias. Note that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This note means that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This note means that the DC bias can be above or below the VOH of the transmitter driver.

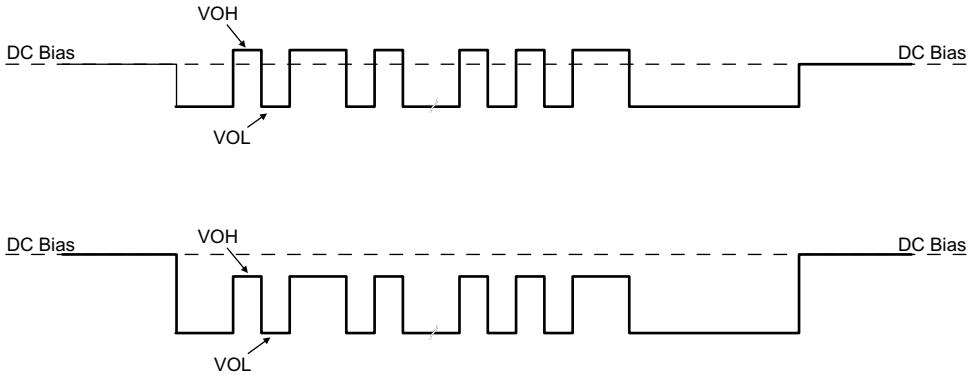


Figure 7-6. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

Figure 7-7 shows the simplified circuit determining Z_{DRIVER}. It is specified such that noise at the receiver is bounded.

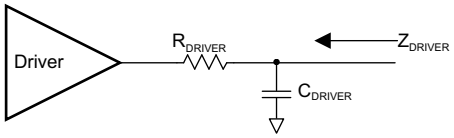


Figure 7-7. ZDRIVER Circuit

7.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS26750 receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 7-8 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

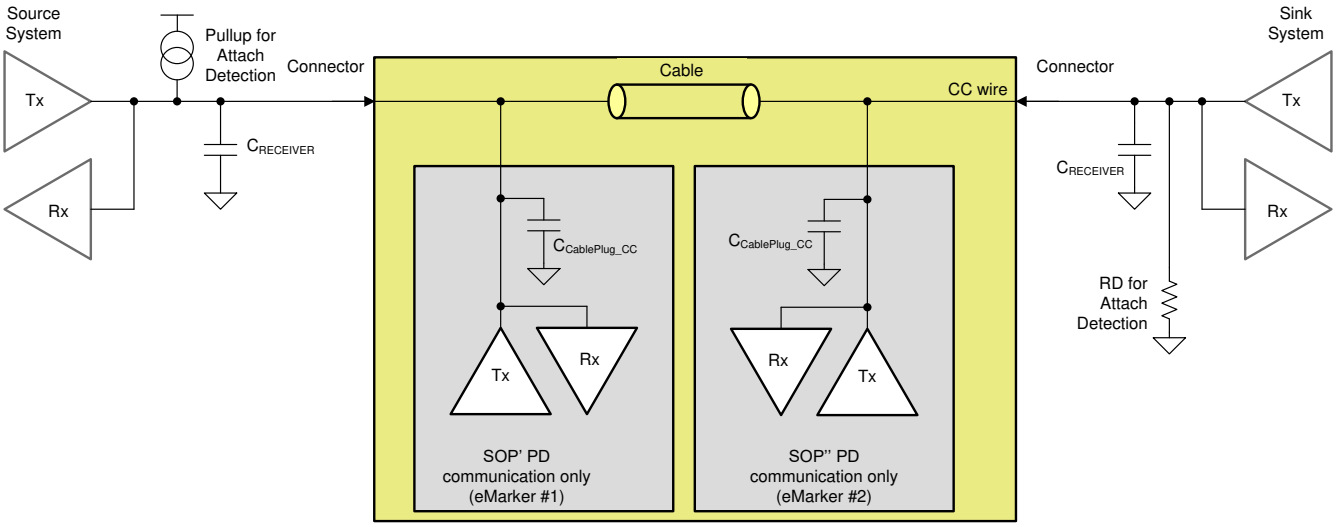


Figure 7-8. Example USB-PD Multi-Drop Configuration

7.3.1.6 Squelch Receiver

The TPS26750 has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

7.3.2 Power Management

The TPS26750 power management block receives power and generates voltages to provide power to the TPS26750 internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 can also be used as a low power output for external EEPROM memory. The power supply path is shown in Figure 7-9.

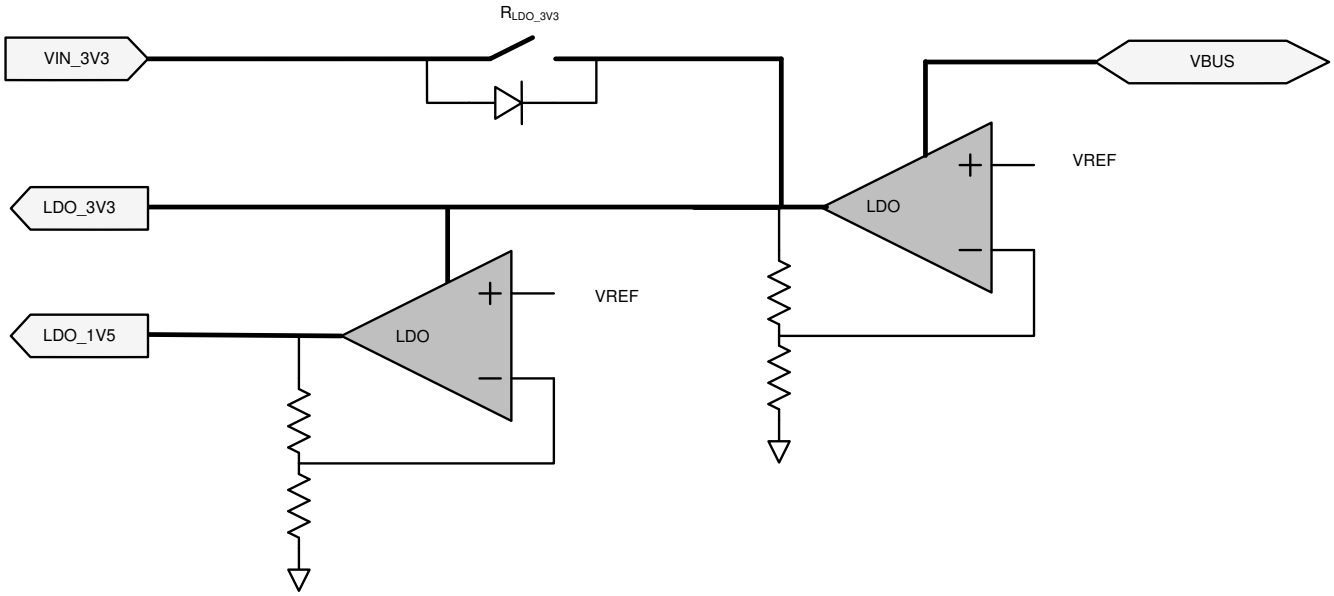


Figure 7-9. Power Supplies

The TPS26750 is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5-V core digital circuitry. When VIN_3V3 power is unavailable and power is available on VBUS, it is referred to as the dead-battery start-up condition. In a dead-battery start-up condition, the TPS26750 opens the VIN_3V3 switch until the host clears the dead-battery flag through I^2C. Therefore, the TPS26750 is powered from the VBUS input with the higher voltage during the dead-battery start-up condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO_3V3.

7.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

7.3.2.2 VBUS LDO

The TPS26750 contains an internal high-voltage LDO which is capable of converting VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used when VIN_3V3 is low (the dead-battery condition). The VBUS LDO is powered from VBUS.

7.3.3 Power Paths

The TPS26750 has internal sourcing power paths: PP_5V and PP_CABLE. Each power path is described in detail in this section.

7.3.3.1 Internal Sourcing Power Paths

Figure 7-10 shows the TPS26750 internal sourcing power paths. The path from PP5V to VBUS is called PP_5V. The path from PP5V to CCx is called PP_CABLE. Each path contains two back-to-back common drain N-FETs, with current clamping protection, overvoltage protection, UVLO protection, and temperature sensing circuitry. PP_5V can conduct up to 3 A continuously, while PP_CABLE can conduct up to 315 mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that can appear on VBUS.

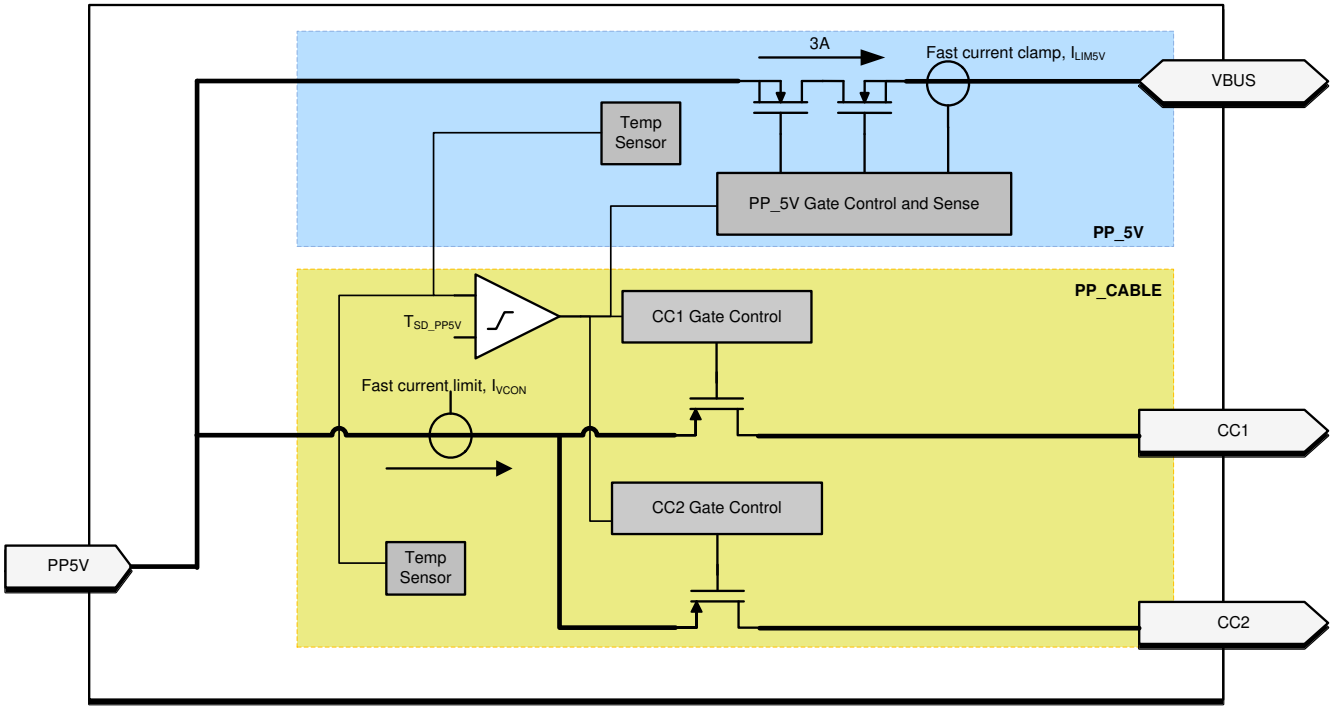


Figure 7-10. Port Power Switches

7.3.3.1.1 PP_5V Current Clamping

The current through the internal PP_5V path are current limited to I_{LIM5V}. The I_{LIM5V} value is configured by application firmware. When the current through the switch exceeds I_{LIM5V}, the current limiting circuit activates within $t_{iOS\_PP\_5V}$ and the path behaves as a constant current source. If the duration of the overcurrent event exceeds t_{ILIM}, the PP_5V switch is disabled.

7.3.3.1.2 PP_5V Local Overtemperature Shut Down (OTSD)

When PP_5V clamps the current, the temperature of the switch begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$, the PP_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

7.3.3.1.3 PP_5V OVP

The overvoltage protection level is automatically configured based on the expected maximum V_{BUS} voltage, which depends upon the USB PD contract. When the voltage on the VBUS pin of a port exceeds the configured value ($V_{OVP4RCP}$) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_ovp}$ and the port enters into the Type-C ErrorRecovery state.

7.3.3.1.4 PP_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_uvlo}$ and the port that had PP_5V enabled enters into the Type-C ErrorRecovery state.

7.3.3.1.5 PP_5Vx Reverse Current Protection

If V_{VBUS} - V_{PP5V} > $V_{PP\_5V\_RCP}$, then the PP_5V path is automatically disabled within $t_{PP\_5V\_rcp}$. If the RCP condition clears, then the PP_5V path is automatically enabled within t_{ON}.

7.3.3.1.6 PP_CABLE Current Clamp

When enabled and providing VCONN power, the TPS26750 PP_CABLE power switch clamps the current to I_{VCON}. When the current through the PP_CABLE switch exceeds I_{VCON}, the current clamping circuit activates within $t_{iOS\_PP\_CABLE}$ and the switch behaves as a constant current source.

7.3.3.1.7 PP_CABLE Local Overtemperature Shut Down (OTSD)

When PP_CABLE clamps the current, the temperature of the switch begins to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$, the PP_CABLE switch is disabled and latched off within $t_{PP\_CABLE\_off}$. The port then enters the USB Type-C ErrorRecovery state.

7.3.3.1.8 PP_CABLE UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}), then the PP_CABLE switch is automatically disabled within $t_{PP\_CABLE\_off}$.

7.3.4 Cable Plug and Orientation Detection

Figure 7-11 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

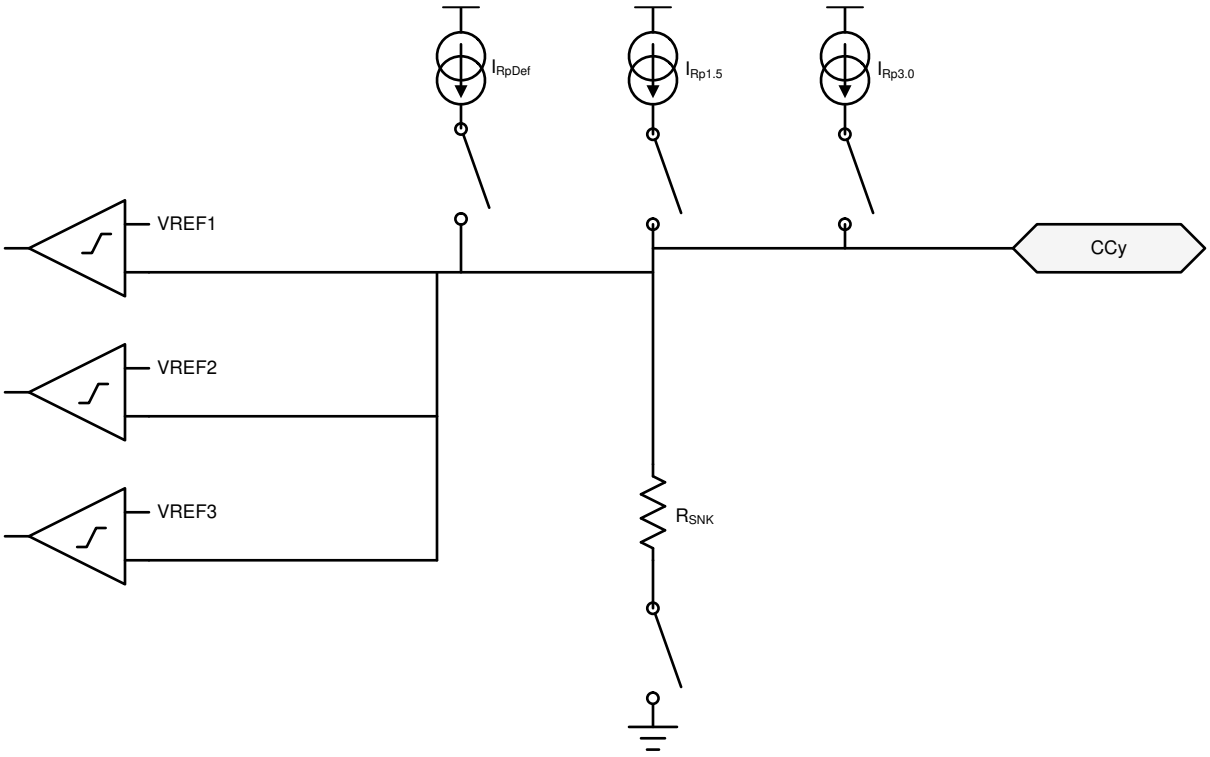


Figure 7-11. Plug and Orientation Detection Block

7.3.4.1 Configured as a Source

When configured as a source, the TPS26750 detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS26750 monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 7-1 shows the Cable Detect States for a Source.

Table 7-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).

Table 7-1. Cable Detect States for a Source (continued)

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either CCy pin for detach.

When a TPS26750 port is configured as a Source, a current I_{RpDef} is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin, a pulldown resistance of Rd to GND exists. The current I_{RpDef} is then forced across the resistance Rd, generating a voltage at the CCy pin. The TPS26750 applies I_{RpDef} until it closes the switch from PP5V to VBUS, at which time application firmware can change to $I_{Rp1.5A}$ or $I_{Rp3.0A}$.

When the CCy pin is connected to an active cable VCONN input, the pulldown resistance is different (Ra). In this case, the voltage on the CCy pin lowers the PD controller recognizes it as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

7.3.4.2 Configured as a Sink

When a TPS26750 port is configured as a Sink, the TPS26750 presents a pulldown resistance R_{SNK} on each CCy pin and waits for a Source to attach and pull up the voltage on the pin. The Sink detects an attachment by the presence of VBUS and determines the advertised current from the Source based on the voltage on the CCy pin.

7.3.4.3 Configured as a DRP

When a TPS26750 port is configured as a DRP, the TPS26750 alternates the CCy pins of the port between the pulldown resistance, R_{SNK}, and pullup current source, I_{Rp}.

7.3.4.4 Dead Battery Advertisement

The TPS26750 supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. TPS26750 hardware is configured to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd once the device no longer requires power from VBUS.

7.3.5 Overvoltage Protection (CC1, CC2)

The TPS26750 detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP_CABLE within $t_{PP\_CABLE\_FSD}$ and disable the USB PD transmitter.

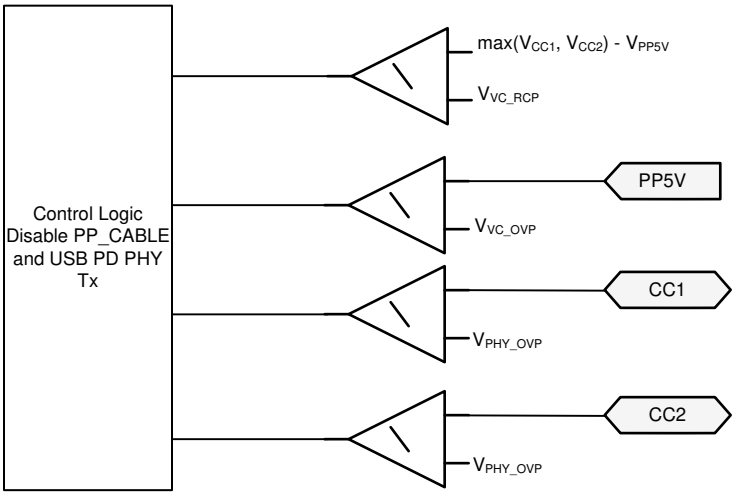


Figure 7-12. Overvoltage and Reverse Current Protection for CC1 and CC2

7.3.6 Default Behavior Configuration (ADCIN1, ADCIN2)

Note

This functionality is firmware controlled and subject to change.

The ADCINx inputs to the internal ADC control the behavior of the TPS26750 in response to VBUS being supplied when VIN_3V3 is low (that is the dead-battery scenario). The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine start-up behavior. The available start-up configurations include options for I^2C target address of I2Ct_SCL/SDA, sink path control in dead-battery, and default configuration.

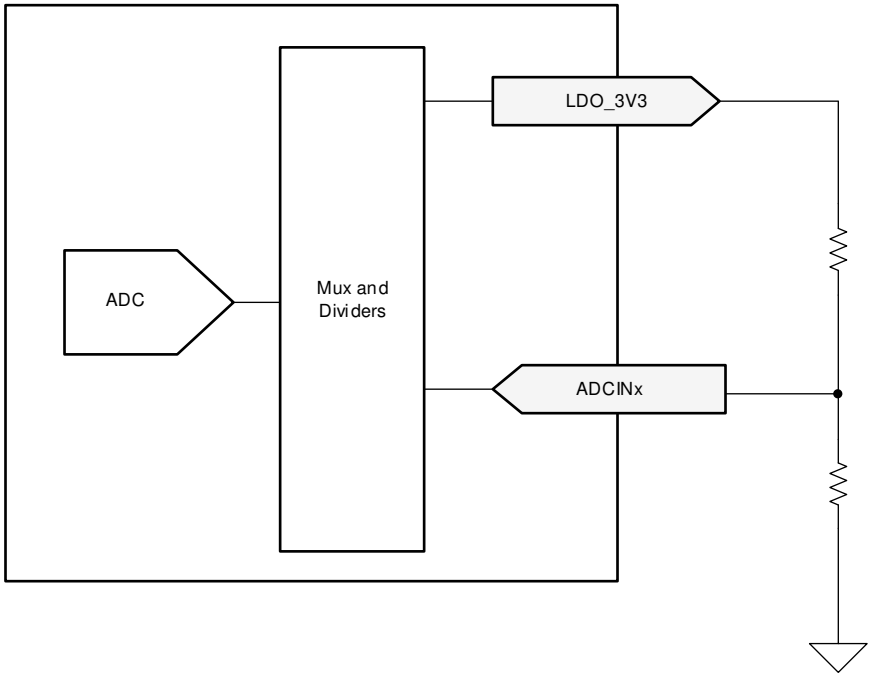


Figure 7-13. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See *Pin Strapping to Configure Default Behavior* for details on how the ADCINx configurations determine default device behavior. See *I²C Address Setting* for details on how ADCINx decoded values affects default I²C target address.

Table 7-2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without Using R_{UP} or R_{DOWN}	ADCINx Decoded Value(2)
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) See *I²C Address Setting* to see the exact meaning of I²C Address Index.
(2) See *Pin Strapping to Configure Default Behavior* for how to configure a given ADCINx decoded value.

7.3.7 ADC

The TPS26750 ADC is shown in Figure 7-14. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

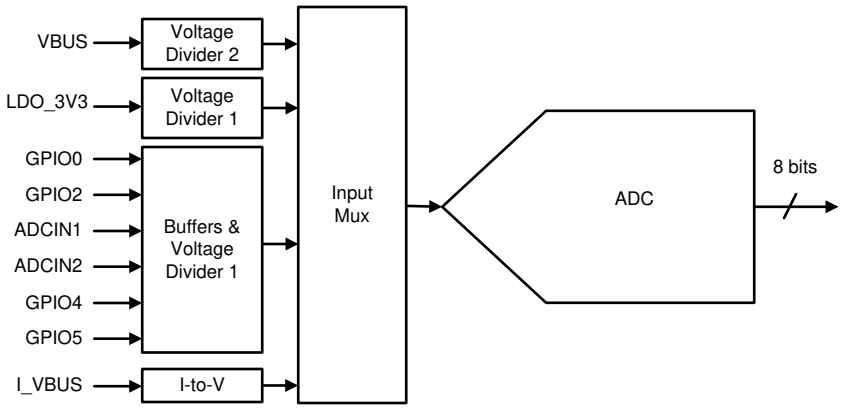


Figure 7-14. SAR ADC

7.3.8 BC 1.2 (USB_P, USB_N)

The TPS26750 supports BC 1.2 as a Portable Device or Downstream Port using the hardware shown in Figure 7-15.

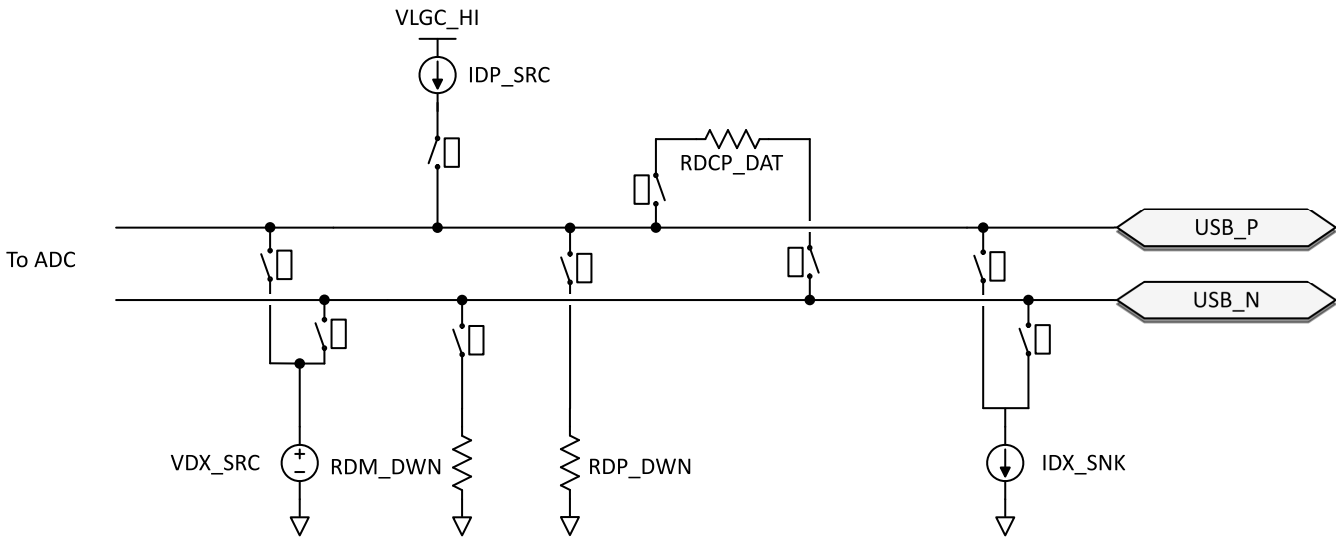


Figure 7-15. BC1.2 Hardware Components

7.3.9 Digital Interfaces

The TPS26750 contains several different digital interfaces which can be used for communicating with other devices. The available interfaces include one I^2C controller, one I2C target and additional GPIOs.

7.3.9.1 General GPIO

GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input . The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V5 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer can be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

Table 7-3. GPIO Functionality Table

PIN NAME	TYPE	SPECIAL FUNCTIONALITY
GPIO0	I/O	General-purpose input or output
GPIO1	I/O	General-purpose input or output
GPIO2	I/O	General-purpose input or output
GPIO3	I/O	General-purpose input or output
GPIO4	I/O	D+, general-purpose input or output, or LD1 for Liquid Detection
GPIO5	I/O	D-, general-purpose input or output, or LD2 for Liquid Detection
GPIO6	I/O	General-purpose input or output
GPIO7	I/O	General-purpose input or output
$\overline{\text{I2Ct\_IRQ}}$(GPIO10)	O	IRQ for optional I2Ct, or used as a general-purpose output
GPIO11	O	General-purpose output
$\overline{\text{I2Cc\_IRQ}}$(GPIO12)	I	IRQ for I2Cc, or used as a general-purpose input

7.3.9.2 I^2C Interface

The TPS26750 features two I^2C interfaces that uses an I^2C I/O driver like the one shown in Figure 7-16. This I/O consists of an open-drain output and an input comparator with de-glitching.

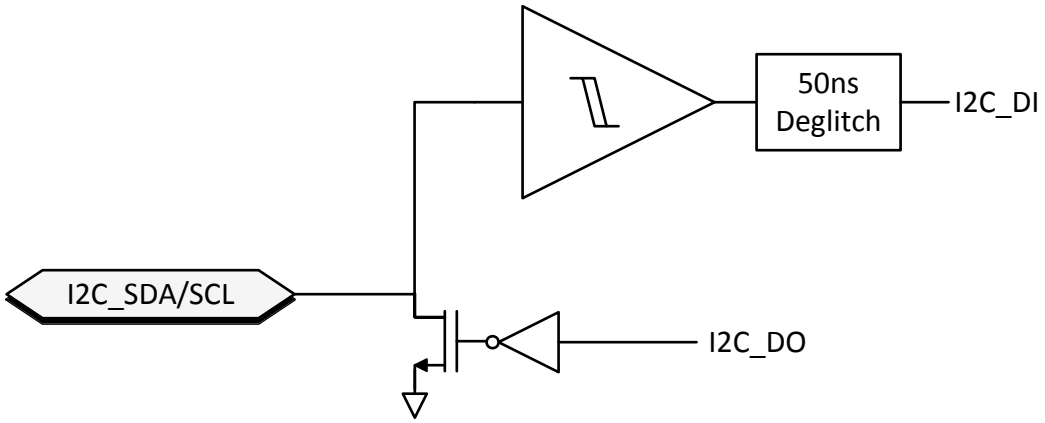


Figure 7-16. I²C Buffer

7.3.10 Digital Core

Figure 7-17 shows a simplified block diagram of the digital core.

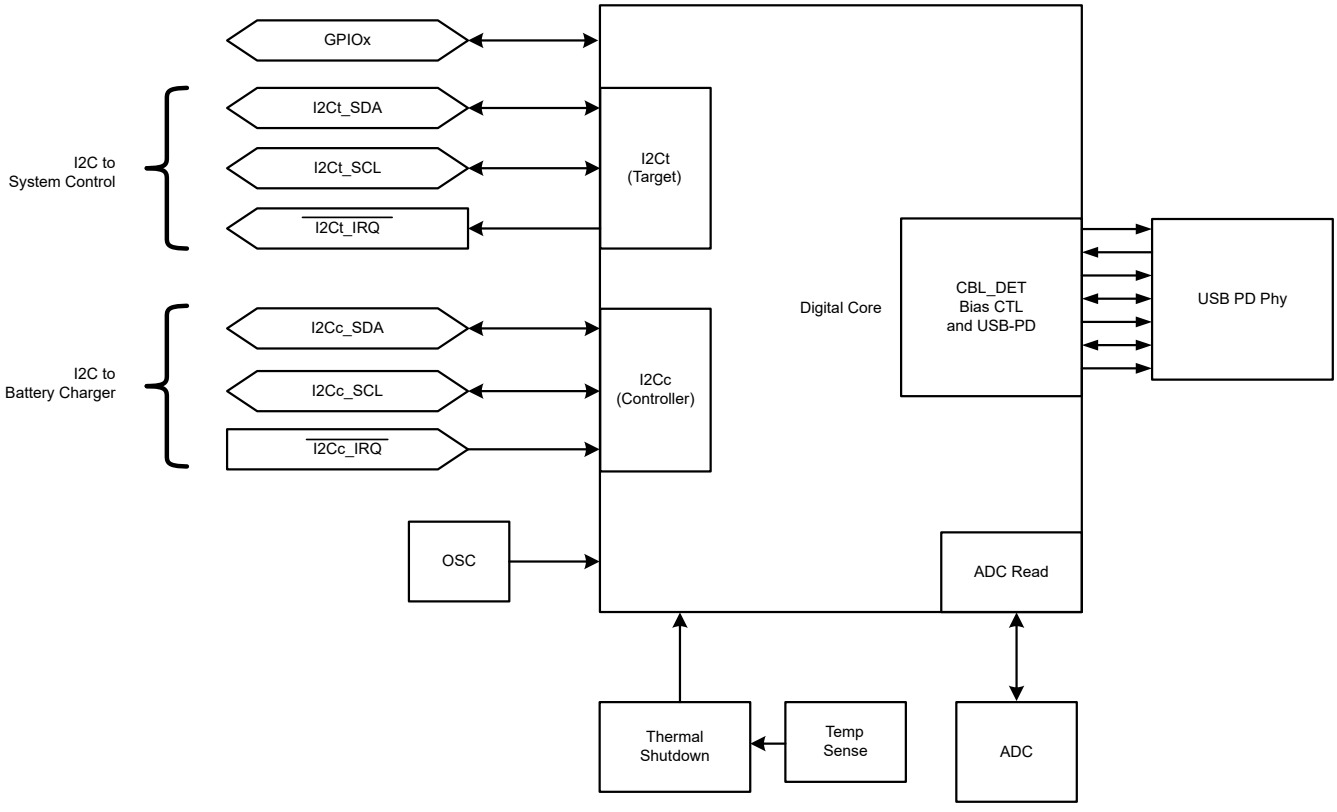


Figure 7-17. Digital Core Block Diagram

7.3.11 I²C Interface

The TPS26750 has one I2C target interface ports: I2Ct. I2C port I2Ct is comprised of the I2Ct_SDA, I2Ct_SCL, and $\overline{\text{I2Ct\_IRQ}}$ pins. This interface provide general status information about the TPS26750, as well as the ability to control the TPS26750 behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS26750 is in 'APP ' mode TI recommends to use standard mode or Fast mode (that is a clock speed no higher than 400 kHz). However, in the BOOT mode when a patch bundle is loaded Fast Mode Plus can be used (see fSCLS).

The TPS26750 has one I²C controller interface port. I²C is comprised of the I2C_SDA and I2C_SCL pins. This interface can be used to read from or write to external target devices.

During boot, the TPS26750 attempts to read patch and Application Configuration data from an external EEPROM with a 7-bit target address of 0x50. The EEPROM must be at least 36 kilo-bytes.

Table 7-4. I²C Summary

I²C BUS	TYPE	TYPICAL USAGE
I2Ct	Target	Optionally can be connected to an external MCU. Also used to load the patch and application configuration.
I2Cc	Controller	Connect to a I²C EEPROM, Battery Charger. Use the LDO_3V3 pin as the pullup voltage. Multi-controller configuration is not supported.

7.3.11.1 I²C Interface Description

The TPS26750 supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer can be initiated only when the bus is not busy.

A controller sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

Figure 7-18 shows the start and stop conditions of the transfer. Figure 7-19 shows the SDA and SCL signals for transferring a bit. Figure 7-20 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

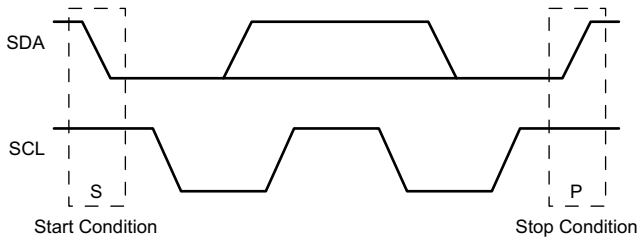


Figure 7-18. I²C Definition of Start and Stop Conditions

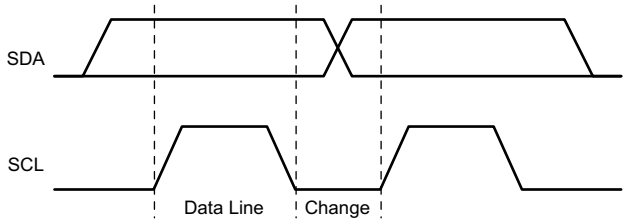


Figure 7-19. I²C Bit Transfer

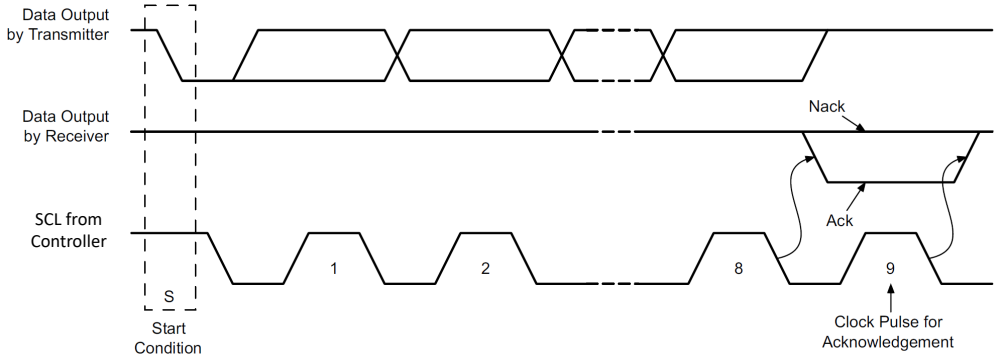


Figure 7-20. I²C Acknowledgment

7.3.11.1.1 I²C Clock Stretching

The TPS26750 features clock stretching for the I²C protocol. The TPS26750 target I²C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

The controller must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse can be stretched but typically it is the interval before or after the acknowledgment bit.

7.3.11.1.2 I²C Address Setting

The I2C controller must only use I2Ct_SCL/SDA for loading a patch bundle.

Once the boot process is complete, the port has a unique target address on the I2Ct_SCL/SDA bus as selected by the ADCINx pins.

Table 7-5. I²C Default Target Address for I2Ct_SCL/SDA.

I²C ADDRESS INDEX (DECODED FROM ADCIN1 AND ADCIN2)(1)	TARGET ADDRESS								AVAILABLE DURING BOOT
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
#1	0	1	0	0	0	0	0	R/W	Yes
#2	0	1	0	0	0	0	1	R/W	Yes
#3	0	1	0	0	0	1	0	R/W	Yes
#4	0	1	0	0	0	1	1	R/W	Yes

(1) See *Pin Strapping to Configure Default Behavior* details about ADCIN1 and ADCIN2 decoding.

7.3.11.1.3 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C controller and a single TPS26750. The I²C target sub-address is used to receive or respond to Host Interface protocol commands. Figure 7-21 and Figure 7-22 show the write and read protocol for the I²C target interface, and a key is included in Figure 7-23 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

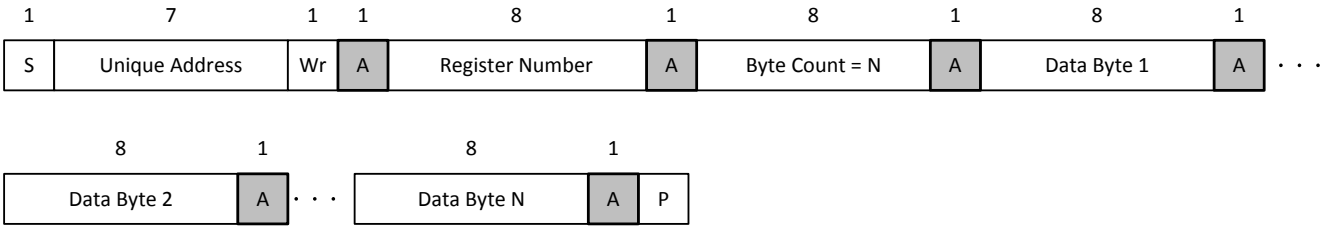


Figure 7-21. I²C Unique Address Write Register Protocol

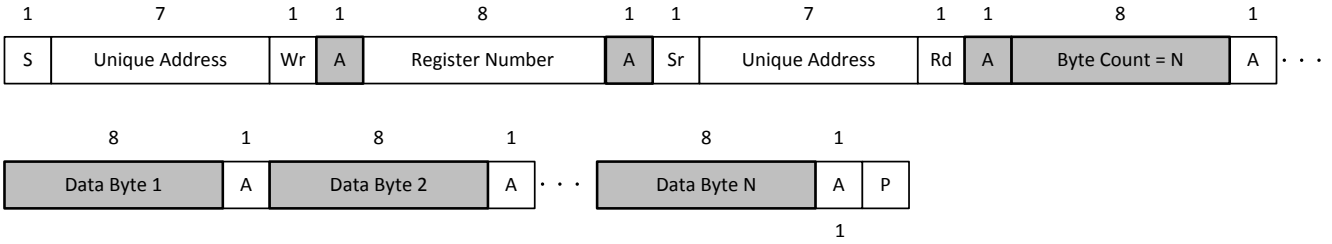
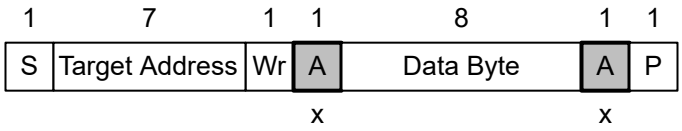


Figure 7-22. I²C Unique Address Read Register Protocol



S Start condition
SR Repeated start condition
Rd Read (bit value of 1)
Wr Write (bit value of 0
X Field is required to have the value x
A Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)
P Stop condition

Controller-to-target

Target-to-controller

Continuation of protocol

Figure 7-23. I²C Read/Write Protocol Key

7.4 Device Functional Modes

7.4.1 Pin Strapping to Configure Default Behavior

During the boot procedure, the device reads the ADCINx pins and set the configurations based on the table below. The device then attempts to load a configuration from an external EEPROM on the I2Cc bus. If no EEPROM is detected, then the device waits for an external host to load a configuration.

When an external EEPROM is used, each device is connected to a unique EEPROM, and cannot be shared for multiple devices. The external EEPROM is set at 7-bit target address 0x50.

Table 7-6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 DECODED VALUE(2)	ADCIN2 DECODED VALUE(2)	I²C ADDRESS INDEX(1)	DEAD BATTERY CONFIGURATION
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded. This configuration is used with an external embedded controller. The embedded controller manages the battery charger in the system when present.
5	5	#2	
2	0	#3	
1	7	#4	
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller enters the 'APP ' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V. The configuration cannot be used when a patch is loaded from EEPROM. This option is not recommended for systems that can boot from 5 V. This configuration is not valid to use with any supported battery chargers.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration can put the device into a source-only mode. This is recommended when the application loads the patch from EEPROM. This configuration is recommended when the PD controller manages the battery charger when present.
0	0	#2	
6	0	#3	
5	7	#4	

(1) See Table 7-5 to see the exact meaning of I²C Address Index.
(2) See Table 7-2 for how to configure a given ADCINx decoded value.

7.4.2 Power States

The TPS26750 can operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in Table 7-7. The device automatically transitions between the three power states based on the circuits that are active and required. See Figure 7-24. In the Sleep state, the TPS26750 detects a Type-C connection. Transitioning between the Active mode to Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I²C transactions
- Voltage alert
- Fault alert

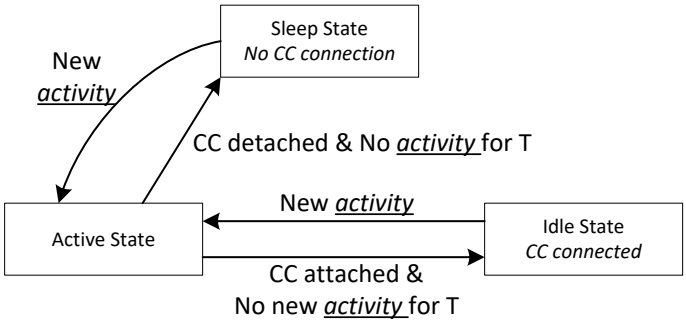


Figure 7-24. Flow Diagram for Power States

Table 7-7. Power Consumption States

	ACTIVE SOURCE MODE(1)	ACTIVE SINK MODE5	IDLE SOURCE MODE	IDLE SINK MODE	MODERN STANDBY SOURCE MODE3	MODERN STANDBY SINK MODE4	SLEEP MODE2
PP_5V	enabled	disabled	enabled	disabled	enabled	disabled	disabled

Table 7-7. Power Consumption States (continued)

	ACTIVE SOURCE MODE(1)	ACTIVE SINK MODE[5]	IDLE SOURCE MODE	IDLE SINK MODE	MODERN STANDBY SOURCE MODE[3]	MODERN STANDBY SINK MODE[4]	SLEEP MODE[2]
PP_CABLE	enabled	enabled	enabled	enabled	disabled	disabled	disabled
external CC1 termination	Rd	Rp 3.0A	Rd	Rp 3.0A	open	open	open
external CC2 termination	open	open	open	open	open	open	open

(1) This mode is used for: $I_{VIN\_3V3,ActSrc}$.
(2) This mode is used for: $I_{VIN\_3V3,Sleep}$
(3) This mode is used for: $P_{MstbySrc}$
(4) This mode is used for: $P_{MstbySnk}$
(5) This mode is used for: $I_{VIN\_3V3,ActSnk}$

7.5 Thermal Shutdown

The TPS26750 features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds T_{SD_PP5V}. Once the temperature falls by at least T_{SDH_PP5V}, the path can be configured to resume operation or remain disabled until re-enabled by firmware.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS26750 is a stand-alone Type-C PD controller for power-only USB-PD applications. Initial device configuration is configured from an external EEPROM through a firmware configuration bundle loaded on to the device during boot. The bundle is loaded over I^2C from an external EEPROM. The TPS26750 firmware configuration can be customized for each specific application. The firmware configuration can be generated through the Web Tool.

The TPS26750 is ideal for single port power applications supporting the following PD architectures.

- Designs for both Power Provider (Source) and Power Consumer (Sink)
- Designs for Power Consumer (Sink)

An external EEPROM is required to download a pre-configured firmware on the TPS26750 device through the I^2C interface.

The TPS26750 firmware can be configured using the Web Tool for the application-specific PD charging architecture requirements and data roles. The tool also provides additional optional firmware configuration that integrates control for select Battery Charger Products (BQ). The TPS26750 I^2C controller interfaces with the Battery Chargers with pre-configured GPIO settings and I^2C controller events. The Application Customization Tool available with the TPS26750 provides details of the supported Battery Charger Products (BQ).

8.2 Typical Application

The following show the block diagrams for various applications. Note that some of these features are GPIO usage dependent.

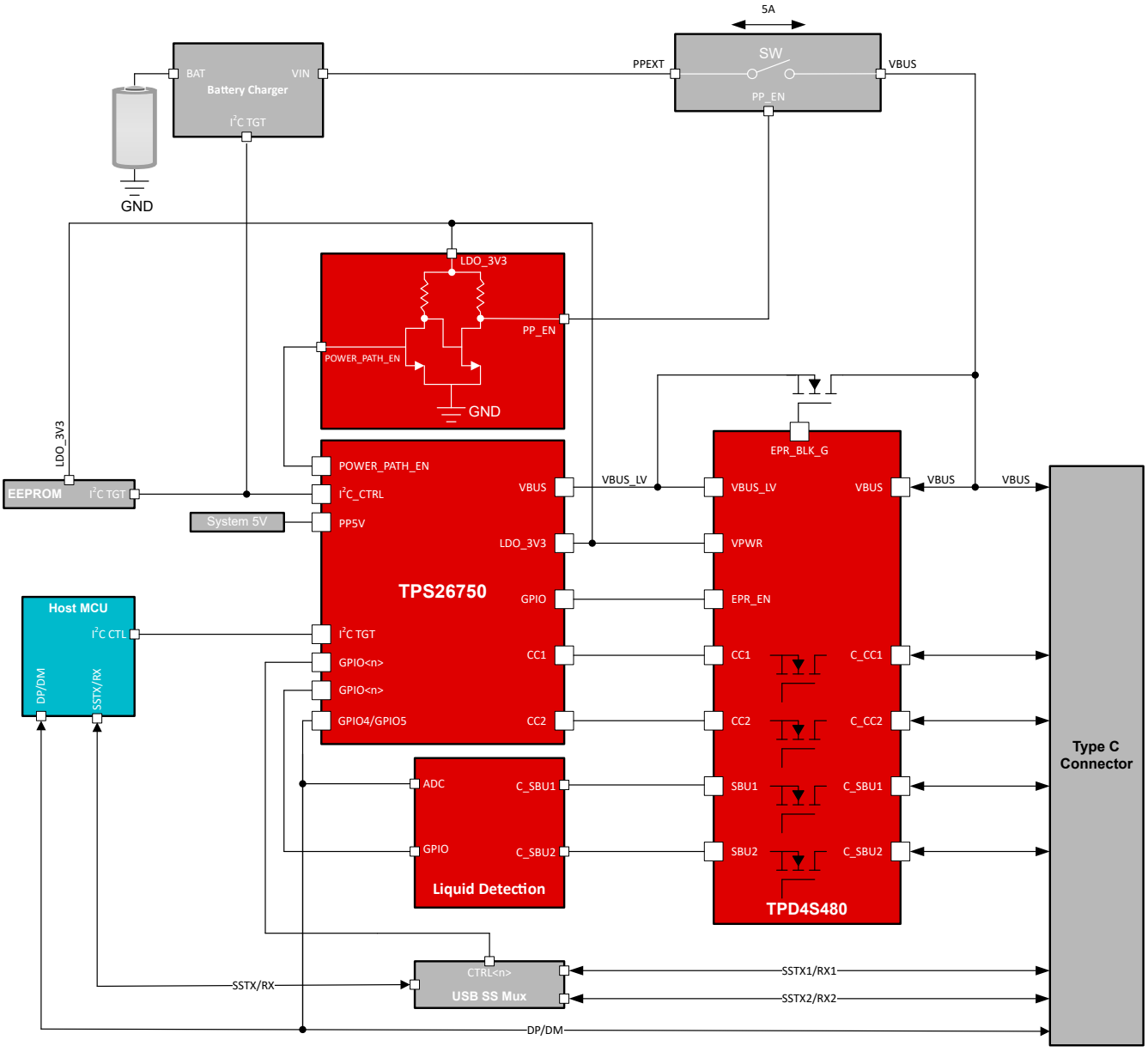


Figure 8-1. TPS26750 Battery Charger & Full System Block Diagram

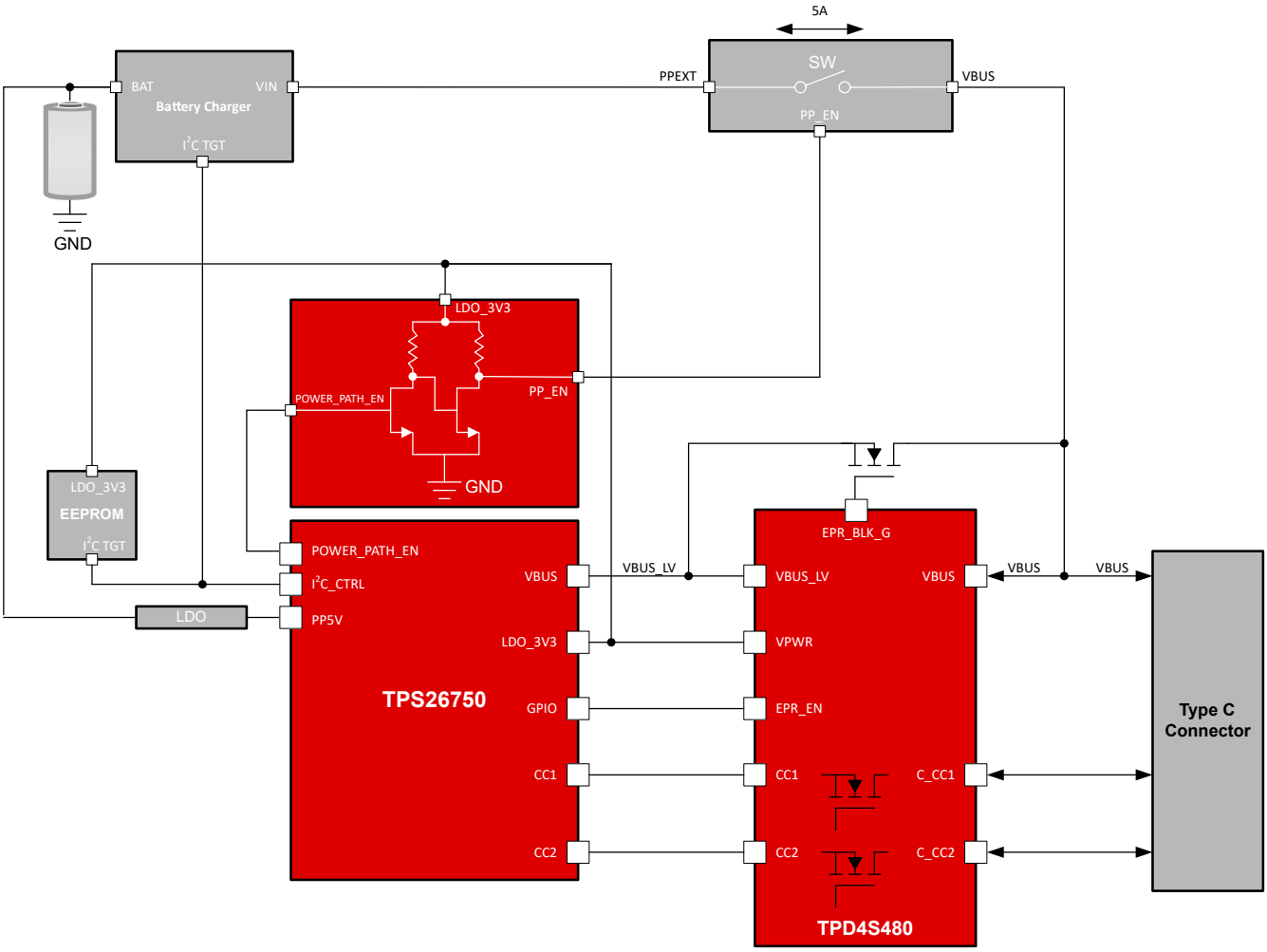


Figure 8-2. TPS26750 Battery Charger System Block Diagram

8.2.1 Design Requirements

8.2.1.1 Programmable Power Supply (PPS) - Design Requirements

Programmable Power Supply (PPS) defines a specific voltage and current (Augmented Power Data Object) that is used in direct charging applications. A PPS source needs to meet the source voltage and current resolution required for direct charging applications. A PPS sink requests the voltage and current required for direct charging within the capabilities of PPS source.

Table 8-1. PPS Source 60W/100W Requirements

Power Path	PD Power Source	VBUS Voltage	VBUS Current
TPS26750	60W/100W	5V - 21V (20mV Steps)	3A/5A (50mA Steps)

Table 8-2. PPS Sink 60W/100W Requirements

Power Path	PD Power Sink	VBUS Voltage	VBUS Current
TPS26750	60W/100W	5V - 21V	3A/5A

8.2.1.2 Liquid Detection Design Requirements

Portable Type-C and PD applications are subject to environments that wet the Type-C connector. Liquid on the Type-C connector leads to corrosion or system damage. Detecting liquid leverages the SBU1/2 pins on the Type-C connector to not interfere with USB2/3 operation or PD communication.

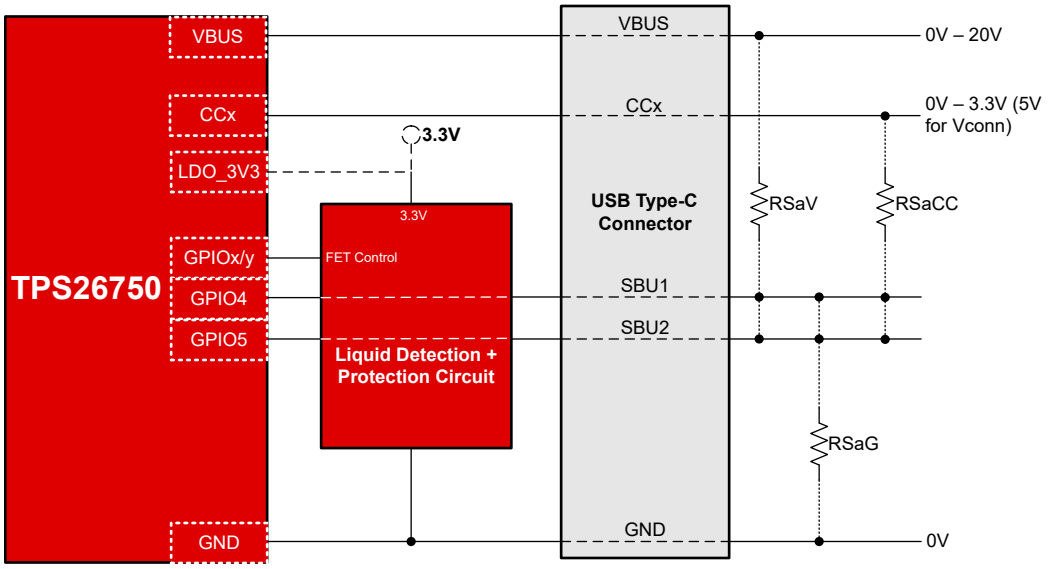


Figure 8-3. Liquid Detection Cases

8.2.1.3 BC1.2 Application Design Requirements

The PD controller taps the USB D+ and D- pins to provide BC1.2 detection and advertisement. The USB D+ and D- are connected to the USB Host (DFP) or USB Device (UFP) from the Type-C connector for Charging Data Port applications.

8.2.1.4 USB Data Support Design Requirements

For USB3 operation, the SSTX/RX are muxed to the Type-C connector. A SuperSpeed Mux generally has two control signals; enable and plug orientation. The PD controller determines when a connection is detected and drives the required GPIO to control the SuperSpeed Mux.

8.2.1.5 EPR Design Requirements

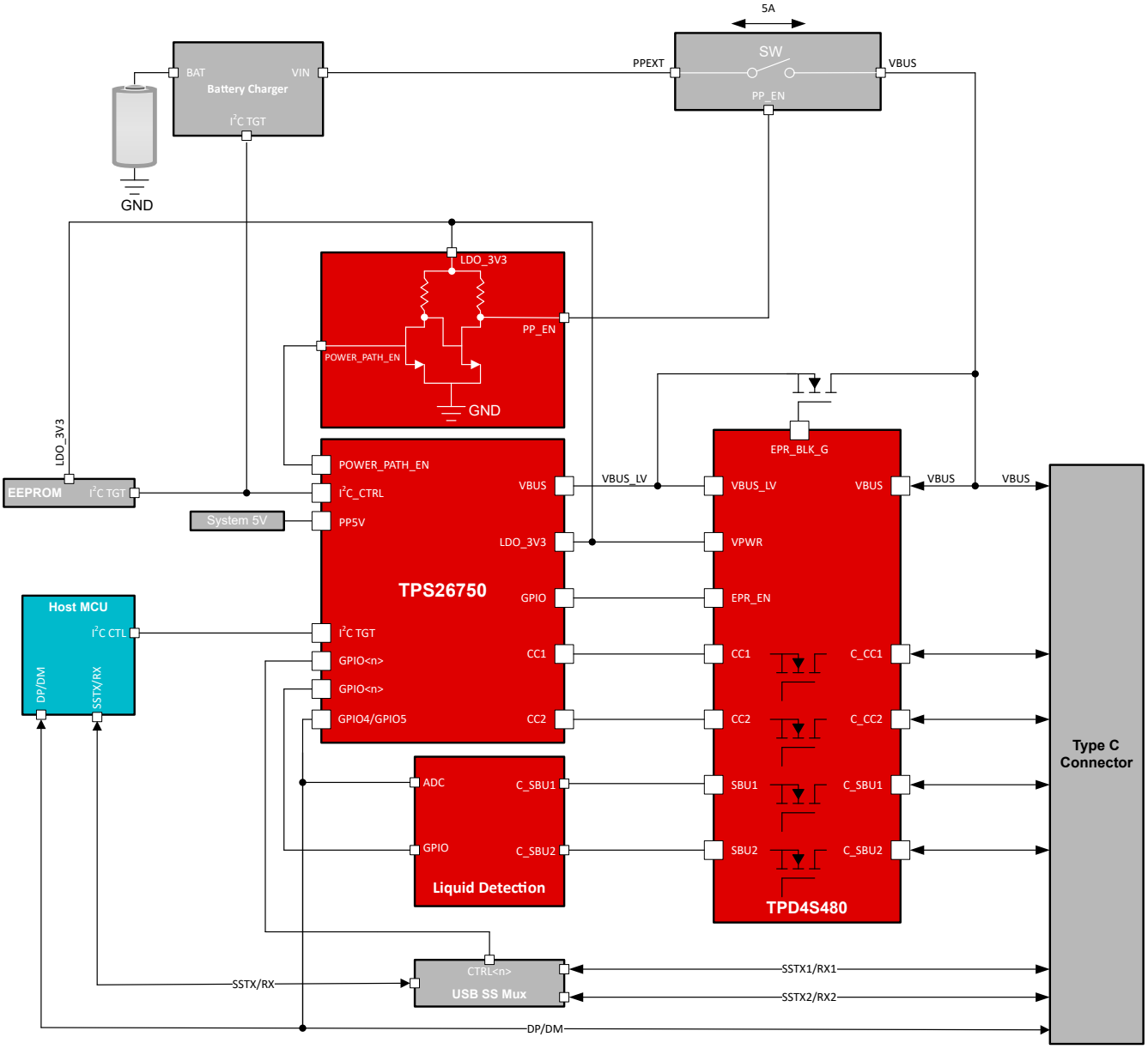


Figure 8-4. EPR Implemenation Diagram

The TPS26750 works in conjunction with the TPD4S480 to provide the following functionality in USB-PD EPR:

- Short to VBUS protection for direct shorts to CC1 and CC2 pins of the Type-C connector.
- Short to VBUS protection for the liquid detection circuitry that is connected to the SBU1 and SBU2 pins of the Type-C connector, if the liquid detection feature is implemented.
- Voltage level translation from up the EPR maximum voltage down to the operation range of the VBUS pins of the TPS26750.
- Gate Drive for a high voltage NMOS transitor to allow the internal 5V power path to be used to source 5V in systems that only require a 5V output.

The TPS26750 also provides an analog signal that is driven to 9V with a 10uA capable charge pump. This signal is buffered with 2 source followers to provide a level shifted signal to control an external power switch, as shown in the figure below.

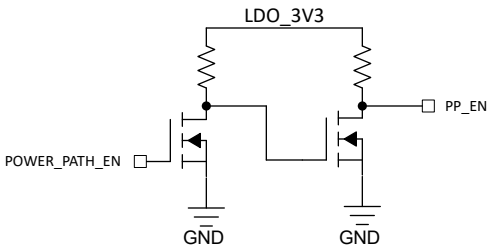


Figure 8-5. POWER_PATH_EN Buffer

8.2.2 Detailed Design Procedure

8.2.2.1 Programmable Power Supply (PPS)

The TPS26750 supports Programmable Power Supply (PPS) source and sink. When the TPS26750 negotiates a PPS contract as a source, the device enables the high-voltage power path (PPHV for D variant, PPEXT for S variant) and communicate with the supported TI battery charger (BQ25792 and BQ25756) to supply the negotiated voltage. TPS26750 only supports PPS within a 5V to 21V range according to PD 3.1 specification and is enabled through the Application Customization Tool.

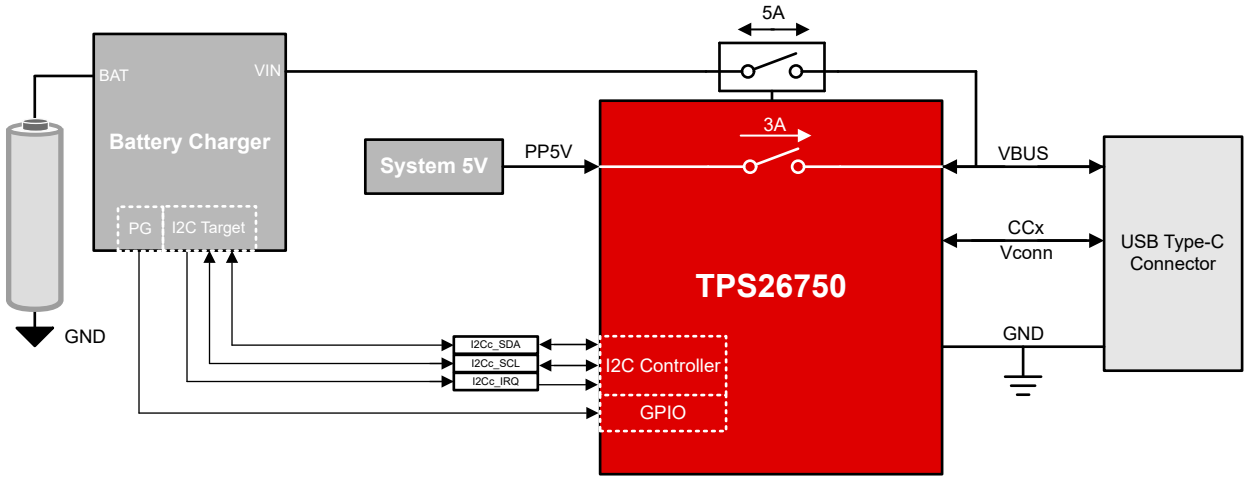


Figure 8-6. TPS26750 PPS with Battery Charger

8.2.2.2 Liquid Detection

The TPS26750 supports liquid detection using the built-in internal ADC and GPIO with external circuitry. Figure 8-7 and Figure 8-8 show the hardware implementation for liquid detection with the TPS26750. The TPD4S480 is used to protect the GPIO, ADC, and LDO_3V3 pins from over voltage conditions when there is liquid shorting VBUS to the SBU1/2 pins. shows the recommended components used to implement the external liquid detection circuitry. When liquid is detected, the TPS26750 takes action to protect the Type-C port. Systems using an embedded host controller can leverage the Host Interface for additional notification and control.

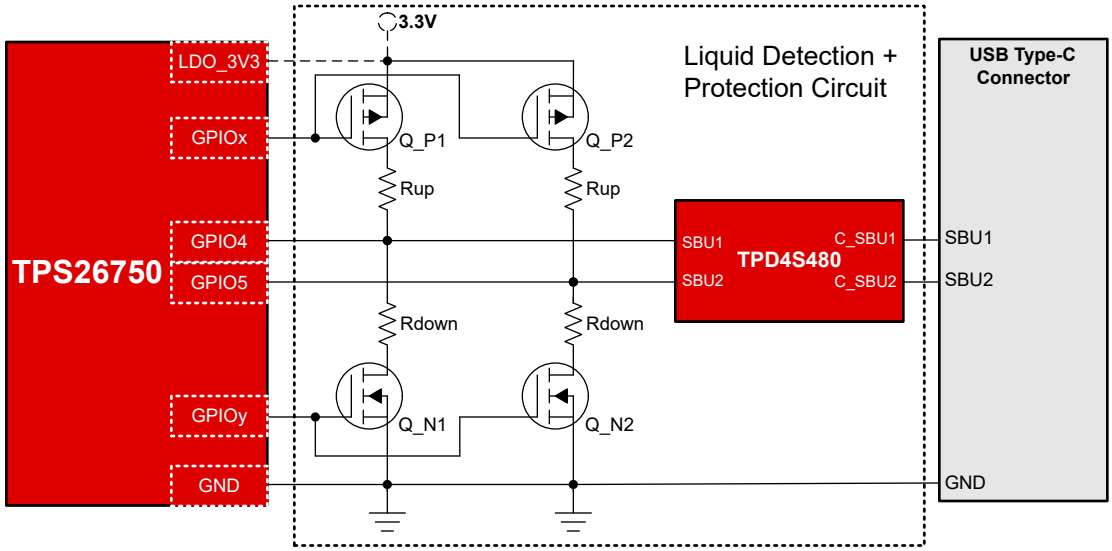


Figure 8-7. TPS26750 Liquid Detection Block Diagram - 2 GPIO Control

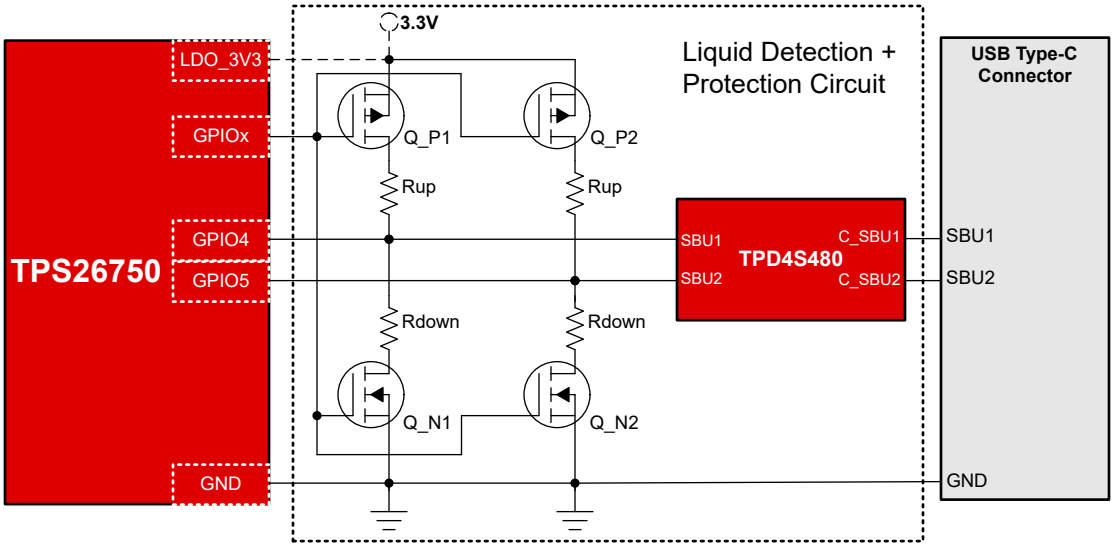


Figure 8-8. TPS26750 Liquid Detection Block Diagram - 1 GPIO Control

Table 8-3. Component Recommendation

Q_Pn (GPIO PMOS)	Q_Nn (GPIO NMOS)	Rup	Rdown
CSD25480F3 (Vgsth -0.95V or similar)	CSD15380F3 (Vgsth 1.1V or similar)	1MOhm (5%)	1MOhm (5%)

8.2.2.3 BC1.2 Application

The TPS26750 supports BC1.2 detection and advertisement modes and are configurable through the Web Tool.

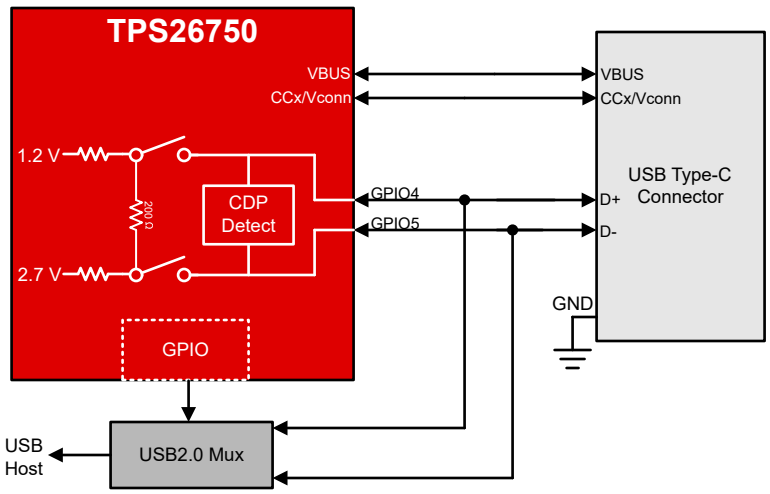


Figure 8-9. BC1.2 Application Block Diargam

8.2.2.4 USB Data Support

The TPS26750 supports USB data speed up to USB 3.2 Gen 2. When entering USB enumeration, the TPS26750 controls USB SuperSpeed Mux (TUSB1142) using GPIO controls. The GPIO control is configured through using the Application Customization Tool, GPIO events are found in the Technical Reference Manual.

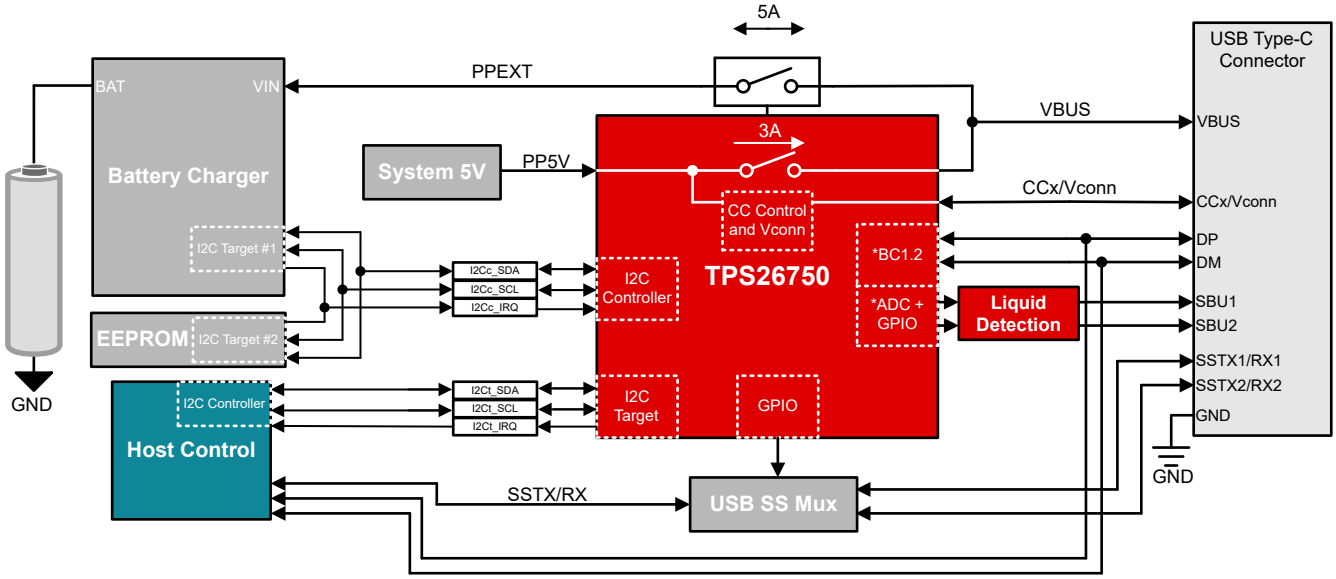


Figure 8-10. TPS26750 USB Data Support

8.2.2.5 Power Delivery EPR Support

In order to support EPR using the TPS26750, the following requirements must be met:

- Short to VBUS protection for CC1/CC2 for voltages up the the maximum EPR voltage of the design
- If Liquid Detection is implemented, then short to VBUS protection for SBU1/SBU2 for voltages up the the maximum EPR voltage of the design
- Voltage level translation from up the maximum EPR voltage down to the operation range of the VBUS pin of the TPS26750
- Level Translation/Buffering of the POWER_PATH_EN pin to implement power switch control

8.2.3 Application Curves

8.2.3.1 Programmable Power Supply (PPS) Application Curves

The following are captured when the TPS26750 is acting as a PPS Source. The VBUS plot shows the PPS negotiation increasing and decreasing from 5V to 21V to 5V. The PD negotaition snap shot shows the VBUS requested voltage increasing by 100mV.

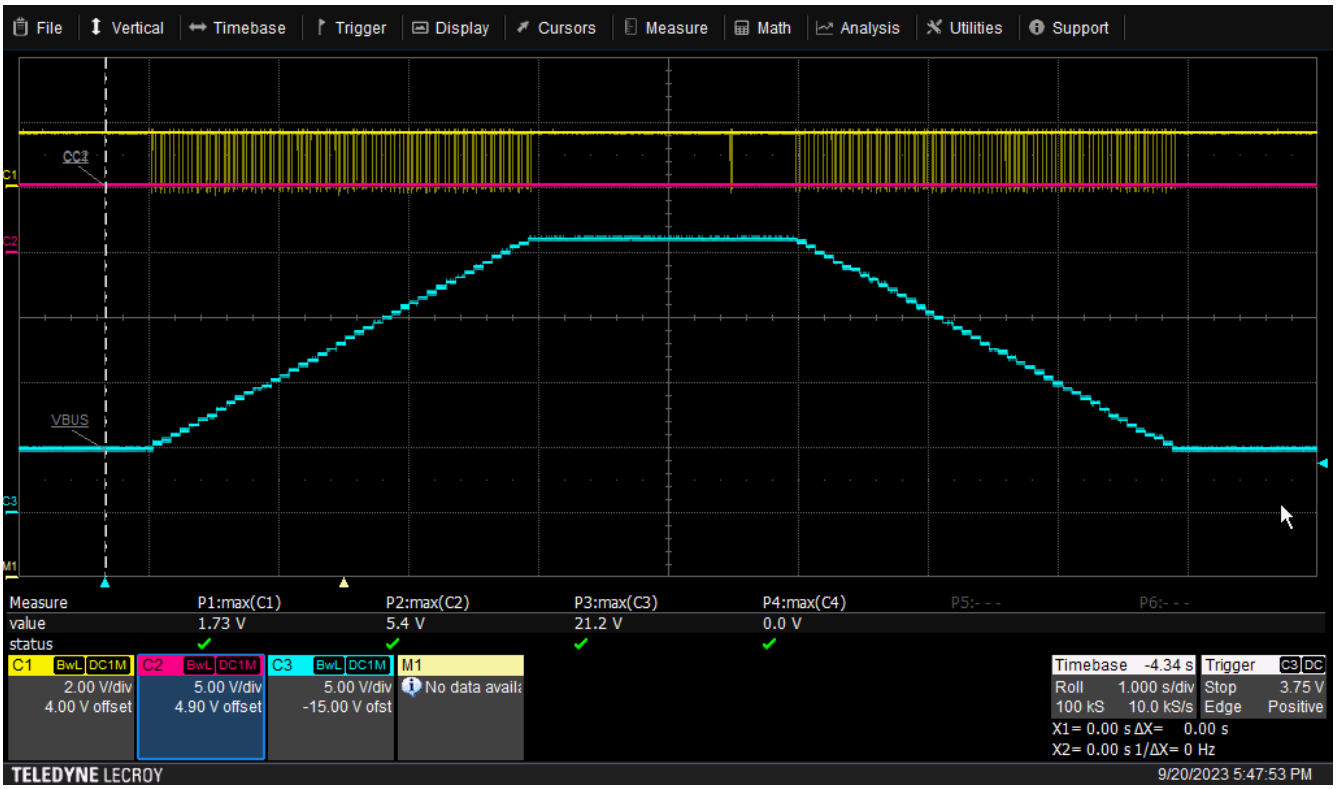


Figure 8-11. PPS PD Negotiation VBUS Increasing/Decreasing

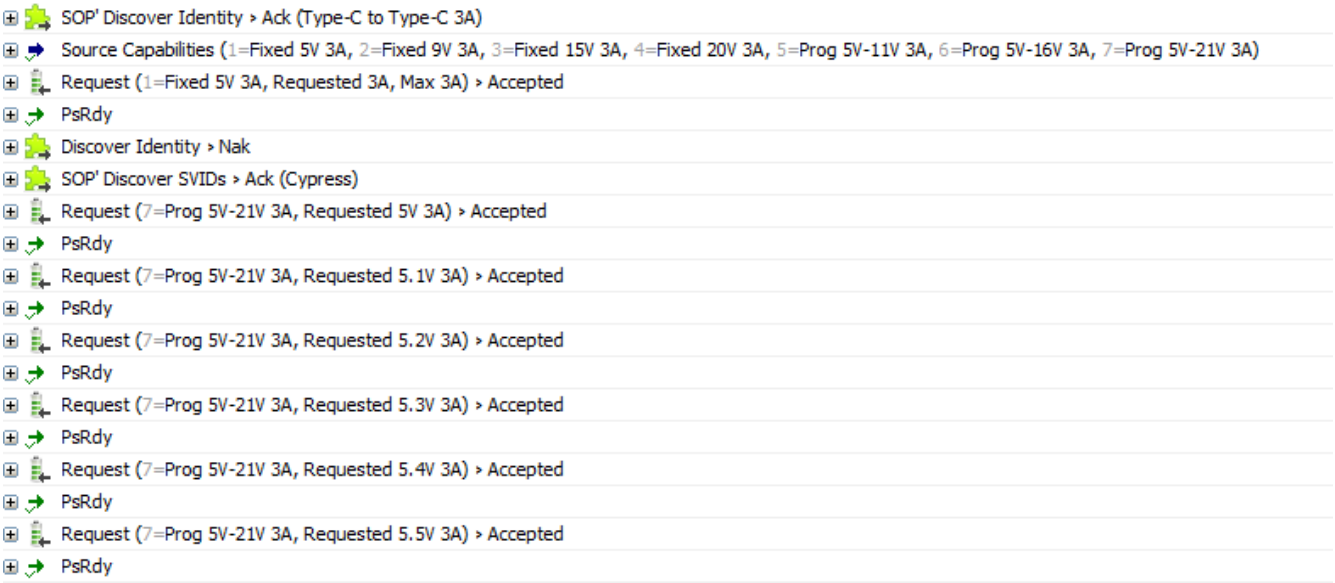


Figure 8-12. PPS PD Negotiation Log

8.2.3.2 Liquid Detection Application Curves

The figures below show the liquid detection behavior with corrosion mitigation disabled and enabled. Liquid is detected on both Liquid Detection Behavior - No Corrosion Mitigation and Liquid Detection Behavior - Corrosion Mitigation on the SBU2 pin.

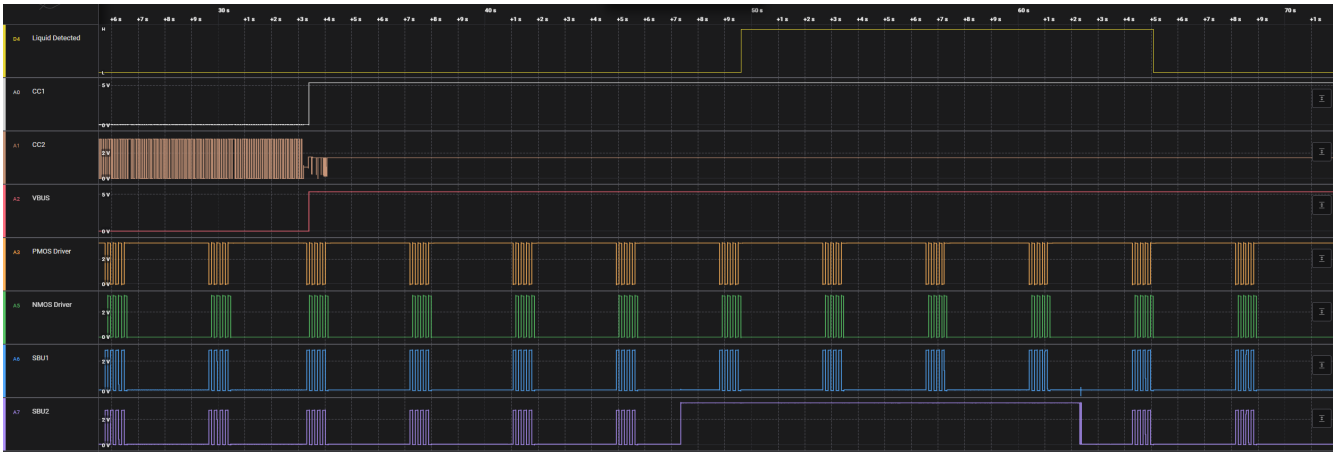


Figure 8-13. Liquid Detection Behavior - No Corrosion Mitigation

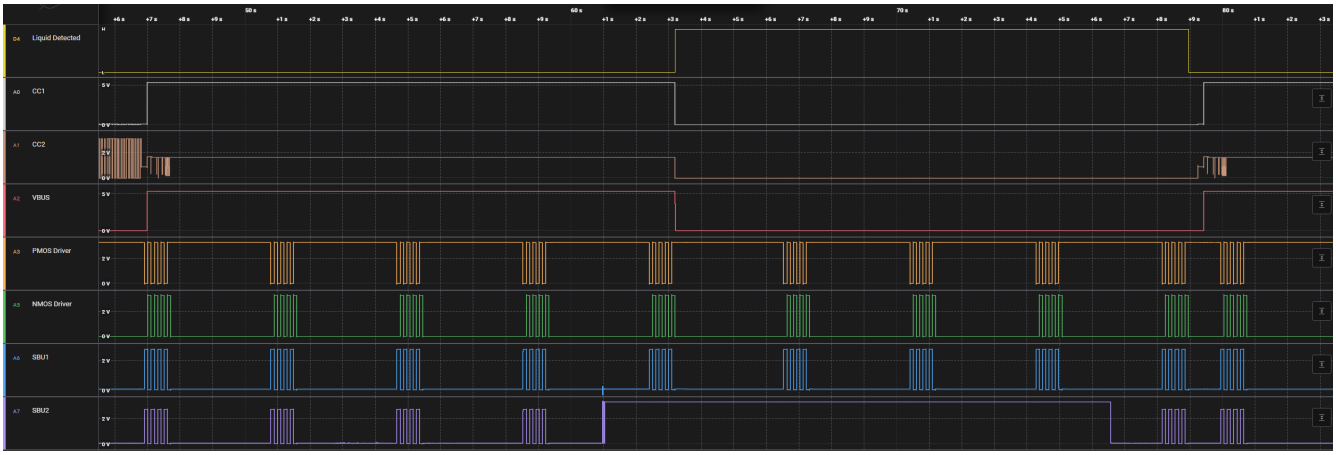


Figure 8-14. Liquid Detection Behavior - Corrosion Mitigation

Liquid Detection occurs in burst which can be configured. When the PD Controller checks for liquid it toggles the SBU1/2 circuitry, and pulls down the SBU1/2 circuitry when liquid detection is disabled.

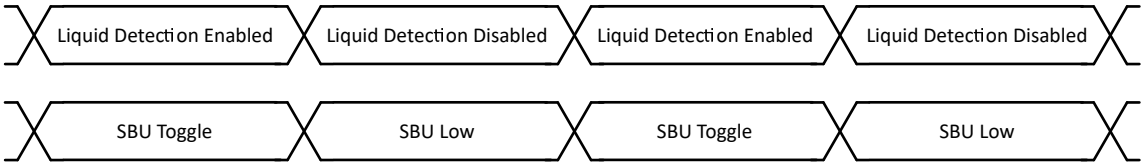


Figure 8-15. Liquid Detection and SBU1/2 Toggle

8.2.3.3 BC1.2 Application Curves

The plots below show the BC1.2 advertisement and detection with the TPS26750.

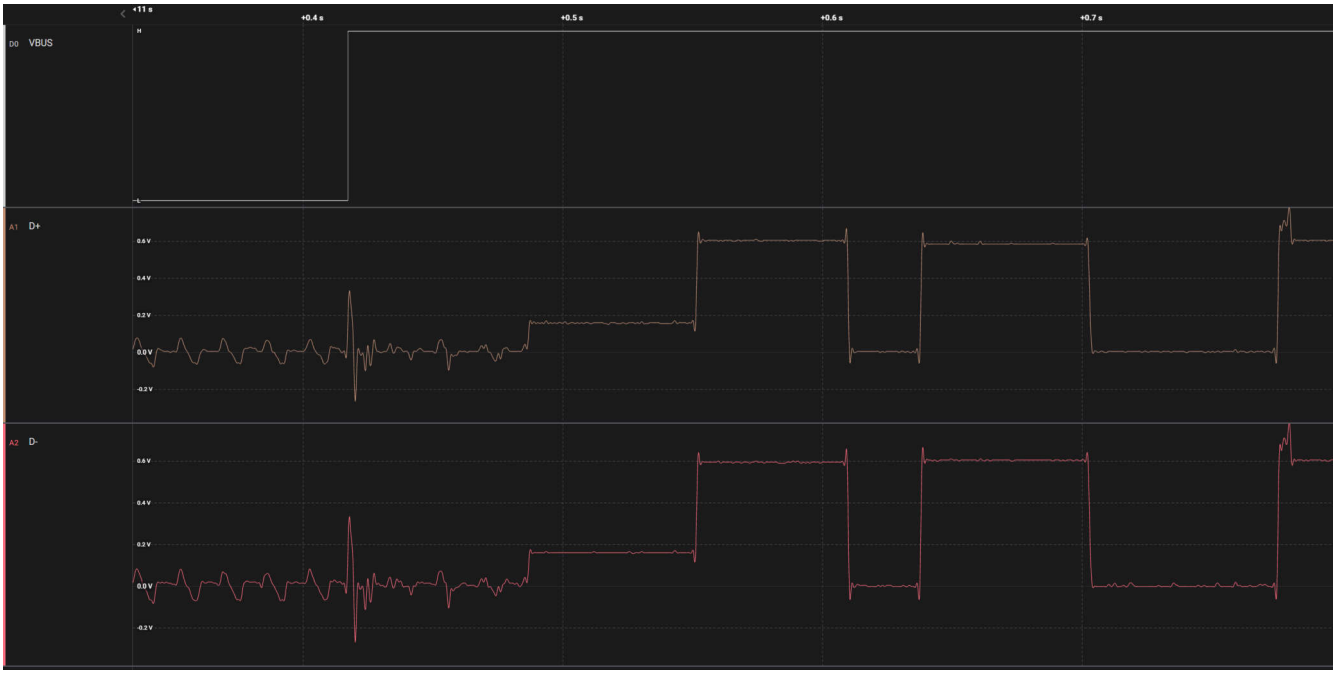


Figure 8-16. BC1.2 DCP Advertisement

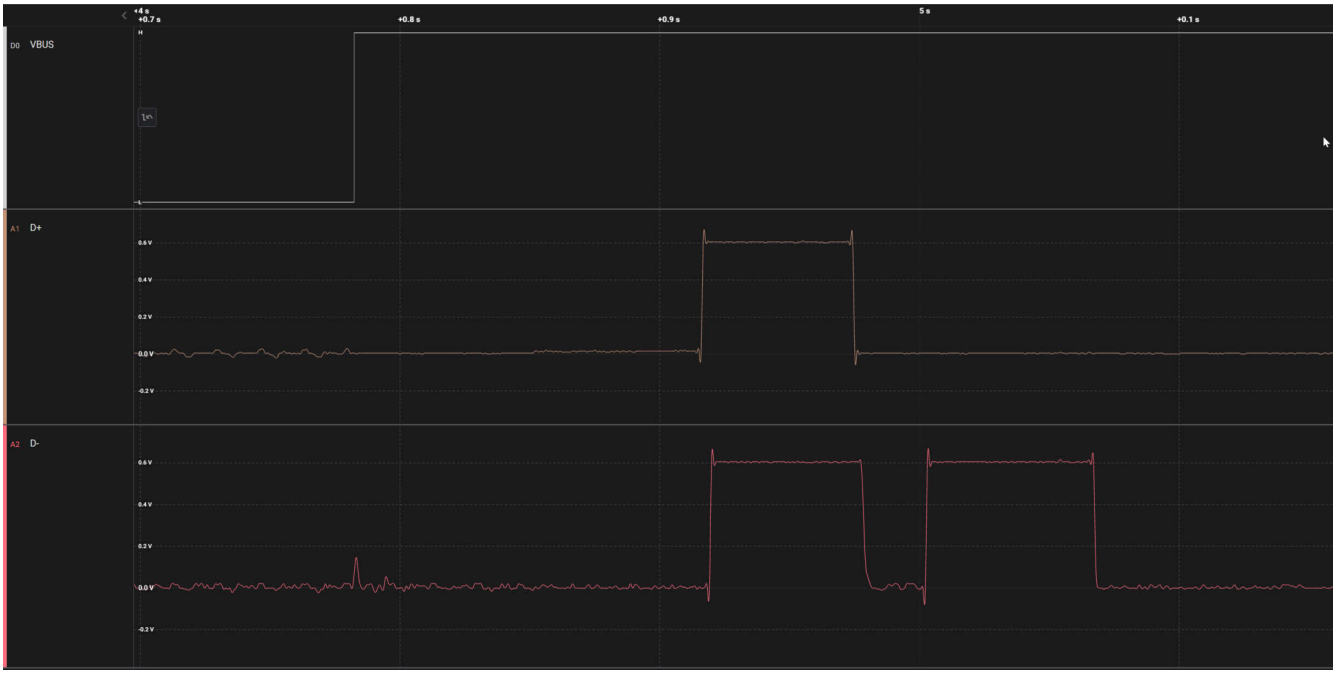


Figure 8-17. BC1.2 CDP Advertisement

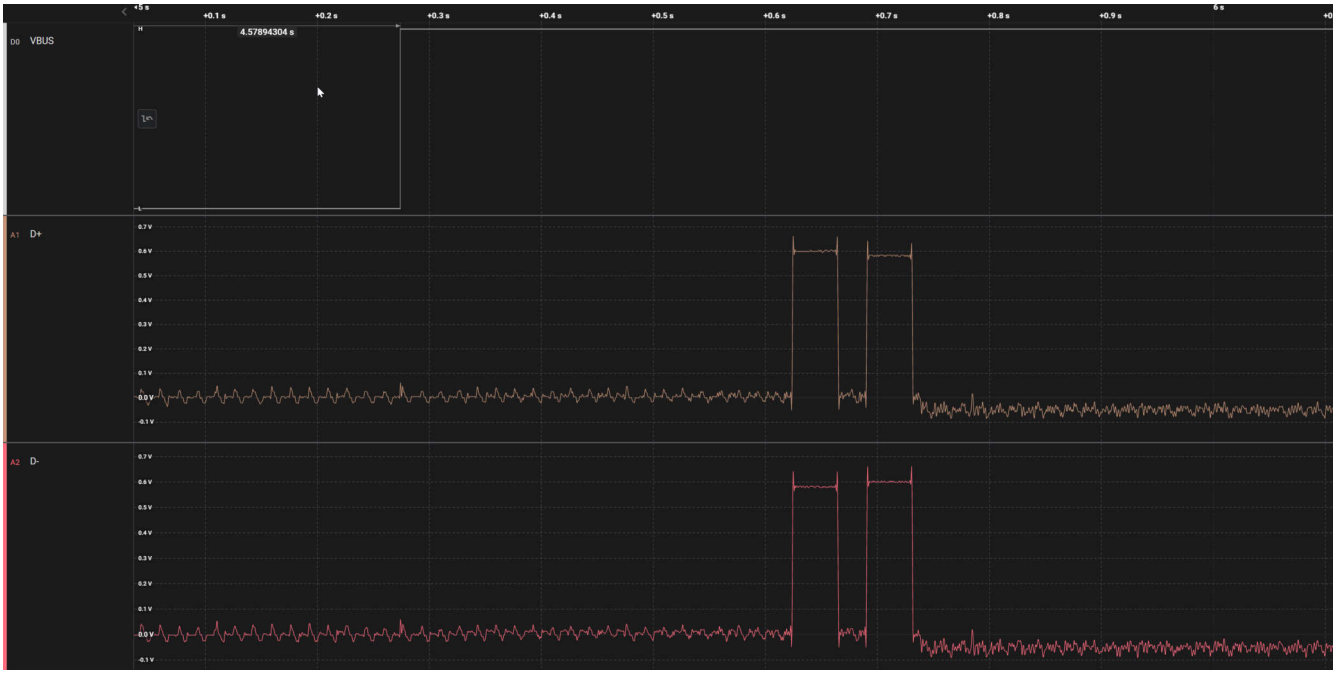


Figure 8-18. BC1.2 DCP Detection

Figure 8-19. BC1.2 CDP Detection

8.2.3.4 USB Data Support Application Curves

The following show the control signals used by a USB SuperSpeed Mux. For a normal orientation, the CC1 pin is connected. For a flipped orientation, the CC2 pin is connected.

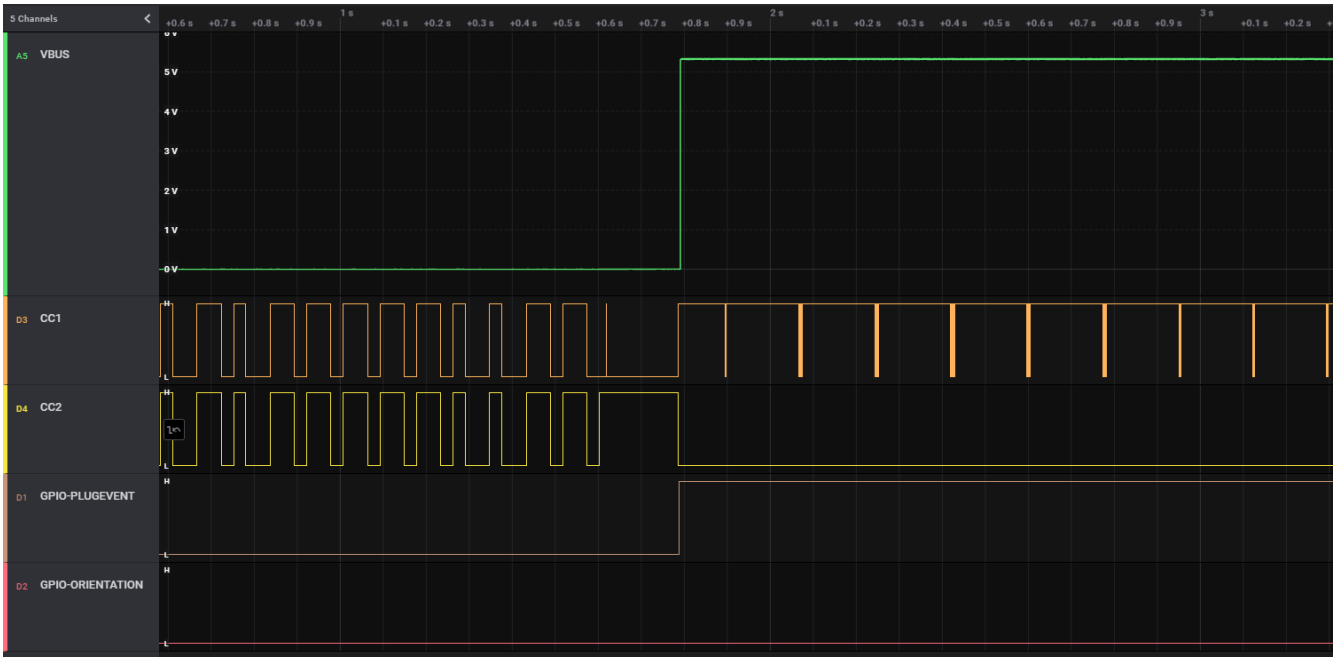


Figure 8-20. USB SuperSpeed Mux Control - Normal Orientation

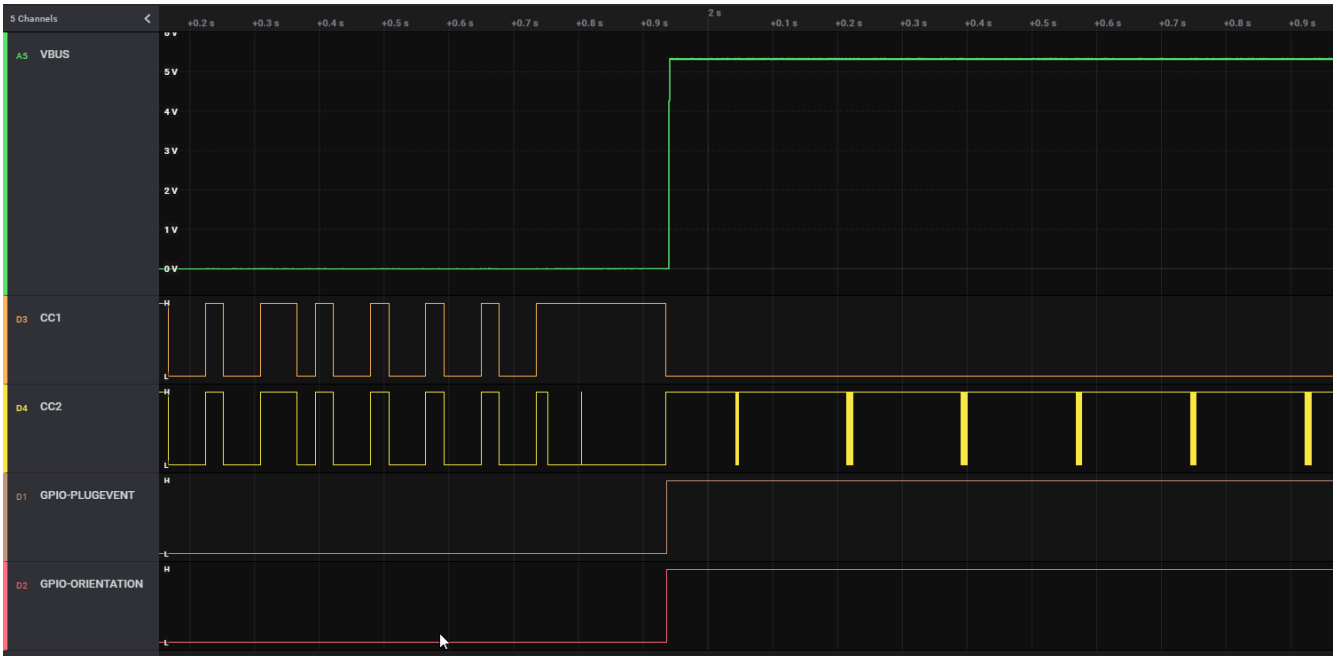


Figure 8-21. USB SuperSpeed Mux Control - Flipped Orientation

8.2.3.5 EPR Application Curves

The following show the PD connection communication required to establish and maintain a 48V EPR contract.

Table 8-4. 48V EPR Sink Contract with Keep Alive Shown PD Log

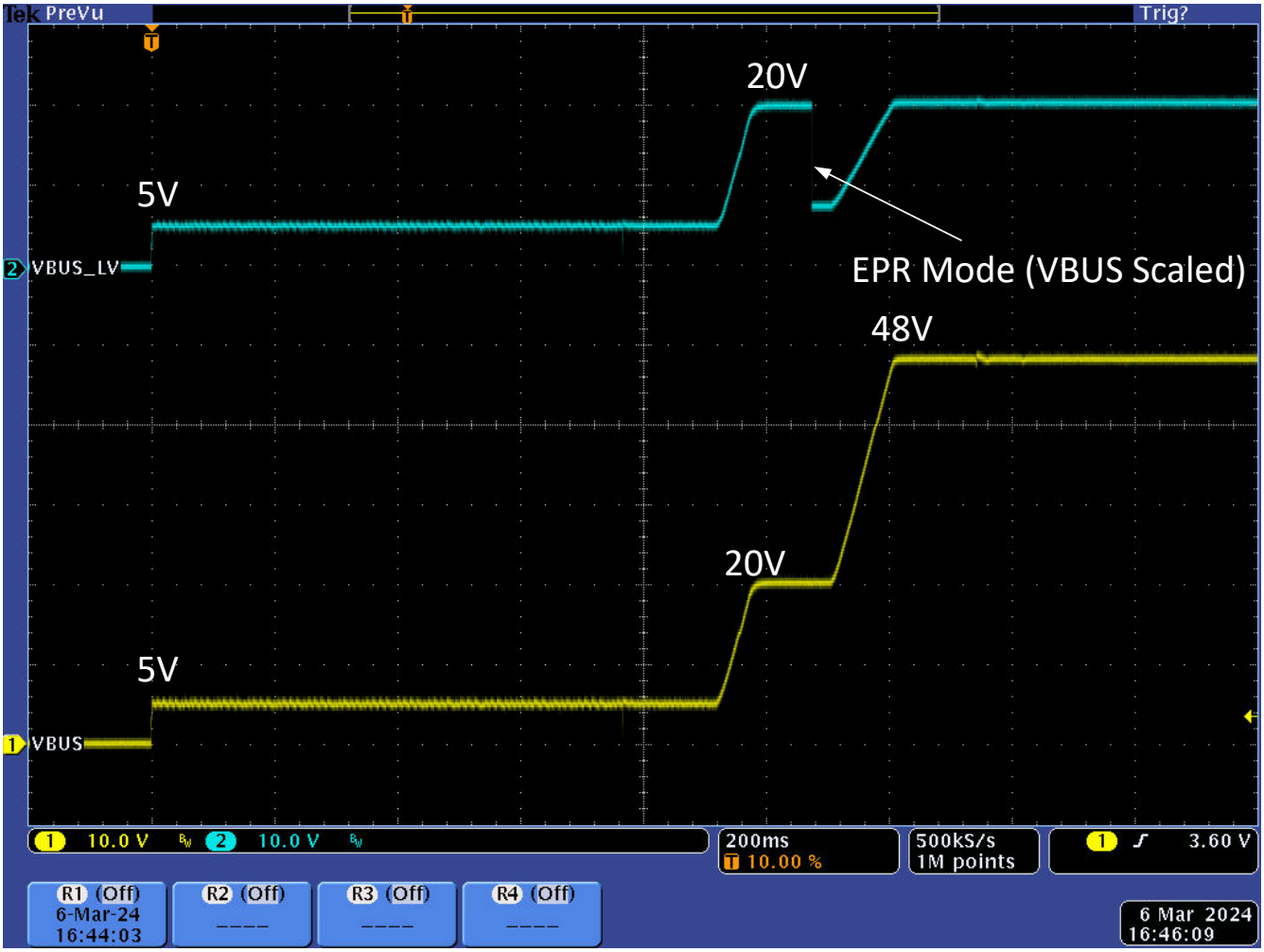
#	Message Type	SOP*	Data Role	Power Role	MsgID	Sender	Time Stamp
0	CONNECT CC1 (CC1-Pin = TYPEC_3p0A, CC2-Pin = NC)						06:20.9

Table 8-4. 48V EPR Sink Contract with Keep Alive Shown PD Log (continued)

#	Message Type	SOP*	Data Role	Power Role	MsgID	Sender	Time Stamp
1	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	0	Port	06:21.1
2	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	0	Port	06:21.1
3	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	0	Port	06:21.1
4	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	1	Port	06:21.2
5	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	1	Port	06:21.2
6	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	1	Port	06:21.2
7	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	2	Port	06:21.4
8	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	2	Port	06:21.4
9	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	2	Port	06:21.4
10	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	3	Port	06:21.6
11	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	3	Port	06:21.6
12	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	3	Port	06:21.6
13	Source_Capabilities (Max: 100W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A)	SOP	DFP	SOURCE	4	Port	06:21.8
14	GoodCRC	SOP	UFP	SINK	4	Port	06:21.8
15	Request (ObjPos=4, Fixed 20V-5A)	SOP	UFP	SINK	0	Port	06:21.8
16	GoodCRC	SOP	DFP	SOURCE	0	Port	06:21.8
17	Accept	SOP	DFP	SOURCE	5	Port	06:21.8
18	GoodCRC	SOP	UFP	SINK	5	Port	06:21.8
19	PS_RDY	SOP	DFP	SOURCE	6	Port	06:21.9
20	GoodCRC	SOP	UFP	SINK	6	Port	06:21.9
21	EPR_Mode (Action=Enter)	SOP	UFP	SINK	1	Port	06:21.9
22	GoodCRC	SOP	DFP	SOURCE	1	Port	06:21.9
23	EPR_Mode (Action=Enter_Acknowledged)	SOP	DFP	SOURCE	7	Port	06:21.9
24	GoodCRC	SOP	UFP	SINK	7	Port	06:21.9
25	EPR_Mode (Action=Enter_Succeeded)	SOP	DFP	SOURCE	0	Port	06:21.9
26	GoodCRC	SOP	UFP	SINK	0	Port	06:21.9
27	EPR_Source_Capabilities (Chunk Response #0)	SOP	DFP	SOURCE	1	Port	06:21.9

Table 8-4. 48V EPR Sink Contract with Keep Alive Shown PD Log (continued)

#	Message Type	SOP*	Data Role	Power Role	MsgID	Sender	Time Stamp
28	GoodCRC	SOP	UFP	SINK	1	Port	06:21.9
29	EPR_Source_Capabilities (Chunk Request #1)	SOP	UFP	SINK	2	Port	06:21.9
30	GoodCRC	SOP	DFP	SOURCE	2	Port	06:21.9
31	EPR_Source_Capabilities (Max: 240W, Fixed 5V-3A, Fixed 9V-3A, Fixed 15V-3A, Fixed 20V-5A, Fixed 28V-5A, Fixed 36V-5A, Fixed 48V-5A, EPR AVS PDP:240-48V-15V)	SOP	DFP	SOURCE	2	Port	06:21.9
32	GoodCRC	SOP	UFP	SINK	2	Port	06:21.9
33	EPR_Request (ObjPos=10, Fixed 48V-5A)	SOP	UFP	SINK	3	Port	06:22.0
34	GoodCRC	SOP	DFP	SOURCE	3	Port	06:22.0
35	Accept	SOP	DFP	SOURCE	3	Port	06:22.0
36	GoodCRC	SOP	UFP	SINK	3	Port	06:22.0
37	PS_RDY	SOP	DFP	SOURCE	4	Port	06:22.1
38	GoodCRC	SOP	UFP	SINK	4	Port	06:22.1
39	Extended_Control (EPR_KeepAlive)	SOP	UFP	SINK	4	Port	06:22.5
40	GoodCRC	SOP	DFP	SOURCE	4	Port	06:22.5
41	Extended_Control (EPR_KeepAlive_Ack)	SOP	DFP	SOURCE	5	Port	06:22.5
42	GoodCRC	SOP	UFP	SINK	5	Port	06:22.5
43	Extended_Control (EPR_KeepAlive)	SOP	UFP	SINK	5	Port	06:22.9
44	GoodCRC	SOP	DFP	SOURCE	5	Port	06:22.9
45	Extended_Control (EPR_KeepAlive_Ack)	SOP	DFP	SOURCE	6	Port	06:22.9
46	GoodCRC	SOP	UFP	SINK	6	Port	06:22.9



5

Figure 8-22. 48V EPR Contract Negotiation VBUS and VBUS LV

8.3 Layout

8.3.1 TPS26750 - Layout

8.3.1.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

8.3.1.1.1 Recommended Via Size

Proper via stitching is recommended to carrying current for the VBUS power paths and grounding. The recommended minimum via size is shown below, but larger vias are an option for low density PCB designs. A single via is capable of carrying 1A, verify the tolerance with the board manufacturing. Vias are recommended to be tented when located close to the PD controller.

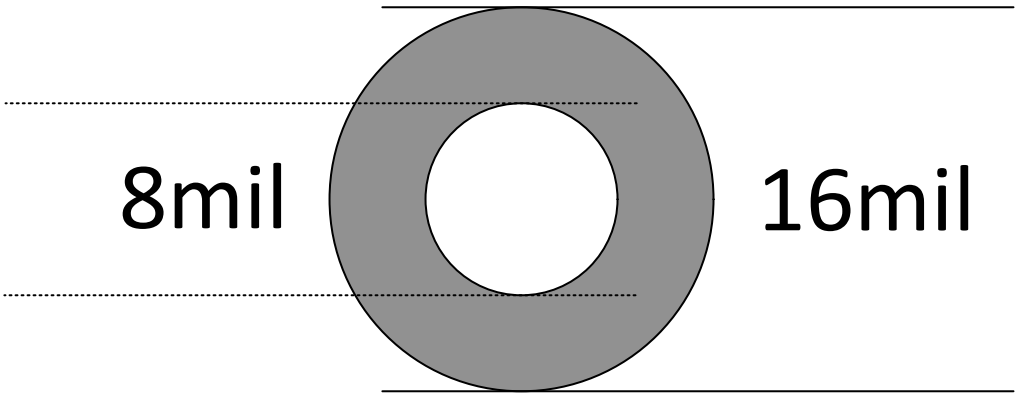


Figure 8-23. Recommend Minimum Via Size

8.3.1.1.2 Minimum Trace Widths

Below are the minimum trace widths for analog and digital pins. The trace width limitations are also defined by the board manufacturing process used. Consult with manufacturing for determining the minimum trace widths and tolerance.

Table 8-5. Minimum Trace Width

Route	Minimum Width (mils)
CC1, CC2	10
VIN_3V3, LDO	10
Component GND	16
GPIO	4

8.3.1.2 Layout Example

8.3.1.2.1 TPS26750 Schematic Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS26750.

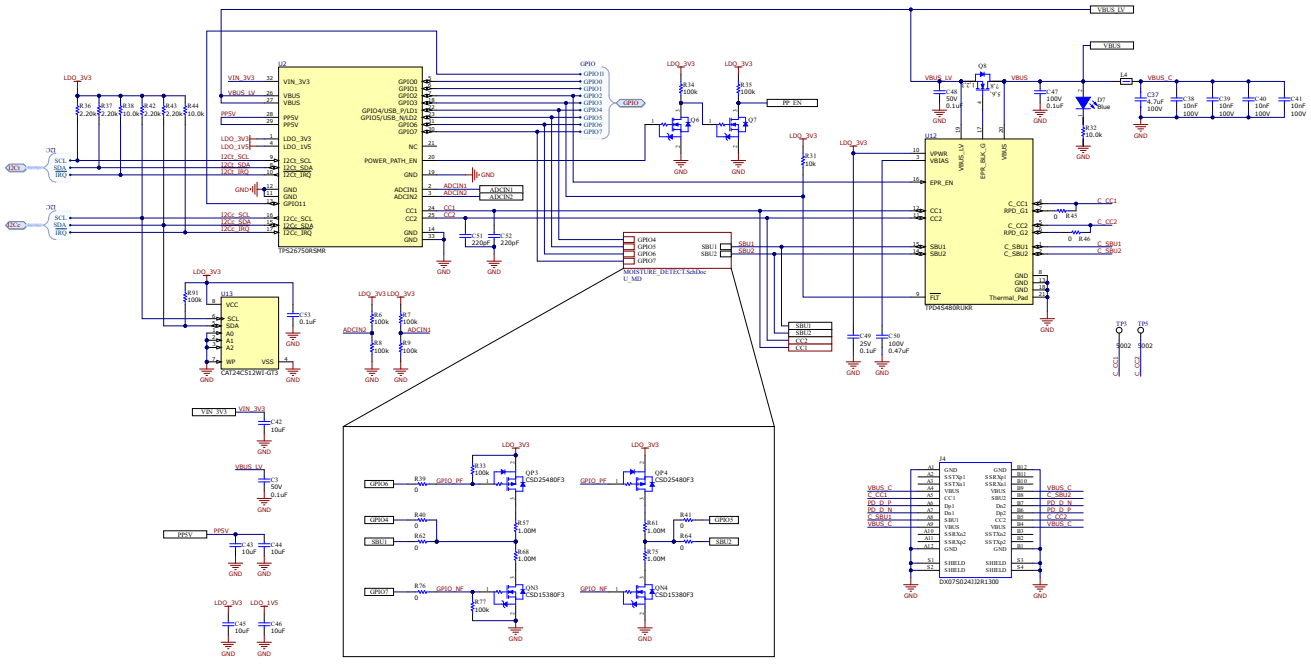


Figure 8-24. Example Schematic

8.3.1.2.2 TPS26750 Layout Example - PCB Plots

The following TPS26750 PCB Layout figures show the recommended layout, placement, and routing.

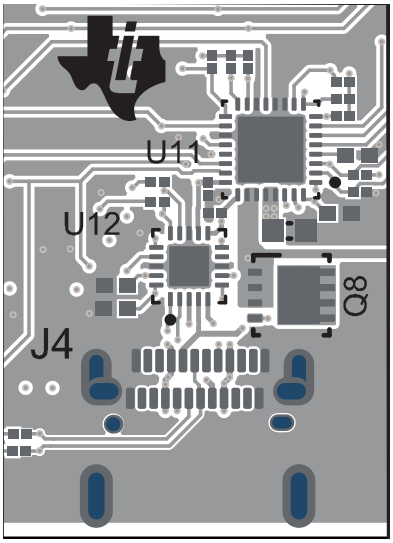


Figure 8-25. TPS26750 PCB Layout - Top Composite

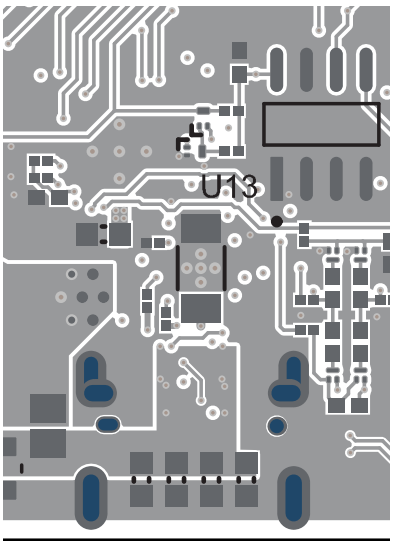


Figure 8-26. TPS26750 PCB Layout - Bottom Composite

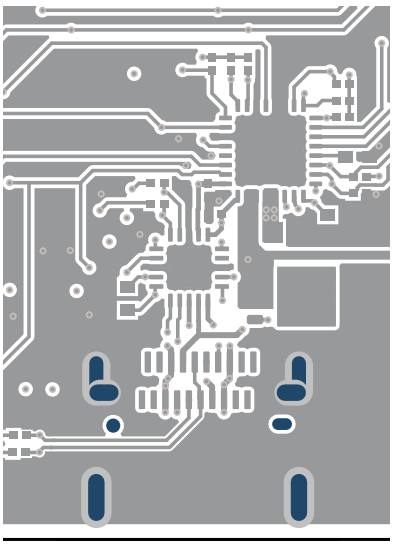


Figure 8-27. TPS26750 PCB Layout - Top Layer 1

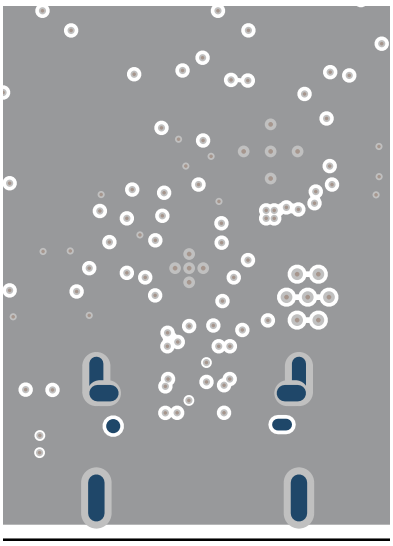


Figure 8-28. TPS26750 PCB Layout - GND Layer 2

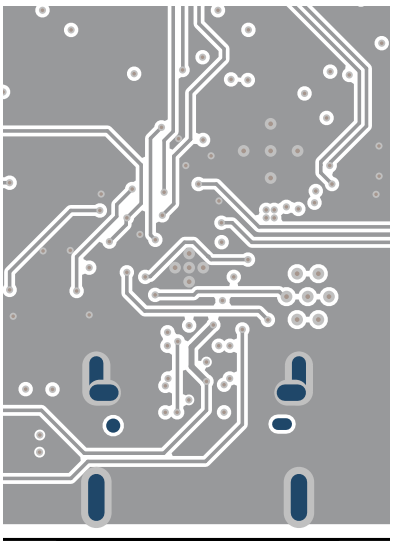


Figure 8-29. TPS26750 PCB Layout - Signal Layer 3

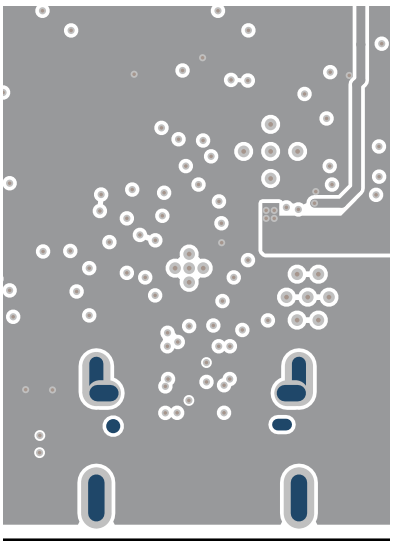


Figure 8-30. TPS26750 PCB Layout - Signal Layer 4

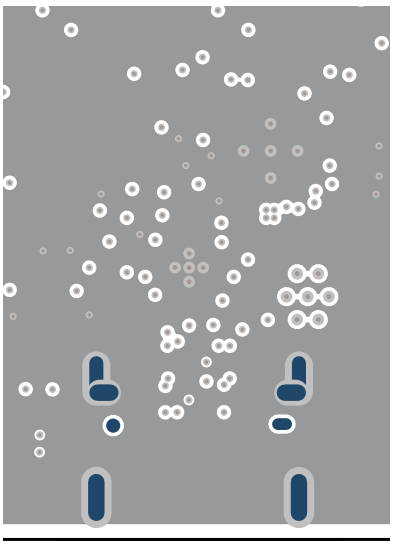


Figure 8-31. TPS26750 PCB Layout - GND Layer 5

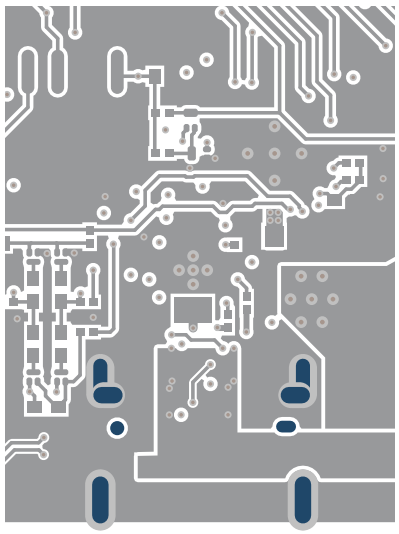


Figure 8-32. TPS26750 PCB Layout - Bottom Layer 6

8.3.1.2.2.1 TPS26750 Component Placement

LDO_1V5 (pin 4), LDO_3V3 (pin 1), and VIN_3V3 (pin 32)

The decoupling capacitors for LDO_3V3, LDO_1V5, and VIN_3V3 (C15, C16, and C17 respectively) need to be placed as close as possible to TPS26750 device for optimal performance. For this example to minimize solution size, the decoupling capacitors are placed on the bottom layer with their ground pads directly underneath the ground pad of TPS26750. Use a maximum of one via per pin from TPS26750 to the decoupling capacitors if placed on a different layer. Use a minimum of 10mil trace width to route these three traces, preferably with 16mil trace width if possible.

CC1 (pin 24) and CC2 (pin 25)

CC1 (C11) and CC2 (C10) capacitors need to be placed as close as possible to their respective pins and on the same layer as the TPS26750 device. When routing the CCx traces, DO NOT via to another layer in between the CCx pins of the TPS26750 to the CCx capacitors. Check to make sure the CCx capacitors are not place outside the CC trace creating an antenna, instead have the traces pass directly through the CCx capacitor pads as shown in the example layout (refer to figure 10-21). Use a minimum of 10mil trace width to ensure Vconn support (5V/0.6A).

8.3.1.2.2.2 TPS26750 PP5V

The 10uF decoupling capacitor (C8) need to be placed as close as possible to the PP5V pins of TPS26750. DO NOT use traces for PP5V. The PP5V power plane needs to be sized to support up to 3.6A (up to 3A for sourcing, 600mA for Vconn). When connecting the PP5V pins (pins 28 and 29) to the 5V power plane, use a minimum of 4 vias in parallel and close to the device to improve current sharing. Minimize the bottle necks cause by other vias or traces, large bottle necks reduces the efficiency of the power plane. The bulk capacitors (C6, C7, and C9) represent capacitances from the system 5V rail, these are placed further away from TPS26750 on the same PP5V power plane. Refer to figure 10-21 and figure 10-22 for placement and trace reference.

8.3.1.2.2.3 TPS26750 PP_EXT

Place the PP_EXT decoupling capacitors (C12, C13, and C14) as close as possible to TPS26750, these do not need to be on the same layer as the device. The PP_EXT power plane needs to be sized to support up to 5A of current. When connecting the PP_EXT plane to a different layer, use a minimum of 6 vias in parallel per layer change. It is highly recommended to have more than 6 vias if possible for layer change to improve current sharing and efficiency.

8.3.1.2.2.4 TPS26750 VBUS

VBUS (pins 26 and 27)

Place the VBUS decoupling capacitor (C37) as close as possible to the VBUS pin of the excernal NMOS transistor (Q8), the capacitor does not need to be on the same layer as the device. The VBUS power plane need to be sized to support up to 3A o fcurrent if the 5V power path is utalized. If this 5V power path is not utilized, then the power path can be sized to support 100mA of current. When connecting the VBUS pins (pins 26 and 27) plane to a different layer, use a minimum of 3 vias per layer change.

At the Type-C port/connector, it is recommended to use minimum of 6 vias from the connector VBUS pins for layer changes. Place the 10nF caps (C2, C3, C4, and C5) as close as possible to the connector VBUS pins as shown in figure 10-22.

When implemented with the TPD4S480, the TPS26750 does not require an external TVS protection device, but the power switch used in the system may require the addition of a TVS protection diode. Please refer to the datasheet of the switch selected to ensure that any protection requirements are met.

The VBUS line of the type C connector needs to be routed to the external power path in a manner that supports it's current and voltage needs. Please refer to the datasheet of the switch selected to ensure that any routing and current requirements are met.

8.3.1.2.2.5 TPS26750 I/O

I2C, ADCIN1/2, and GPIO pins

Fan these traces out from the TPS26750, use vias to connect the net to a routing layer if needed. For these nets, use 4mil to 10mil trace width.

I2Cc_SDA/SCL/IRQ (pins 8, 9, and 10) and I2Ct_SCL/SDA/IRQ (pins 15, 16, and 17)

Minimize trace width changes to avoid I2C communication issues.

ADCIN1 and ADCIN2 (pins 2 and 3)

Keep the ADCINx traces away from switching elements. If a resistor divider is used, place the divider close to LDO_3V3 or LDO_1V5.

GPIO (pins 5, 6, 7, 18, 22, 23, 31, 30, and 13)

Separate GPIO traces running in parallel by a trace width. Keep the GPIOx traces away from switching elements.

8.3.1.2.2.6 TPS26750 PPEXT Gate Driver

POWER_PATH_EN (pin 20)

The POWER_PATH_EN pin (pin 20) shall be connected to the gate of an NMOS source follower pair that implement a level shifter and buffer (Q6,Q7, R34 and R35) . The pull up resistors of the follower shall be connected the LDO_3V3 pin (pin 1) as shown in Figure 8-24.

This circuit is a non-inverting buffer that will create a 3.3V signal that is driven to 3.3V when the power switch selected needs to be driven to ground to be enabled, then an inverting circuit can be implemented by removiung Q7 and R35. This implements and inverting level shifter that will be driven to ground when the switch is to be enabled.

8.3.1.2.2.7 TPS26750 GND

The GND pad is used to dissipate heat for the TPS26750 device. Connect the GND pins (11, 12, 14 and 31) to the Ground pad (39) underneath the TPS26750 device. Connect the through hole vias from the ground pad on the top layer to a copper pour on the bottom layer to help dissipate heat. Additional vias can be added to improve thermal dissipation.

8.4 Power Supply Recommendations

8.4.1 3.3-V Power

8.4.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS26750 device. The VIN_3V3 switch (see *Power Management*) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3-V supply is available and the dead-battery flag is cleared. The recommended capacitance C_{VIN_3V3} (see *Recommended Capacitance*) must be connected from the VIN_3V3 pin to the GND pin).

8.4.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see *Recommended Capacitance*) from the LDO_1V5 pin to the GND pin.

8.4.3 Recommended Supply Load Capacitance

Recommended Capacitance lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS26750SRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26750S BG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

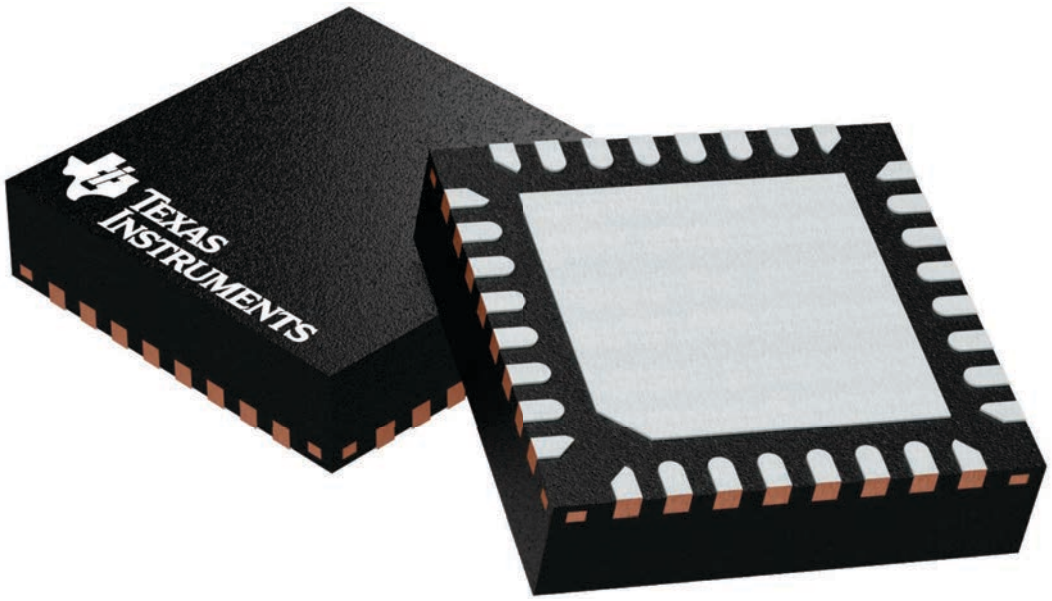
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



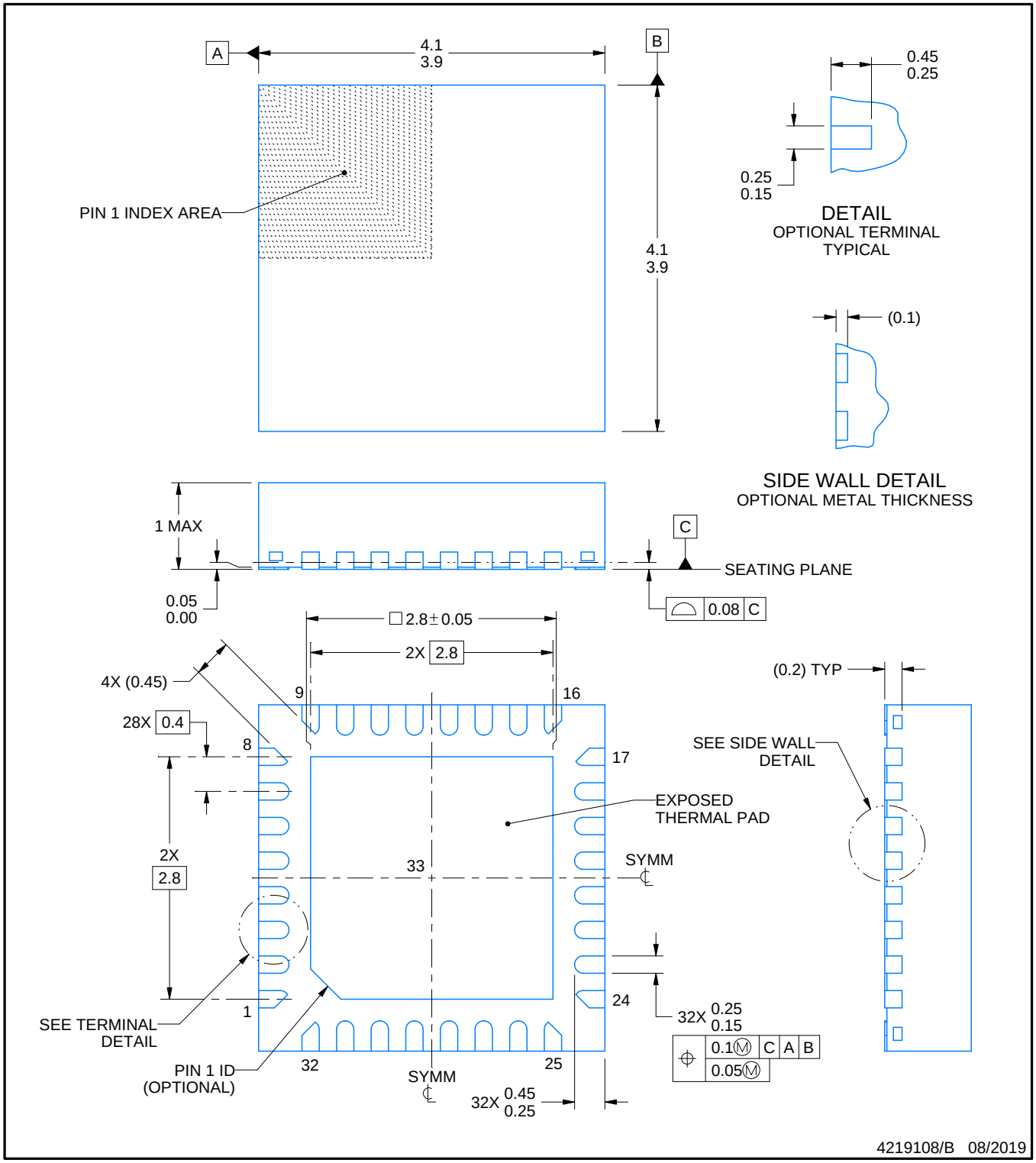
4224982/A

PACKAGE OUTLINE

RSM0032B

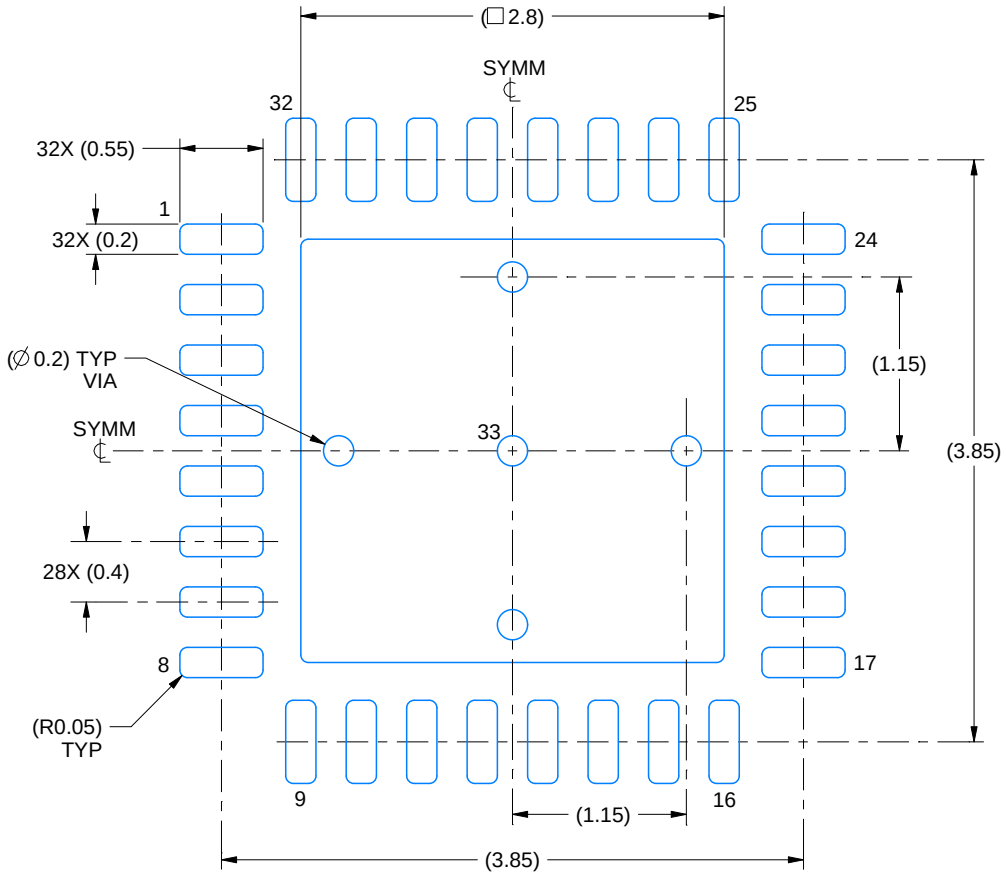
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

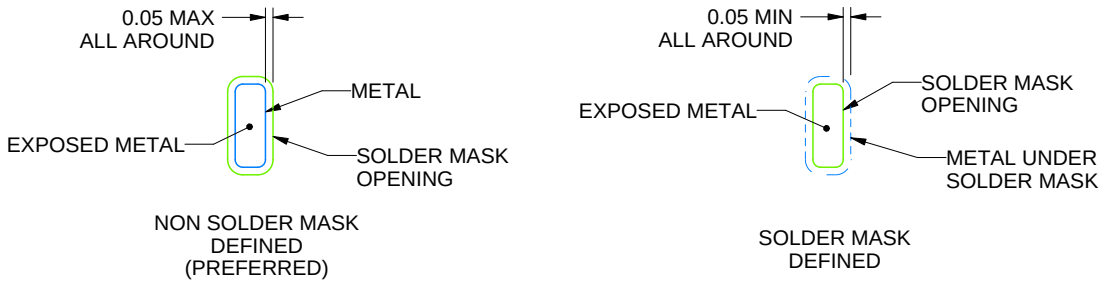


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

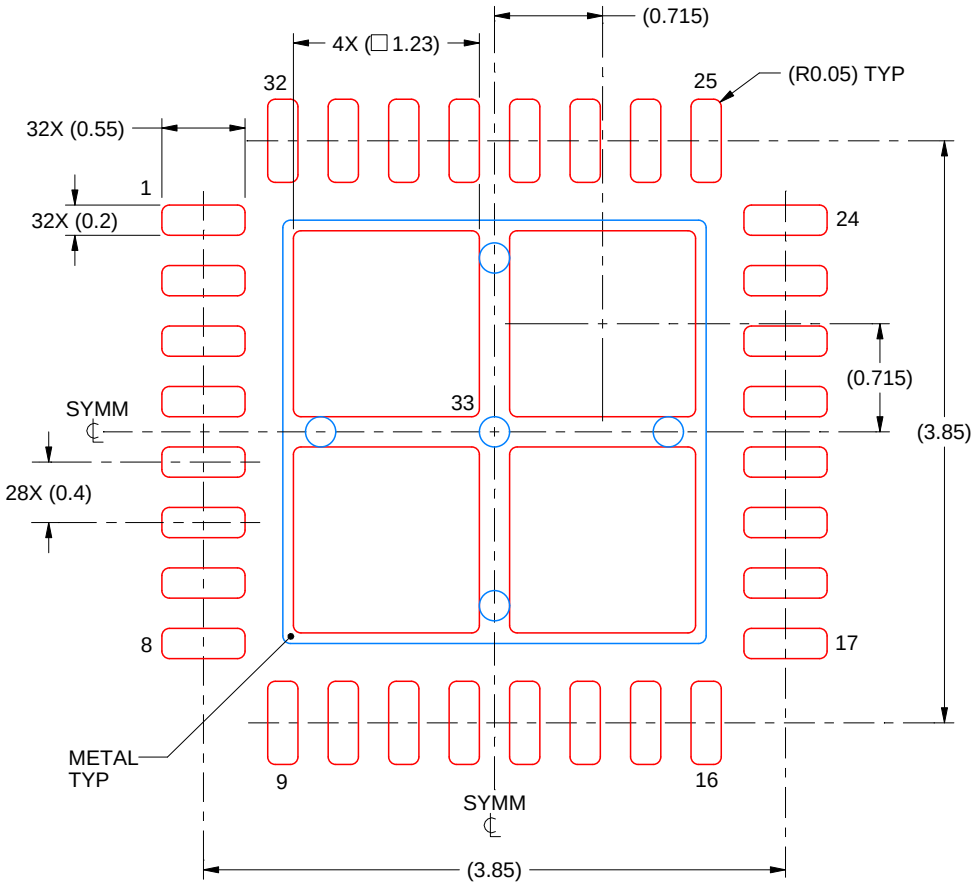


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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