TPS3423, TPS3424, Nano-Power, Push-Button Controllers With Configurable Delay to enable Battery Freshness Seal

1 Features

- Operating voltage range: 1V to 6V
- Nano supply current: 22nA (typical)
- HBM ESD rating on push-button pin: 10kV
- Programmable short press and long press duration
  - TPS3423, TPS3424 fixed timing options:
    - Short press duration: 50msec to 13 sec
    - Long press duration: 1sec to 30 sec
    - Timer accuracy (max): 10 %
  - TPS3424: user-programmable option (50 msec to 50 sec) through external capacitor
- Output configurations:
  - RESET configurations:
    - Push-pull / open-drain, active high / low
    - Latched / non-latched
    - 100msec to 1sec pulse option for non-latched version
  - $\overline{INT}$ configurations:
    - open drain, active low
    - non-latched (100msec to 1sec pulse duration)
- Kill feature: used as feedback from the host to de-assert RESET
- Available in pin compatible 8 pin and 6 pin DRL package

2 Applications

- Wearables
- Gaming consoles
- Home theater entertainment
- Printers
- Health care
- Portable electronics
- Factory automation & control

3 Description

TPS3423 and TPS3424 are push-button controllers which offer wide range of independent short press and long press functionality. These devices offer up to two outputs per push-button (RESET and $\overline{INT}$), which can be used for various use cases including enabling the voltage regulator or circuit breakers, sending an interrupt to micro controller and generating logic. The device generates an interrupt pulse both for short press and long press notifying the micro controller. RESET output changes the state based on the device configuration.

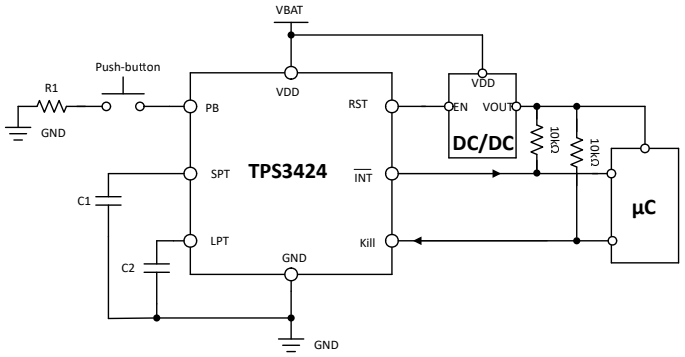
By controlling the power tree running off the battery, TPS3423/4 extends battery life and prolongs device shelf life. This feature is also known as battery freshness seal.

TPS3423/4 are offered in fixed timing options for short and long press durations. To provide flexibility to the designer, TPS3424 also offers user-programmable short and long press durations through an external capacitor. Kill pin in TPS3424 enables feedback from the microcontroller to asynchronously de-assert RESET.

Device Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (3)
TPS3423	DRL (SOT-5X3)	2.10mm × 1.60mm
	DRL (SOT-5X3) (2)	1.60mm × 1.20mm
TPS3424	DRL (SOT-5X3)	2.10mm × 1.60mm
	DRL (SOT-5X3) (2)	1.60mm × 1.20mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package
(3) The package size (length × width) is a nominal value and includes pins, where applicable



TPS3424 Typical Application Diagram

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4 Device Comparison

Figure 4-1 and Figure 4-3 shows the device nomenclature of the TPS3423 and TPS3424, for output / push-button input, short press and long press, interrupt, reset and kill timing options.Figure 4-2 extends nomenclature of TPS3423 to provide 2 different timing option for channels. Refer Section 7 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.

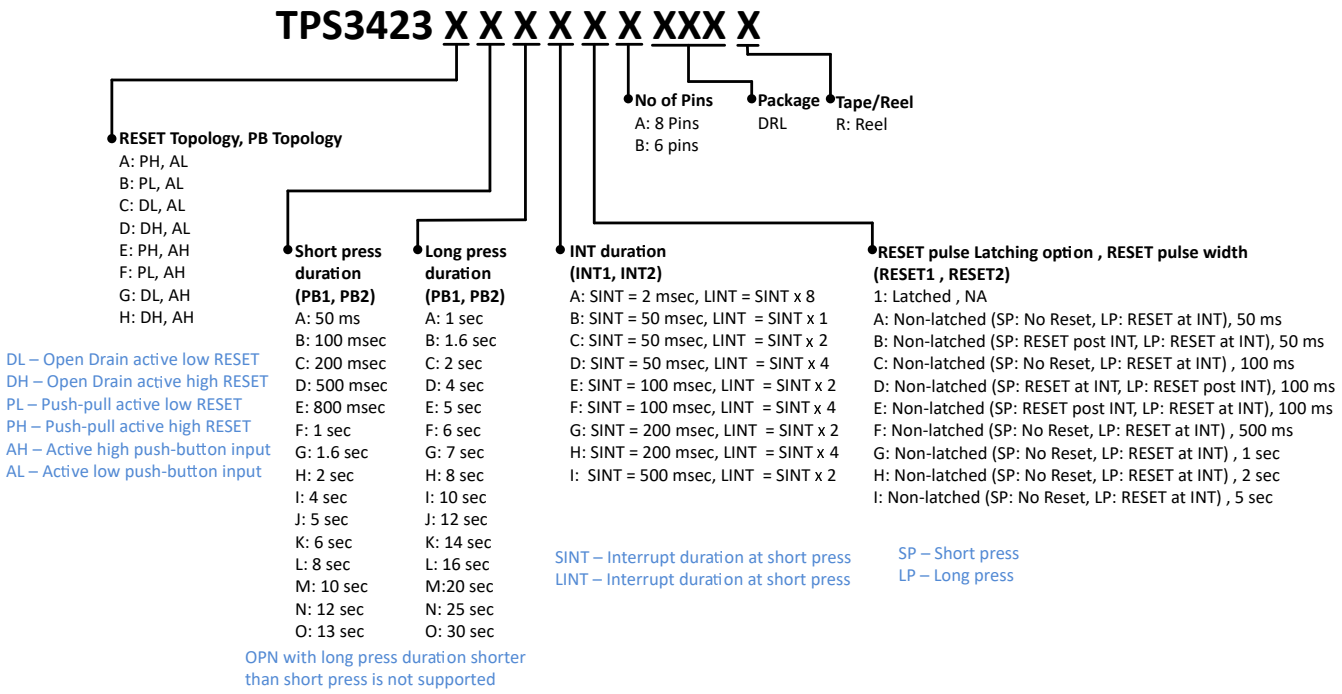

Figure 4-1. Dual Push-Button Nomenclature

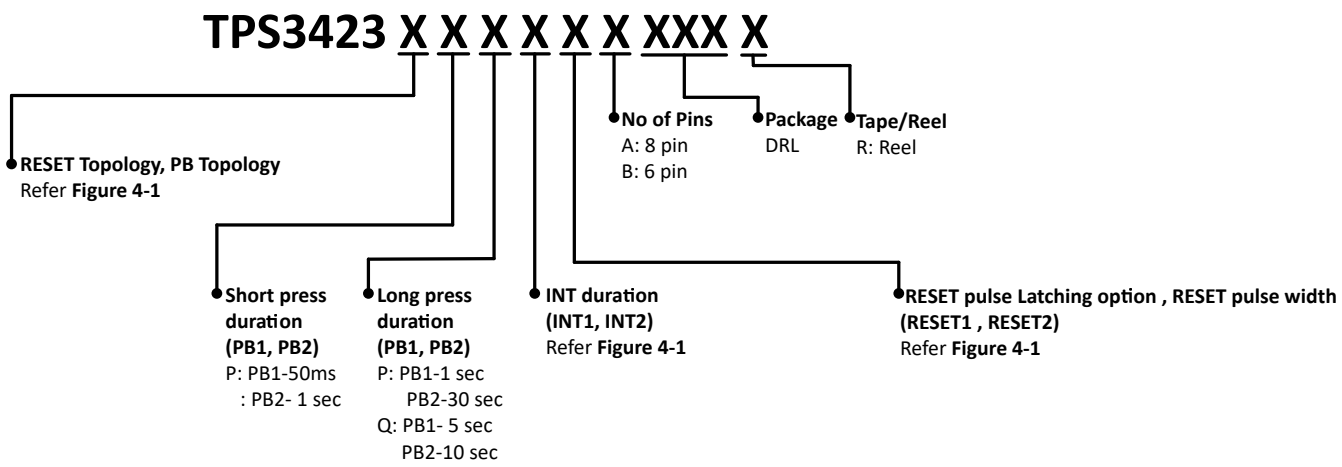

Figure 4-2. Dual Push-Button Extended Nomenclature

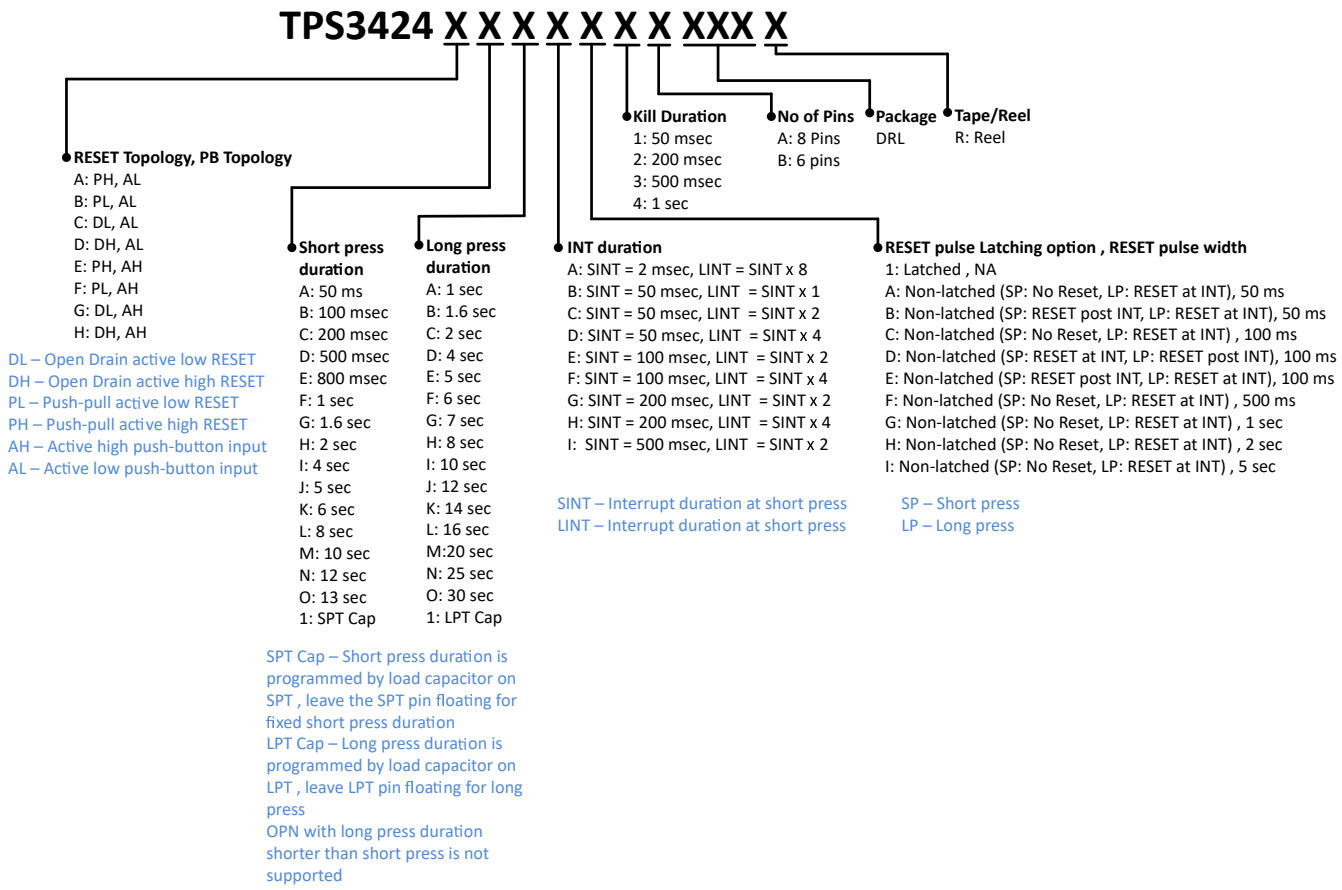

Figure 4-3. Single Push-Button Nomenclature

TPS3423/4 belongs to family of devices offering different feature sets as highlighted in Device Information.

Device Information

PART NUMBER	NO. OF PUSH-BUTTONS	PUSH-BUTTON TIMING OPTION	KILL FEATURE
TPS3423	2	Fixed	No
TPS3424	1	Fixed , programmable with external capacitor	Yes

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5 Pin Configuration and Functions

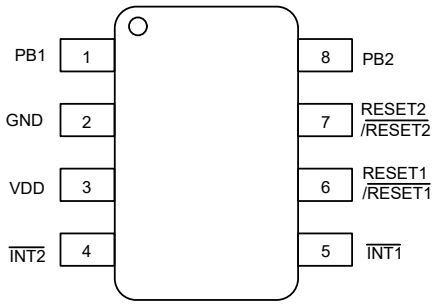

Figure 5-1. Pin Configuration Option: TPS3423
DRL Package
8-Pin SOT-5X3
Top View

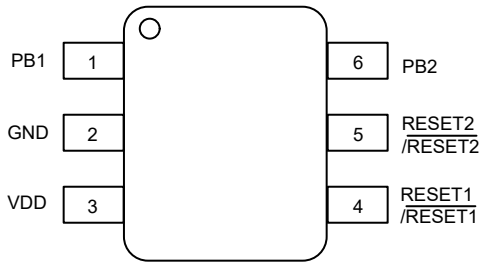

Figure 5-2. Pin Configuration Option TPS3423
DRL Package
6-Pin SOT-5X3
Top View

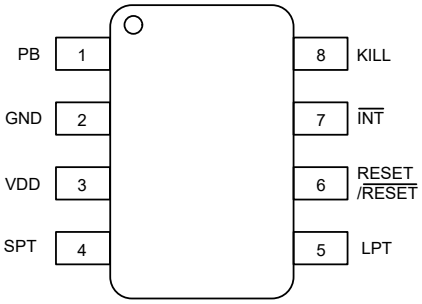

Figure 5-3. Pin Configuration Option TPS3424
DRL Package
8-Pin SOT-5X3
Top View

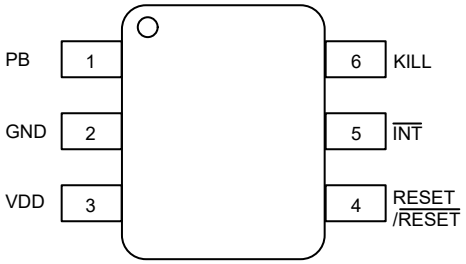

Figure 5-4. Pin Configuration Option TPS3424
DRL Package
6-Pin SOT-5X3
Top View

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Table 5-1. TPS3423 - Pin Functions

TPS3423			I/O	DESCRIPTION
PIN NAME	8 PIN SOT-5X3	6 PIN SOT-5X3		
PB1	1	1	I	Push-button input 1, refer Section 7.3.1.1 for additional details.
GND	2	2	-	Ground connection for IC.
V_{DD}	3	3	I	Supply connection, connect a 0.1µF capacitor near the pin for best performance.
$\overline{INT2}$	4		O	Interrupt output for push-button input 2, $\overline{INT2}$ is open drain active low output which toggles from every short press and long press on push-button input 2 as described in Section 7.3.2.1
$\overline{INT1}$	5		O	Interrupt output for push-button input 1, $\overline{INT1}$ is open drain active low output which toggles from every short press and long press on push-button input 1 as described in Section 7.3.2.1
RESET1/ $\overline{RESET1}$	6	4	O	RESET output for push-button input 1. The response of RESET to short press and long press is described in Section 7.3.2.2.
RESET2/ $\overline{RESET2}$	7	5	I	RESET output for push-button input 2. The response of RESET to short press and long press is described in Section 7.3.2.2.
PB2	8	6		Push-button input 2, refer Section 7.3.1.1 for additional details.

Table 5-2. TPS3424 - Pin Functions

TPS3424			I/O	DESCRIPTION
PIN NAME	8 PIN SOT-5X3	6 PIN SOT-5X3		
PB	1	1	I	Push-button input, refer Section 7.3.1.1 for additional details.
GND	2	2	-	Ground connection for IC.
V_{DD}	3	3	I	Supply connection, connect a 0.1µF capacitor near the pin for best performance.
SPT	4			Connect capacitor to program short press time as described in Section 7.3.1.1 for SPT Cap version.
LPT	5		O	Connect capacitor to program long press time as described in Section 7.3.1.1 for LPT Cap version.
RESET/ $\overline{\text{RESET}}$	6	4	O	RESET output for the device. The response of RESET to short press and long press is described in Section 7.3.2.2.
$\overline{\text{INT}}$	7	5	I	Interrupt output. $\overline{\text{INT}}$ is open drain active low output which toggles from every short press and long press on push-button input as described in Section 7.3.2.1
KILL	8	6		Kill is feedback from the host. RESET can be de-asserted in the latched version by pulling KILL low. Connect this pin to V_{DD} if not used. Please refer Section 7.3.1.3 for additional details.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	6.5	V
	V_{PB} (1)	–0.3	V_{DD} + 0.3	V
	V_{KILL} (1)	–0.3	V_{DD} + 0.3	V
Current	I_{RESET}	-6	6	mA
Temperature(2)	Operating free-air temperature, T_A	-40	125	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD ratings (Industrial)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (PB pin only) (1)	±10000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101	±750	V

(1) AEC Q-100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1		6	V
V_{PB}	Push-button pin input voltage	0		V_{DD}	V
V_{KILL}	KILL pin Voltage	0		V_{DD}	V
$V_{\overline{INT}}$	Interrupt pin voltage	0		V_{DD}	V
V_{RESET}	Output pin voltage	0		V_{DD}	V
I_{RESET}	Output pin current	0		5	mA
T_A	Ambient temperature (free-air temperature)	-40		125	℃
C_{SPT}	SPT capacitor (1)			125	nF
C_{LPT}	LPT capacitor			125	nF

(1) SPT capacitor value must be less than LPT capacitor

6.4 Thermal Information

THERMAL METRIC(1)		TPS3423 / TPS3424		UNIT
		DRL (SOT-583)	DRL (SOT-563)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance			°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance			°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance			°C/W
Ψ_{JT}	Junction-to-top characterization parameter			°C/W
Ψ_{JB}	Junction-to-board characterization parameter			°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance			°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 1 V <V_{DD} <6 V, SPT = LPT = Open, KILL = VDD C_{RESET} = 50 pF, INT = 10K pull up to VDD and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{DD}	Supply Voltage			1		6	V
$I_{DD(Standby)}$	Standby supply current(1)	V_{DD} = 3V	T_A = 25°C		22	30	nA
			T_A = –40°C to 85°C			90	
		V_{DD} = 6V	T_A = –40°C to 85°C		45	100	
		V_{DD} = 6V			45	350	
Push-button PIN							
$I_{DD(Active)}$	Supply current when $V_{\overline{PB}}$ = 0V (two push-button is pressed)(2)	V_{DD} = 3V				12	µA
	Supply current when $V_{\overline{PB}}$ = 0V (one push-button is pressed)(2)					7	
	Supply current when V_{PB} = VDD (both-push buttons are pressed)(3)					1.1	
$V_{IH(\overline{PB} / PB)}$	PB Logic high input(2)	V_{DD} = 3V		0.8*V_{DD}			
$V_{IL(\overline{PB} / PB)}$	PB Logic low Input(2)					0.3*VDD	
R_{PB}	PB pin internal pull-up / pull-down resistance(2) (3)				1000		kΩ
INT and RESET							
$V_{OL(\overline{INT})}$	Low level output voltage	V_{DD} = 1V, $\overline{INT}$ = 100µA				200	mV
	Low level output voltage	V_{DD} = 3V, $\overline{INT}$ = 1mA				300	
$I_{LKG(\overline{INT})}$	Open drain output leakage current for $\overline{INT}$	V_{DD} = $V_{\overline{Pullup}}$ = 6V				100	nA

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6.5 Electrical Characteristics (continued)

At 1 V <V_{DD} <6 V, SPT = LPT = Open, KILL = VDD C_{RESET} = 50 pF, INT = 10K pull up to VDD and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OL(RESET)}$	Low level output voltage (Open Drain)	V_{DD} = 1V, I_{RESET} = 300µA			200	mV
	Low level output voltage (Push-Pull)(4)	V_{DD} = 1V, I_{RESET} = 300µA			200	
	Low level output voltage (Open Drain)	V_{DD} = 3V, I_{RESET} = 5mA			300	
	Low level output voltage (Push-Pull)(4)	V_{DD} = 3V, I_{RESET} = 5mA			300	
$V_{OH(RESET)}$	High level output voltage (Push-Pull)(4)	V_{DD} = 1V, I_{RESET} = 200µA	0.7*V_{DD}			
	High level output voltage (Push-Pull)(4)	V_{DD} = 3V, I_{RESET} = 5mA	0.7*$_{VDD}$			
$I_{LKG\ (RESET)}$	Open drain output leakage current for (RESET)	V_{DD} = $V_{\overline{Pullup}}$ = 6V			300	nA
KILL , SPT , LPT						
I_{KILL}	Kill Input current			25		nA
V_{KILL_L}	$\overline{KILL}$ logic low input				0.3*V_{DD}	
V_{KILL_H}	$\overline{KILL}$ logic high input		0.7*V_{DD}			

(1) PB pin is floating.
(2) PB pin as active low.
(3) PB pin as active high.
(4) This spec holds true both for active high RESET and active low RESET.

6.6 Timing Requirements

At 1 V <V_{DD} <6 V, SPT = LPT = Open, KILL = VDD, C_{RESET} = 50 pF, INT = 10K pull up to VDD and over the operating free-air temperature range of - 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

Parameter		Test Condition	MIN	TYP	MAX	UNIT
t_{SP} Accuracy	Short press duration accuracy for fixed version(1)		-10		10	%
	Short press duration accuracy for adjutable version(1)	SPT = 330pF, LPT = 4.7nF	-20		20	%
t_{LP} Accuracy	Long press duration accuracy for fixed version		-10		10	%
	Long press duration accuracy for adjutable version	SPT = 330pF, LPT = 4.7nF	-20		-20	%
t_{SINT} Accuracy	Interrupt pulse width accuracy for PB long press		-10		10	%
t_{LINT} Accuracy	Interrupt pulse width accuracy for PB short press		-10		10	%
t_{KILL} Accuracy	PB/KILL debounce accuracy when RESET deaaserts in latched version		-10		10	%
t_{RESET}	Reset pulse duration (non latched) - Accuracy		-10		10	%
$t_{GI(KILL)}$	Glitch Immunity at KILL pin			250		ns
$t_{PD(KILL)}$	KILL falling edge to RESET assert delay			500		ns

(1) t_{SPD} should always be less than t_{LPD}.

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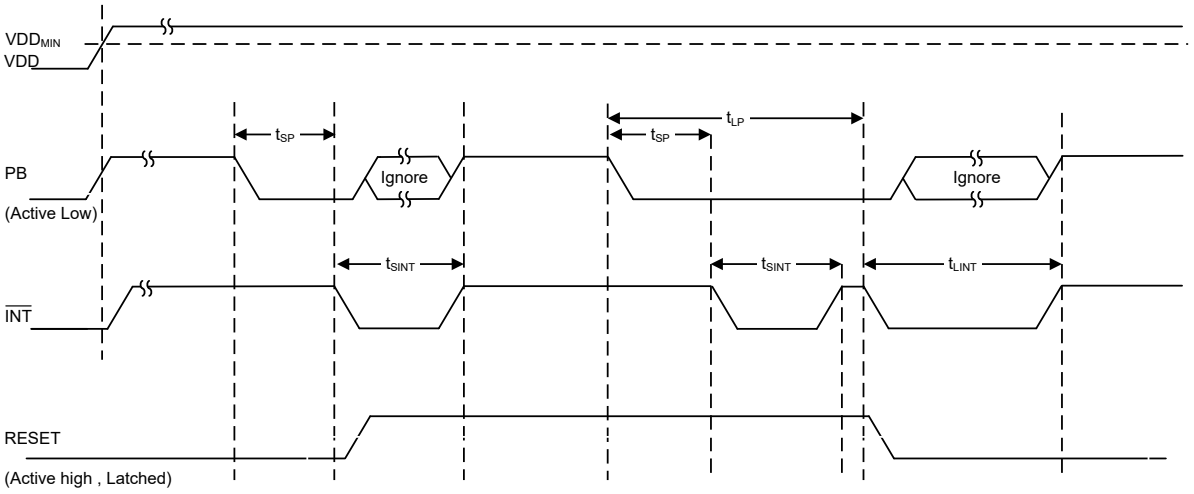
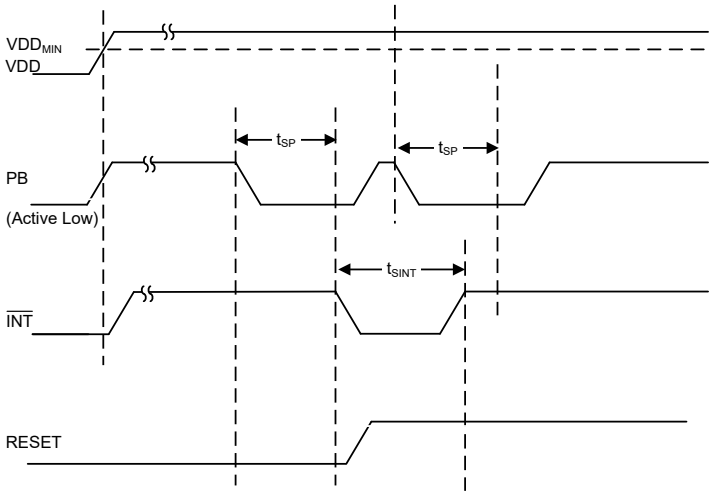
6.7 Timing Diagrams



PB input is ignored if it is released and again pressed during
- Interrupt pulse

Figure 6-1. Timing Diagram: Latched RESET



-No Interrupt pulse for second press during $\overline{INT}$ pulse

Figure 6-2. Timing Diagram: Example of PB Input Ignore

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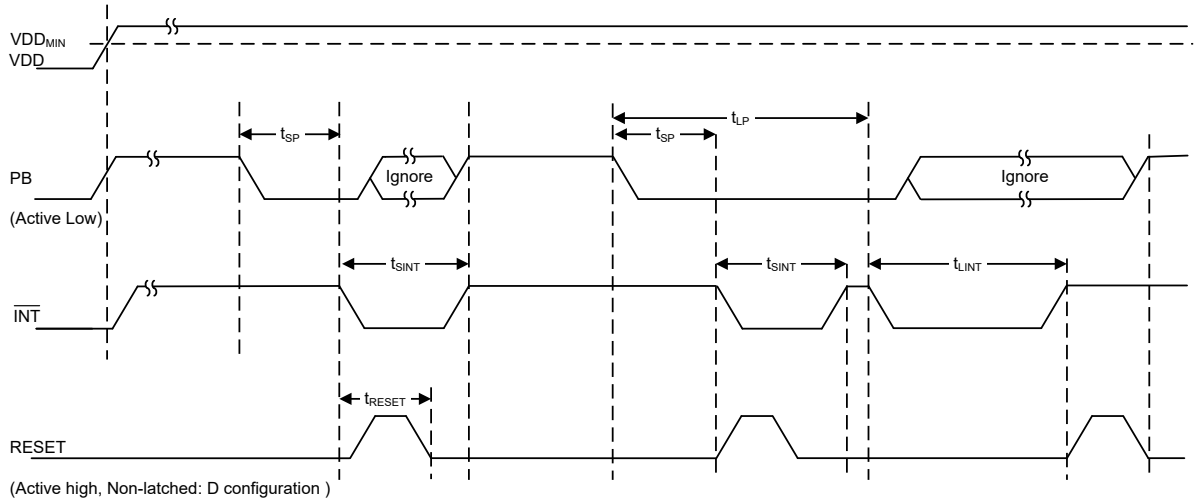
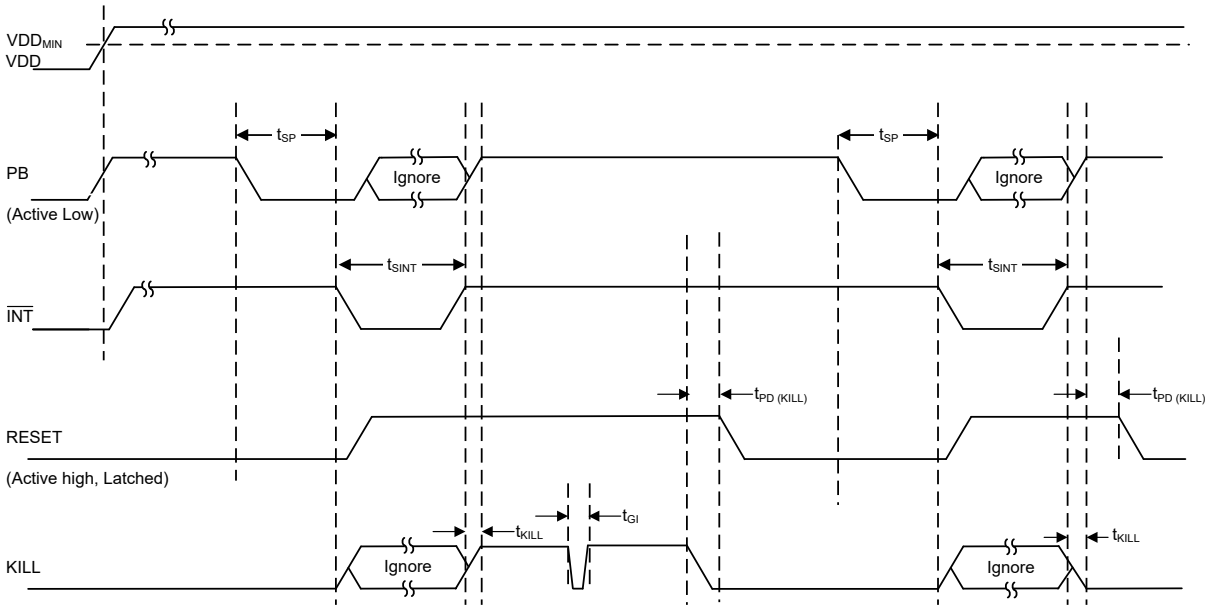


PB input is ignored if it is released and again pressed during
- Interrupt pulse
- Non-latched RESET pulse

Figure 6-3. Timing Diagram: Non-Latched RESET



PB input is ignored if it is released and again pressed during
- Interrupt pulse
- KILL debounce

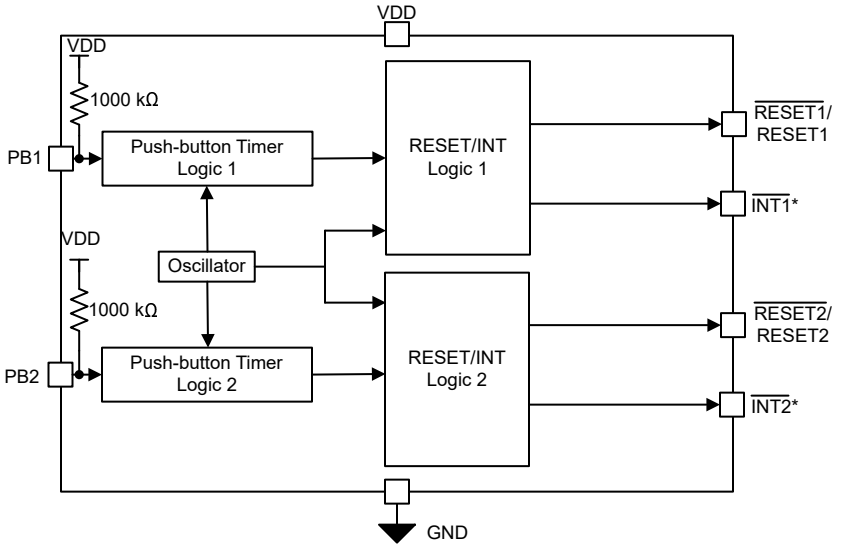
Figure 6-4. Timing Diagram: KILL

7 Detailed Description

7.1 Overview

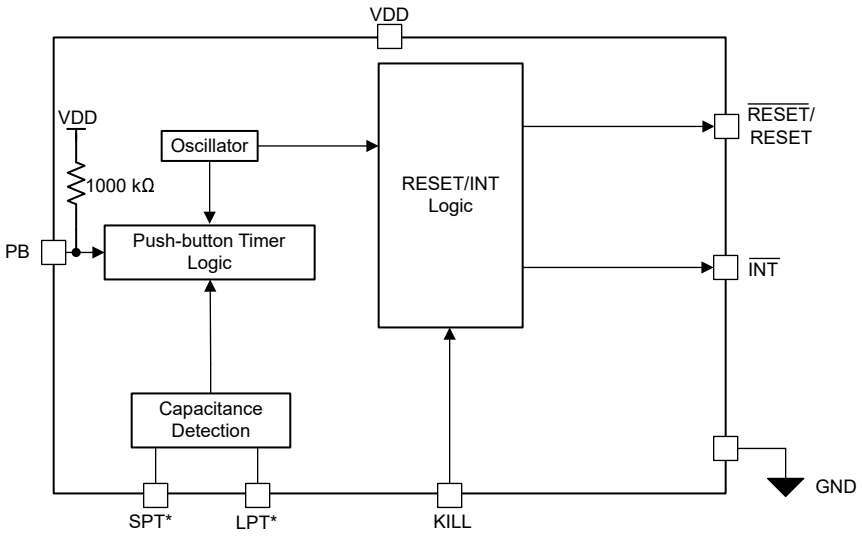
The TPS3423 & TPS3424 are nano power push-button family which offer wide range of timing option for input (PB, KILL) and output (RESET, $\overline{INT}$) pins. This device family is available in two different pinout with 8 and 6 pin DRL package and various output and input configuration as per Device Comparison to support various applications.

7.2 Functional Block Diagrams



* Available only in 8 pin DRL (SOT5X3) package

Figure 7-1. TPS3423 Block Diagram



* Available only in 8 pin DRL (SOT5X3) package

Figure 7-2. TPS3424 Block Diagram

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7.3 Feature Description

7.3.1 Inputs

This section discusses the inputs of the TPS3423 & TPS3424 devices.

7.3.1.1 Push-Button Input (PB)

Push-button input (PB) for TPS3423 and TPS3424 is available in active low and active high configuration as per Table 7-1 as shown in Figure 7-1 and Figure 7-2.

Table 7-1. Push-Button Configuration

PUSH-BUTTON CONFIGURATION	INTERNAL RESISTOR ORIENTATION	PB TRIGGER STATE
Active low	1000kΩ , pulled up to VDD	Pull the PB pin to GND level
Active High	1000kΩ , pulled down to GND	Pull the PB pin to VDD level

PB pin should be connected to a switch with ON resistance less than 20% of the pull-up / pull-down resistance to provide the correct PB input trigger for the device.

A precise timer gets started once PB pin is triggered. The device generates the output corresponding to short press, once PB pin is kept low (for active low PB) or kept high (for active high PB) for more than short press (t_{SP}) duration. The device generates output corresponding to long press if the PB pin is held in the same state for long press (t_{LP}) duration. The timer stops and gets reset when PB pin is released. If PB is released during interrupt pulse (Figure 7-3), non-latched RESET pulse or KILL debounce time then next PB input is ignored as described in Section 6.7.

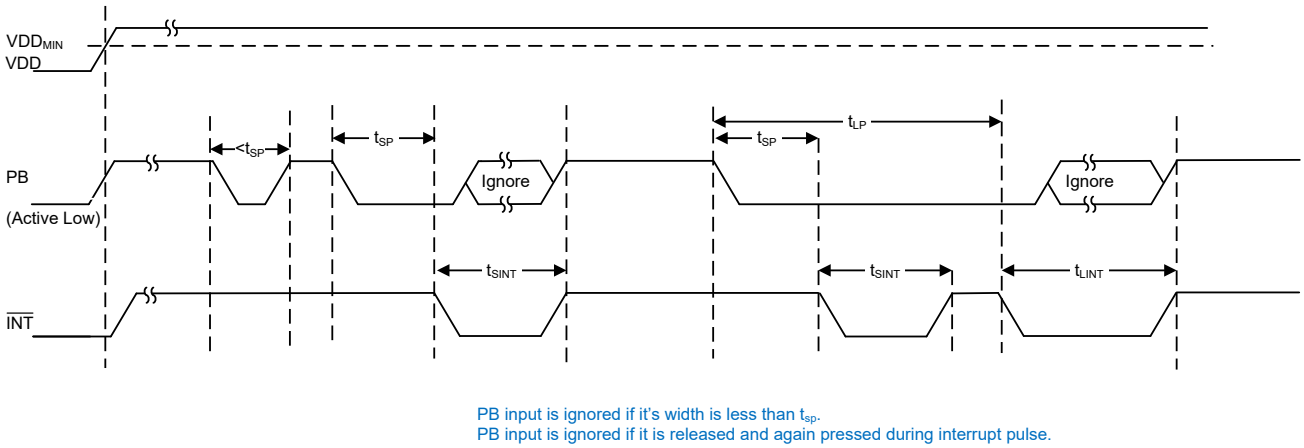

Figure 7-3. Push Button Functionality

TPS3423 has two independent push-button pins PB1 and PB2. These pins are factory programmed for short press (t_{SP}) and long press (t_{LP}) duration. TPS3424 has single PB pin. PB pin in TPS3424 is available both in fixed timing and user programmable option (8-pin DRL package) through capacitor connection on SPT and LPT pins. SPT and LPT pins must be floating for fixed timing option of TPS3424.

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7.3.1.2 Push-Button Timing Programmability

TPS3424x11xxx8DRLR has options to program short press duration (t_{SP}) and long press duration (t_{LP}) with capacitor on SPT pin and LPT pin respectively. Equation 1 shows the relation between the press duration and the capacitance. If the pin is left floating, the device defaults to fixed timer of 50msec. Connecting a capacitor which provides less than 50msec press duration as per, programs to 50msec press duration. Make sure t_{LP} is greater than t_{SP} for proper device operation.

$$t_{SP} \text{ or } t_{LP}(\text{sec}) = 0.422 \times C(\text{nF}) \quad (1)$$

where

- Press duration is t_{SP} for SPT capacitor and t_{LP} for LPT capacitor.
- C is the value capacitance connected on SPT or LPT pin.

7.3.1.3 KILL

KILL pin is used as a control input from the host in the latched RESET version. A short press on PB pin asserts the RESET in latched version. The host pulls KILL high if RESET assert for the host has performed all the expected tasks like enabling the whole power tree. The device ignores the KILL input for t_{SINT} + t_{KILL} time, allowing sufficient time for host to monitor the operation. The Host pulls KILL low if RESET assert doesn't perform all expected operations. Push-button de-asserts RESET if KILL is low after debounce period as shown in Figure 6-4. Host can pull KILL low at any time to de-assert RESET without any button press. KILL input is ignored for non-latched RESET configuration. Short kill to VDD is unused.

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7.3.2 Outputs

This section discusses the outputs of the TPS3423/4 devices.

7.3.2.1 Interrupt ($\overline{INT}$)

$\overline{INT}$ is open drain active low output. This pin generates low pulse for short press and long press as shown in Figure 6-1. Pulse duration for short press t_{INTS} and long press t_{INTL} is factory programmed. Please refer Section 4 section for the available option for the interrupt duration.

7.3.2.2 RESET / $\overline{RESET}$

RESET output of the device supports multiple configurations as described in Table 7-2. This device is available in all combination as described in Section 4.

Table 7-2. RESET CONFIGURATIONS

PARAMETER	VALUE
Latching option	Latched, Non-latched
Logic	Active High (AH), Active Low (AL)
Output configuration	Open Drain (OD), Push-Pull (PP)

RESET is asserted for short press and de-asserted for long press on PB pin for latched version as shown in Figure 6-1. Pulling KILL pin low also de-asserts the RESET in latched version as described in Figure 6-4. Non-latched RESET helps in achieving complex logic function with push-button. Non-latched RESET version of device supports multiple pattern as described in Section 4. RESET pattern is always different for short press and long press. One of the non-latched RESET pattern is shown in Figure 6-3.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Push-button controllers play an important role in any human-machine interface (HMI) design. They decode user inputs from single or multiple button presses, control system power or reset, and perform other essential user interface functions. TPS3423 and TPS3424 devices are designed to extend the shelf life of battery powered applications.

8.2 Typical Applications

8.2.1 Power Button Control with TPS3424

TPS3424 is designed for power button applications which need to put the system in deep sleep mode with very small standby power. TPS3424 controls enable for load switch or DC-DC converter in latched mode of RST pin.

An application diagram is shown in Figure 8-1.

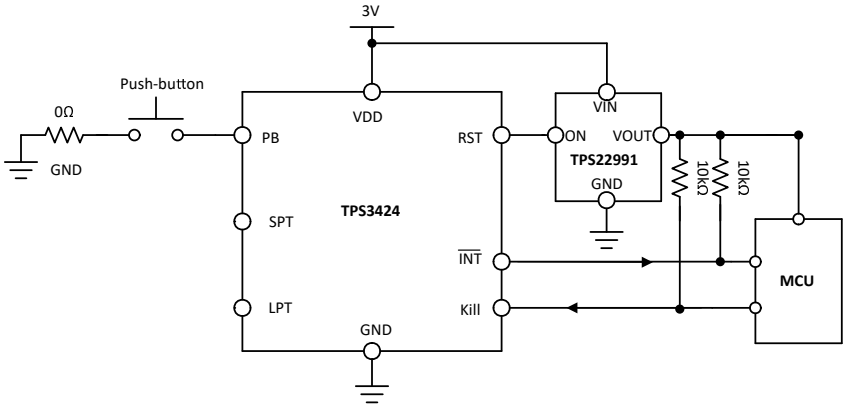

Figure 8-1. TPS3424 Application Diagram

8.2.1.1 Design Requirements

Table 8-1 lists the design requirements for Figure 8-1.

Table 8-1. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT
Single input	PB
T_{ON} = 100ms	t_{SP}= 100ms
T_{OFF} = 1sec	t_{SP}= 1sec
Supply = 3V	VDD = 3V
MCU IO pin current rating < 500uA	INT & KILL pull up = 10kΩ

8.2.1.2 Detailed Design Procedure

Short press on the PB pin triggers the RESET, which enables the load switch TPS22991 and INT signal notifies to MCU. Load switch TPS22991 can be disabled either by a long press on the PB pin as shown Figure 8-2 or through KILL pin as shown in Figure 8-3 and Figure 8-4.

ADVANCE INFORMATION

ADVANCE INFORMATION

8.2.1.3 Application Curve

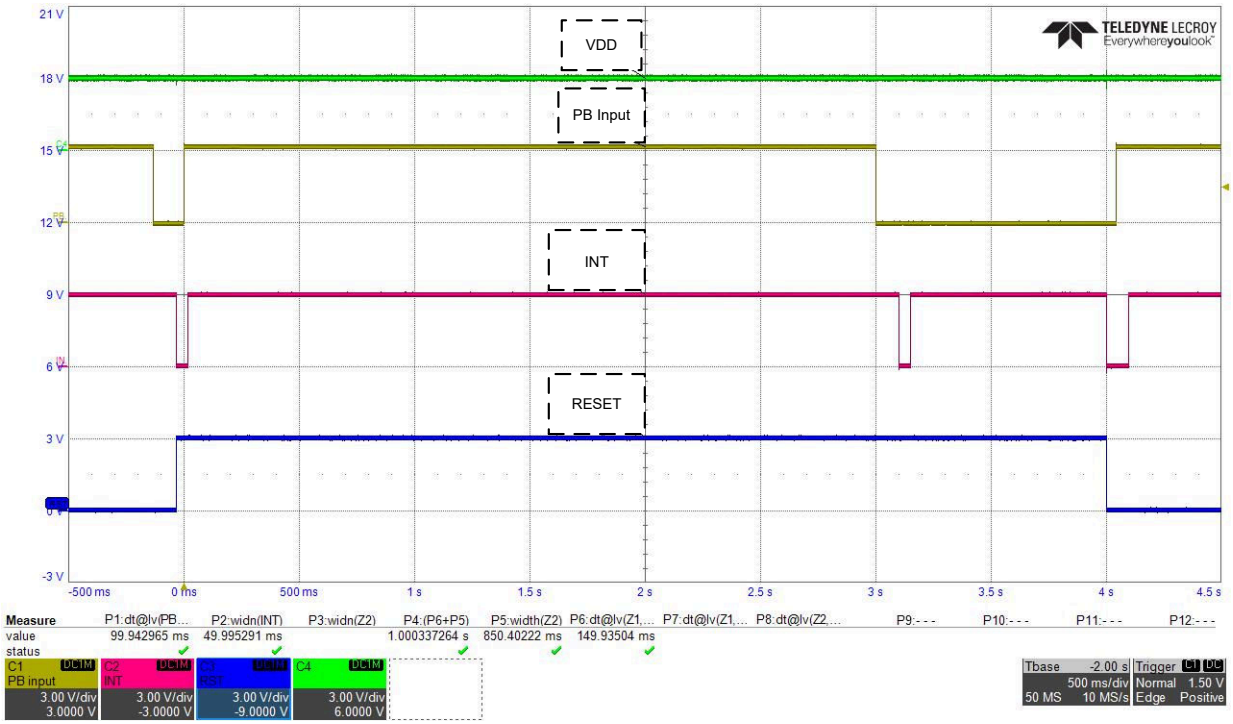

Figure 8-2. ON and OFF functionality of Push button

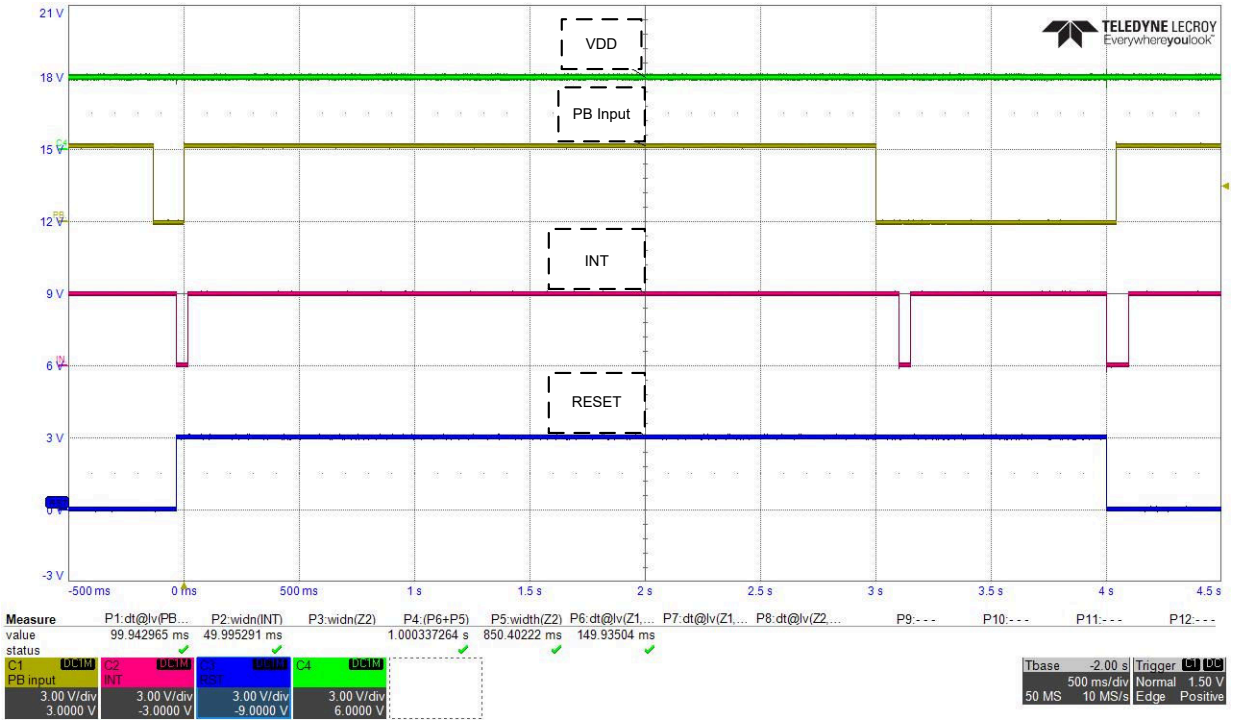

Figure 8-3. Asynchronous RESET deassert from HOST through KILL

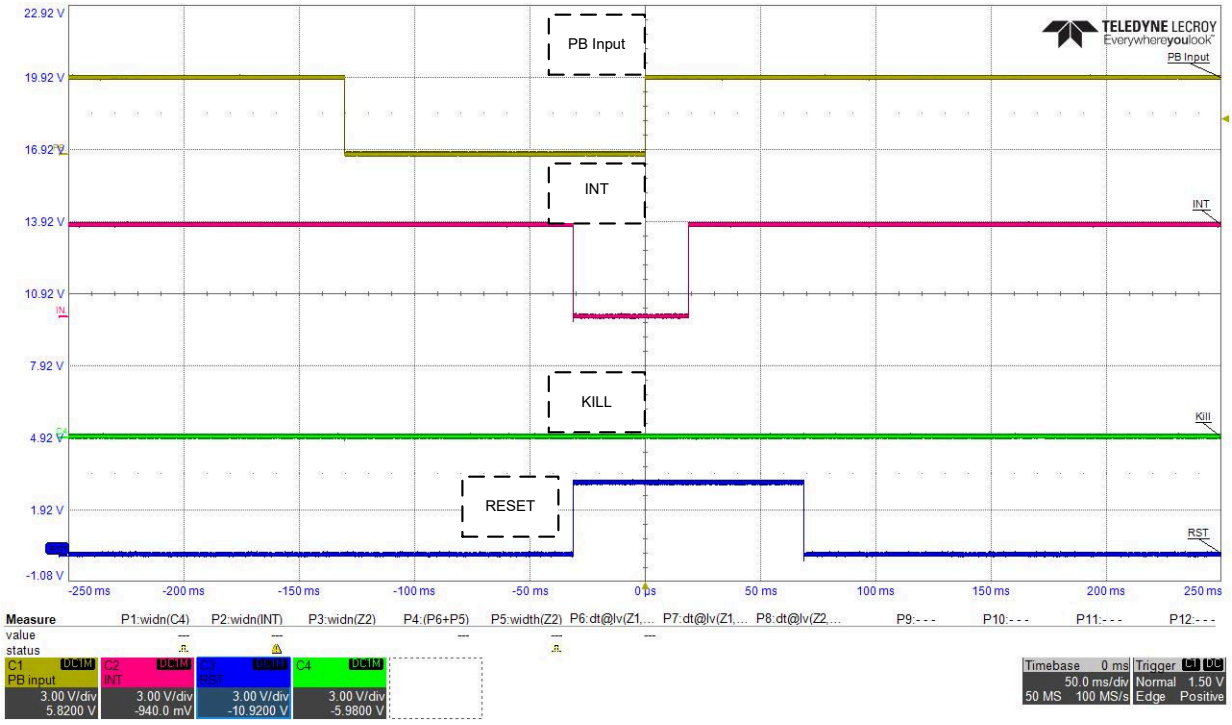

Figure 8-4. RESET deassertion by the HOST at the time of power ON

8.2.2 High Voltage Connection

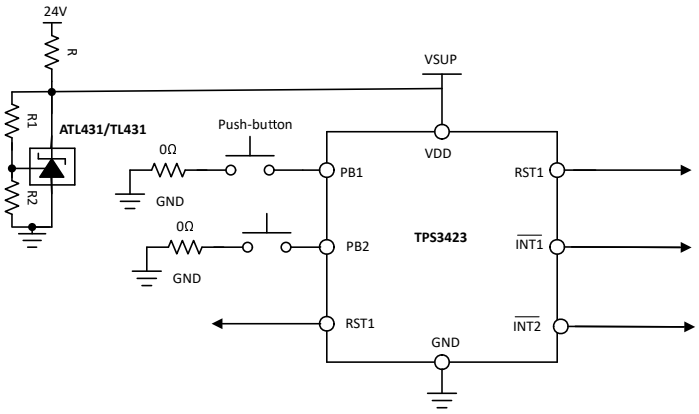

Figure 8-5. High voltage support with ATL431

8.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1V and 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1µF capacitor between the VDD pin and the GND pin.

8.4 Layout

8.4.1 Layout Guidelines

Follow these guidelines for laying out the printed circuit board (PCB) that is used for the TPS3423 and TPS3424.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1µF ceramic capacitor as near as possible to the VDD pin.
- Place the external capacitor on close to LPT and SPT pin for TPS3424.

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- Parasitic on LPT and SPT must be less than 50pF when these pins are floating for TPS3424.

8.4.2 Layout Example

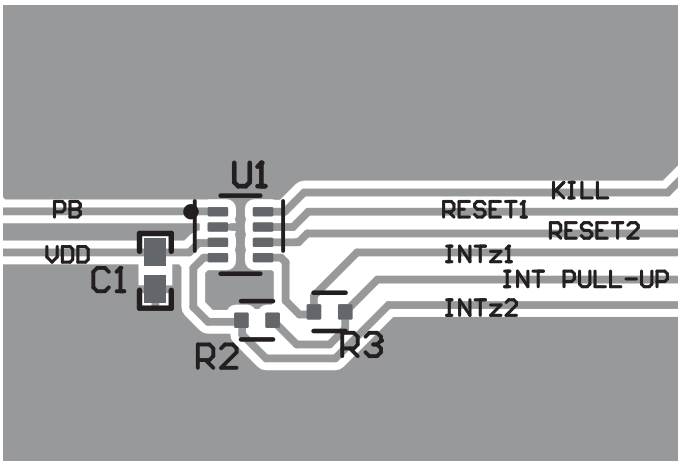

Figure 8-6. TPS3423: Layout Example (8-Pin DRL Package)

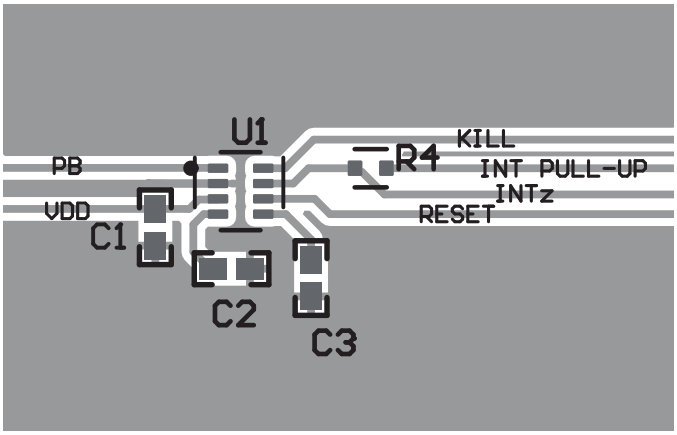

Figure 8-7. TPS3423: Layout Example (8-Pin DRL Package)

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PPS3424A11C13ADRLR	ACTIVE	SOT-5X3	DRL	8	4000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

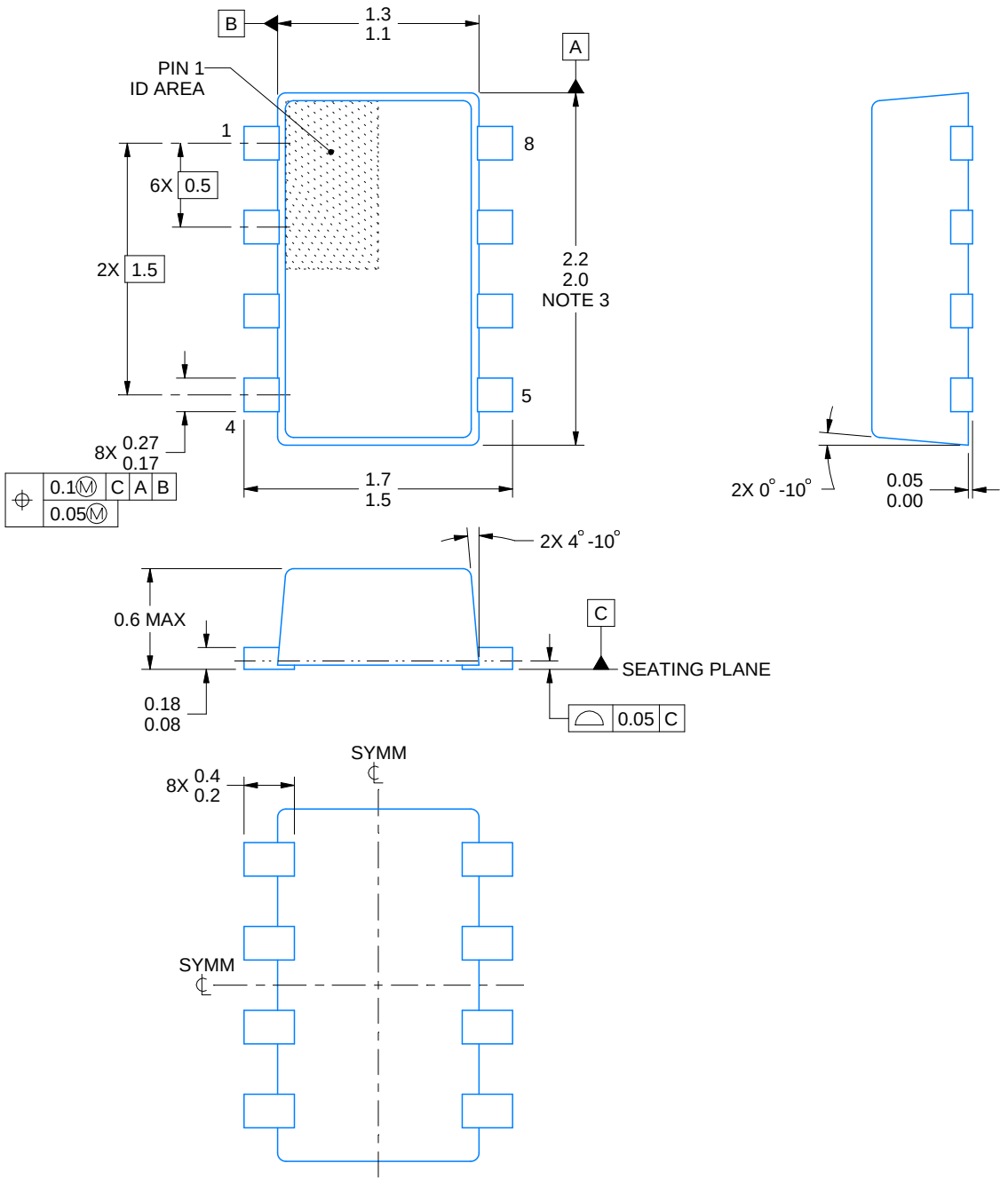
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

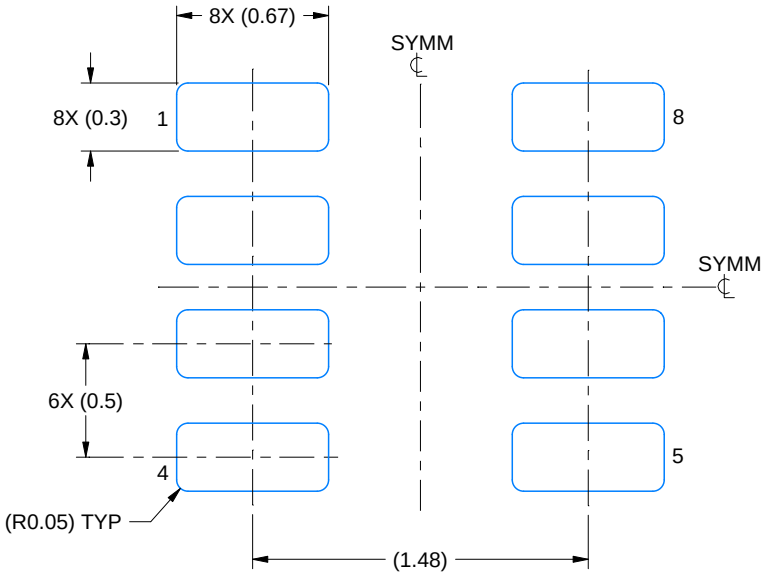
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

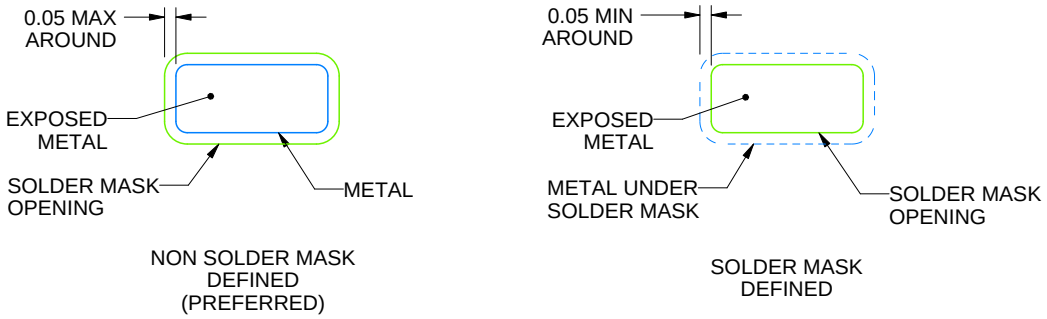
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

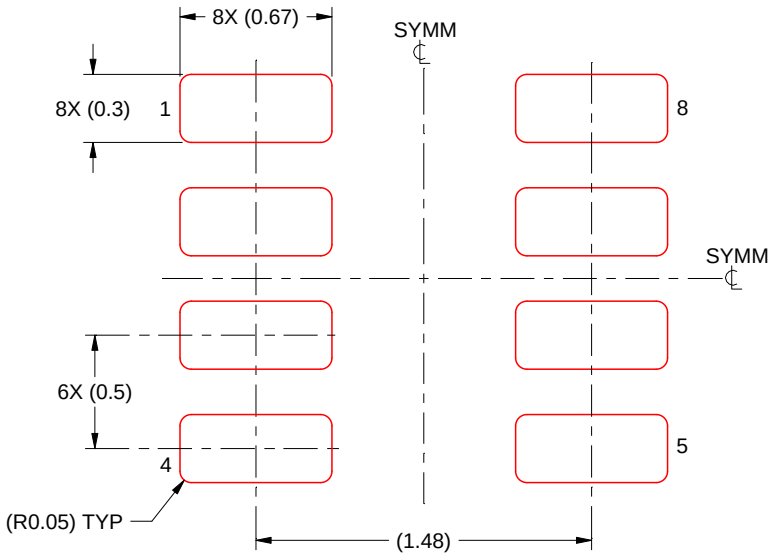
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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