



## VRM10.0 COMPLIANT PROGRAMMABLE FEEDBACK DIVIDER

### FEATURES

- VRM 10.x VID Code Table
- 14-Pin TSSOP

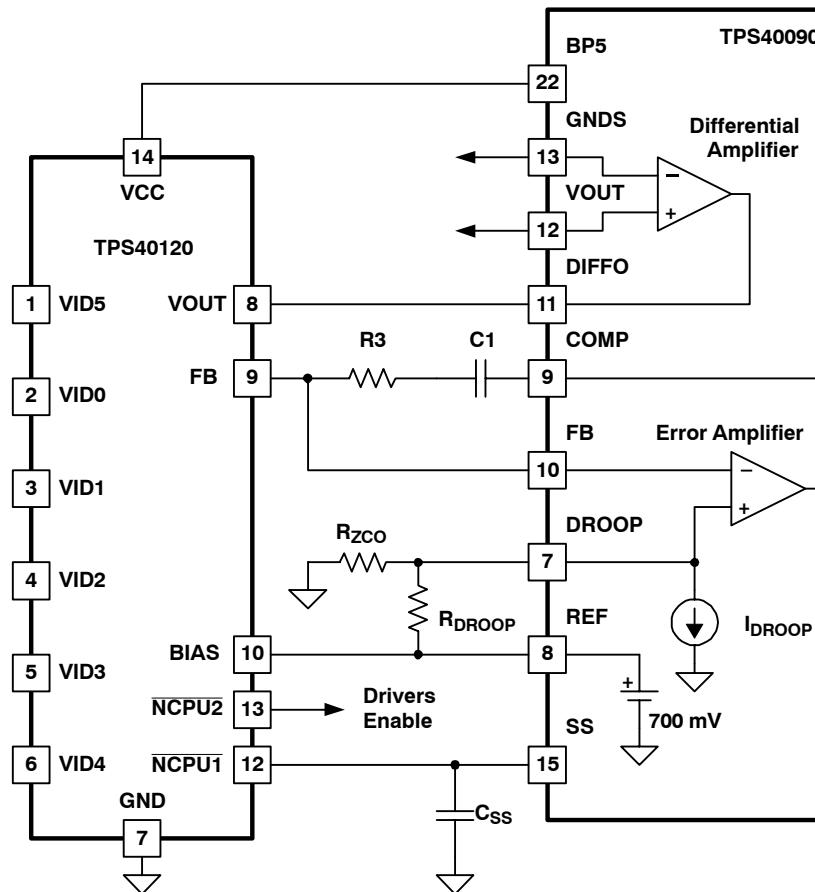
### APPLICATIONS

- Voltage Regulator Modules VRM/EVRD 10.x
- Multiphase Processor Power Supplies

### DESCRIPTION

The TPS40120 is a 6-bit digitally programmed feedback divider designed to work with TPS40090 multiphase controller or other controllers having 0.7-V internal reference to support VRM 10.x compliant power supplies. The TPS40120 is designed to support discrete DC/DC converters for Intel® processors using 5-bit (Pentium® 4 or Xeon™) or 6-bit VID codes with 12.5 mV steps.

### TYPICAL APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOSFET gates.

**ORDERING INFORMATION**

$T_A$	PLASTIC HTTSOP <sup>(1)</sup>
-40°C to 85°C	TPS40120PW

(1) The PW package is available taped and reeled. Add an R suffix to the device type (i.e. TPS40120PWR).

**ABSOLUTE MAXIMUM RATING<sup>(1)</sup>**

over operating free-air temperature range unless otherwise noted

			TPS40120	UNITS
$V_{IN}$	Input voltage range	VID0, VID1, VID2, VID3, VID4, VID5, VOUT	-0.3 to 5.5	V
$V_{OUT}$	Output voltage range	FB, N <sub>CPU2</sub>	-0.3 to 5.5	V
		VCC, N <sub>CPU1</sub>	-0.3 to 7.0	
$T_A$	Operating ambient temperature range		-40 to 85	°C
$T_{stg}$	Storage temperature		-55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.3	5.0	5.5	V
I/O voltage range	VID0, VID1, VID2, VID3, VID4, VID5, VOUT	-0.1		5.5	
Operating free-air temperature, $T_A$		-40		85	°C

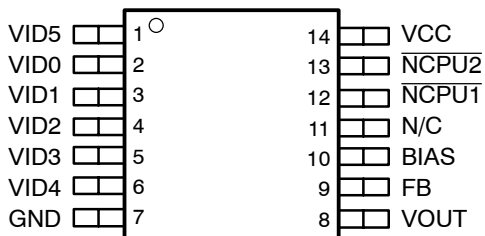
**ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCC}$	Supply voltage		4.3	5.0	5.5	V
$I_{VCC}$	Supply current	All VID inputs low			1	mA
$R_{FB}$	Resistance between FB and OUT		7.5	10	14.5	kΩ
	Divider accuracy		-0.5%		0.5%	
$VID_{THD}$	VID input logic high		0.85			V
$VID_{TLD}$	VID input logic low				0.3	
$I_{BIAS}$	BIAS input leakage	$V_{BIAS} = 0.7 V$			100	μA
	Logic low voltage	$I_{PULLUP} = 1 mA$			0.8	V
	Logic high leakage current				1	μA
	No CPU output voltage	$I_{L(SNK)} = 0.5 mA, I_{L(SRC)} = 0.5 mA$	$V_{VSS} + 0.5$		$V_{VCC} - 0.5$	V

**DEVICE INFORMATION**

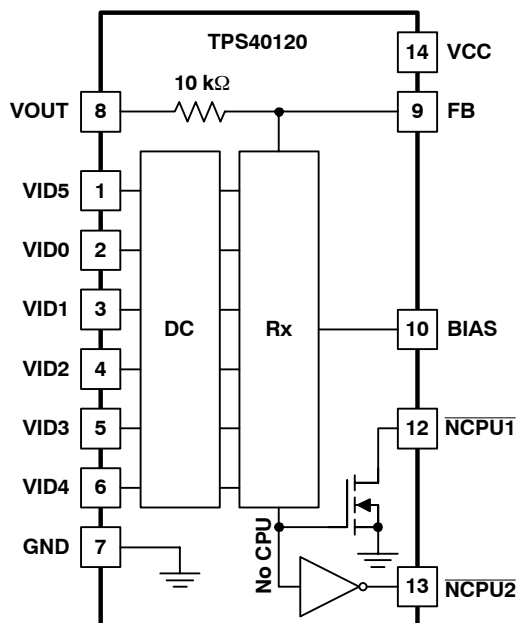
**PW PACKAGE  
(TOP VIEW)**



**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BIAS	10	I	Provides controller's reference voltage into the divider for improved tolerance.
FB	9	O	Middle point of the feedback divider connected to the inverting input of the controller's error amplifier
GND	7	-	Signal ground pin.
$\overline{\text{NCPU1}}$	12	O	Signals no CPU state. VID = x11111. Open drain output.
$\overline{\text{NCPU2}}$	13	O	Signals no CPU state. VID = x11111. TTL logic output.
VCC	14	I	Power to the device.
VID0	2	I	Voltage identification inputs. $V_{\text{REF}}$ voltage is set in accordance with VRM 10.x codes applied to these pins.
VID1	3	I	
VID2	4	I	
VID3	5	I	
VID4	6	I	
VID5	1	I	
VOUT	8	I	This pin is connected to the output of the VR module or to the output of the differential amplifier of the TPS40090 controller.

**FUNCTIONAL BLOCK DIAGRAM**



DETAILED DESCRIPTION

Operation

The digitally programmed feedback divider TPS40120 substitutes for a discrete output voltage set-divider and allows for multiphase PWM controllers such as the TPS4009x, TPS40130 and with internal reference of 0.7 V to provide voltage identification (VID) feature to power supply designs.

The TPS40120 operates as a resistive divider with constant value of the upper resistor and variable and code determined value of the lower resistor, refer to the functional block diagram. The VID code truth table is presented in Table 1.

Dynamic VID

Most modern processors adjust their core voltage depending on the workload and clock frequency by commanding voltage identification (VID) codes to the power supply. The power supply reads these VID codes and adjusts the output voltage in a control manner per processor requirements. To provide safe transition from one VID code to another (and to ensure that no erroneous output voltage is produced by the power supply), the TPS40120 VID inputs have internal anti-skew circuit with approximately 500 ns of filtering time. With a rate of change of 12.5 mV in 5  $\mu$ s, nothing else is required to achieve smooth upward and downward core voltage transitions. See Figure 1 and Figure 2.

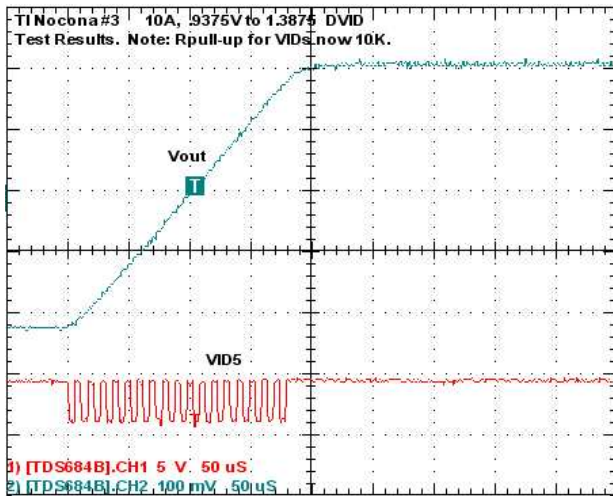


Figure 1. VID Step-Up Transition

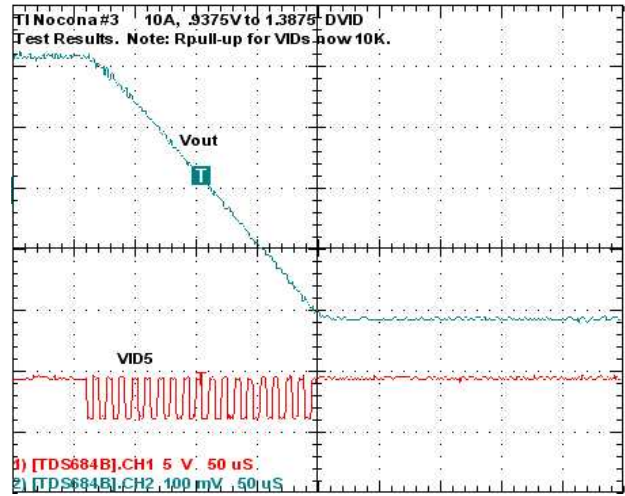


Figure 2. VID Step-Down Transition

**DETAILED DESCRIPTION (continued)**
**Table 1. Voltage Identification (VID)**

PROCESSOR PINS (0=LOW, 1=HIGH)						V <sub>REF</sub> (V)
VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375
0	1	0	0	1	1	0.8500
0	1	0	0	1	0	0.8625
0	1	0	0	0	1	0.8750
0	1	0	0	0	0	0.8875
0	0	1	1	1	1	0.9000
0	0	1	1	1	0	0.9125
0	0	1	1	0	1	0.9250
0	0	1	1	0	0	0.9375
0	0	1	0	1	1	0.9500
0	0	1	0	1	0	0.9625
0	0	1	0	0	1	0.9750
0	0	1	0	0	0	0.9875
0	0	0	1	1	1	1.0000
0	0	0	1	1	0	1.0125
0	0	0	1	0	1	1.0250
0	0	0	1	0	0	1.0375
0	0	0	0	1	1	1.0500
0	0	0	0	1	0	1.0625
0	0	0	0	0	1	1.075
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	OFF <sup>(1)</sup>
1	1	1	1	1	0	OFF <sup>(1)</sup>
1	1	1	1	0	1	1.1000
1	1	1	1	0	0	1.1125
1	1	1	0	1	1	1.1250
1	1	1	0	1	0	1.1375
1	1	1	0	0	1	1.1500
1	1	1	0	0	0	1.1625
1	1	0	1	1	1	1.1750
1	1	0	1	1	0	1.1875
1	1	0	1	0	1	1.2000
1	1	0	1	0	0	1.2125
1	1	0	0	1	1	1.2250
1	1	0	0	1	0	1.2375
1	1	0	0	0	1	1.2500
1	1	0	0	0	0	1.2625
1	0	1	1	1	1	1.2750
1	0	1	1	1	0	1.2875
1	0	1	1	0	1	1.3000
1	0	1	1	0	0	1.3125
1	0	1	0	1	1	1.3250
1	0	1	0	1	0	1.3375
1	0	1	0	0	1	1.3500

 (1)  $\overline{\text{NCPU1}}$  and  $\overline{\text{NCPU2}}$  outputs go low.

**DETAILED DESCRIPTION (continued)**

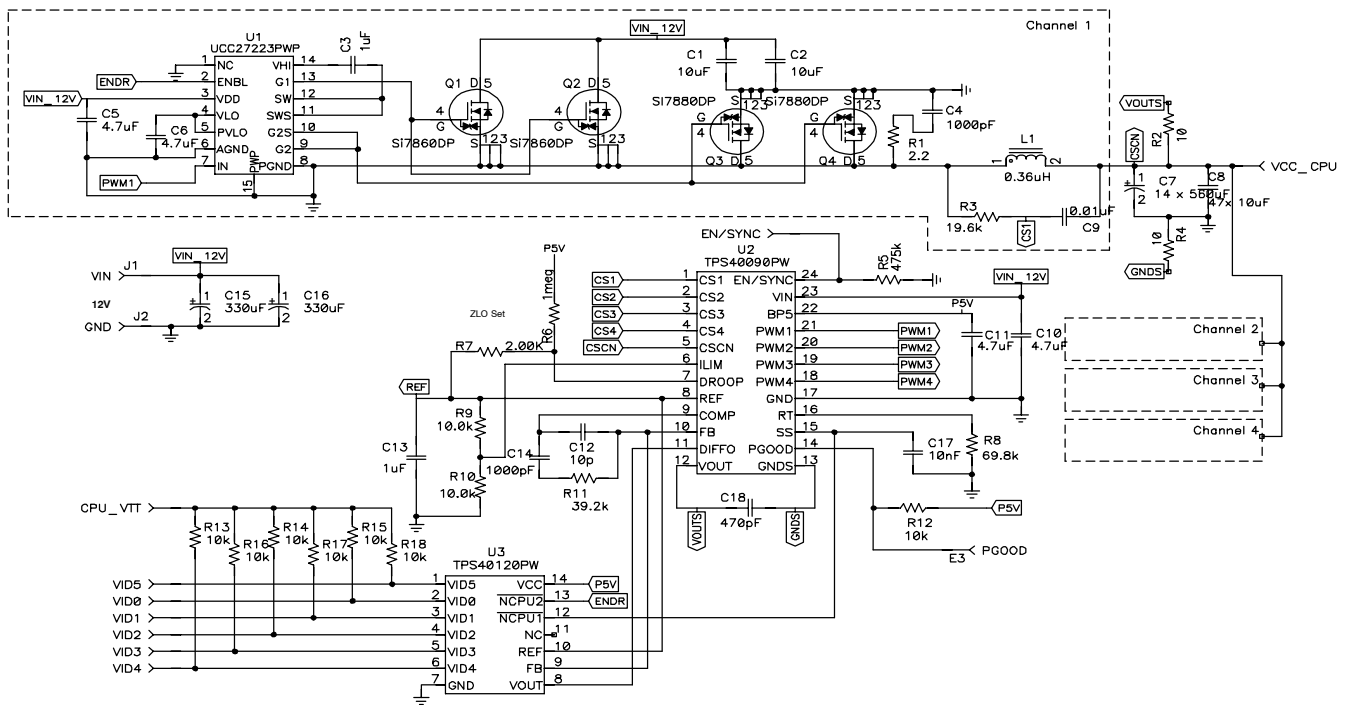
**Table 1. Voltage Identification (VID) (continued)**

PROCESSOR PINS (0=LOW, 1=HIGH)						V <sub>REF</sub> (V)
VID4	VID3	VID2	VID1	VID0	VID5	
1	0	1	0	0	0	1.3625
1	0	0	1	1	1	1.3750
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4000
1	0	0	1	0	0	1.4125
1	0	0	0	1	1	1.4250
1	0	0	0	1	0	1.4375
1	0	0	0	0	1	1.4500
1	0	0	0	0	0	1.4625
0	1	1	1	1	1	1.4750
0	1	1	1	1	0	1.4875
0	1	1	1	0	1	1.5000
0	1	1	1	0	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	0	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	0	1.5875
0	1	0	1	0	1	1.6000

**APPLICATION INFORMATION**

Typical application circuit for TPS40120 and TPS40090 combination is presented on the front page. Normally, the TPS40120 accepts power from the BP5 pin of the TPS40090 multiphase controller which simplifies its enable/disable control. The upper resistor of the programmable divider (pin 8) is connected to the output of the differential amplifier DIFFO. The center tap of the divider (pin 9) is connected to the joint point of the FB pin of the multi-phase controller and error amplifier compensation network. TPS40120 has two logic  $\overline{\text{NCPU}}_x$  outputs that can be used to control output and the gate drivers in a multi-phase power supply when no-CPU code is asserted. The  $\overline{\text{NCPU}}_1$  output is an open drain that can be useful by discharging the soft-start capacitor and bringing the output voltage down. The push-pull  $\overline{\text{NCPU}}_2$  output can be used to control gate drivers to provide high impedance of the power supply output in off state.

The application circuit for a four-phase 105-A CPU VRM10.x compliant power supply is shown in Figure 3.



**Figure 3. VRM 10.x Compliant CPU Power Supply**

For detailed information on TPS40090 multiphase controller and design example request the TPS4009x datasheet (SLUS578) and the user's guide (SLUU026).

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40120PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40120	Samples
TPS40120PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40120	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40120PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40120PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS40120PW	PW	TSSOP	14	90	530	10.2	3600	3.5

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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