

# TPS653860/61-Q1 Power Management IC For Safety-Relevant Applications

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the following results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature
  - Device Temperature Grade 0:  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- **Functional Safety-Compliant** (targets, confirmed on device release)
  - Developed for Functional Safety Applications
  - Documentation Available to Aid ISO 26262 System Design up to ASIL D
  - Systematic Capability and Hardware Integrity up to ASIL D
- Input Voltage Range
  - 5 to 36 V for Initial Power Up
  - 3.5 to 36 V Full Functionality After Initial Power Up, limited operation to 2.3 V
- Output Supply Rails
  - Synchronous Buck-Boost Preregulator with configurable Spread-Spectrum, 4.3 V, 5 V, or 6 V and low IQ mode with the following options:
    - 2.8 A in Buck Mode (Option 0 Variant)
    - 1.5 A in Buck Mode (Option 1 Variant)
  - Four LDOs: 1.0 V to 1.8 V in 50 mV steps, 2.5 V, 3.0 V, 3.3 V, 5 V, bypass or voltage monitor mode. Each LDO with Independent Configurable Current Limit.
    - LDO1 and LDO2: Low IQ, up to 600 mA
    - LDO3 and LDO4: Low Noise, Low IQ, 1% Accuracy, up to 200 mA
  - Two Protected LDOs for Sensor or Peripheral Supplies, PLDO1 and PLDO2
    - Configurable for Tracking Mode or Fixed Output: 1.0 V to 1.8 V in 50 mV steps, 2.5 V, 3.0 V, 3.3 V or 5 V up to 200 mA
    - Short-to-Chassis ( $-2$  V) and Supply (+36 V) Protection
- Power Sequence Control:
  - Configurable power-up and down sequences (NVM default including output voltages)
  - Output rails, external voltage monitor and external enable signals can be included
- Monitoring, Protection and Diagnostics
  - Undervoltage and Overvoltage Monitoring on All Regulator Outputs, Battery Voltage, and Internal Supplies

- Two External Voltage Monitors (Pins)
- All Regulator Outputs Protected with Independent Current Limit
- All Regulators Protected with Independent Overtemperature Prewarning and Shutdown
- Watchdog: Configurable for Open and Close Window or Question-Answer
- Error Signal Monitor (ESM) for Monitoring MCU Error Output (PWM and Level Modes)
- SAFE State for Device and System Protection
- Clock Monitor for Internal Oscillators
- Analog and Logic Built-In Self-Test (BIST)
- CRC on Non-Volatile Memory (NVM), Device Configuration Registers, and SPI Communication
- Diagnostic Output Pin: Multiplexes Analog and Digital Signals to MCU ADC and Input
- Compare Module: 2 Channels Configurable as General Purpose Comparators or up to 4 Channels of Voltage Monitoring
- Timer (Low IQ) for Wake-Up and Measurement, 64- $\mu\text{s}$  to 203.6 Days
- SPI for Configuration, Status and Error Reporting
- Reset Output (NRST), Two Configurable Safing Outputs (SAFE\_OUTx) for System Safe State on Detected Faults Interrupt Output (NINT), and Power Good Output (PGOOD)
- Two Configurable Wake-up Pins (WAKEx)
- 48-Pin HTSSOP PowerPAD™ IC Package

## 2 Applications

- Safety-Relevant Automotive Applications

## 3 Description

The TPS65386x-Q1 device is a multirail power supply designed to supply microcontrollers, sensors, transceivers and peripherals in safety relevant applications.

### Package Information

PART NUMBER <sup>(2)</sup>	PREREGULATOR	PACKAGE <sup>(1)</sup>
TPS653860-Q1	Buck-Boost 2.8 A	DCA (HTSSOP, 48)
TPS653861-Q1	Buck-Boost 1.5 A	DCA (HTSSOP, 48)

- (1) For all available packages and more information, see [Section 6, Mechanical Packaging and Orderable Information](#) at the end of the data sheet.
- (2) For additional details on device sub-family variants and NVM default configuration options, see Device Comparison Table.



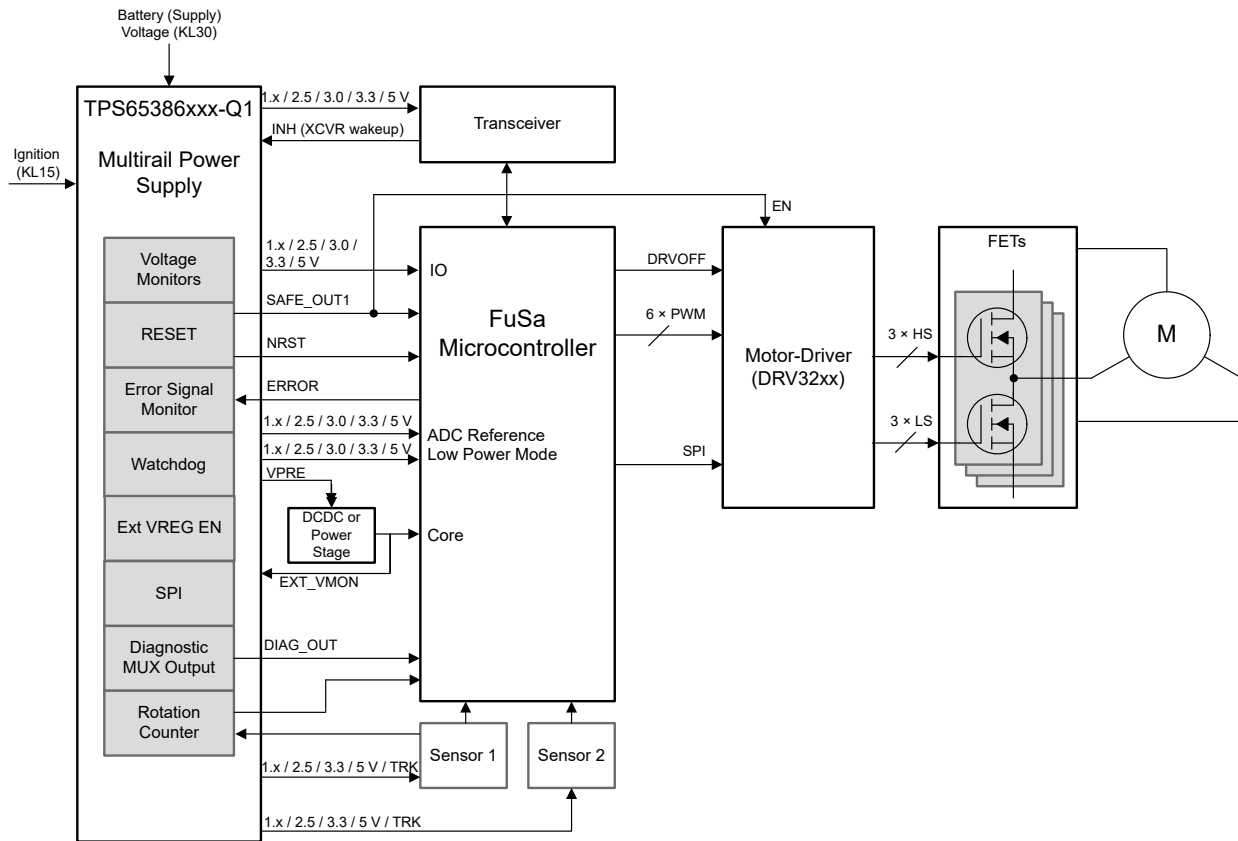


Figure 3-1. Typical Application Diagram

ADVANCE INFORMATION

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## 4 Device and Documentation Support

### 4.1 Documentation Support

#### 4.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, full data sheet, application notes and functional safety information such as the Functional Safety Manual for TPS65386xyz-Q1 Multirail Power Supply, are available under non-disclosure agreement. Request more information using the link on the [www.ti.com](http://www.ti.com) product folder, [TPS653860-Q1](#) or [TPS653861-Q1](#).
- Texas instruments, [A Guide to Board Layout for Best Thermal Resistance for Exposed Packages application report](#)
- Texas instruments, [PowerPAD™ Made Easy application report](#)
- Texas instruments, [PowerPAD™ Thermally Enhanced Package application report](#)

#### 4.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

### 4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 4.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 4.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments. All trademarks are the property of their respective owners.

### 4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Table 5-1. Revision History**

DATE	REVISION	NOTES
October 2023	*	Advance Information

## 6 Mechanical, Packaging, and Orderable Information

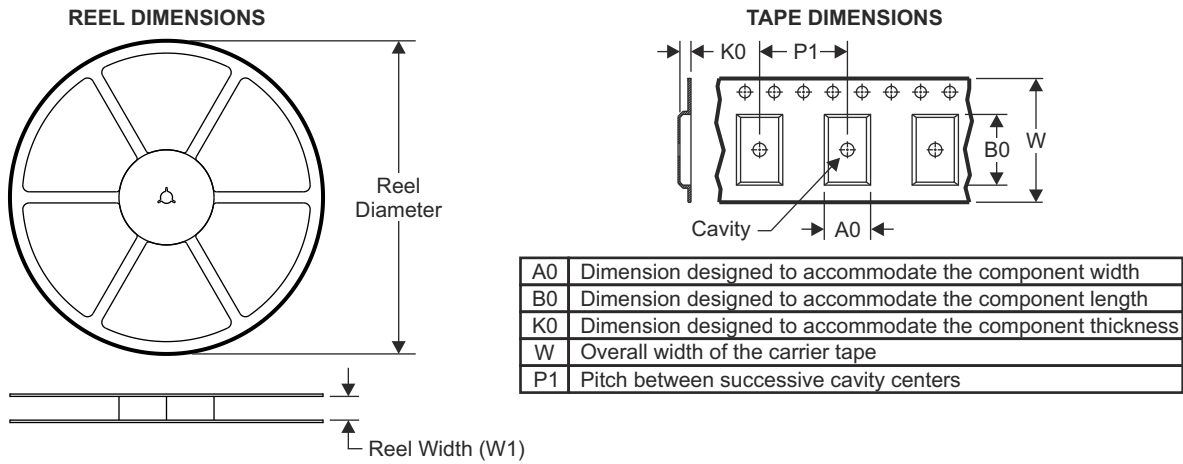
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 6.1 Package Option Addendum

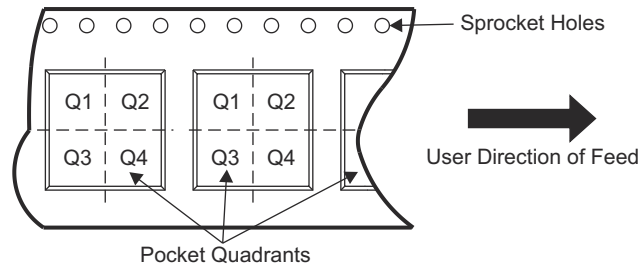
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4) (5)
See Device TRM for Grade 1 Device	See Device TRM	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NiPdAu	Level-3-260C-168 HR	-40 to 125	See Device TRM
See Device TRM for Grade 0 Device	See Device TRM	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NiPdAu	Level-3-260C-168 HR	-40 to 150	See Device TRM

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.  
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 In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### 6.2 Tape and Reel Information



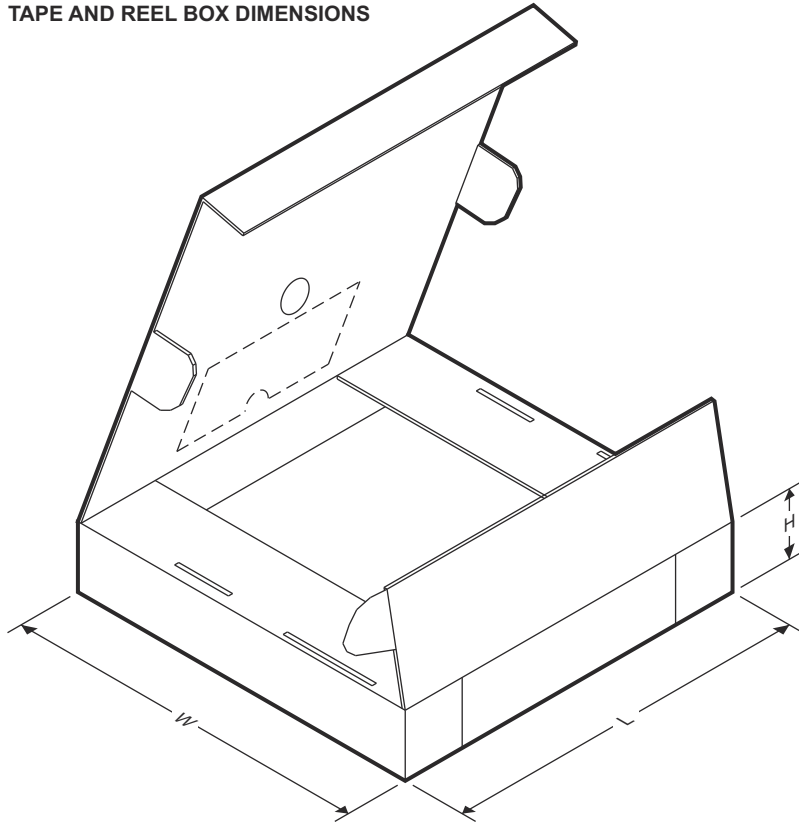
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
O386003QDCARQ1	HTSSOP	DCA	48	2000	330	24.4	8.6	15.8	1.8	12	24	1

**ADVANCE INFORMATION**

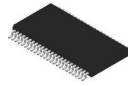
TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6538600QDCARQ1	HTSSOP	DCA	48	2000	367	367	45
TPS6538600EDCARQ1	HTSSOP	DCA	48	2000	367	367	45



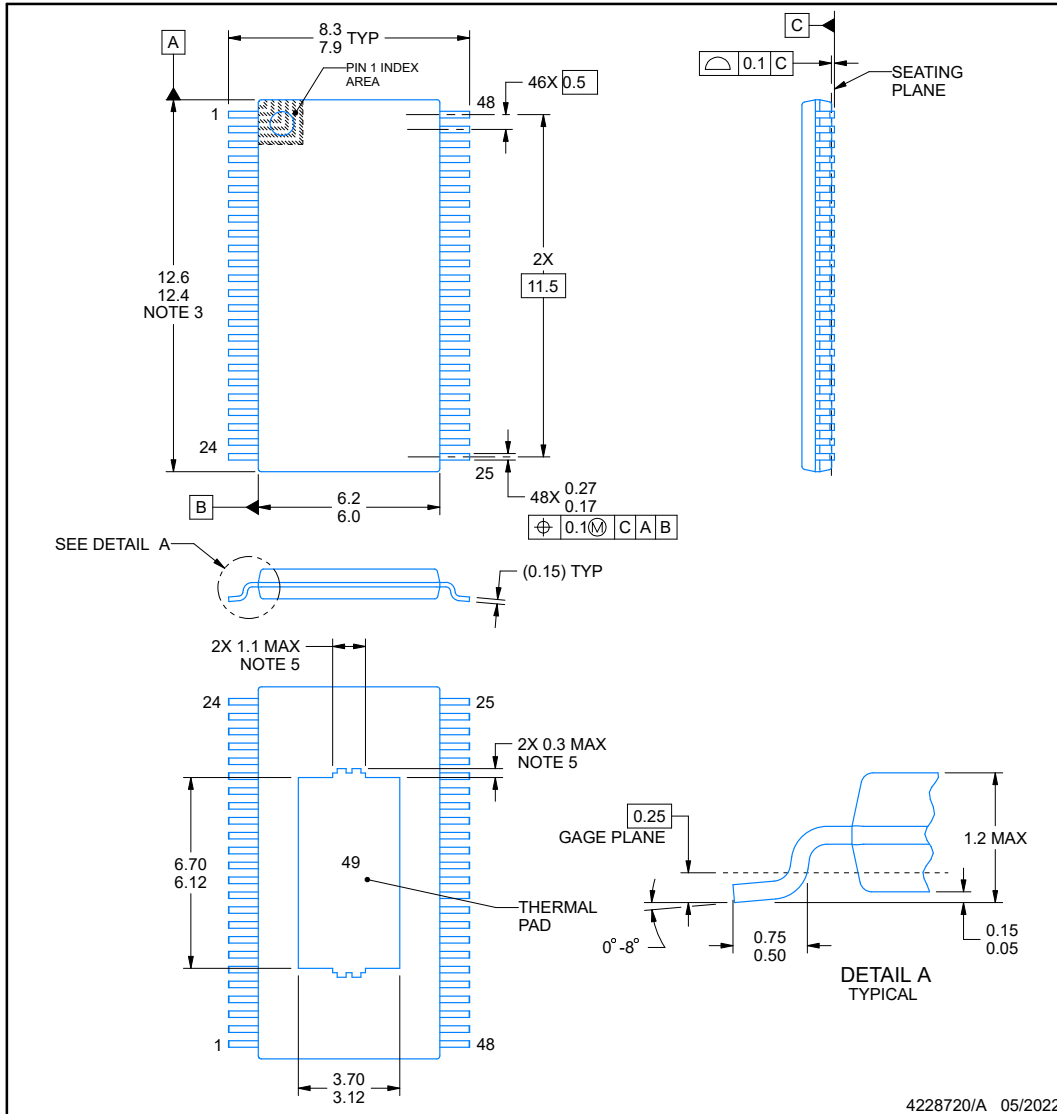


**PACKAGE OUTLINE**

**DCA0048J**

**PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

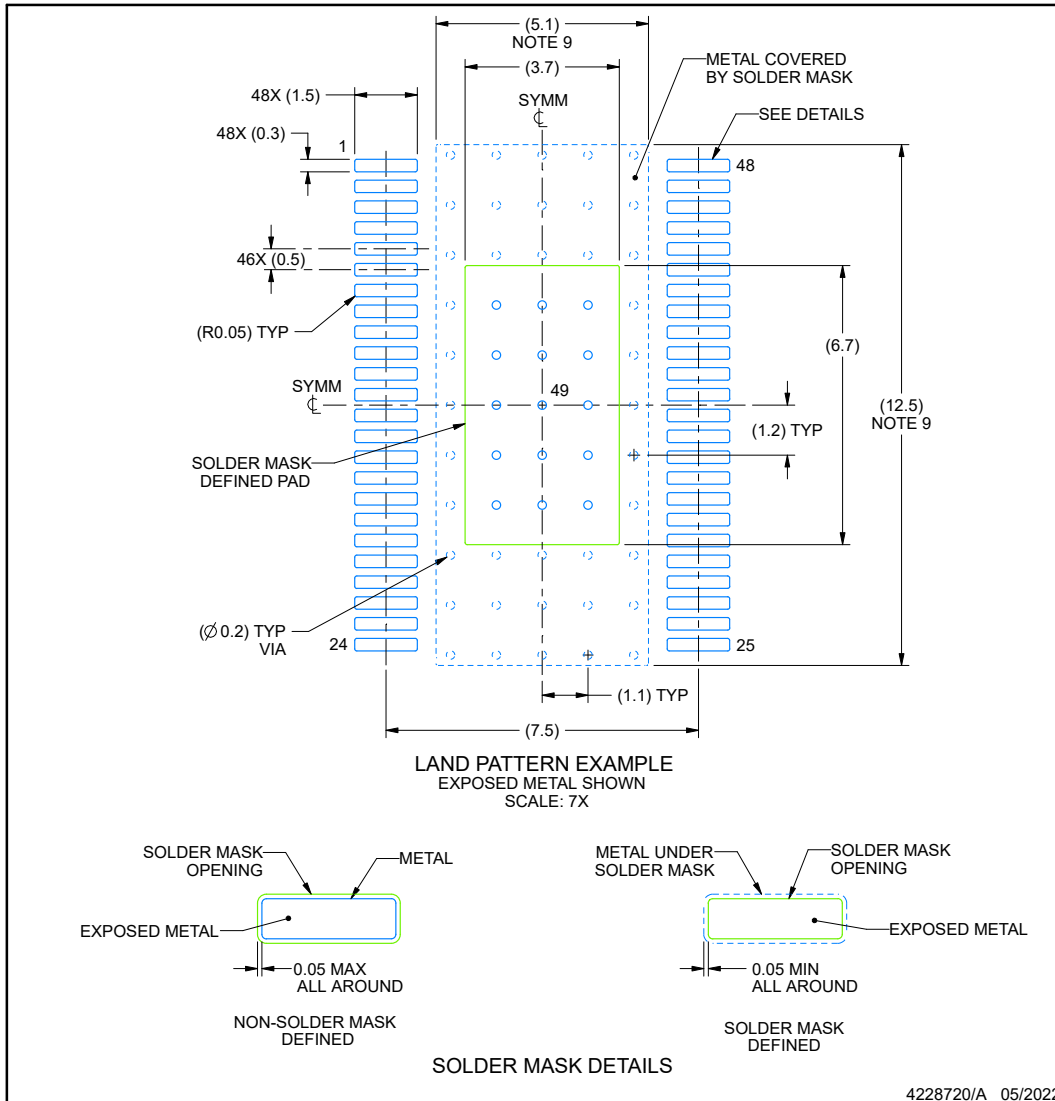
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

## EXAMPLE BOARD LAYOUT

DCA0048J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

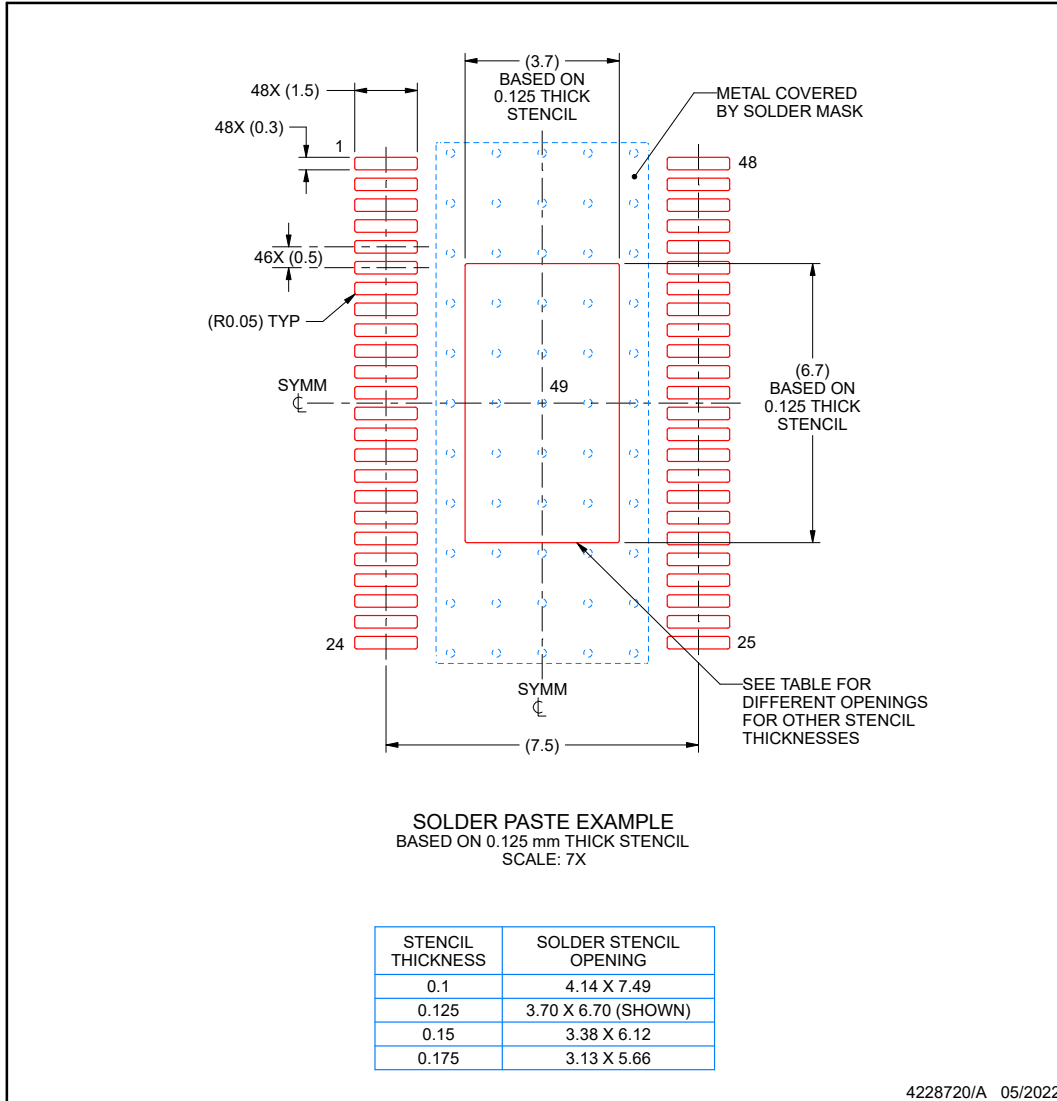
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN**

**DCA0048J**

**PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

REVISIONS							
REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER			
A	RELEASE NEW DRAWING	2199680	05/10/2022	J. MILLER / K. SINCERBOX			
		SCALE	SIZE	4228720		REV	PAGE
			A			A	5 OF 5

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PO386003QDCARQ1	ACTIVE	HTSSOP	DCA	48	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## GENERIC PACKAGE VIEW

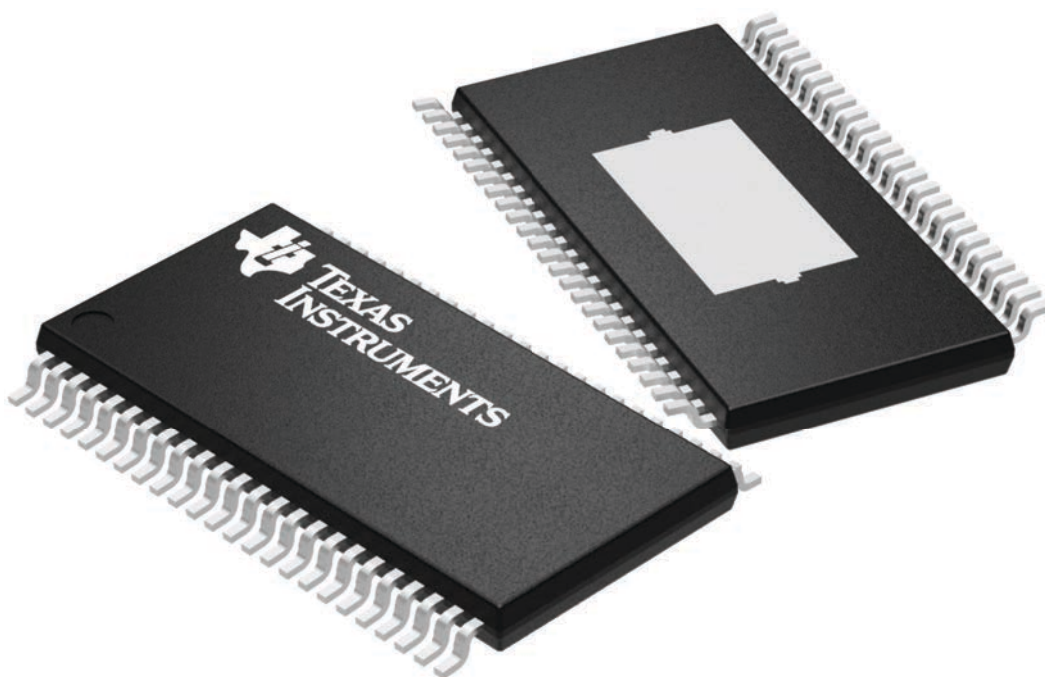
**DCA 48**

**HTSSOP - 1.2 mm max height**

12.5 x 6.1, 0.5 mm pitch

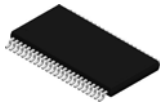
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224608/A

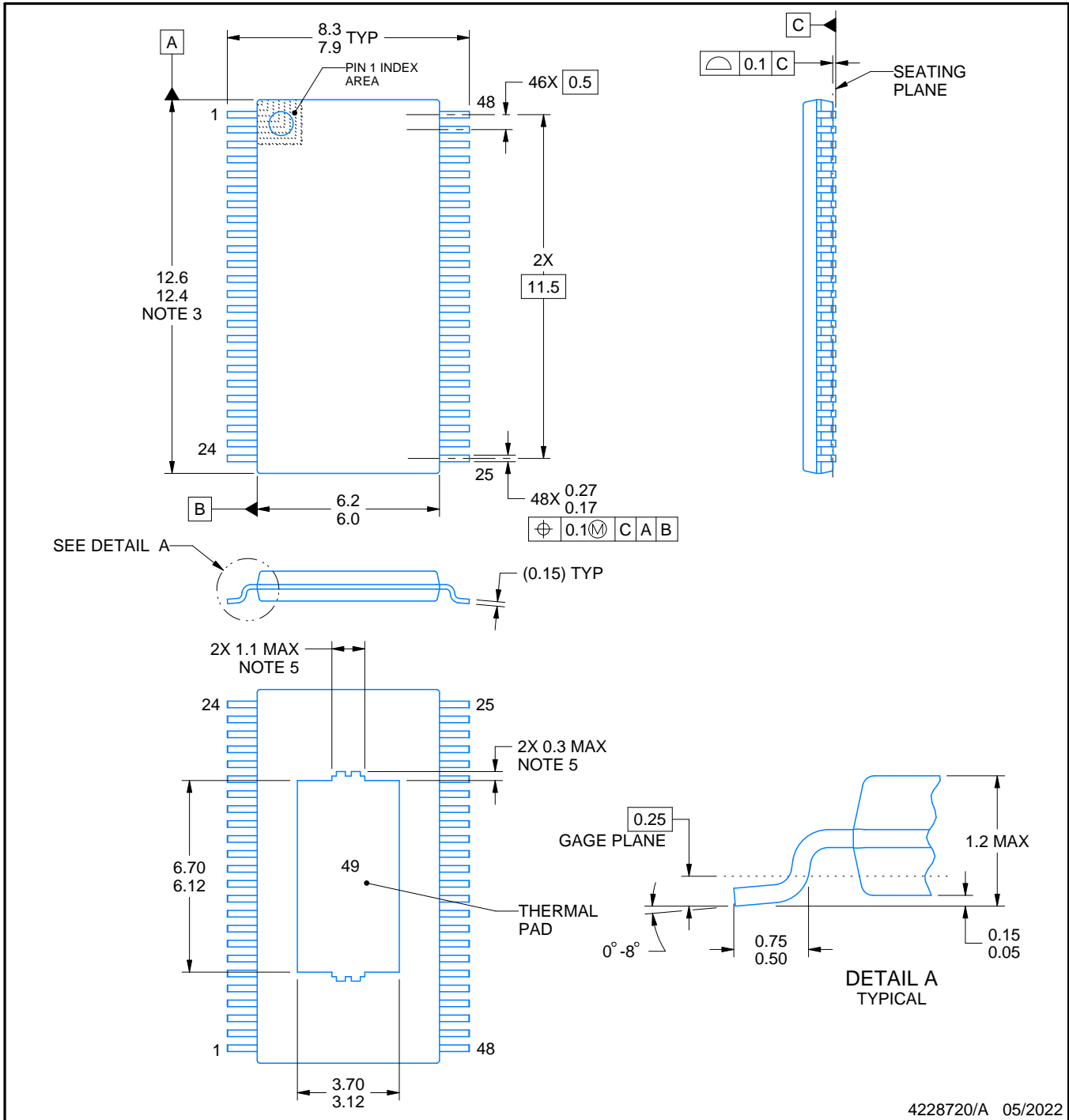
DCA0048J



# PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4228720/A 05/2022

NOTES:

PowerPAD is a trademark of Texas Instruments.

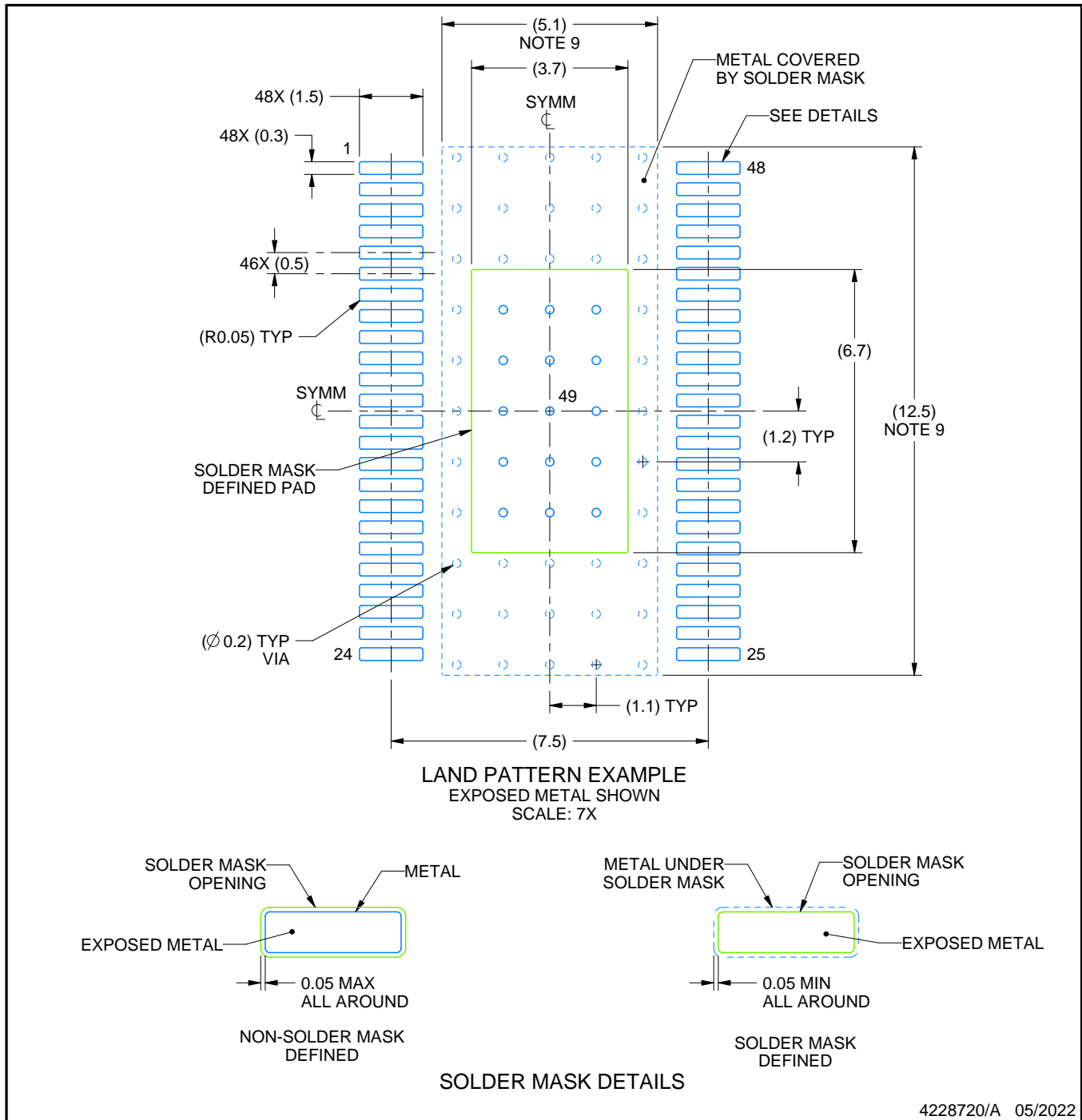
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DCA0048J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

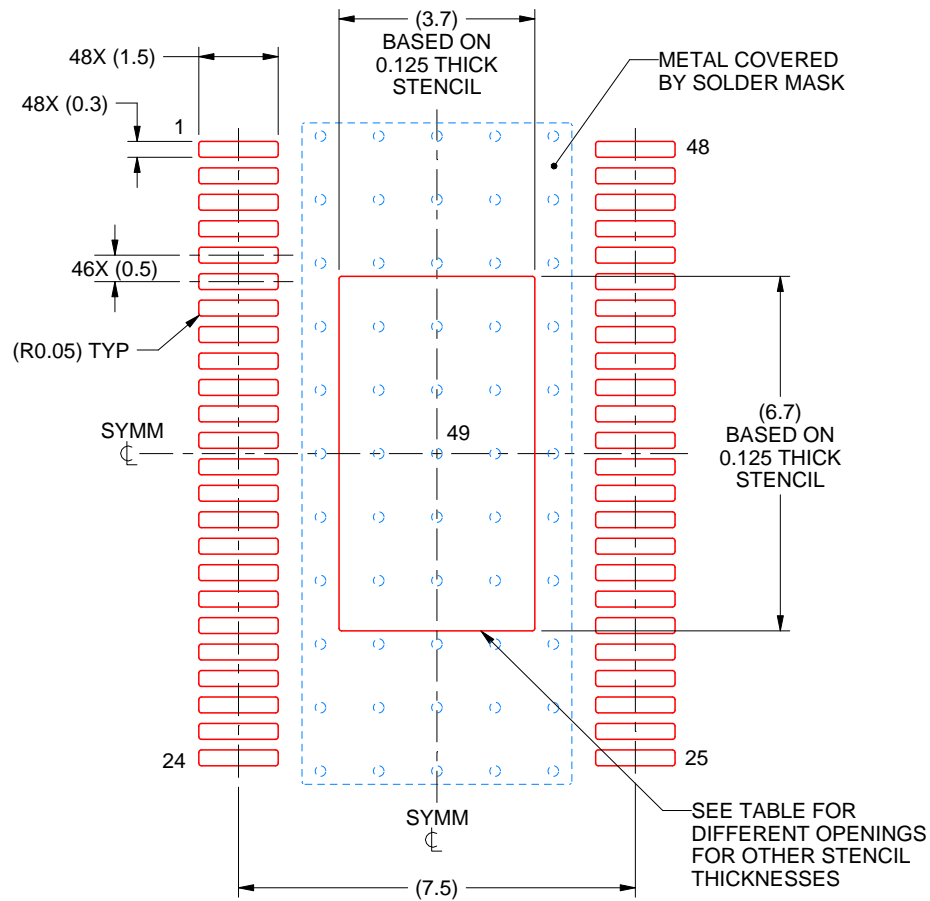


# EXAMPLE STENCIL DESIGN

DCA0048J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 7X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.14 X 7.49
0.125	3.70 X 6.70 (SHOWN)
0.15	3.38 X 6.12
0.175	3.13 X 5.66

4228720/A 05/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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