TRS213 5V Multichannel RS-232 Line Driver and Receiver with ±15kV ESD Protection

1 Features

- ESD Protection for RS-232 bus pins
  - ±15kV Human-body model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates at 5V V_{CC} supply
- Four drivers and five receivers
- Operates up to 120kbit/s
- Low supply current in shutdown mode: 15µA typical
- External Capacitors: 4 × 0.1µF
- Designed to be interchangeable with industry standard '213 devices
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- Battery-powered systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held equipment

3 Description

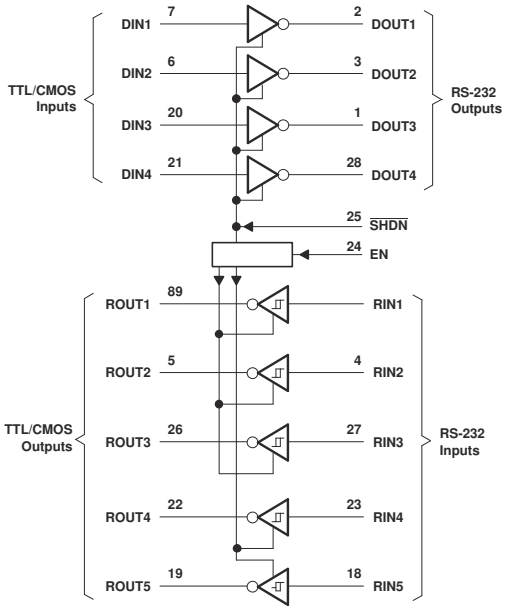
The TRS213 device consists of four line drivers, five line receivers, and a dual charge-pump circuit with ±15kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5V supply. The devices operate at data signaling rates up to 120kbit/s and a maximum of 30V/µs driver output slew rate.

The TRS213 has an active-low shutdown ($\overline{SHDN}$) and an active-high enable control (EN). In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V– is pulled to GND, and the transmitter outputs are disabled. This reduces supply current typically to 1µA. Two receivers of the TRS213 are active during shutdown.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRS213	DB (SSOP)	10.2 mm x 7.8mm
	DW (SOIC)	17.9mm x 10.3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

DB, DW, OR PW PACKAGE
(TOP VIEW)

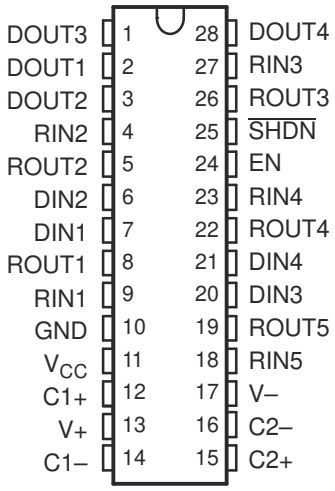


Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DOUT3	1	O	RS-232 driver outputs
DOUT1	2	O	RS-232 driver outputs
DOUT2	3	O	RS-232 driver outputs
RIN2	4	I	RS-232 receiver input
ROUT2	5	O	Receiver output
DIN2	6	I	Driver inputs
DIN1	7	I	Driver inputs
ROUT1	8	O	Receiver output
RIN1	9	I	RS-232 receiver input
GND	10	-	Ground
V_{CC}	11	-	Supply voltage
C1+	12	-	Positive terminal of the voltage-doubler charge-pump capacitor
V+	13	-	Positive charge pump output voltage
C1−	14	-	Negative terminal of the voltage-doubler charge-pump capacitor
C2+	15	-	Positive terminal of the voltage-doubler charge-pump capacitor
C2−	16	-	Negative terminal of the voltage-doubler charge-pump capacitor
V−	17	-	Negative charge pump output voltage
RIN5	18	I	RS-232 receiver input
ROUT5	19	O	Receiver output
DIN3	20	I	Driver inputs
DIN4	21	I	Driver inputs
ROUT4	22	O	Receiver output
RIN4	23	I	RS-232 receiver input

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	24	I	Active high enable
$\overline{\text{SHDN}}$	25	I	Active low shutdown
ROUT3	26	O	Receiver output
RIN3	27	I	RS-232 receiver input
DOUT4	28	O	RS-232 driver outputs

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	6	V
V+	Positive charge-pump voltage range(2)		V_{CC} – 0.3	14	V
V–	Negative charge-pump voltage range(2)		0.3	–14	V
V_I	Input voltage range	Drivers	–0.3	V+ + 0.3	V
		Receivers (DB Package)		±25	V
		Receivers (DW Package)		±30	V
V_O	Output voltage range	Drivers	V– – 0.3	V+ + 0.3	V
		Receivers	–0.3	V_{CC} + 0.3	V
DOUT	Short-circuit duration			Continuous	
T_J	Operating virtual junction temperature			150	C°
T_{stg}	Storage temperature range		–65	150	C°

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 Recommended Operating Conditions

See Figure 6-4,and note (1)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
	Control high-level input voltage	EN, $\overline{SHDN}$	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, EN, $\overline{SHDN}$			0.8	V
V_I	Driver and control input voltage	DIN, EN, $\overline{SHDN}$	0		5.5	V
	Receiver input voltage	RIN (DB package)	–25		25	
		RIN (DW package)	-30		30	V
T_A	Operating free-air temperature	TRS213C	0		70	°C
		TRS213I	–40		85	

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

5.3 Thermal Information

THERMAL METRIC(1)		DW (SOIC) 28 PINS	DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	66.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	33.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	37.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	4.6	°C/W

5.3 Thermal Information (continued)

THERMAL METRIC[1]		DW (SOIC)	DB (SSOP)	UNIT
		28 PINS	28 PINS	
ψ_{JB}	Junction-to-board characterization parameter	37.1	36.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load,	See Figure 8-1		14	20	mA
I_{SHDN}	Shutdown supply current	T_A = 25°C,	See Figure 6-1		15	50	µA

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.5 Electrical Characteristics, Driver

over operating free-air temperature range (unless otherwise noted) (see Figure 6-4,and note (3))

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND		5	9		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND		–5	–9		V
I_{IH}	Control high-level input current	EN, $\overline{SHDN}$ = 5V			3	10	µA
I_{IL}	Driver low-level input current	DIN = 0V			–15	–200	µA
	Control low-level input current	EN, $\overline{SHDN}$ = 0V			–3	–10	
I_{OS} (2)	Short-circuit output current	V_{CC} = 5.5V,	V_O = 0V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V– = 0V,	V_O = ±2V	300			Ω

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V

5.6 Switching Characteristics, Driver

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 50pF to 1000pF, One DOUT switching,	R_L = 3kΩ to 7kΩ, See Figure 6-3	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500pF, All drivers loaded,	R_L = 3kΩ, See Figure 6-3		2		µs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500pF, All drivers loaded,	R_L = 3kΩ, See Figure 6-3		2		µs
$t_{sk(p)}$	Pulse skew(3)	C_L = 150pF to 2500pF, See Figure 6-3	R_L = 3kΩ to 7kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 6-2)	C_L = 50pF to 1000pF, V_{CC} = 5V	R_L = 3kΩ to 7kΩ,	3	6	30	V/µs

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(3) Pulse skew is defined as (t_{PLH} – t_{PHL}) of each channel of the same device.

5.7 ESD Protection, Driver

over operating free-air temperature range (unless otherwise noted)

PIN	TEST CONDITIONS	TYP	UNIT
DOUT	Human-Body Model	±15	kV

5.8 Electrical Characteristics, Receiver

over operating free-air temperature range (unless otherwise noted) (see Figure 8-1), and see note(3)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA			V_{CC} – 0.4		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6mA				0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5V, T_A = 25°C	Active mode		1.7	2.4	V
			Shutdown mode (R4–R5)		1.5	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5V, T_A = 25°C	Active mode	0.8	1.2		V
			Shutdown mode (R4–R5)	0.6	1.5		
V_{hys} (2)	Input hysteresis (V_{IT+}, $V_{IT–}$)	V_{CC} = 5V			0.5	1	V
r_I	Input resistance	V_{CC} = 5V, T_A = 25°C		3	5	7	kΩ
	Output leakage current	EN = 0V, 0 ≤ ROUT ≤ V_{CC}, R1–R3			±0.05	±10	μA

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) No hysteresis in shudown mode
(3) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5 V.

5.9 Switching Characteristics, Receiver

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150pF,	See Figure 6-4	$\overline{SHDN}$ = V_{CC}		0.5	10	μs
				$\overline{SHDN}$ = 0V, R4–R5		4	40	
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150pF,	See Figure 6-4			0.5	10	μs
t_{en}	Output enable time	C_L = 150pF,	See Figure 6-5			600		ns
t_{dis}	Output disable time	C_L = 150pF,	See Figure 6-5			200		ns

(1) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.10 ESD Protection, Receiver

over operating free-air temperature range (unless otherwise noted)

PIN	TEST CONDITIONS	TYP	UNIT
RIN	Human-Body Model	±15	kV

6 Parameter Measurement Information

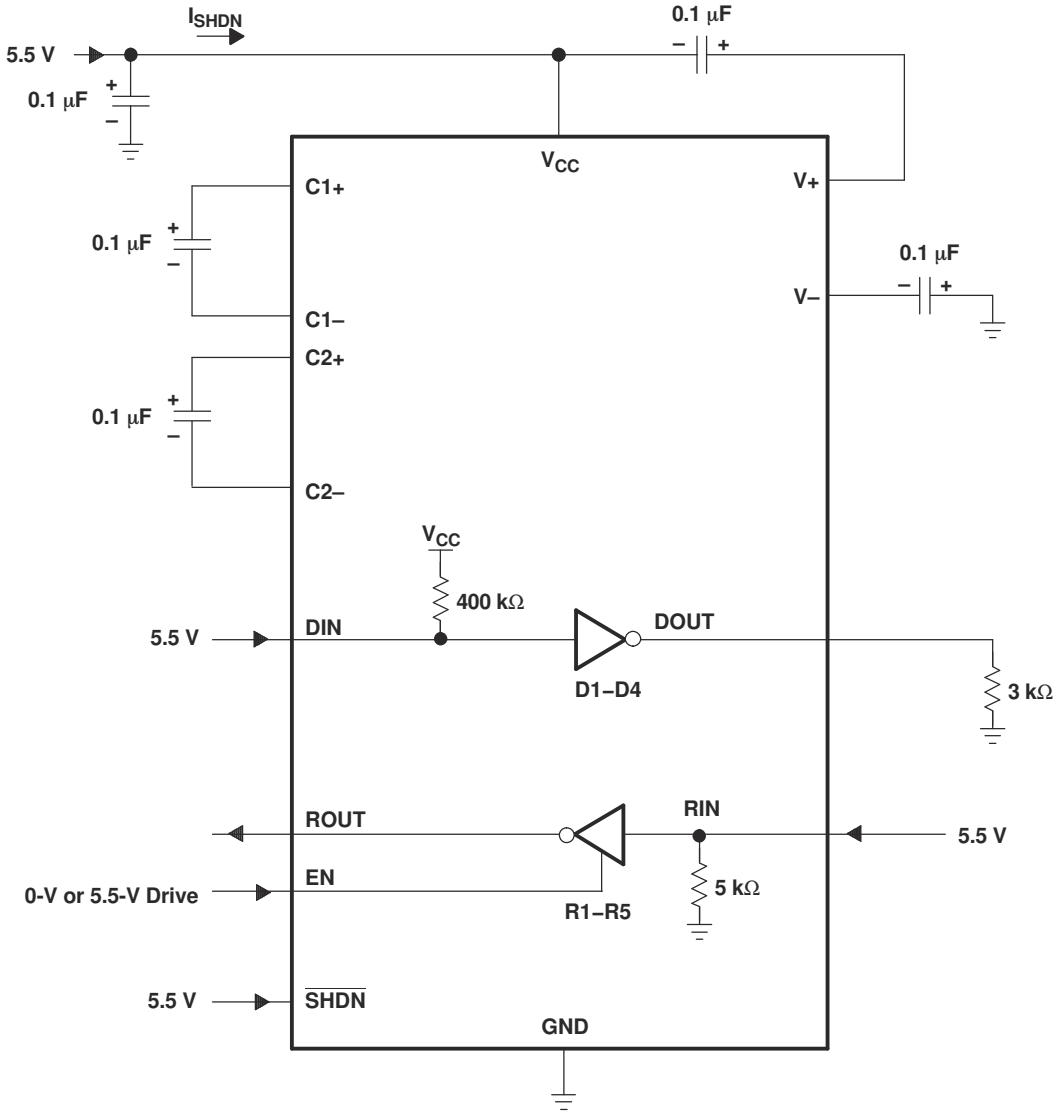
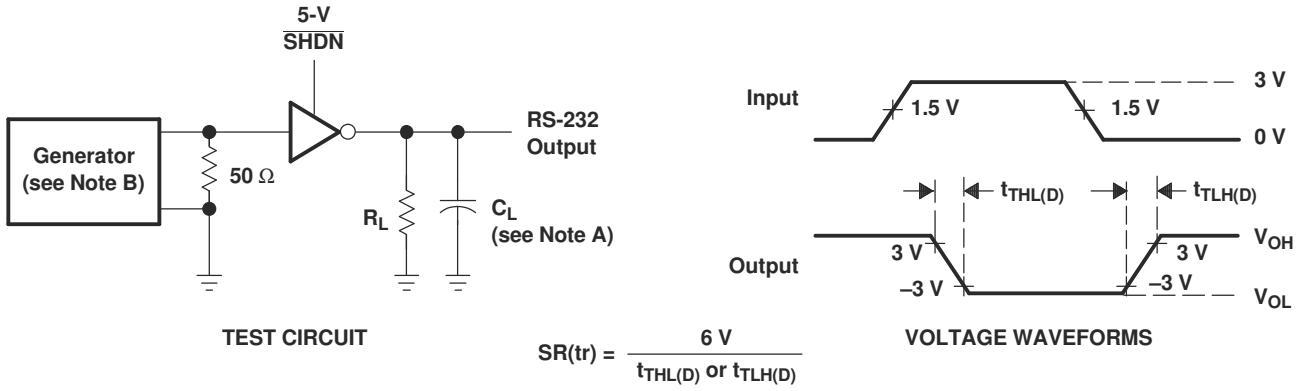
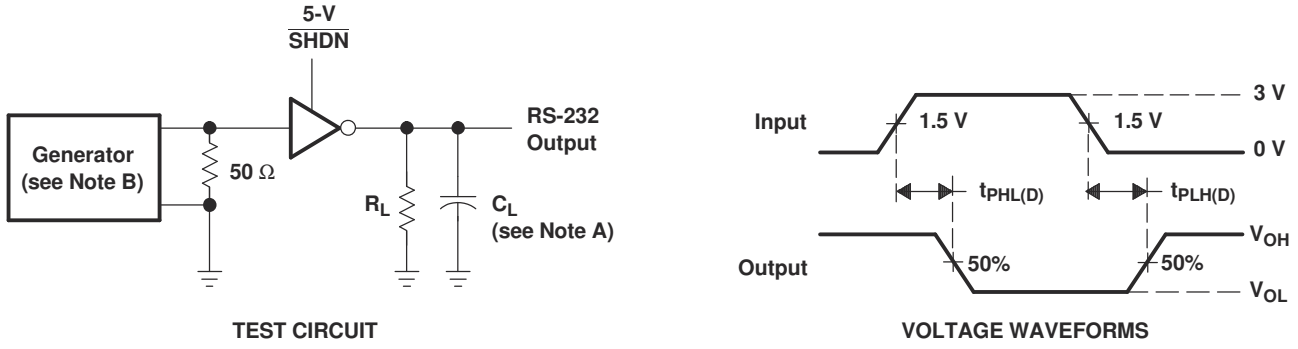


Figure 6-1. Shutdown Current Test Circuit



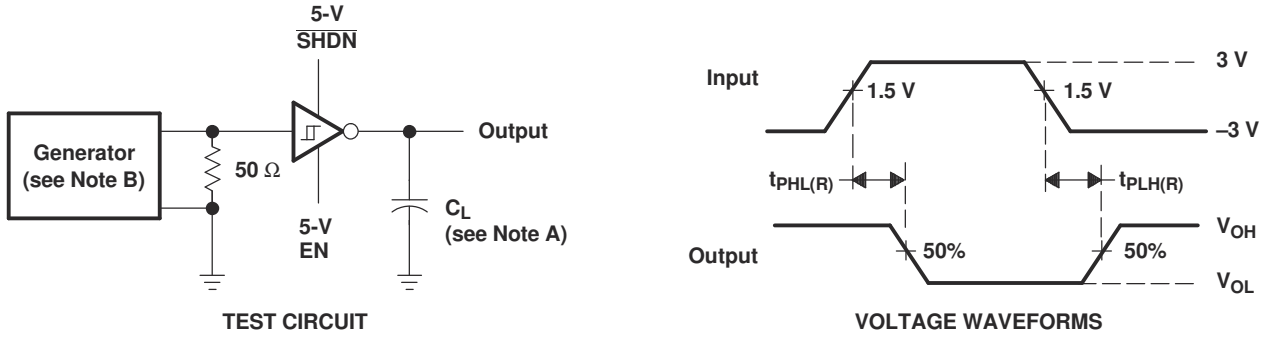
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-2. Driver Slew Rate



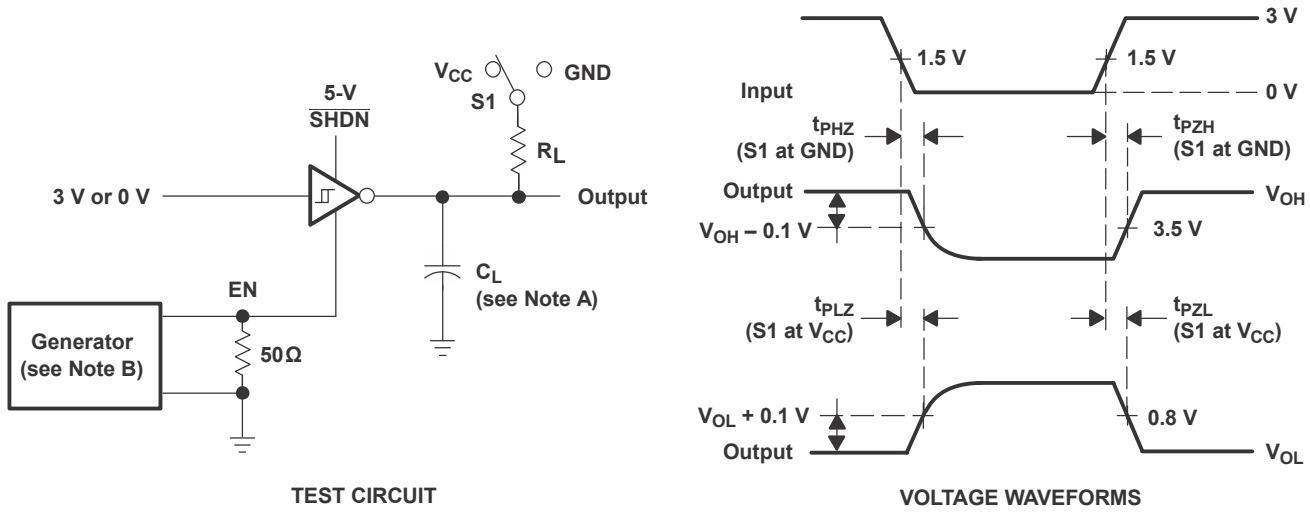
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-3. Driver Pulse Skew and Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-4. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-5. Receiver Enable and Disable Times

7 Functional Modes

Table 7-1. Function Table

INPUTS		DRIVER D1–D4	RECEIVER		DEVICE STATUS
$\overline{SHDN}$	EN		R1–R3	R4–R5	
L	L	Z	Z	Z	Shutdown
L	H	Z	Z	Active(1)	Shutdown
H	L	All active	Z	Z	Normal operation
H	H	All active	Active	Active	Normal operation

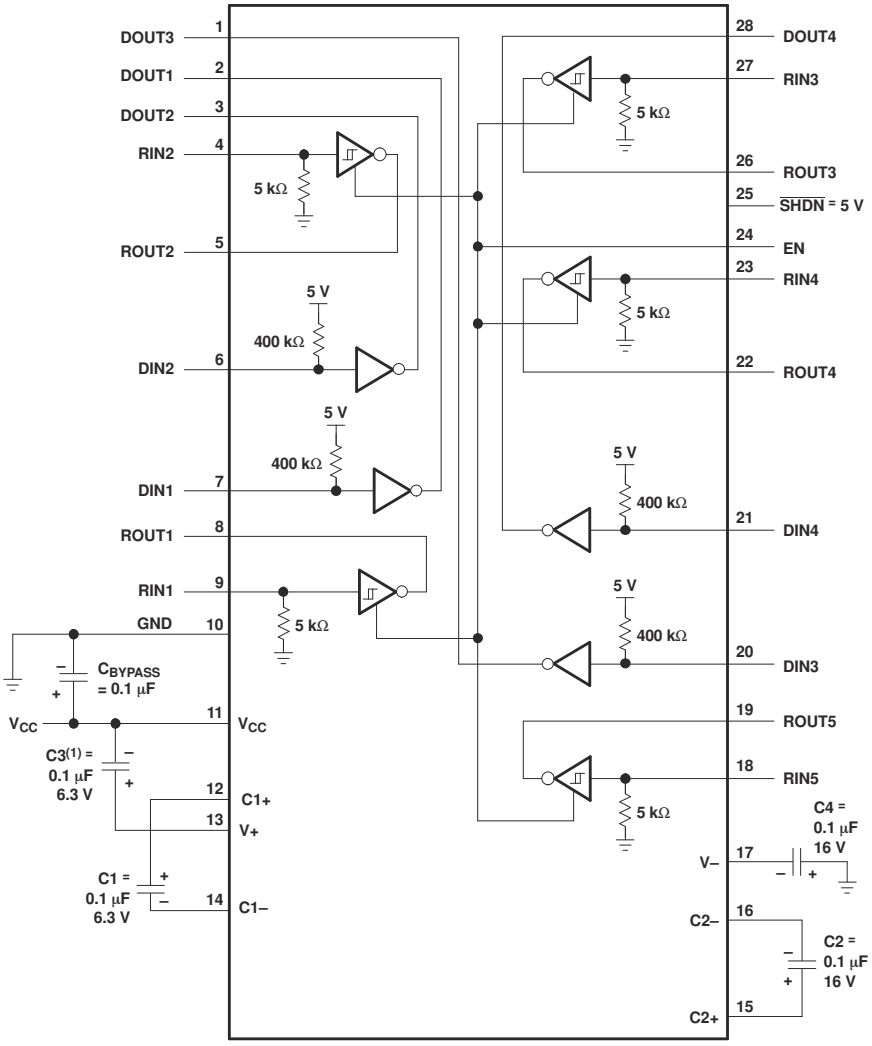
(1) See the V_{IT+} and V_{IT-} change in the *Electrical Characteristics* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application



(1) C3 can be connected to V_{CC} or GND.
NOTES: A. Resistor values shown are nominal.
B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8-1. Typical Operating Circuit and Capacitor Values

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2007) to Revision A (July 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the DB package Input voltage range for Receivers from ±30V to ±25V in the *Absolute Maximum Ratings* and the *Recommended Operating Conditions*	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS213CDBR	OBSOLETE	SSOP	DB	28		TBD	Call TI	Call TI	0 to 70	TRS213C	
TRS213IDB	OBSOLETE	SSOP	DB	28		TBD	Call TI	Call TI	-40 to 85	TRS213I	
TRS213IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I	Samples
TRS213IDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

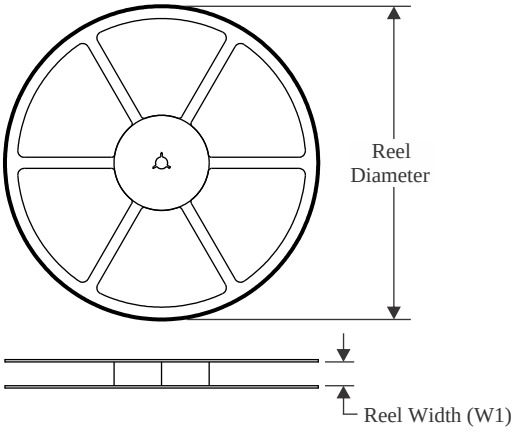
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

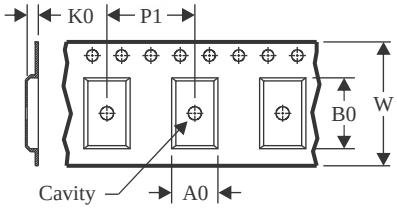
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

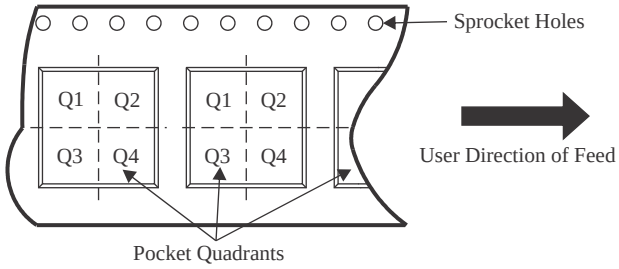


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

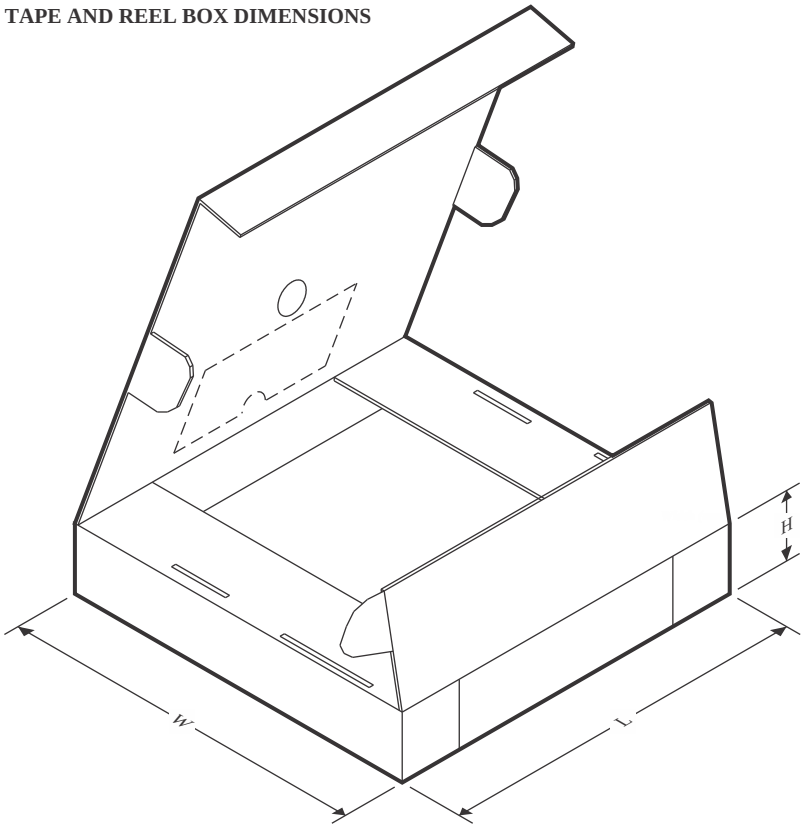
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS213IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS213IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS213IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

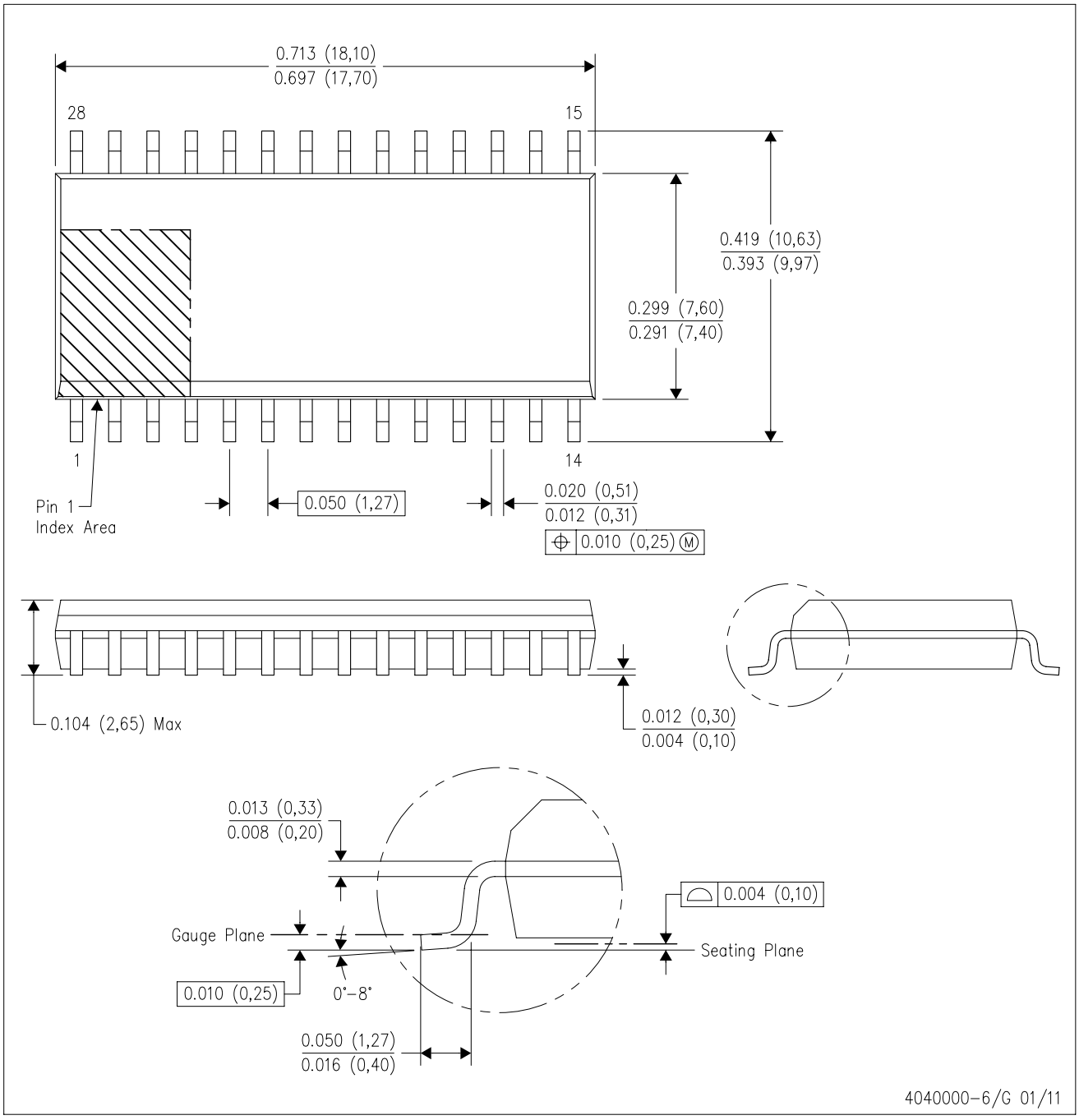
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS213IDBR	SSOP	DB	28	2000	353.0	353.0	32.0
TRS213IDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS213IDWR	SOIC	DW	28	1000	350.0	350.0	66.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



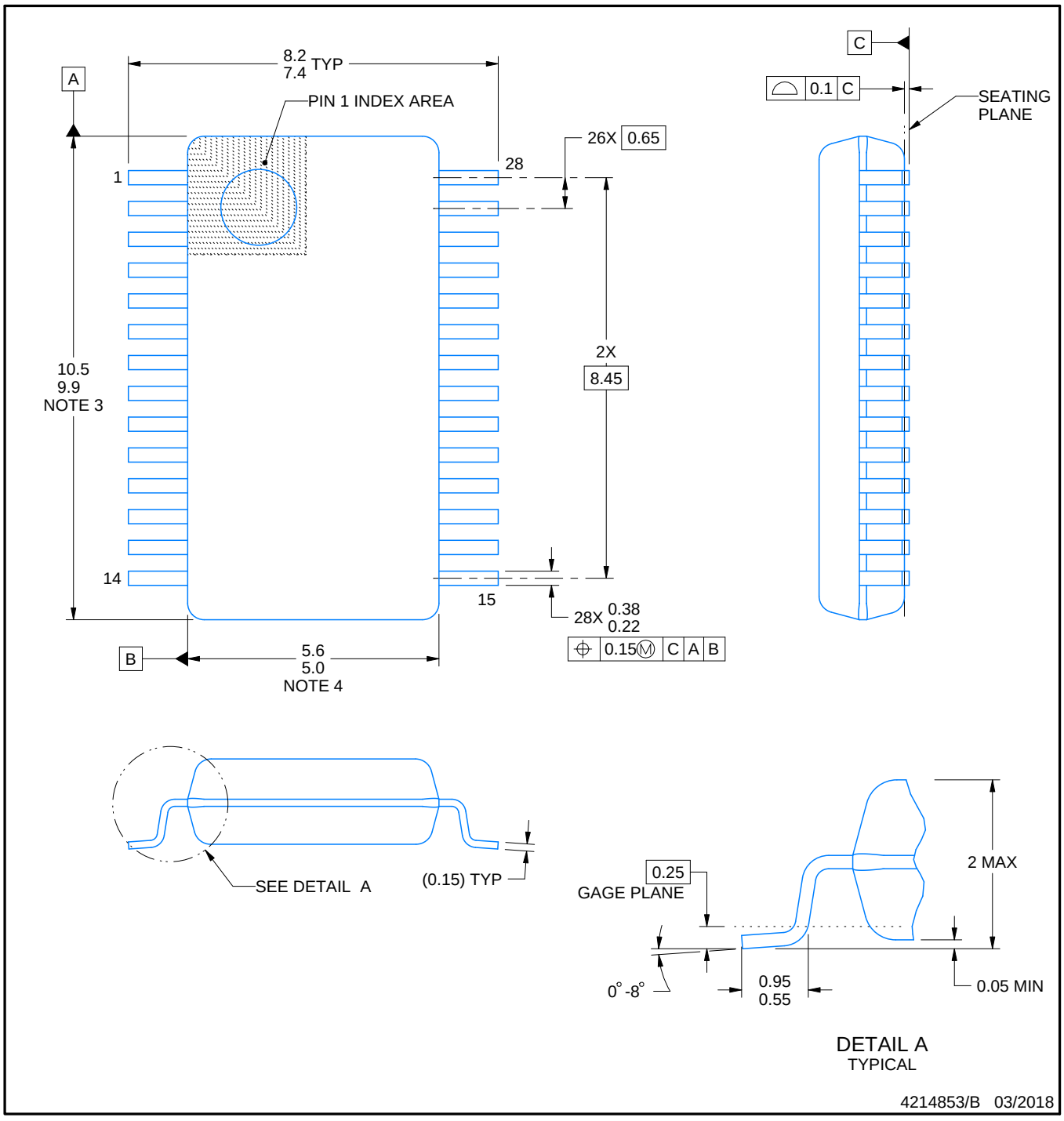
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PACKAGE OUTLINE

DB0028A

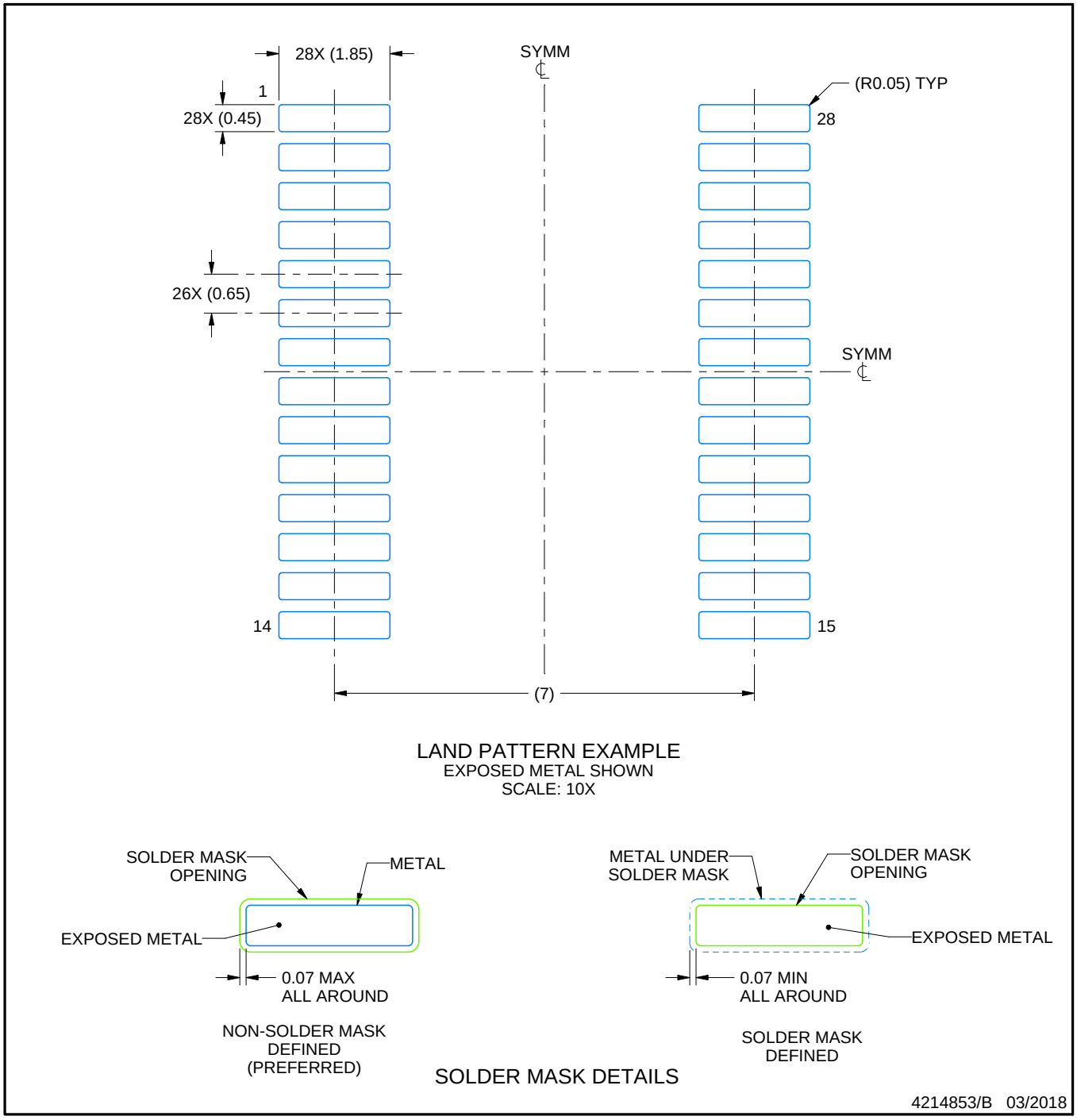
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



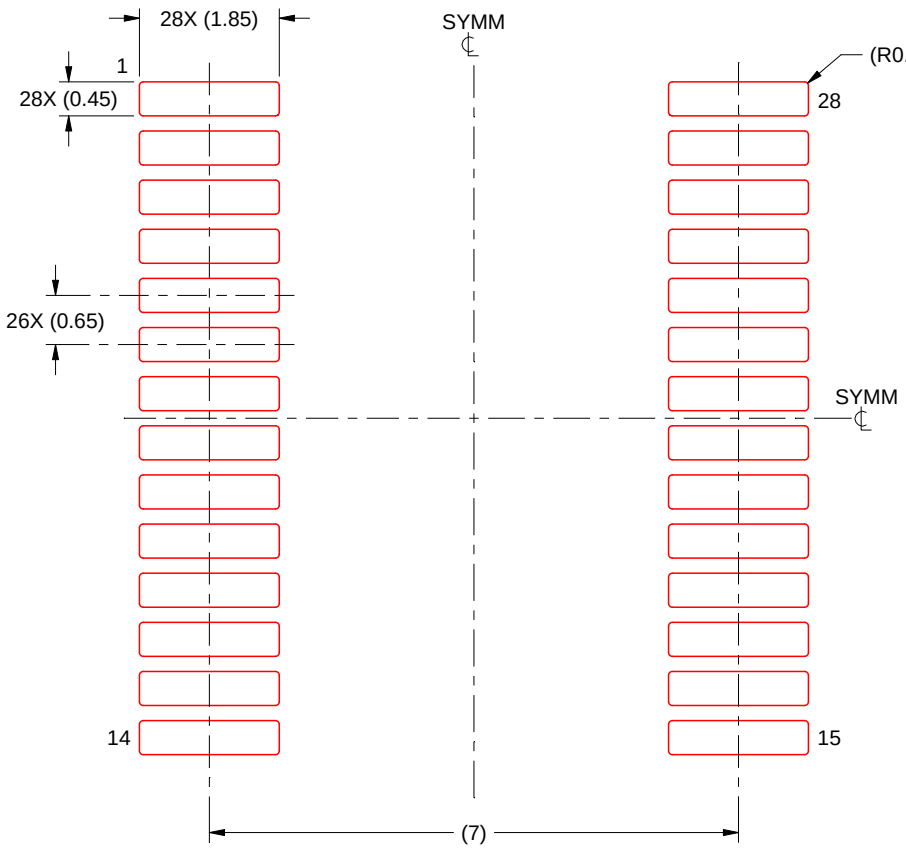
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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