TRS213E Multichannel 120kbps RS-232 Line Driver and Receiver with ±9V output and ±15kV IEC ESD Protection

1 Features

- ESD Protection for RS-232 bus pins
  - ±15kV Human-body model (HBM)
  - ±8kV IEC61000-4-2, Contact discharge
  - ±15kV IEC61000-4-2, Air-gap discharge
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates at 5V V_{CC} supply
- Four drivers and five receivers
- Operates up to 120kbit/s
- Low supply current in shutdown mode: 15µA typical
- Designed to be interchangeable with industry standard '213 devices
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- Battery-powered systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held equipment

3 Description

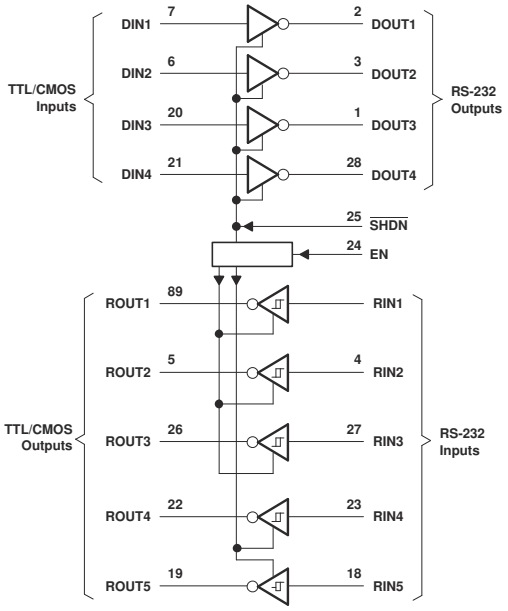
The TRS213E consists of four line drivers, five line receivers, and a dual charge-pump circuit with ±15kV IEC ESD protection on the RS-232 bus pins. The device meets the requirements of TIA/EIA-232-F, and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5V supply. The devices operate at data signaling rates up to 120kbit/s and a maximum of 30V/µs driver output slew rate.

The TRS213E has an active-low shutdown ($\overline{SHDN}$) and an active-high enable control (EN). In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V– is pulled to GND, and the transmitter outputs are disabled. This reduces supply current typically to 1µA. Two receivers of the TRS213E are active during shutdown.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRS213E	SSOP (DB)	10.2mm x 7.8mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

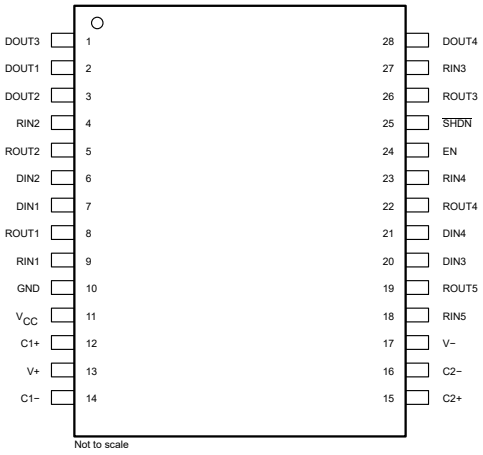


Figure 4-1. DB (SSOP) Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME(2)	NO.		
DOUT3	1	O	RS-232 driver outputs
DOUT1	2		
DOUT2	3		
RIN2	4	I	RS-232 receiver input
ROUT2	5	O	Receiver output
DIN2	6	I	Driver inputs
DIN1	7		
ROUT1	8	O	Receiver output
RIN1	9	I	RS-232 receiver input
GND	10	-	Ground
V_{CC}	11	-	Supply voltage
C1+	12	-	Positive terminal of the voltage-doubler charge-pump capacitor
V+	13	-	Positive charge pump output voltage
C1−	14	-	Negative terminal of the voltage-doubler charge-pump capacitor
C2+	15	-	Positive terminal of the voltage-doubler charge-pump capacitor
C2−	16	-	Negative terminal of the voltage-doubler charge-pump capacitor
V−	17	-	Negative charge pump output voltage
RIN5	18	I	RS-232 receiver input
ROUT5	19	O	Receiver output
DIN3	20	I	Driver inputs
DIN4	21		
ROUT4	22	O	Receiver output
RIN4	23	I	RS-232 receiver input
EN	24	I	Active high enable
$\overline{SHDN}$	25	I	Active low shutdown
ROUT3	26	O	Reciver output
RIN3	27	I	RS-232 receiver input
DOUT4	28	O	RS-232 driver output

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.
(2) DIN pins have 400KΩ internal pull up to V_{CC} .

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V_{S+}	Positive output supply voltage(2)		–0.6	14	V
$V_{S–}$	Negative output supply voltage(2)		–0.3	–14	V
V_I	Input voltage	Driver, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	–0.3	6.3	V
		Receiver	–25	25	
V_O	Output voltage	Driver	–14.3	14.3	V
		Receiver, $\overline{\text{INVALID}}$	–0.3	6.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, non bus (logic/supply) pins(1)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, RS-232 driver output/receiver input pins	±15000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		IEC 61000-4-2, Contact Discharge, RS-232 driver output/receiver input pins(3)	±8000	
		IEC 61000-4-2, Air-Gap Discharge, RS-232 driver output/receiver input pins(4)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) For IEC ESD contact discharge test, 100 pF capacitor was connected to the DOUT3 pin to GND pin and recommended for given ESD performance.
(4) For IEC ESD Air-Gap discharge test, 50Ω series resistor was connected to SHDN and EN pins for hard bound conditions and recommended for given ESD performance when not driven by the microcontroller.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver and control high-level input voltage(1)	DIN, $\overline{\text{SHDN}}$, EN	2			V
V_{IL}	Driver and control low-level input voltage(1)	DIN, $\overline{\text{SHDN}}$, EN			0.8	V
V_I	Driver and control input voltage(1)	DIN, $\overline{\text{SHDN}}$, EN	0		5.5	V
	Receiver input voltage(1)		–25		25	V
T_A	Operating free-air temperature		–40		85	°C

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 mF, C2–µF, C2-C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.4 Thermal Characteristics

THERMAL METRIC(1)		DB (SSOP) 28 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	66.1	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	33.2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	37.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics, Power and Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	All ouputs open		8	20	mA
I_{SHDN}	Supply current	T_A=25°C, EN=High or Low, $\overline{SHDN}$=High		1	10	uA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND, DIN = GND		5	9		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND, DIN = V_{CC}			–9	–5	V
I_{IH}	Control high-level input current (EN and $\overline{SHDN}$)	V_I = V_{CC}			3	10	µA
I_{IL}	Control low-level input current (EN and $\overline{SHDN}$)	V_I at GND		–10	–3		µA
I_{IL}	Low-level input current (DIN pins) Internal pull up present	V_I at GND		–200	–15		µA
I_{OS}	Short-circuit output current(3)	V_{CC} = 5.5 V, Pside ON	V_O = 0 V		10	60	mA
I_{OS}	Short-circuit output current(3)	V_{CC} = 5.5 V, Nside ON	V_O = 0 V	–60	–10		mA
r_o	Output resistance	V_{CC} = 0 V, V_{S+} = 0 V, and $V_{S–}$ = 0 V	V_O = ±2 V	300			Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

5.7 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	3.5			V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V, T_A=25°C		1.7	2.4	V
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5 V, T_A=25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)		0.2	0.5	1	V

5.7 Electrical Characteristics, Receiver (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
r_I	Input resistance	V_I = ±3V to ±25V	3	5	7	kΩ
IOZ	Output leakage current	EN=0V, 0V<ROUT<VCC, R1-R3	–10	0.05	10	uA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

5.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature(unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ to 7 kΩ One DOUT switching	C_L = 50pF to 1000 pF See Figure 1	120	250		kbps
$t_{sk(p)}$	Pulse skew(3)	R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 2500 pF See Figure 2		300		ns
$t_{PLH(D)}$	Propagation delay time, low to high level output	R_L = 3 kΩ	C_L = 2500 pF, all outputs loaded See Figure 2		2		us
$t_{PHL(D)}$	Propagation delay time, high to low level output	R_L = 3 kΩ	C_L = 2500 pF, all outputs loaded See Figure 2		2		us
SR(tr)	Slew rate, transition region	R_L = 3 kΩ to 7 kΩ	C_L = 50pF to 1000 pF	3	6	30	V/us

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as$|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.9 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF		0.5	10	us
t_{PHL}	Propagation delay time, high- to low-level output			0.5	10	us
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF, V_{CC}=5V, T_A=25^{0}C		300		ns
t_{en}	Output enable time	C_L = 150 pF		600		ns
t_{dis}	Output disable time	C_L = 150 pF		200		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as$|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6 Parameter Measurement Information

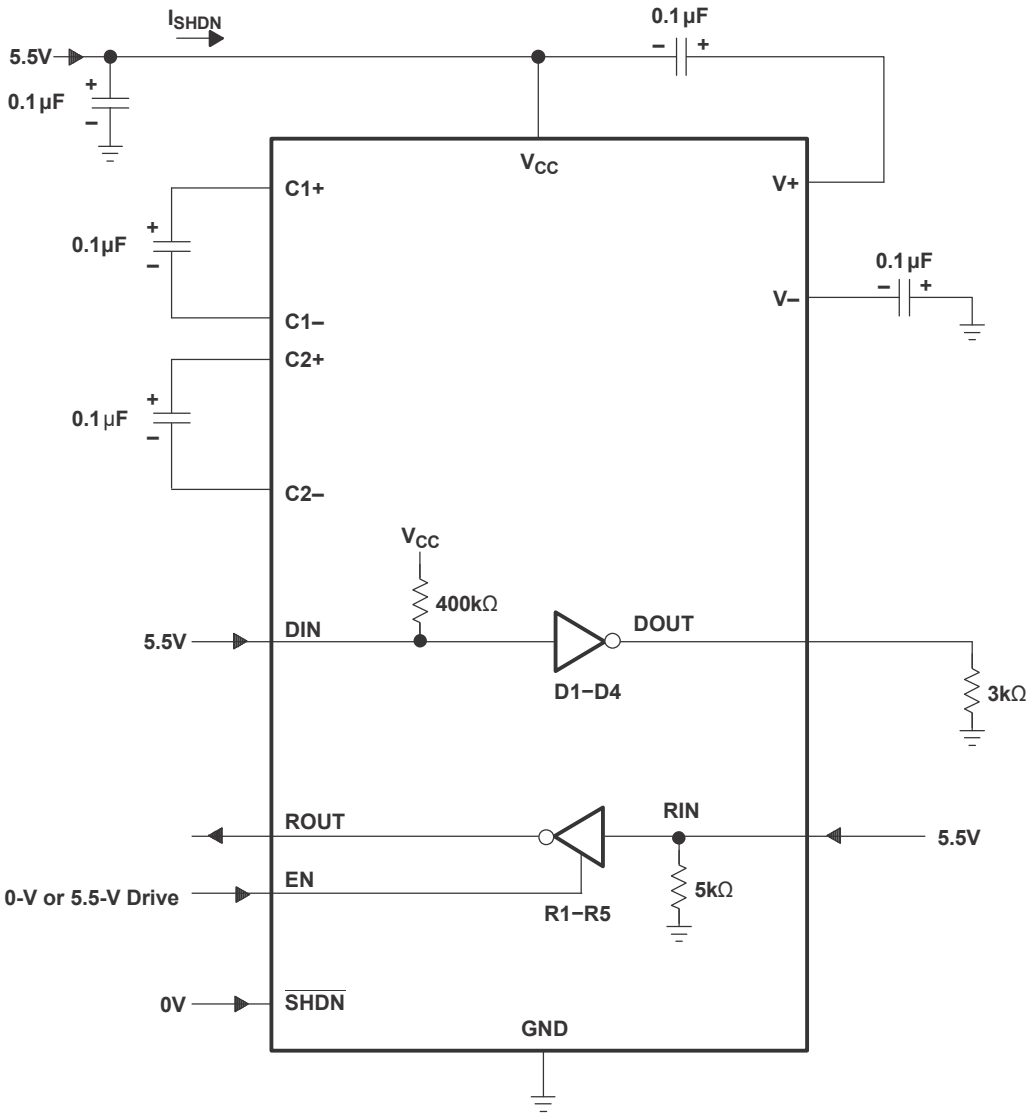
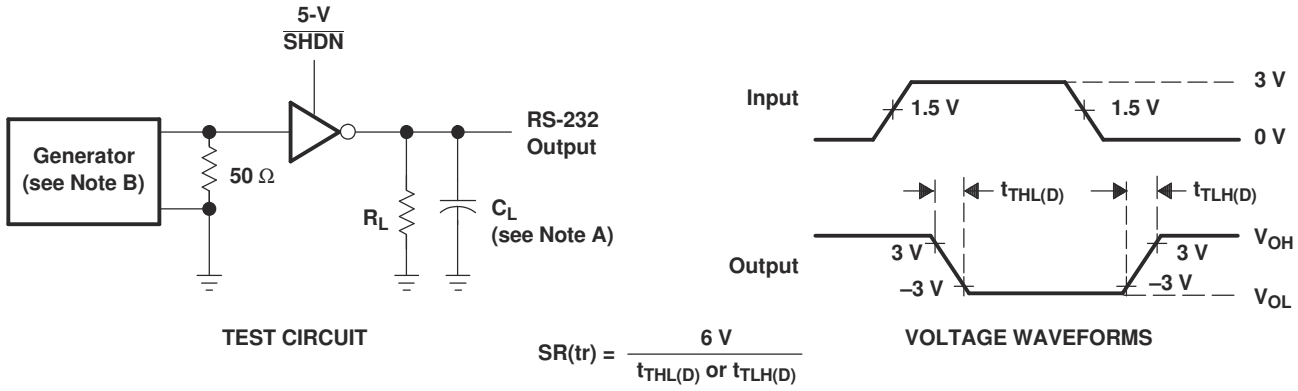
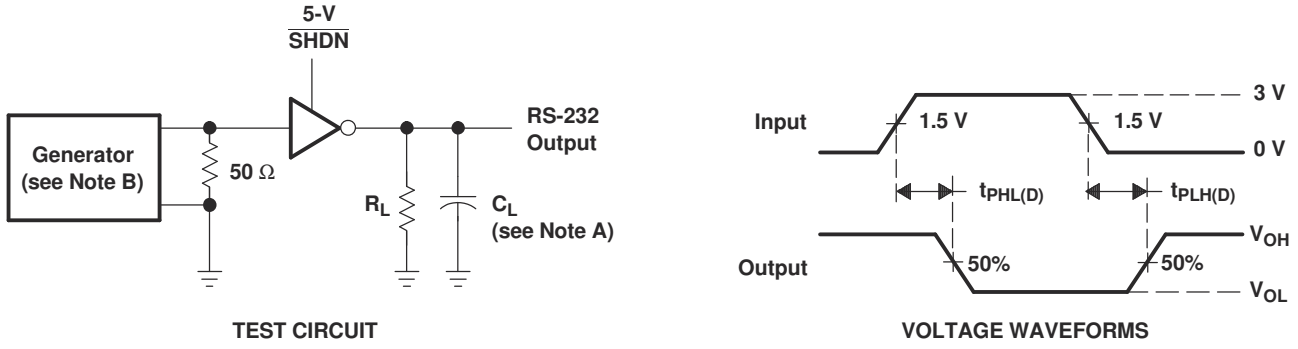


Figure 6-1. Shutdown Current Test Circuit



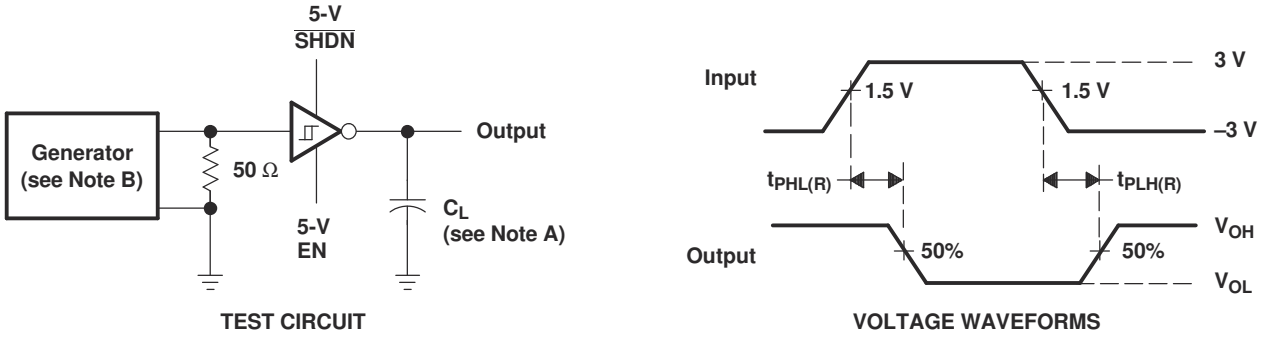
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-2. Driver Slew Rate



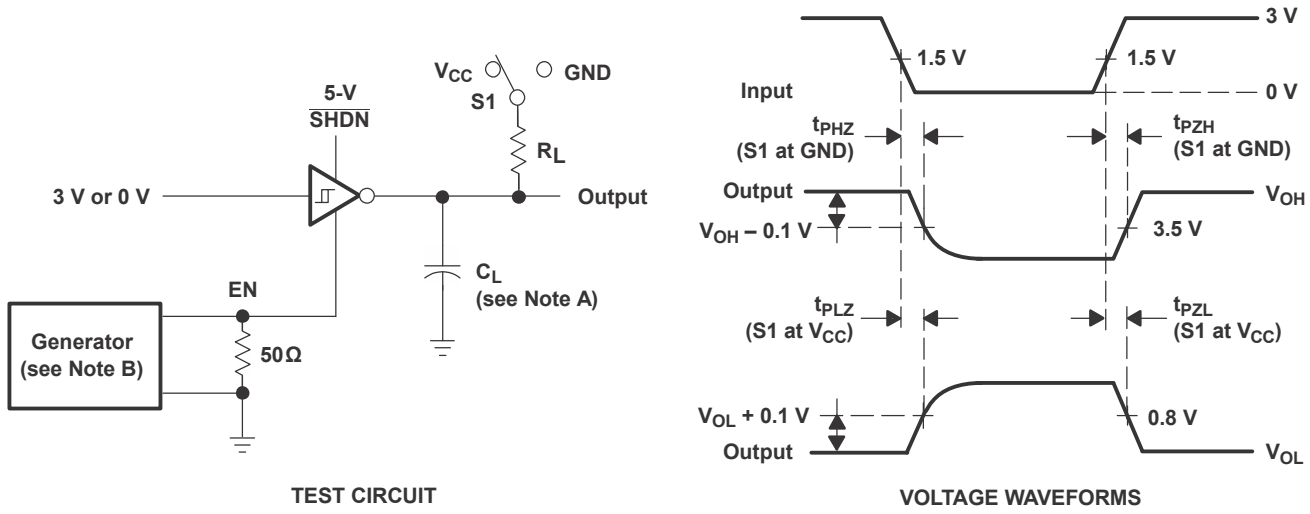
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-3. Driver Pulse Skew and Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-4. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-5. Receiver Enable and Disable Times

7 Functional Modes

Table 7-1. Function Table

INPUTS		DRIVER D1–D4	RECEIVER		DEVICE STATUS
$\overline{SHDN}$	EN		R1–R3	R4–R5	
L	L	Z	Z	Z	Shutdown
L	H	Z	Z	Active(1)	Shutdown
H	L	All active	Z	Z	Normal operation
H	H	All active	Active	Active	Normal operation

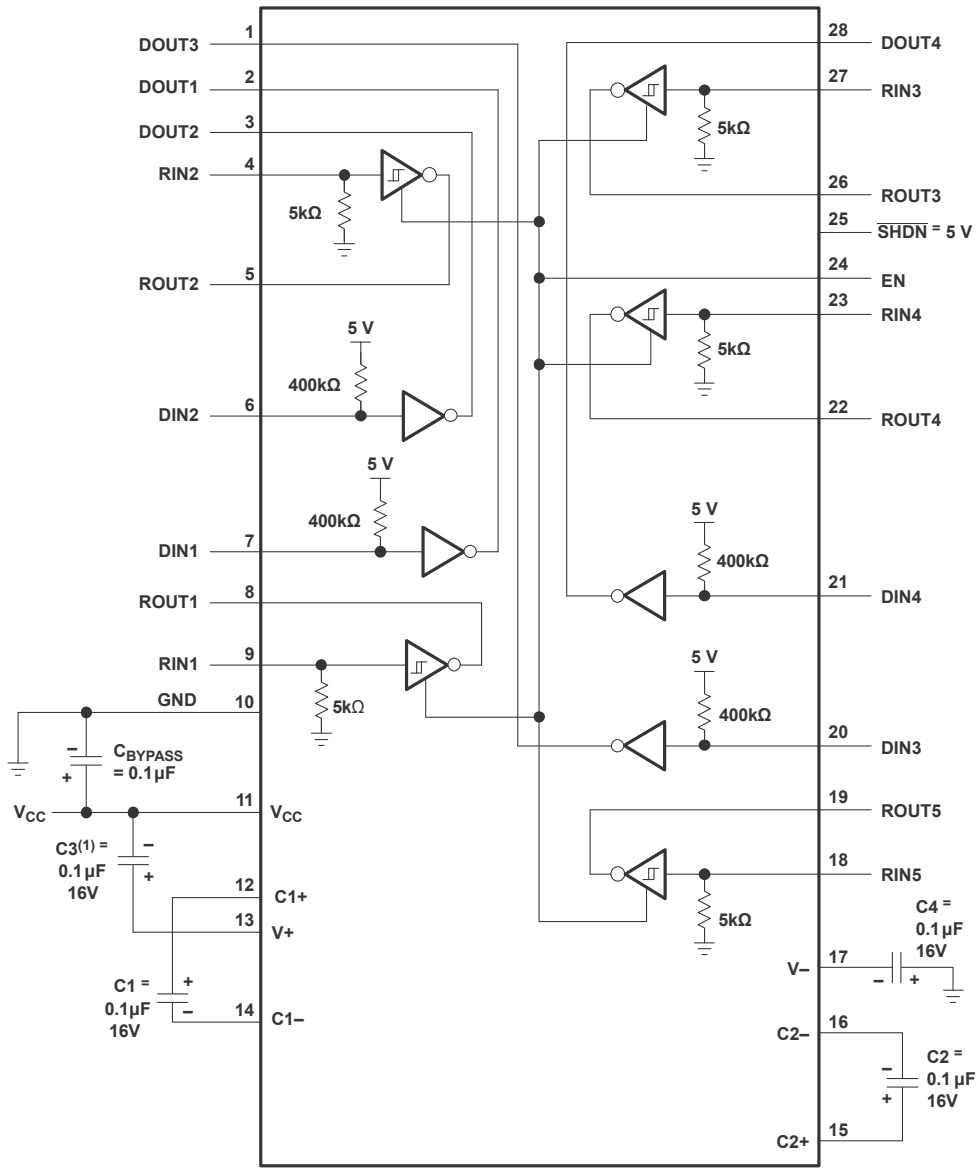
(1) See the V_{IT+} and V_{IT-} change in the *Electrical Characteristics* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application



(1) C3 can be connected to VCC or GND.
NOTES: A. Resistor values shown are nominal.
B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8-1. Typical Operating Circuit and Capacitor Values

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS213EIDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

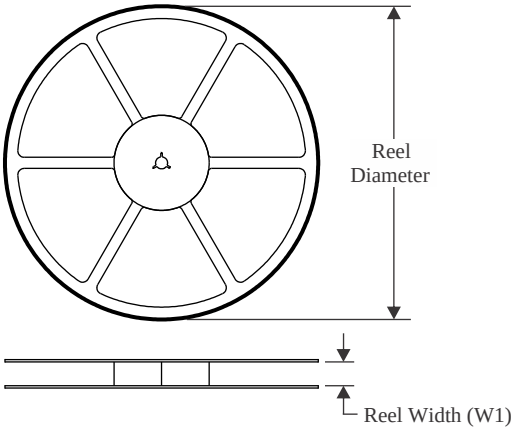
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

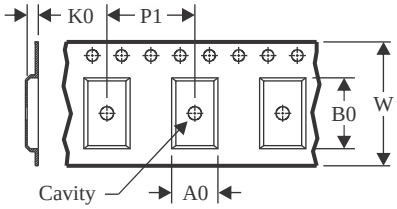
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

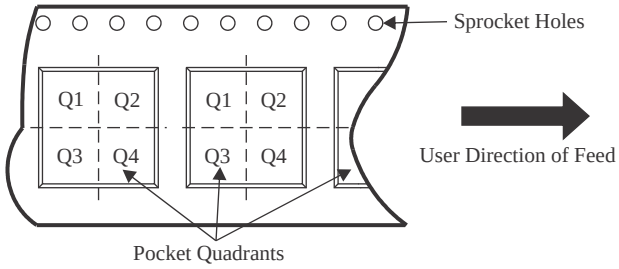


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

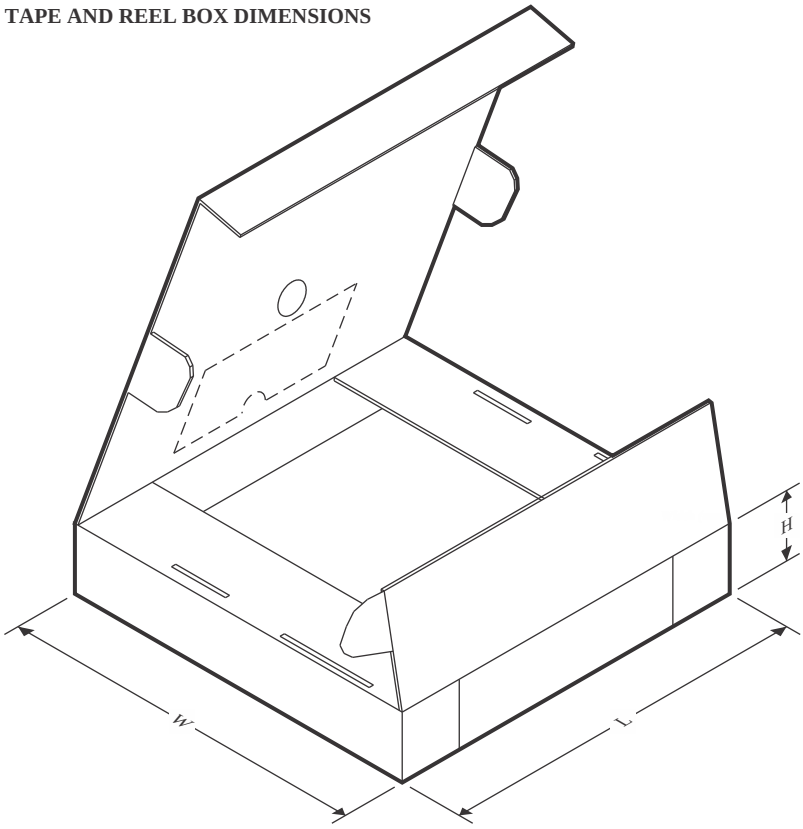
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS213EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

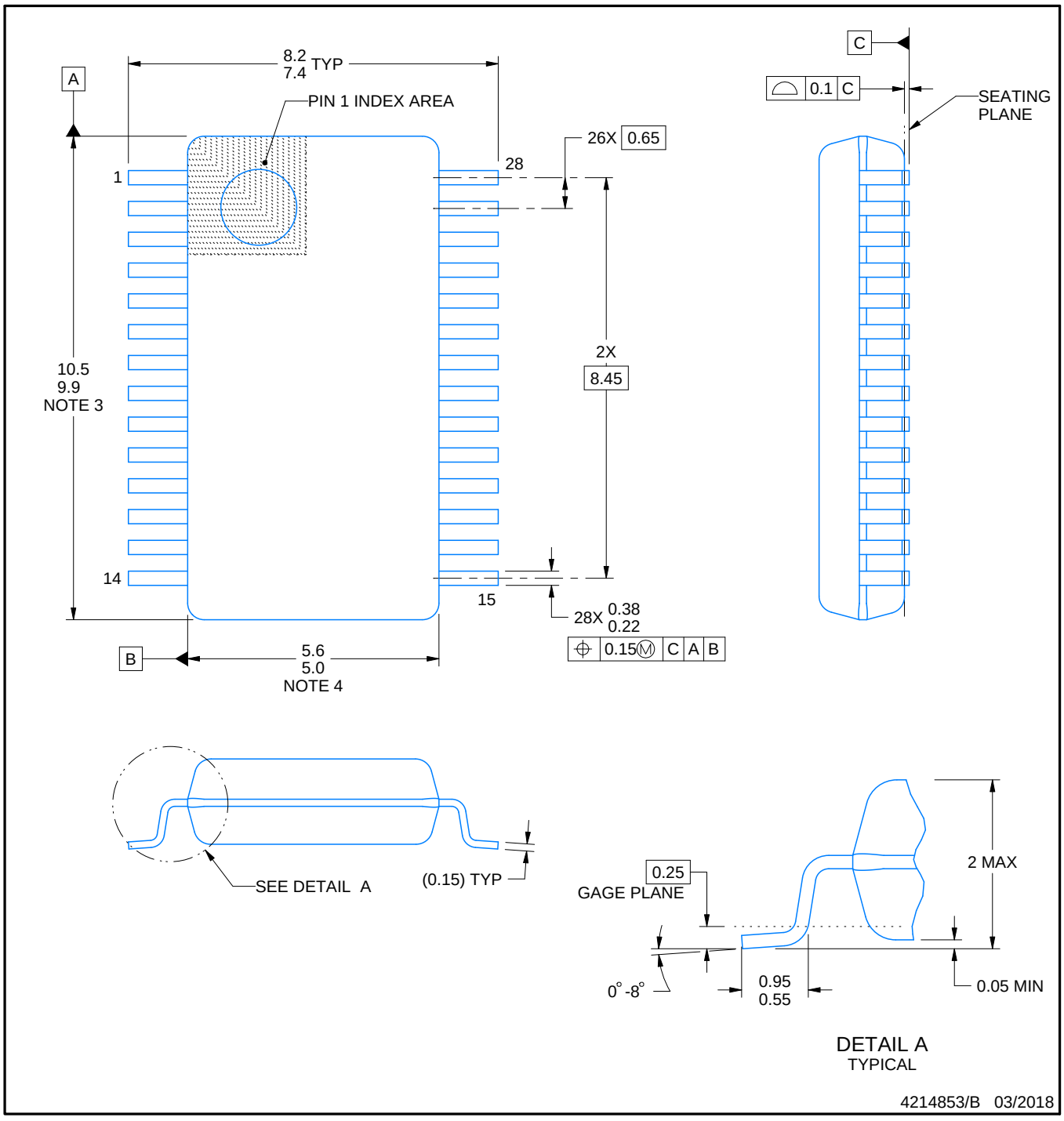
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS213EIDBR	SSOP	DB	28	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DB0028A

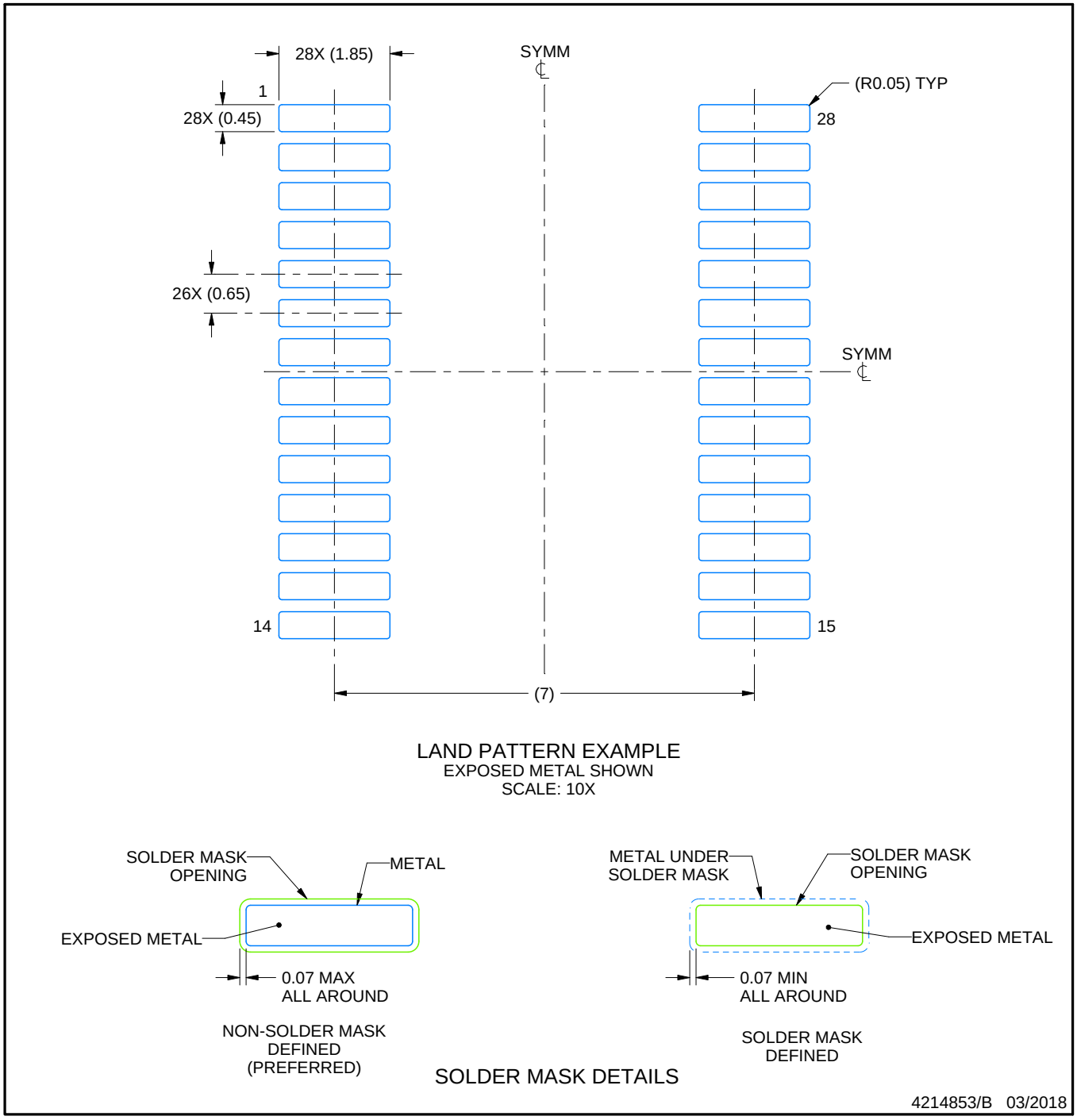
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



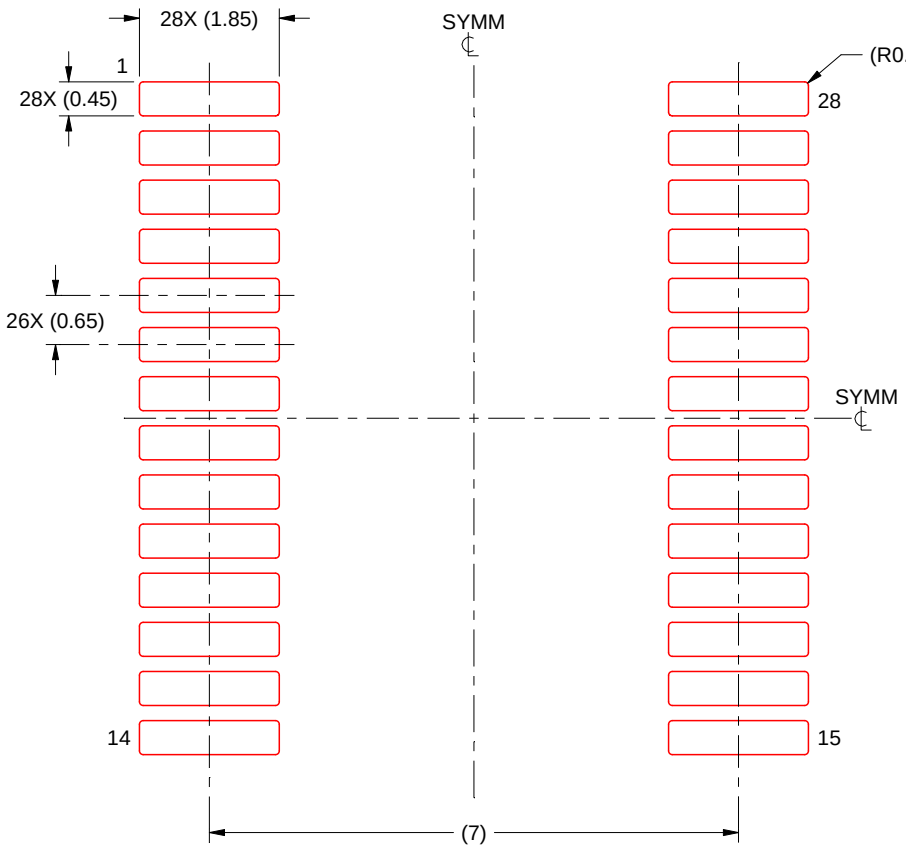
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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