

TRS3221 3-V to 5.5-V RS-232 Line Driver and Receiver With ± 15 -kV ESD Protection

1 Features

- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 250 kbps
- One Driver and One Receiver
- Low Standby Current: 1- μ A Typical
- External Capacitors: 4 \times 0.1 μ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbps)
 - SNx5C3221
- Automatic Power-Down Feature Automatically Disables Drivers for Power Savings

2 Applications

- Battery-Powered, Hand-Held, and Portable Equipment
- Notebooks, Subnotebooks, and Laptops
- Digital Cameras
- Mobile Phones and Wireless Devices

3 Description

The TRS3221 device consists of one line driver, one line receiver with dedicated enable pin, and a dual charge-pump circuit with ± 15 -kV ESD protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The TRS3221 device operates at data signaling rates up to 250 kbps and a maximum of 30-V/ μ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The automatic power-down feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled and the supply current is reduced to 1 μ A. The INVALID output notifies the user if an RS-232 signal is present at the receiver input.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRS3221	SSOP (32)	6.20 mm x 5.30 mm
	TSSOP (32)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

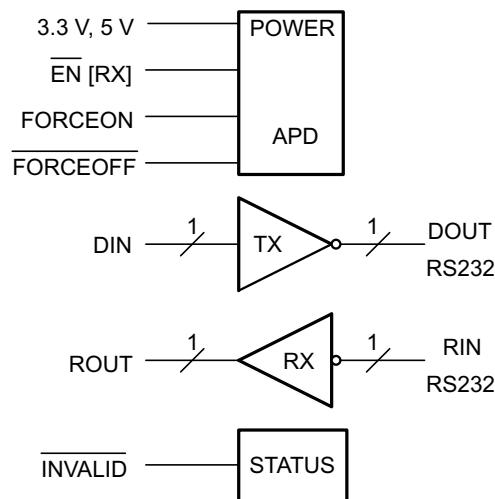


Table of Contents

1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Pin Configuration and Functions 3 6 Specifications 4 6.1 Absolute Maximum Ratings 4 6.2 ESD Ratings 4 6.3 Recommended Operating Conditions 4 6.4 Thermal Information 5 6.5 Electrical Characteristics—Power 5 6.6 Electrical Characteristics—Driver 5 6.7 Electrical Characteristics—Receiver 6 6.8 Electrical Characteristics—Status 6 6.9 Switching Characteristics—Driver 6 6.10 Switching Characteristics—Receiver 7 6.11 Switching Characteristics—Status 7 6.12 Typical Characteristics 7 7 Parameter Measurement Information 8	8 Detailed Description 11 8.1 Overview 11 8.2 Functional Block Diagram 11 8.3 Feature Description 11 8.4 Device Functional Modes 12 9 Application and Implementation 13 9.1 Application Information 13 9.2 Typical Application 13 10 Power Supply Recommendations 15 11 Layout 15 11.1 Layout Guidelines 15 11.2 Layout Example 15 12 Device and Documentation Support 16 12.1 Community Resources 16 12.2 Trademarks 16 12.3 Electrostatic Discharge Caution 16 12.4 Glossary 16 13 Mechanical, Packaging, and Orderable Information 16
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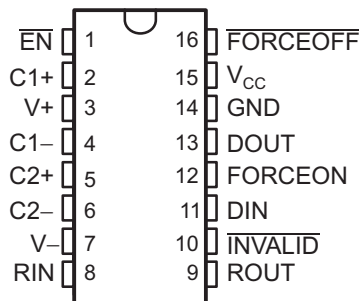
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2007) to Revision A	Page
• Added <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted <i>Ordering Information</i> table.	1
• Changed <i>Typical Operating Circuit and Capacitor Values</i> image	13

5 Pin Configuration and Functions

DB or PW Package
16-Pin SSOP or TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2+	5	—	
C1-	4	—	
C2-	6	—	
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
$\overline{\text{EN}}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
$\overline{\text{FORCEOFF}}$	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	GND	Ground
$\overline{\text{INVALID}}$	10	O	Invalid output pin. Output is low when all RIN inputs are unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V _{CC}	15	—	3-V to 5.5-V supply voltage
V+	3	O	5.5-V supply generated by the charge pump
V-	7	O	-5.5-V supply generated by the charge pump

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC} to GND			-0.3	6	V
V+ to GND			-0.3	7	V
V- to GND			0.3	-7	V
V+ + V- ⁽²⁾				13	V
V _I	Input voltage	DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, and FORCEON to GND	-0.3	6	V
		RIN to GND		±25	
V _O	Output voltage	DOUT to GND		±13.2	V
		ROUT to GND	-0.3	V _{CC} + 0.3	
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) V+ and V- can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.
- (3) Maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A) / R_{θJA}. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except Pin 8 and Pin 13	±3000	V
			Pin 8, Pin 13 (RS232 ports)	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 (see [Figure 9](#))⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	V _{CC} = 3.3 V	2		V
			V _{CC} = 5 V	2.4		
V _{IL}	Driver low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$			0.8	V
V _I	Driver input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	0		5.5	V
	Receiver input voltage		-25		25	
T _A	Operating free-air temperature	TRS3221C	0		70	°C
		TRS3221I	-40		85	

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TRS3221		UNIT
		DB (SSOP)	PW (TSSOP)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	98.0	106.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	48.3	41.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	48.7	51.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10.1	3.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	48.1	50.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics—Power

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON, EN			±0.01	±1	μA
I _{CC}	Supply current	Automatic power down disabled	No load, V _{CC} = 3.3 V to 5 V	No load, FORCEOFF and FORCEON at V _{CC}	0.3	1	mA
	Powered off	No load, FORCEOFF at GND		1	10	μA	
	Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded		1	10		

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = GND		5	5.4		V
V _{OL}	Low-level output voltage	D _{OUT} at R _L = 3 kΩ to GND, D _{IN} = V _{CC}		–5	–5.4		
I _{IH}	High-level input current	V _I = V _{CC}			±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V	V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V	V _O = 0 V		±35	±60	
r _O	Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V		300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V			±25	μA
			V _O = ±12 V, V _{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics—Receiver

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		
I _{off}	Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

 (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

 (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Electrical Characteristics—Status

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}			2.7	V
V _{T-(valid)}	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-2.7			V
V _{T(invalid)}	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-0.3		0.3	V
V _{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} - 0.6			V
V _{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}			0.4	V

 (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

 (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.9 Switching Characteristics—Driver

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	C _L = 1000 pF, R _L = 3 kΩ, (see Figure 3)	150	250		kbps
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 to 2500 pF, R _L = 3 kΩ to 7 kΩ, (see Figure 4)		100		ns
SR(tr)	Slew rate, transition region (see Figure 3)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 to 1000 pF	6	30	V/μs
			C _L = 150 to 2500 pF	4	30	

 (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

 (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

 (3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

6.10 Switching Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, (see Figure 5)		150		ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, (see Figure 5)		150		ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, (see Figure 6)		200		ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, (see Figure 6)		200		ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 5		50		ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

6.11 Switching Characteristics—Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

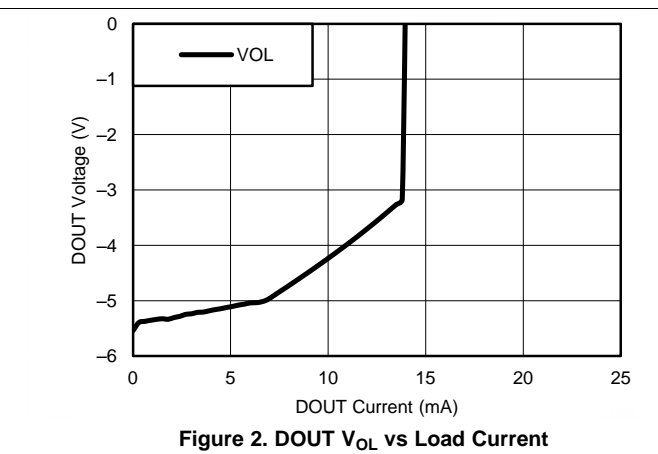
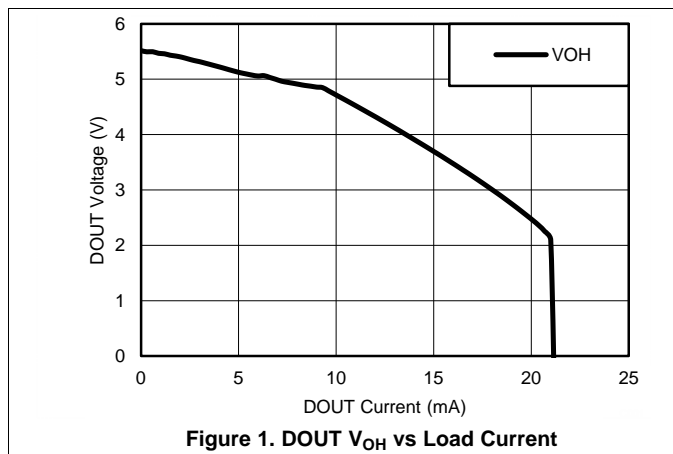
PARAMETER		MIN	TYP ⁽²⁾	MAX	UNIT
t _{valid}	Propagation delay time, low- to high-level output		1		μs
t _{invalid}	Propagation delay time, high- to low-level output		30		μs
t _{en}	Supply enable time		100		μs

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

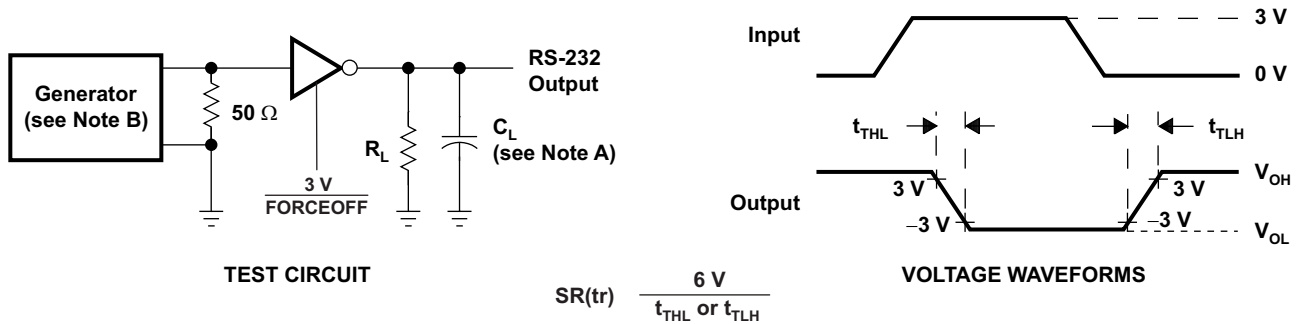
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.12 Typical Characteristics

V_{CC} = 3.3 V

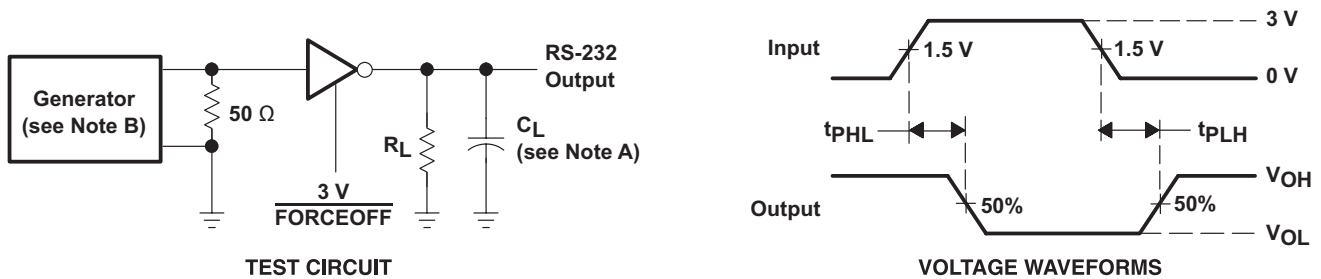


7 Parameter Measurement Information



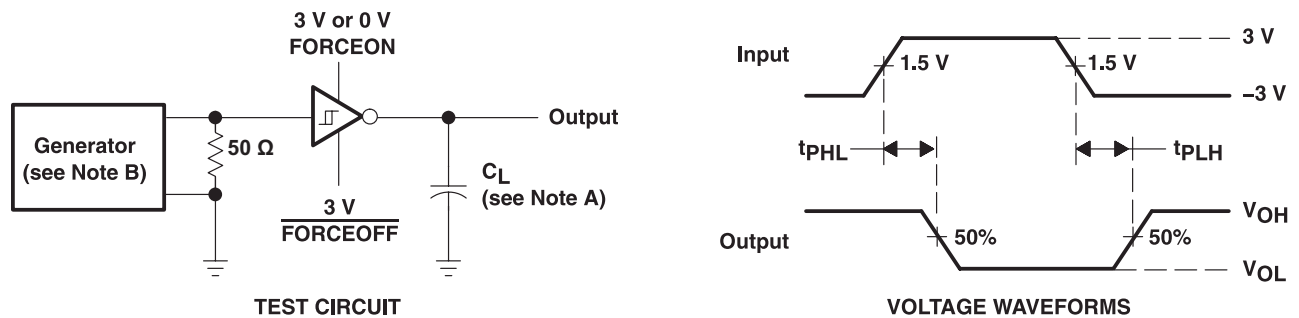
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbps, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

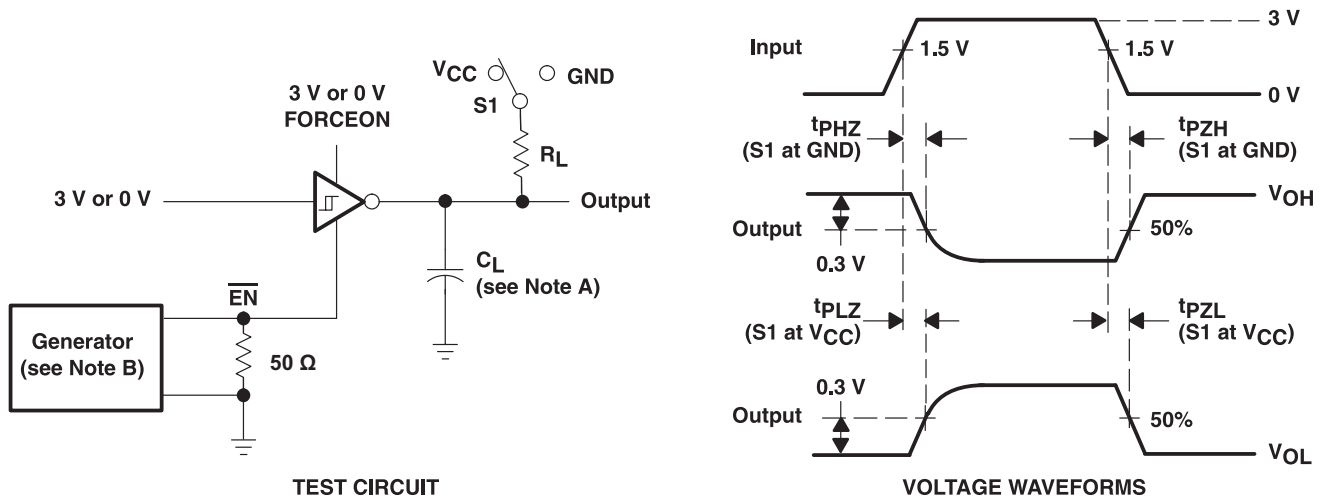
Figure 4. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 5. Receiver Propagation Delay Times

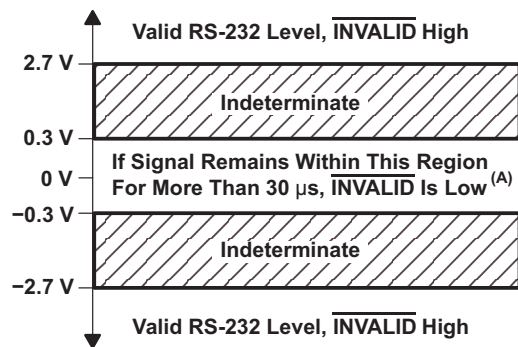
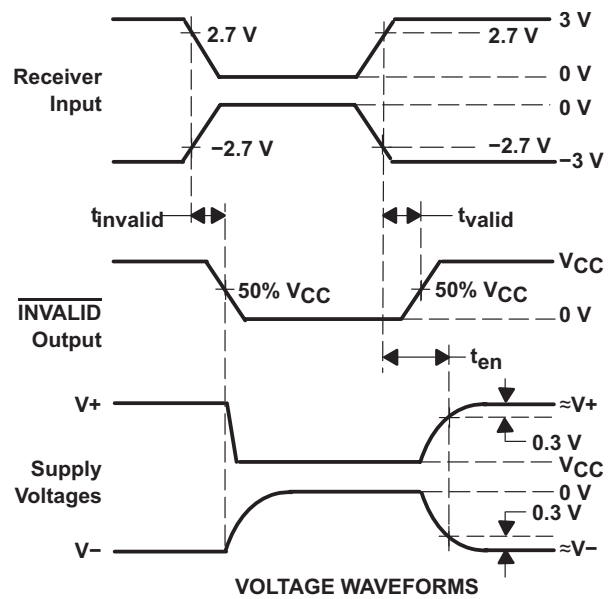
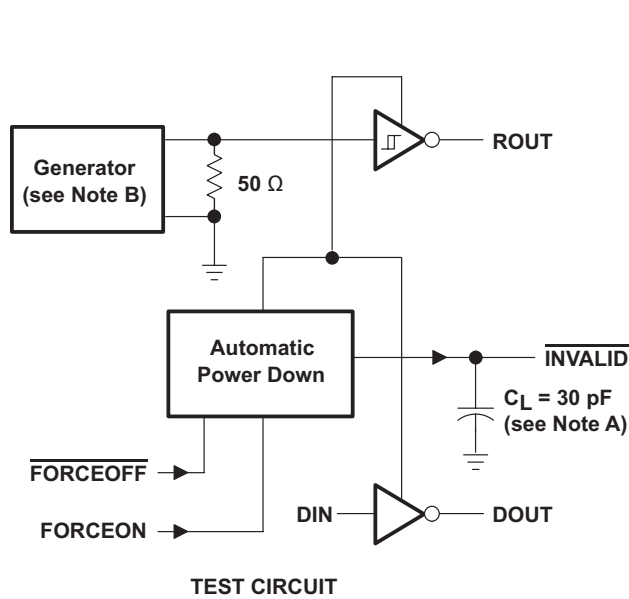
Parameter Measurement Information (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 6. Receiver Enable and Disable Times

Parameter Measurement Information (continued)



- A. Automatic Power Down disables drivers and reduces supply current to 1 μ A.
- B. C_L includes probe and jig capacitance.
- C. The pulse generator has the following characteristics: PRR = 5 kbps, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 7. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

8 Detailed Description

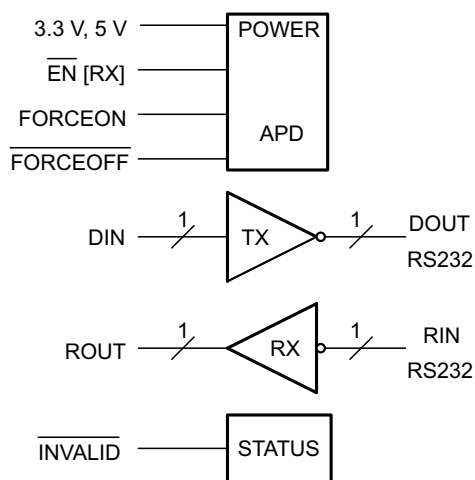
8.1 Overview

The TRS3221 device is a one-driver and one-receiver RS-232 interface device. All RS-232 inputs and outputs are protected up to ± 15 kV using the Human-Body Model. The charge pump requires only four small 0.1- μ F capacitors for operation from a 3.3-V supply. The TRS3221 device is capable of running at data rates up to 250 kbps while maintaining RS-232-compliant output levels.

Automatic power down can be disabled when $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ are high. With automatic power down plus enabled, the device activates automatically when a valid signal is applied to any receiver input. The device can automatically power down the driver to save power when the RIN input is unpowered.

$\overline{\text{INVALID}}$ is high (valid data) if receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. $\overline{\text{INVALID}}$ is low (invalid data) if receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to [Figure 7](#) for receiver input levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at $V+$ and $V-$ pins using a charge pump that requires four external capacitors. The automatic power-down feature for the driver is controlled by $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs. The receiver is controlled by the $\overline{\text{EN}}$ input (see [Table 1](#) and [Table 2](#)).

When the TRS3221 device is unpowered, it can be safely connected to an active remote RS232 device.

8.3.2 RS232 Driver

One driver interfaces standard logic level to RS232 levels. DIN input must be valid high or low.

8.3.3 RS232 Receiver

One receiver interfaces RS232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

8.3.4 RS232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30 μ s. The $\overline{\text{INVALID}}$ output goes high when the receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{CC} is powered regardless of $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs (see [Table 3](#)).

8.4 Device Functional Modes

Table 1. Driver⁽¹⁾

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with automatic power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by automatic power-down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, Yes = |RIN| > 2.7 V, No = |RIN| < 0.3 V

Table 2. Receiver⁽¹⁾

INPUTS			OUTPUT	RECEIVER STATUS
RIN	EN	VALID RIN RS-232 LEVEL	ROUT	
X	H	X	Z	Output off
L	L	X	H	Normal operation
H	L	X	L	
Open	L	No	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 3. INVALID⁽¹⁾

INPUTS				OUTPUT
RIN	FORCEON	FORCEOFF	EN	INVALID
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

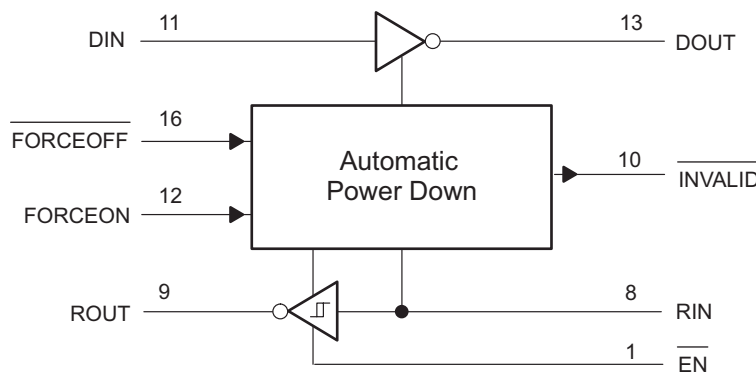


Figure 8. Logic Diagram

9 Application and Implementation

NOTE

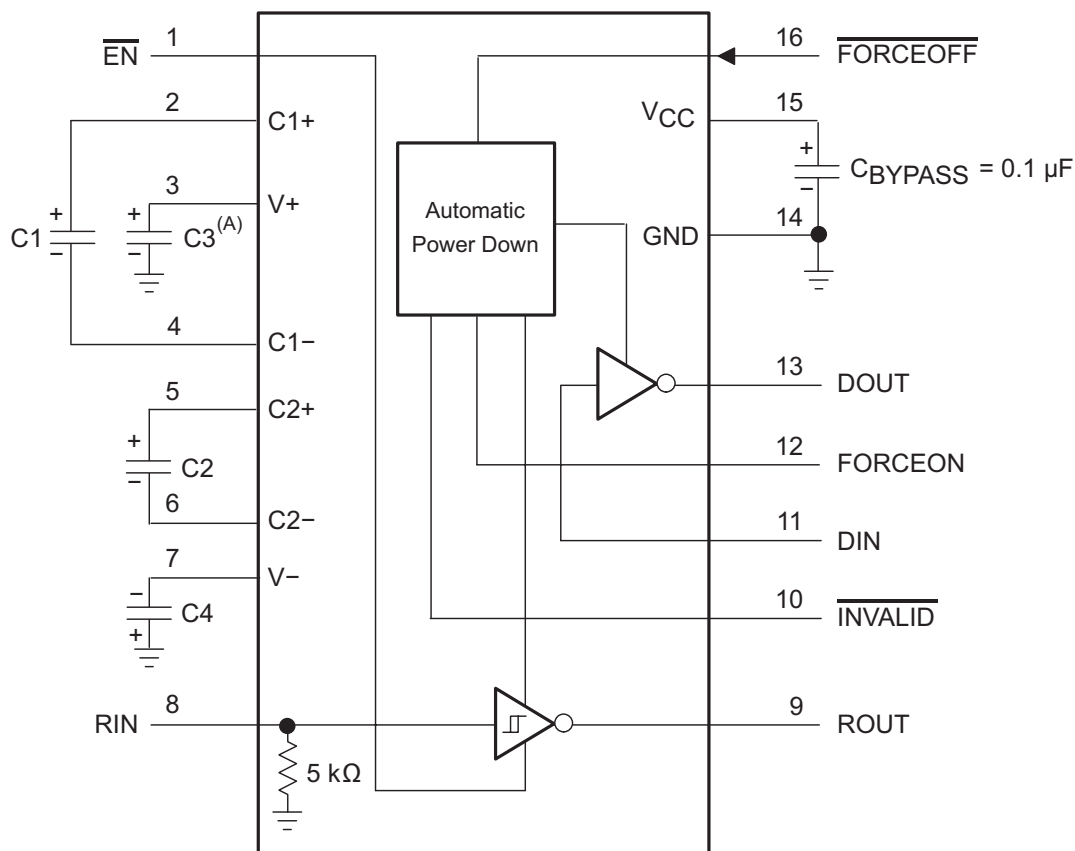
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TRS3232 device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector.

9.2 Typical Application



- A. C3 can be connected to V_{CC} or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.
- D. See [Table 4](#) for capacitor values.

Figure 9. Typical Operating Circuit

Typical Application (continued)

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V
 - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbps
- Use capacitors as shown in [Figure 9](#) and [Table 4](#)

Table 4. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

9.2.2 Detailed Design Procedure

For proper operation, add capacitors as shown in [Figure 9](#) and [Table 4](#).

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on V_{CC} level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC} . INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

9.2.3 Application Curve

V_{CC} of 3.3 V and 250 kbps alternative bit data stream

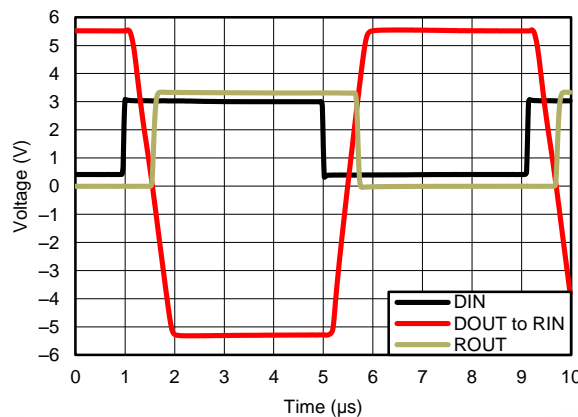


Figure 10. 250 kbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

10 Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using [Table 4](#).

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

11.2 Layout Example

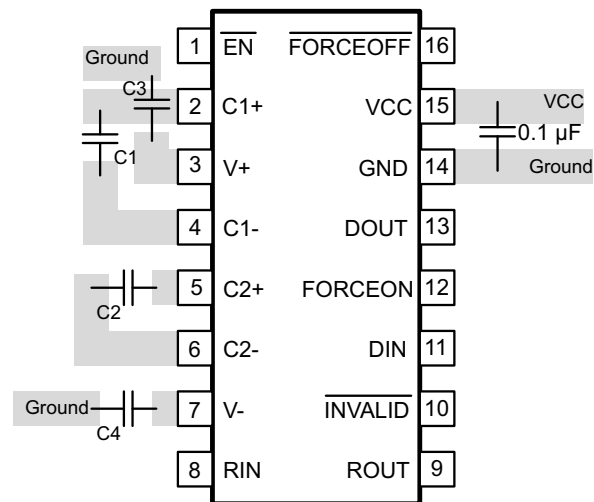


Figure 11. Layout Diagram

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3221CDBR	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70	RS21C	
TRS3221PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3221PWR	TSSOP	PW	16	2000	356.0	356.0	35.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

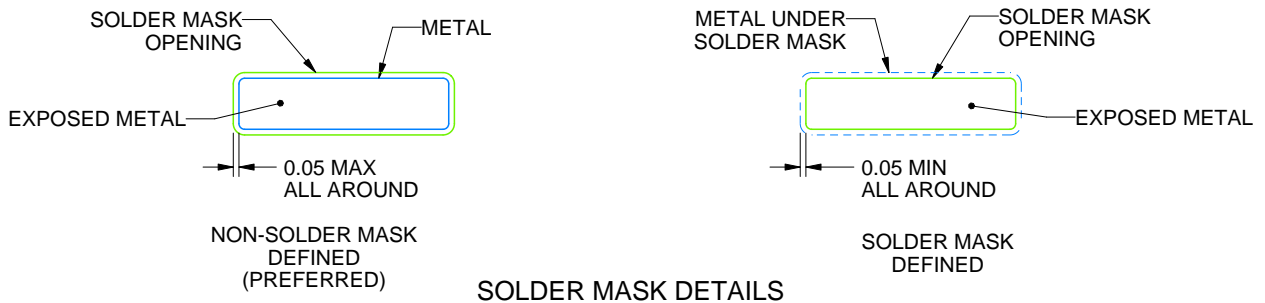
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

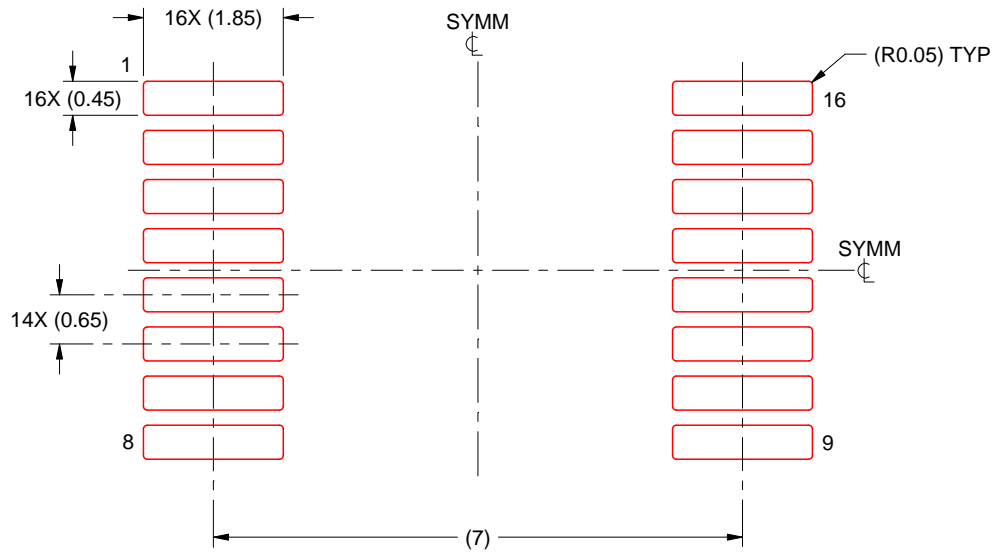
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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