

## FEATURES

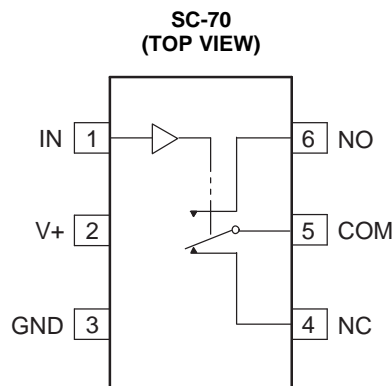
- Isolation in Power-Down Mode,  $V_{+} = 0$
- Specified Break-Before-Make Switching
- Low ON-State Resistance ( $1\ \Omega$ )
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

## APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

## DESCRIPTION

The TS5A4624 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.



Switches are shown for logic 0 input.

## FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TS5A4624**  
**1-Ω SPDT ANALOG SWITCH**  
**5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

SLYS014A–DECEMBER 2005–REVISED AUGUST 2006

**SUMMARY OF CHARACTERISTICS<sup>(1)</sup>**

Configuration	2:1 Multiplexer/ Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance $r_{on}$	1.1 Ω
ON-state resistance match ( $\Delta r_{on}$ )	0.1 Ω
ON-state resistance flatness $r_{on(flat)}$	0.15 Ω
Turn-on/turn-off time ( $t_{ON/tOFF}$ )	20 ns/15 ns
Break-before-make time ( $t_{BBM}$ )	12 ns
Charge injection ( $Q_C$ )	-20 pC
Bandwidth (BW)	100 MHz
OFF isolation ( $O_{ISO}$ )	-65 dB at 1 MHz
Crosstalk ( $X_{TALK}$ )	-66 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ( $I_{NO(OFF)}/I_{NC(OFF)}$ )	±20 nA
Power-supply current ( $I_+$ )	0.1 μA
Package options	6-pin DCK

(1)  $V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
-40°C to 85°C	SOT (SC-70) – DCK	Tape and reel	TS5A4624DCKR	JW_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).  
(2) DCK: The actual top-side marking has one additional character that designates the assembly/test site.

### Absolute Minimum and Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
V <sub>NO</sub> V <sub>NC</sub> V <sub>COM</sub>	Analog voltage range <sup>(3)(4)(5)</sup>	-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> < 0		mA
I <sub>NO</sub> I <sub>NC</sub> I <sub>COM</sub>	On-state switch current	-200	200	mA
	On-state peak switch current <sup>(6)</sup>	-400	400	
V <sub>I</sub>	Digital input voltage range <sup>(3)(4)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>I</sub> < 0		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>		100	mA
I <sub>GND</sub>	Continuous current through GND	-100	100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(7)</sup>		259	°C/W
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

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**Electrical Characteristics for 5-V Supply<sup>(1)</sup>**

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.8	1.1	Ω	
				Full			1.5		
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.7	0.9	Ω	
				Full			1.1		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.05	0.1	Ω	
				Full			0.1		
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.15		Ω	
				25°C		0.1	0.25		
				Full		0.25			
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = 1\text{ V to }4.5\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V to }4.5\text{ V}$ ,	Switch OFF, See Figure 14	25°C	5.5 V	-20	2	20	nA
				Full		-100	100		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ ,	Switch OFF, See Figure 14	25°C	0 V	-1	0.2	1	μA
				Full		-20	20		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	5.5 V	-20	2	20	nA
				Full		-100	100		
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ ,	Switch OFF, See Figure 14	25°	0 V	-1	0.1	1	μA
				Full		-20	20		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 1\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 4.5\text{ V}$ ,	Switch ON, See Figure 15	25°C	5.5 V	-20	2	20	nA
				Full		-100	100		
<b>Digital Input (IN)</b>									
Input logic high	$V_{IH}$			Full		2.4	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.8	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$		25°C	5.5 V	-2	2	nA	
				Full		100	100		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

### Electrical Characteristics for 5-V Supply<sup>(1)</sup> (Continued)

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	4	12	22	ns
				Full	4.5 V to 5.5 V	2		25	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	1	5	8	ns
				Full	4.5 V to 5.5 V	1		10	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 18	25°C	5 V	1	8	13	ns
				Full	4.5 V to 5.5 V	1		15	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See Figure 22	25°C	5 V		15.5	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		18	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		55	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		55	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See Figure 19	25°C	5 V		90	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See Figure 20	25°C	5 V		-63	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, See Figure 21	25°C	5 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 200\text{ Hz to }20\text{ kHz}$ , See Figure 23	25°C	5 V		0.004	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V		10	50	nA
				Full				500	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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**1-Ω SPDT ANALOG SWITCH**  
**5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

SLYS014A–DECEMBER 2005–REVISED AUGUST 2006

**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>**

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	3 V	1.3	1.6	$\Omega$	
				Full					
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	3 V	1.2	1.5	$\Omega$	
				Full					
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2\text{ V}, 0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	3 V	0.1	0.15	$\Omega$	
				Full					
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	3 V	0.2		$\Omega$	
				25°C					
				Full					
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}, V_{COM} = 1\text{ V to }3\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 3\text{ V}, V_{COM} = 1\text{ V to }3\text{ V}$ ,	Switch OFF, See Figure 14	25°C	3.6 V	-20	2	20	nA
				Full					
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0\text{ to }3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to }0$ ,	Switch OFF, See Figure 14	25°C	0 V	-1	0.2	1	$\mu\text{A}$
				Full					
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}, V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 3\text{ V}, V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	3.6 V	-10	2	10	nA
				Full					
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 3.6\text{ V to }0$ , $V_{COM} = 0\text{ to }3.6\text{ V}$ ,	Switch OFF, See Figure 14	25°C	0 V	-1	0.2	1	$\mu\text{A}$
				Full					
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}, V_{COM} = 1\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = \text{Open}, V_{COM} = 3\text{ V}$ ,	Switch ON, See Figure 15	25°C	3.6 V	-10	2	10	nA
				Full					
<b>Digital Input (IN)</b>									
Input logic high	$V_{IH}$			Full		2.4	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.8	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$		25°C	3.6 V	-2	2	nA	
				Full					

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

### Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (Continued)

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	4	16	25	ns
				Full	3 V to 3.6 V	2		27	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	1	5.5	8	ns
				Full	3 V to 3.6 V	1		11	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See Figure 18	25°C	3.3 V	2	12	20	ns
				Full	3 V to 3.6 V	2		25	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See Figure 22	25°C	3.3 V		9	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		55	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		55	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See Figure 19	25°C	3.3 V		90	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See Figure 20	25°C	3.3 V		-63	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, See Figure 21	25°C	3.3 V		-63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 23	25°C	3.3 V		0.01	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		10	50	nA
				Full				100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>**

$V_+ = 2.3 \text{ V to } 2.7$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	1.8	2.5	Ω	
				Full			2.7		
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.8 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	1.5	2	Ω	
				Full			2.4		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.8 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	0.15	0.2	Ω	
				Full			0.2		
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	0.6		Ω	
				25°C			0.6		1
				Full			1		
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.5 \text{ V}$ , $V_{COM} = 0.5 \text{ V to } 2.3 \text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 2.3 \text{ V}$ , $V_{COM} = 0.5 \text{ V to } 2.3 \text{ V}$ ,	Switch OFF, See Figure 14	25°C	2.7 V	-20	2	20	nA
				Full		-50	50		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 3.6 \text{ V}$ , $V_{COM} = 3.6 \text{ V to } 0$ ,	Switch OFF, See Figure 14	25°C	0 V	-1	0.1	1	μA
				Full		-10	10		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.5 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 2.2 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	2.7 V	-10	2	10	nA
				Full		-20	20		
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 2.7 \text{ V to } 0$ , $V_{COM} = 0 \text{ to } 2.7 \text{ V}$ ,	Switch OFF, See Figure 14	25°	0 V	-1	0.1	10	μA
				Full		-10	10		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0.5 \text{ V}$ , or $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 2.2 \text{ V}$ ,	Switch ON, See Figure 15	25°C	2.7 V	-10	2	10	nA
				Full		-20	20		
<b>Digital Input (IN)</b>									
Input logic high	$V_{IH}$			Full		1.8	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.6	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$		25°C	2.7 V	-2	2	nA	
				Full		20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



### Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (Continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	10	22	32	ns
			Full	2.3 V to 2.7 V	8		35	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	3	6	11	ns
			Full	2.3 V to 2.7 V	2		12	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 18	25°C	2.5 V	5	19	30	ns
			Full	2.3 V to 2.7 V	5		35	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1 \text{ nF}$ , See Figure 22	25°C	2.5 V		-7		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		18		pF
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		55		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		55		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON, See Figure 19	25°C	2.5 V		90		MHz
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ , Switch OFF, See Figure 20	25°C	2.5 V		-63		dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ , Switch ON, See Figure 21	25°C	2.5 V		-63		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , See Figure 23	25°C	2.5 V		0.02		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V	10	20		nA
			Full			150		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**TS5A4624**  
**1-Ω SPDT ANALOG SWITCH**  
**5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

SLYS014A–DECEMBER 2005–REVISED AUGUST 2006

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>**

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, See Figure 13	25°C	1.65 V	5		Ω	
				Full		15			
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, See Figure 13	25°C	1.65 V	2	2.5	Ω	
				Full		3.5			
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, See Figure 13	25°C	1.65 V	0.15	0.4	Ω	
				Full		0.4			
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, See Figure 13	25°C	1.65 V	5		Ω	
				25°C		4.5			
				Full					
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = 0.3\text{ V to }1.65\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V to }1.65\text{ V}$ ,	Switch OFF, See Figure 14	25°C	1.95 V	-5	2	5	nA
				Full		-20	20		
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 1.95\text{ V}$ , $V_{COM} = 1.95\text{ V to } 0$ ,	Switch OFF, See Figure 14	25°C	0 V	-1	0.1	1	μA
				Full		-5	5		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	1.95 V	-5	2	5	nA
				Full		-20	20		
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 1.95\text{ V to } 0$ , $V_{COM} = 0 \text{ to } 1.95\text{ V}$ ,	Switch OFF, See Figure 14	25°	0 V	-1	0.1	1	μA
				Full		-5	5		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0.3\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 1.65\text{ V}$ ,	Switch ON, See Figure 15	25°C	1.95 V	-5	2	5	nA
				Full		-20	20		
<b>Digital Input (IN)</b>									
Input logic high	$V_{IH}$			Full		1.5	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.6	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$		25°C	1.95 V	-2	2	nA	
				Full		20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

### Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (Continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See Figure 17	25°C	1.8 V	17	35	65	ns
				Full	1.65 V to 1.95 V	15		70	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See Figure 17	25°C	1.8 V	3	7	13	ns
				Full	1.65 V to 1.95 V	2		15	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\ \text{pF}$ , See Figure 18	25°C	1.8 V	15	33	60	ns
				Full	1.65 V to 1.95 V	15		65	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\ \text{nF}$ , See Figure 22	25°C	1.8 V		4	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		55	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		55	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See Figure 19	25°C	1.8 V		90	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\ \text{MHz}$ ,	Switch OFF, See Figure 20	25°C	1.8 V		63	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\ \text{MHz}$ ,	Switch ON, See Figure 21	25°C	1.8 V		63	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\ \text{pF}$ ,	$f = 20\ \text{Hz to }20\ \text{kHz}$ , See Figure 23	25°C	1.8 V		0.05	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		5	15	$\mu\text{A}$
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

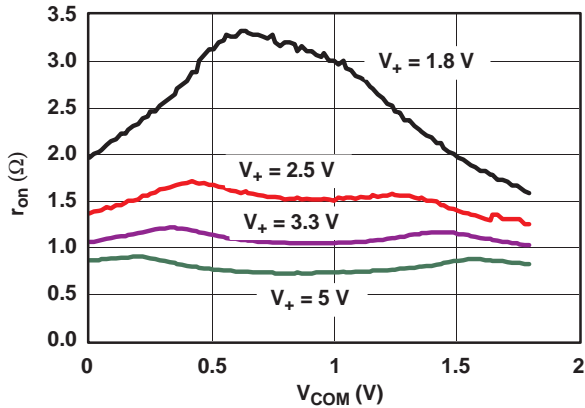


Figure 1.  $r_{on}$  vs  $V_{COM}$

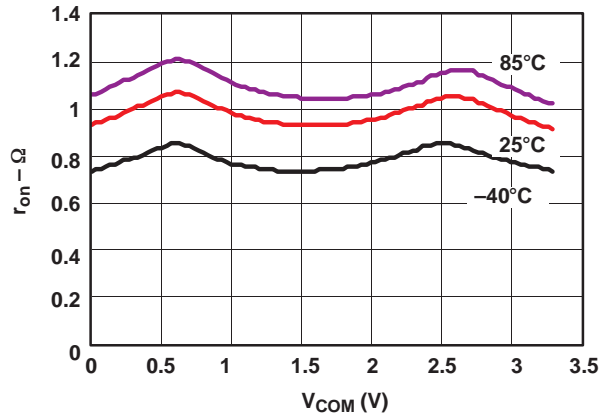


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3$  V)

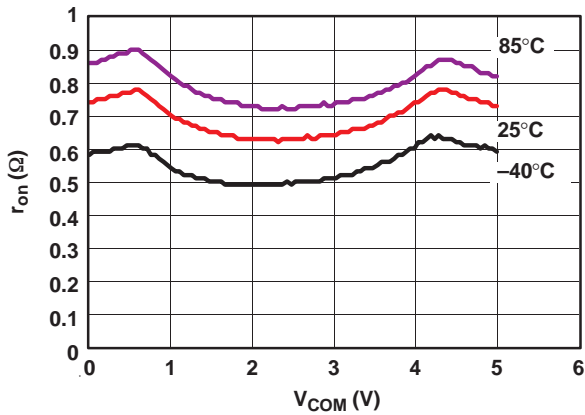


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5$  V)

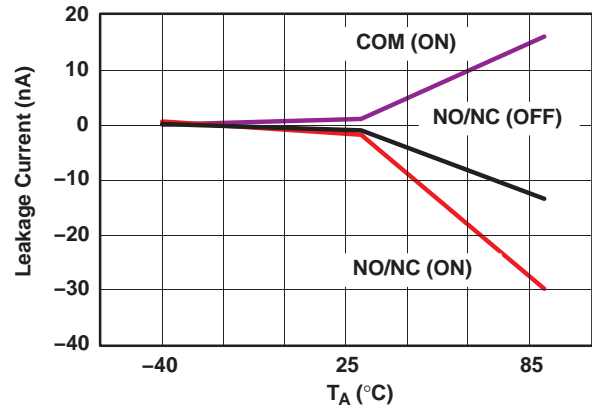


Figure 4. Leakage Current vs Temperature ( $V_+ = 3.3$  V)

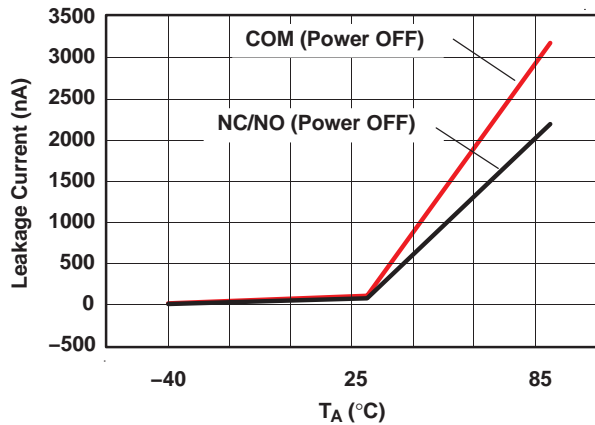


Figure 5. Leakage Current vs Temperature ( $V_+ = 5$  V)

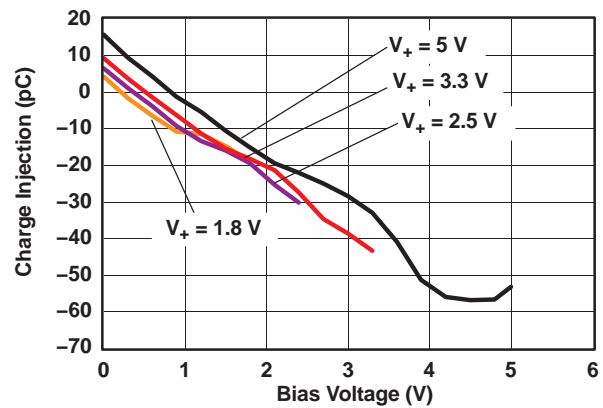


Figure 6. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

TYPICAL PERFORMANCE (continued)

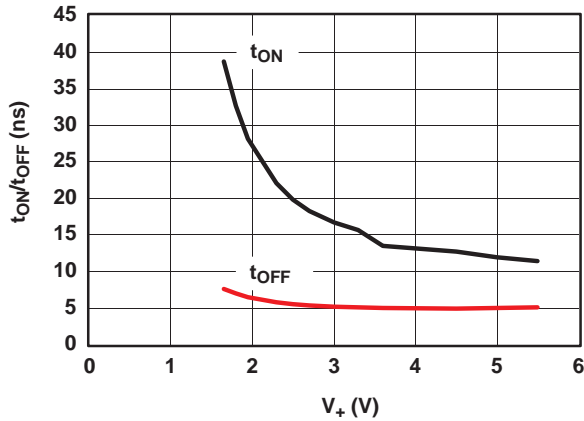


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

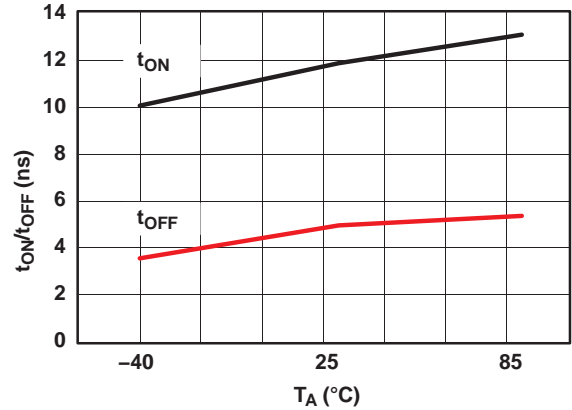


Figure 8.  $t_{ON}$  and  $t_{OFF}$  vs Temperature

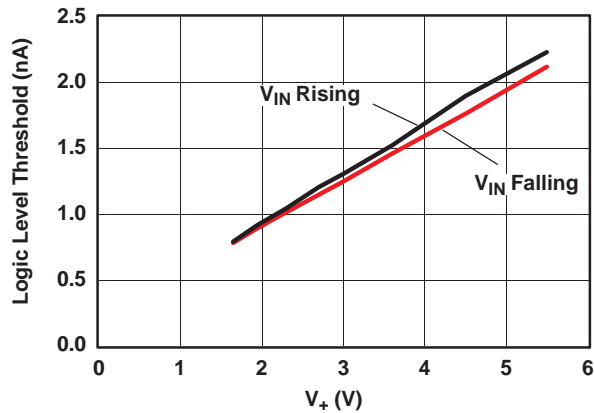


Figure 9.  $V_{IN}$  and  $t_{OFF}$  vs Supply Voltage

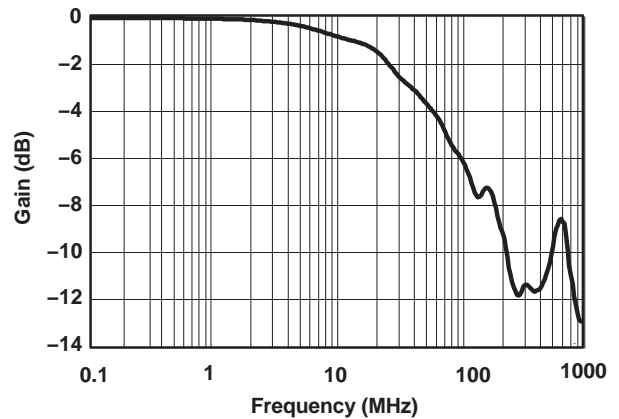


Figure 10. Bandwidth ( $V_+ = 5\text{ V}$ )

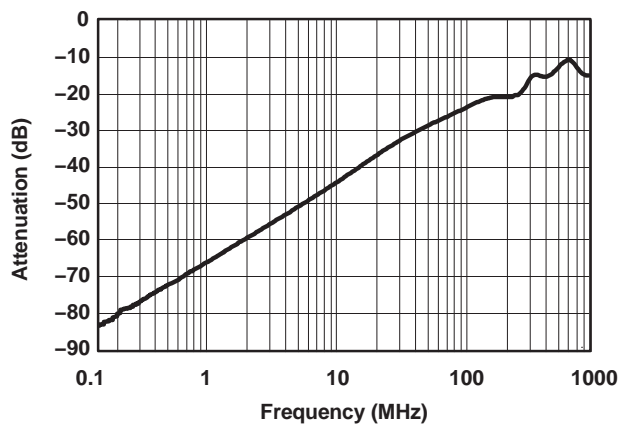


Figure 11. OFF Isolation vs Frequency

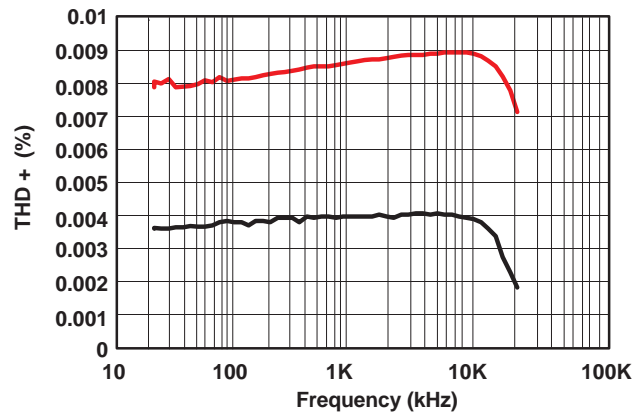


Figure 12. Total Harmonic Distortion vs Frequency ( $V_+ = 5\text{ V}$ )

TYPICAL PERFORMANCE (continued)

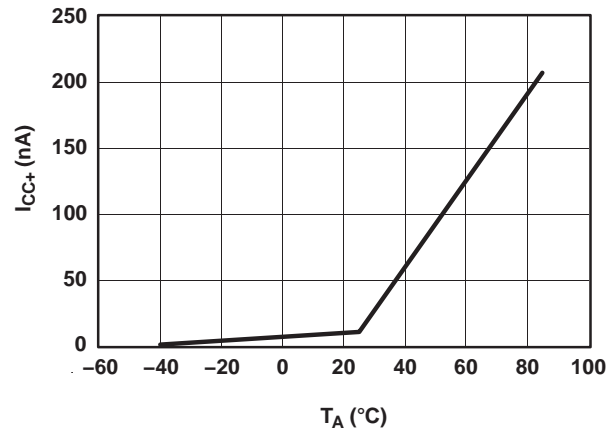


Figure 13. Current vs Temperature ( $V_+ = 5$  V)

**PIN DESCRIPTION**

<b>PIN NO.</b>	<b>NAME</b>	<b>DESCRIPTION</b>
1	IN	Digital control to connect COM to NO
2	V <sub>+</sub>	Power supply
3	GND	Digital ground
4	NC	Normally closed
5	COM	Common
6	NO	Normally open

## PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NC}$	Voltage at NC
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NC or COM and NO ports when the channel is ON
$r_{peak}$	Peak ON-state resistance over a specified voltage range
$\Delta r_{on}$	Difference of $r_{on}$ between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at IN
$I_{IH}, I_{IL}$	Leakage current measured at IN
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning OFF.
$t_{BBM}$	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$ , $C_L$ is the load capacitance and $\Delta V_O$ is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_{IN}$	Capacitance of IN
OISO	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
$X_{TALK}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio or root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND



PARAMETER MEASUREMENT INFORMATION

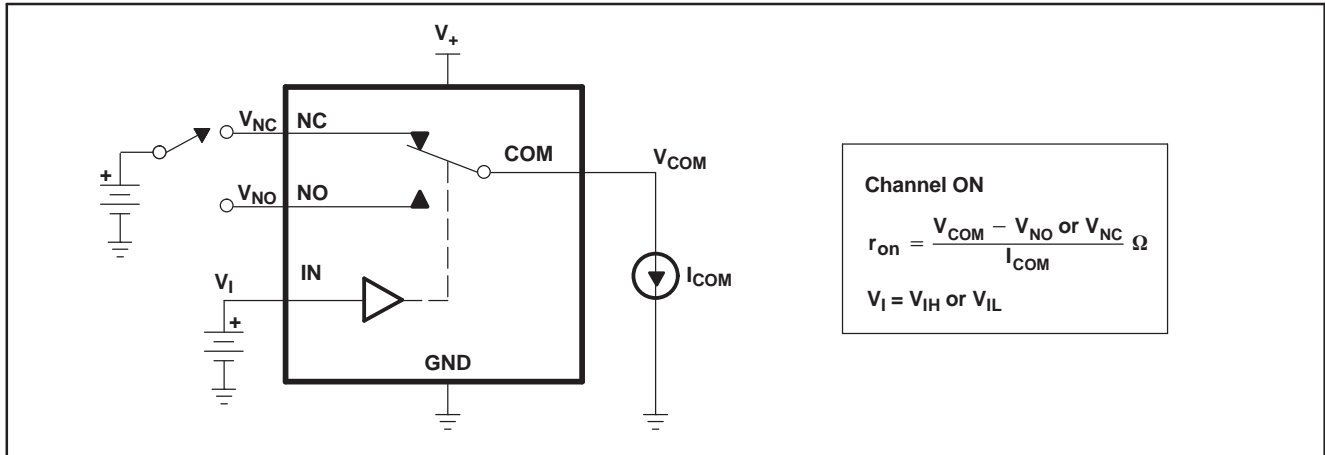


Figure 14. ON-State Resistance ( $r_{on}$ )

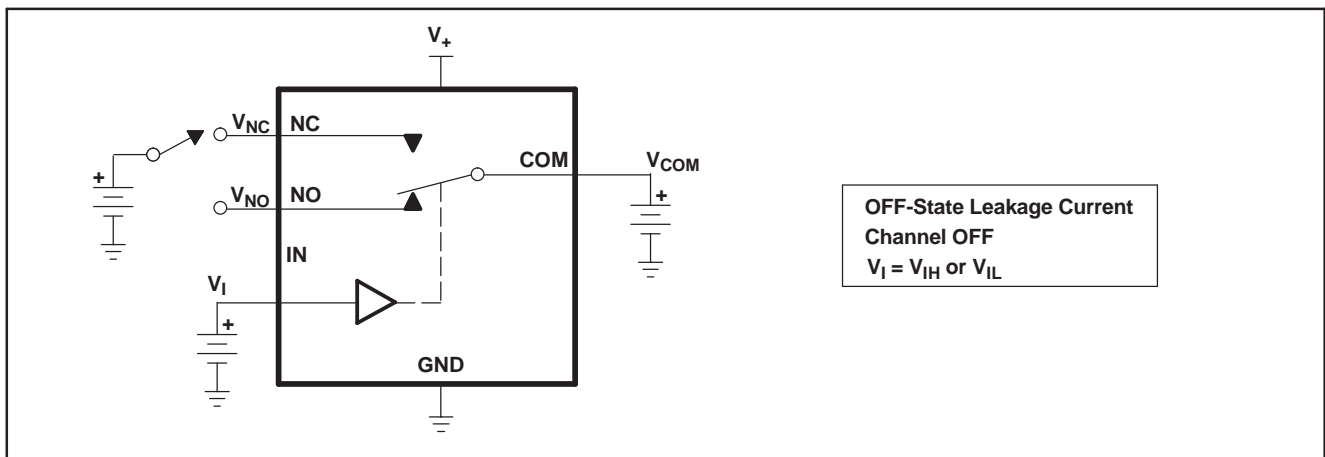


Figure 15. OFF-State Leakage Current ( $I_{NC(OFF)}$ ,  $I_{NC(PWROFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{NO(PWROFF)}$ ,  $I_{COM(OFF)}$ ,  $I_{COM(PWROFF)}$ )

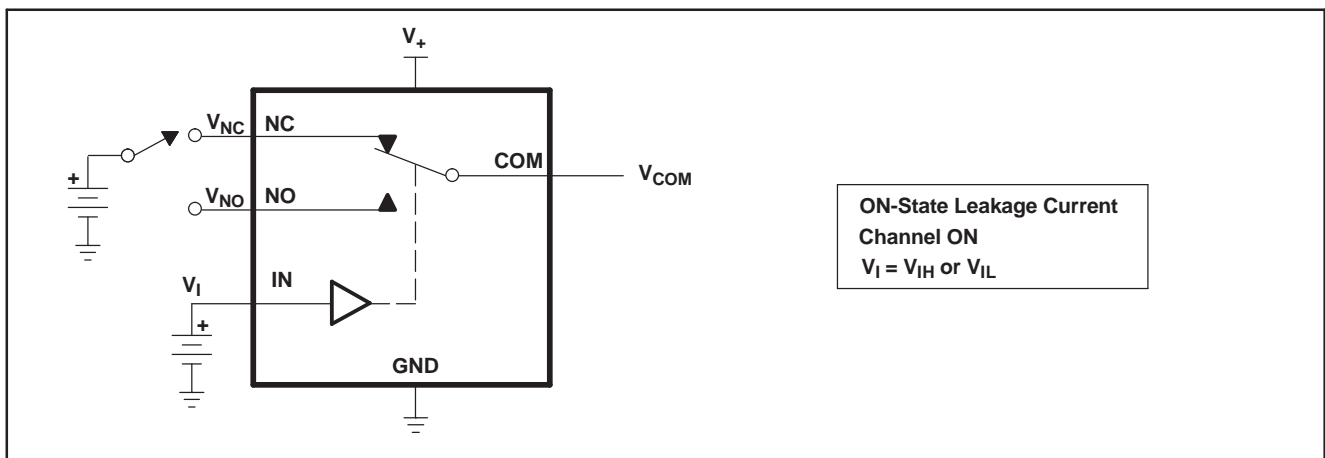


Figure 16. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )

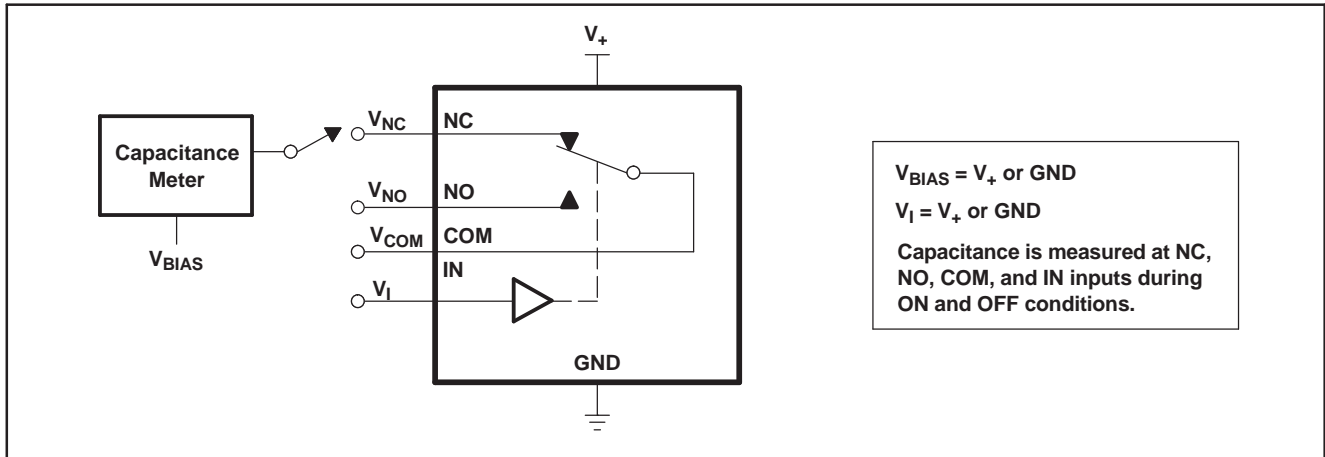
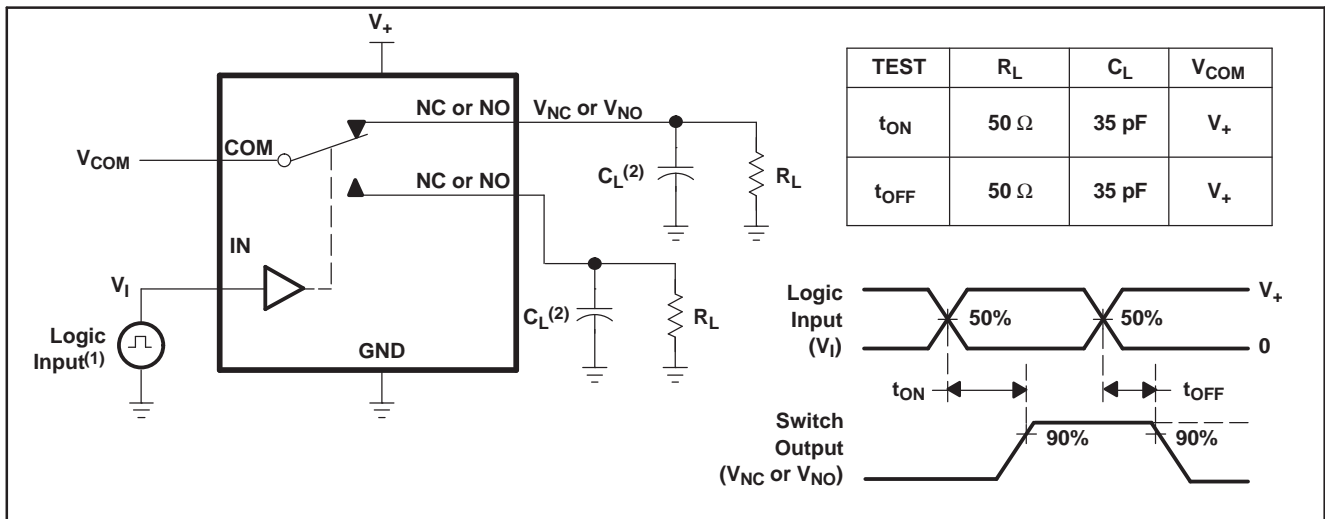
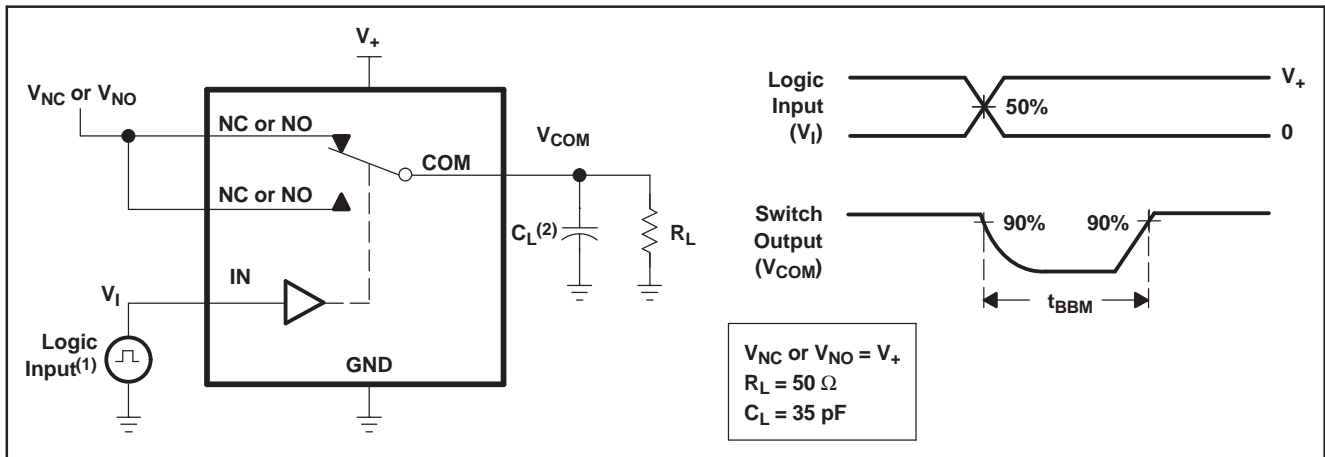


Figure 17. Capacitance ( $C_I$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NO(OFF)}$ ,  $C_{NC(ON)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2)  $C_L$  includes probe and jig capacitance.

Figure 18. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )



- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .
- (2)  $C_L$  includes probe and jig capacitance.

Figure 19. Break-Before-Make Time ( $t_{BBM}$ )

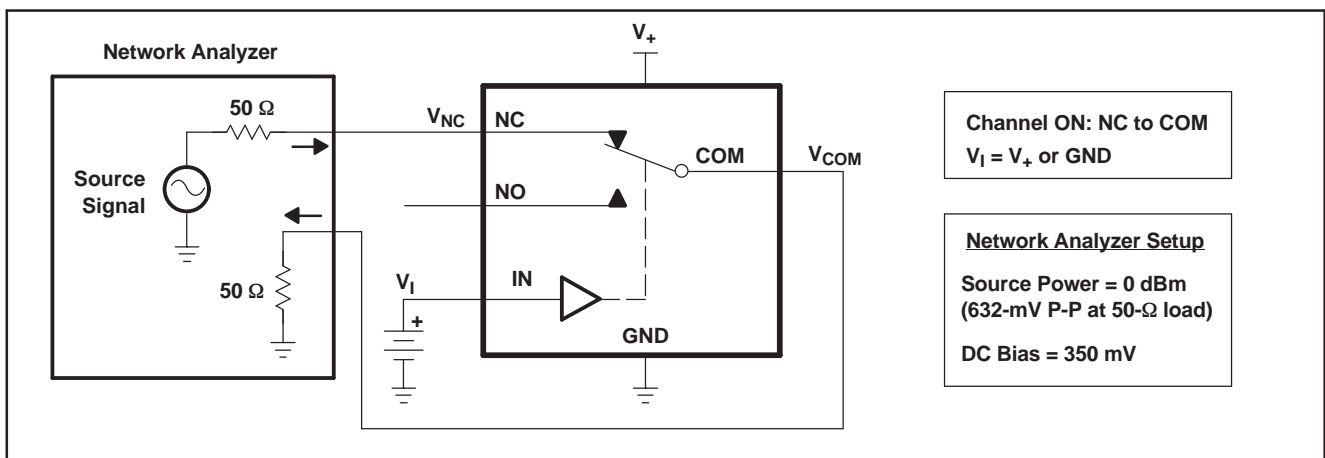


Figure 20. Bandwidth (BW)

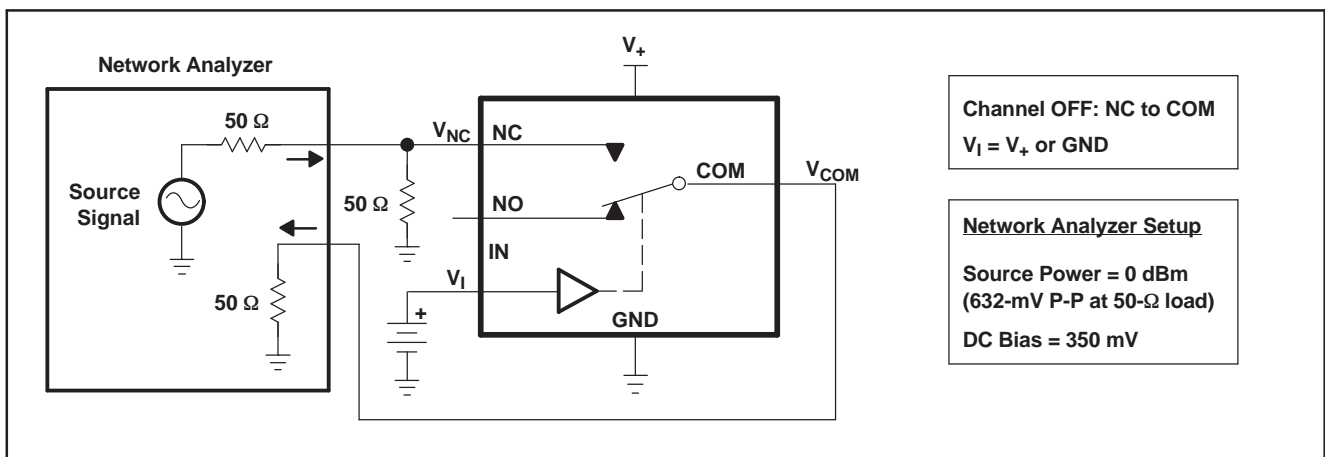


Figure 21. OFF Isolation (OISO)

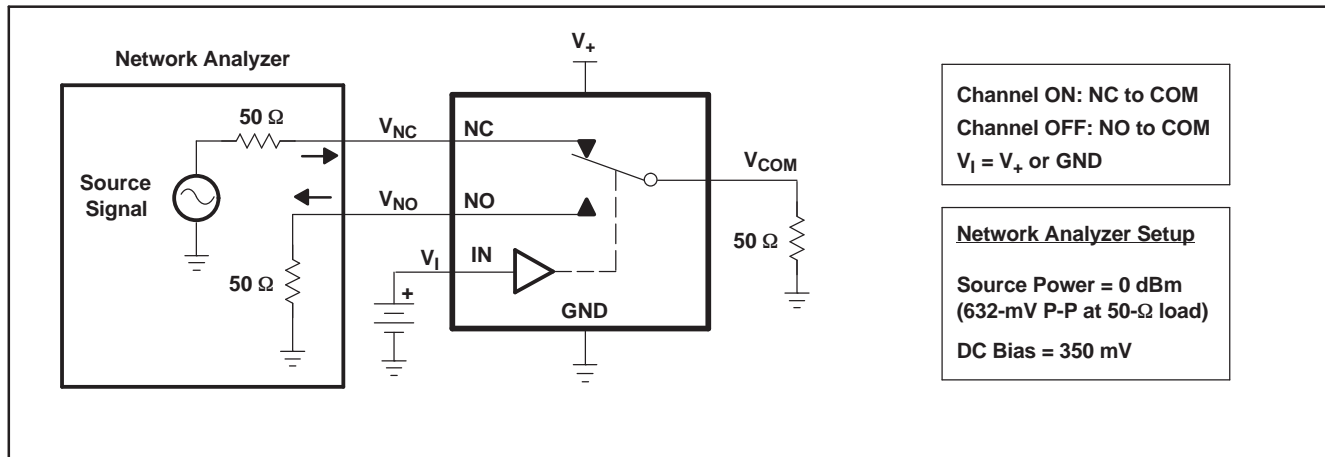
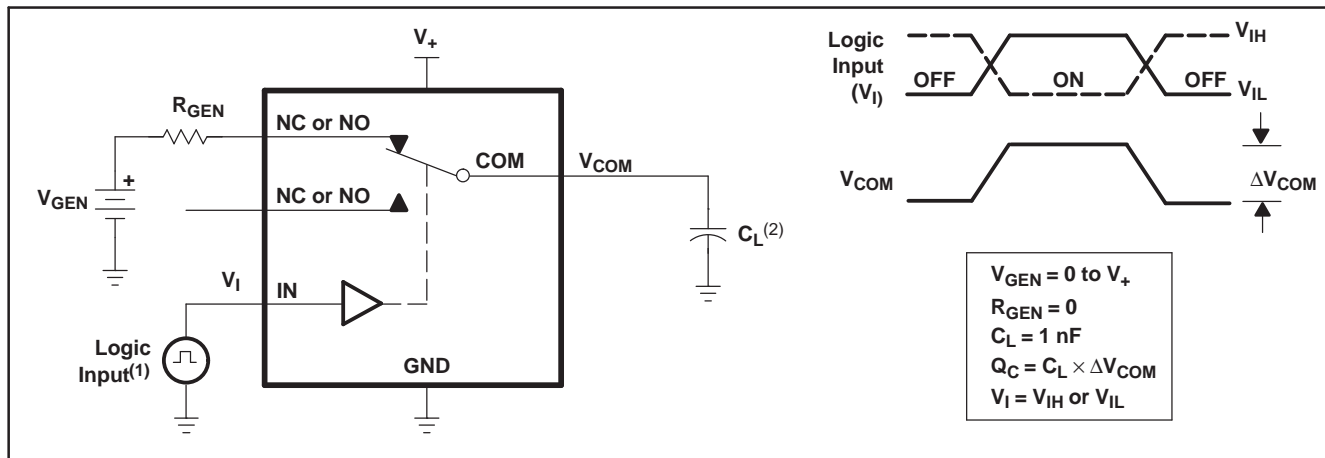
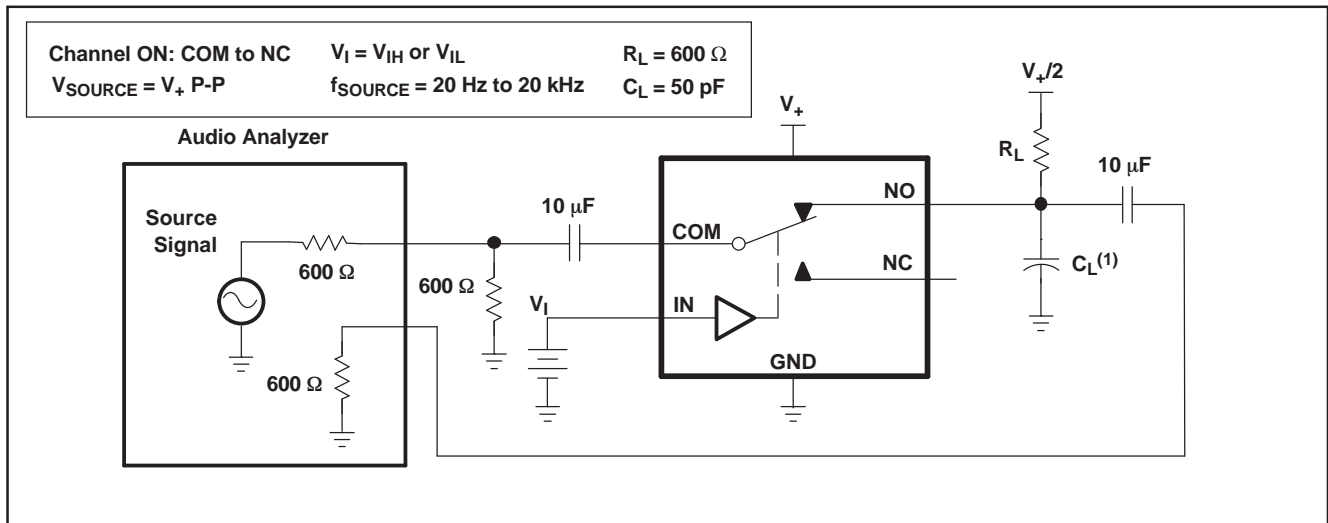


Figure 22. Crosstalk ( $X_{TALK}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- (2)  $C_L$  includes probe and jig capacitance.

Figure 23. Charge Injection ( $Q_C$ )



(1)  $C_L$  includes probe and jig capacitance.

**Figure 24. Total Harmonic Distortion (THD)**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A4624DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JWF, JWR)	Samples
TS5A4624DCKT	LIFEBUY	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JWR	
TS5A4624DCKTG4	LIFEBUY	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JWR	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A4624DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A4624DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A4624DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A4624DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A4624DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TS5A4624DCKT	SC70	DCK	6	250	202.0	201.0	28.0

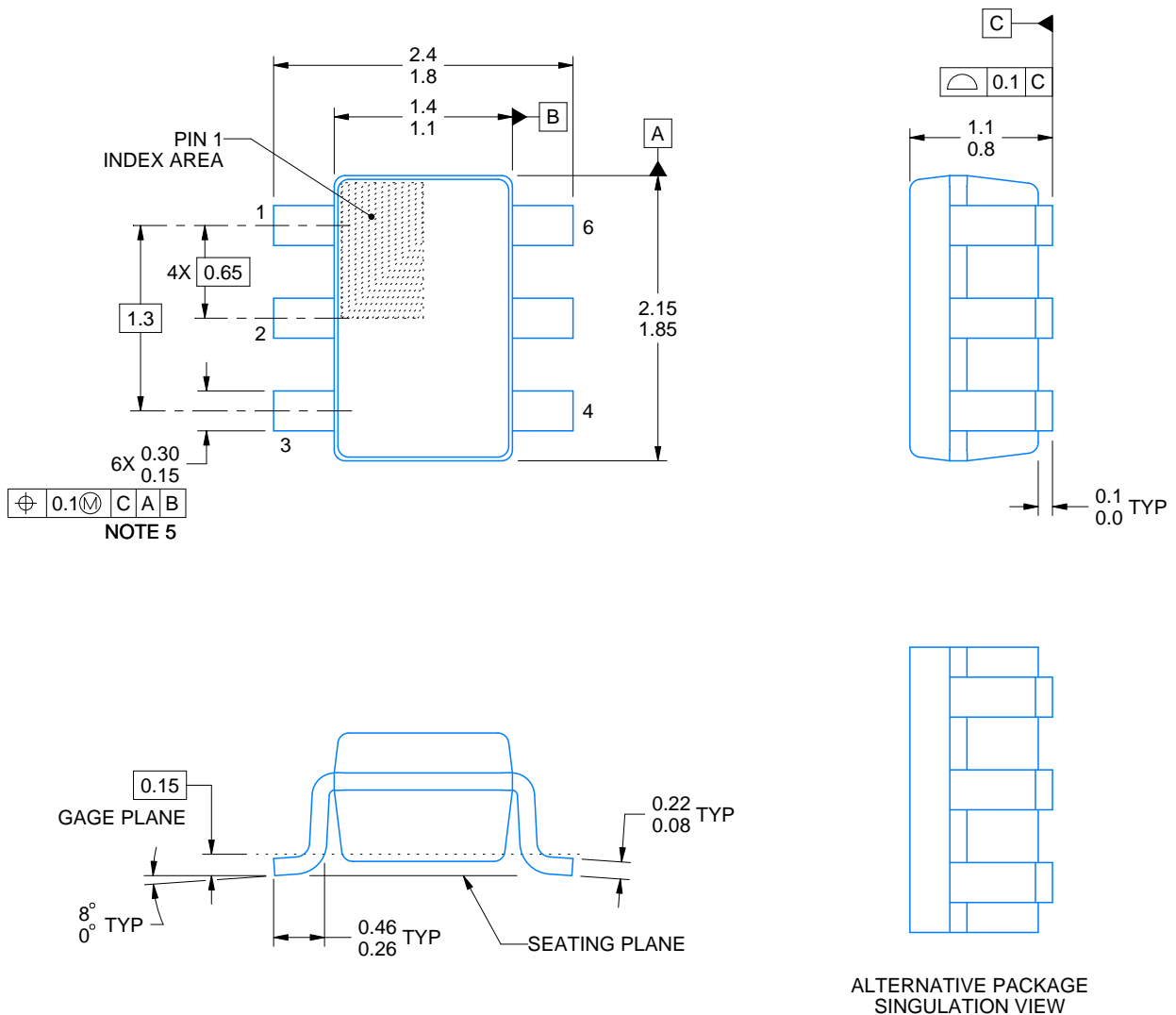
# DCK0006A



# PACKAGE OUTLINE

SOT - 1.1 max height

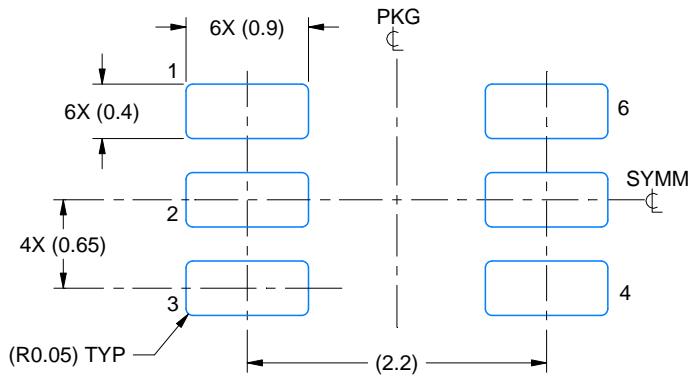
SMALL OUTLINE TRANSISTOR



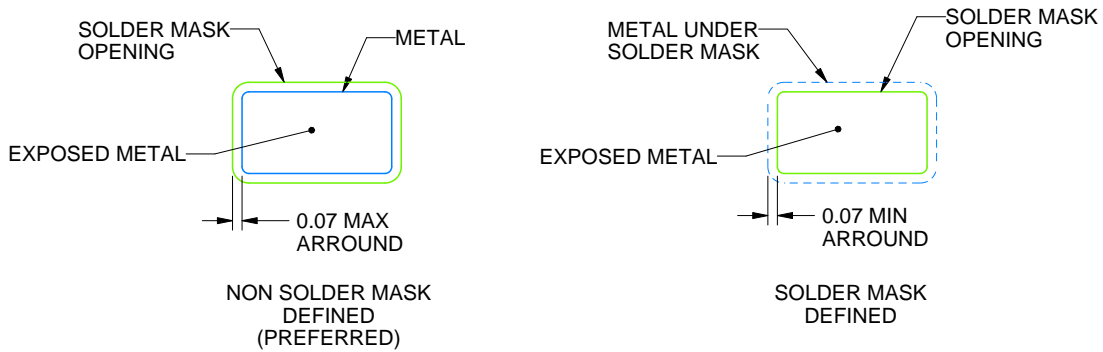
4214835/B 04/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

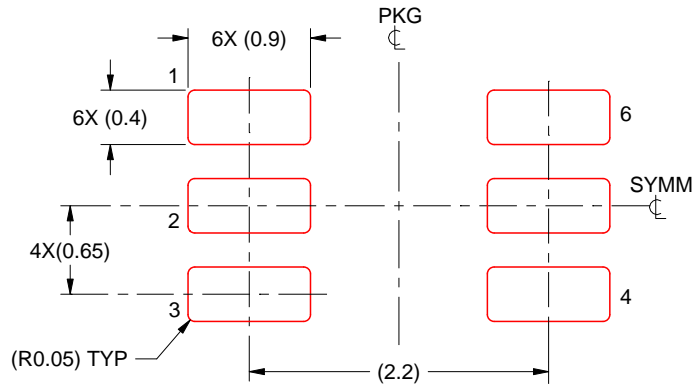


SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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