TSMU818A030 8-Channel, 18-Bit, 30V, 100mA Output, High-Capacitive Drive Parametric Measurement Unit (PMU)

1 Features

- 8-channel 4-quadrant PMU
  - FV, FI, FZ (high-Z), MV, and MI functions
- Programmable current ranges
  - Internal ±5µA, ±40µA, ±200µA, ±2mA ranges
  - Up to ±100mA with external R_{SENSE}
- 30V FV span with asymmetrical range choices
- Stable operation with up to 10µF C_{LOAD}
- Channel independent DACs
  - 18-bit force DAC with multiple voltage ranges
  - 16-bit offset, and voltage clamp DACs
  - 15-bit current clamp DACs
- Offset error and gain error calibration with true 18-bit endpoint performance
- Dual configuration state digital architecture
- Fast current clamps

2 Applications

- Memory test
- Semiconductor test
- Source measurement units

3 Description

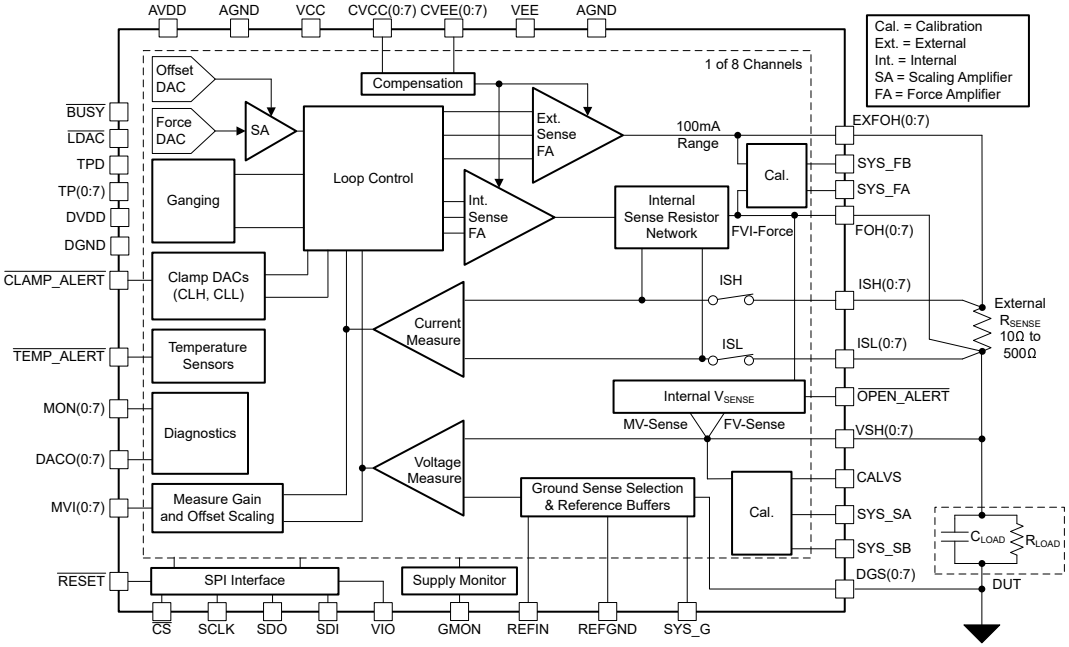
The TSMU818A030 is a high-performance, highly integrated parametric measurement unit (PMU) consisting of eight independent channels. Each channel includes one voltage output DAC that sets the programmable input levels for the force voltage amplifier and two clamp input DACs. Five resistor based programmable force and measure current ranges are available, ranging from ±5µA to ±100mA. Four of these ranges use on-chip sense resistors.

Measurements for the eight channels can be multiplexed in a wired-or configuration, which eliminates the need for an external multiplexer. Individual measurement outputs for respective channels are also available. The PMU functions are controlled using a simple SPI-compatible serial interface. Interface clock of 80MHz allows for fast mode updates and state changes with the dual-state double-buffered architecture. Configuration registers allow the user to easily change force or measure conditions, DAC levels, and selected current ranges.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TSMU818A030	ACQ (FCBGA, 144)	16mm × 16mm
	AMO (FCBGA, 196)	20mm × 20mm

(1) For more information, see Section 6.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and aid development are listed below.

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.3 Trademarks

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4.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSMU818A030ACQ	ACTIVE	FCBGA	ACQ	144	84	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 100	TSMU818A030ACQ	Samples
TSMU818A030AMO	ACTIVE	FCBGA	AMO	196	60	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 100	TSMU818A030	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

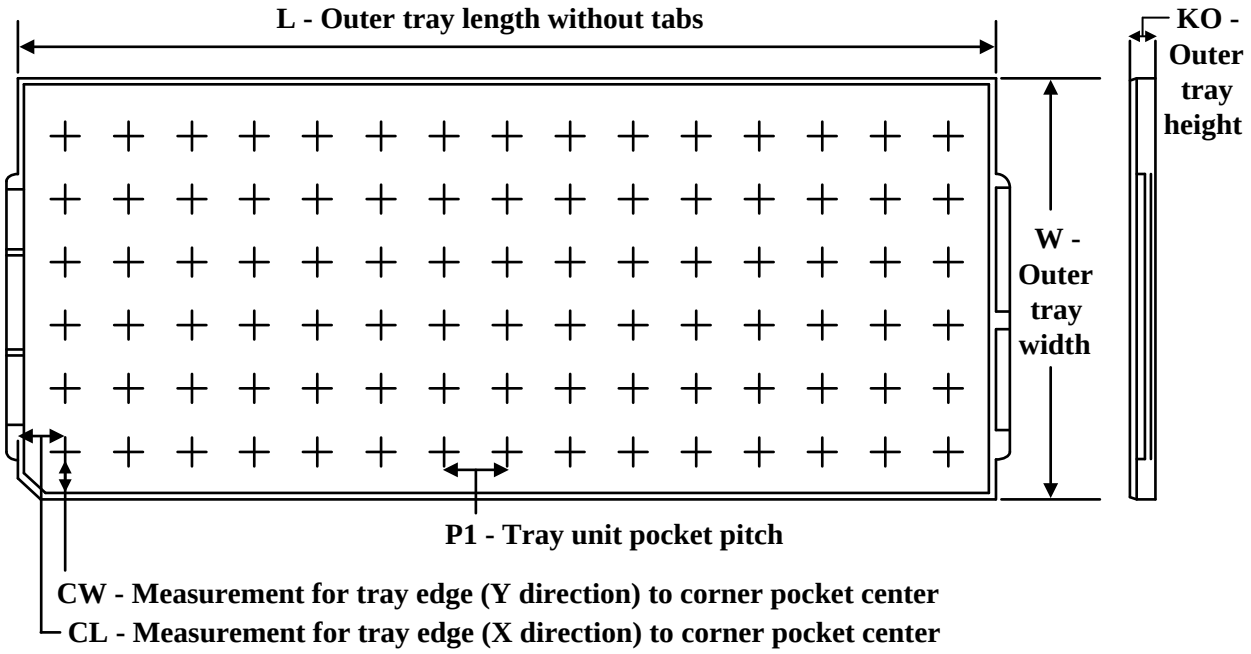
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSMU818A030AMO	AMO	FCBGA	196	60	5 x 12	150	315	135.9	12190	23.9	26.05	20.15

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265